INTEGRATED CIRCUITS

DATA SHEET

TDA9875A
Digital TV sound processor (DTVSP)

Product specification
File under Integrated Circuits, IC02

1998 Aug 13

Philips Semiconductors

PHILIPS

CONTENTS

1 FEATURES

1.1 Demodulator and decoder section

- Sound IF (SIF) input switch e.g. to select between terrestrial TV SIF and SAT SIF sources
- SIF AGC with 24 dB control range
- SIF 8-bit Analog-to-Digital Converter (ADC)
- DQPSK demodulation for different standards, simultaneously with 1-channel FM demodulation
- NICAM decoding (B/G, I and L standard)
- Two-carrier multistandard FM demodulation (B/G, D/K and M standard)
- Decoding for three analog multi-channel systems (A2, A2+ and A2*) and satellite sound
- Optional AM demodulation for system L, simultaneously with NICAM
- Programmable identification (B/G, D/K and M standard) and different identification times.

1.2 DSP section

- Digital crossbar switch for all digital signal sources and destinations
- Control of volume, balance, contour, bass, treble, pseudo stereo, spatial, bass boost and soft-mute
- Plop-free volume control
- Automatic Volume Level (AVL) control
- Adaptive de-emphasis for satellite
- Programmable beeper
- Monitor selection for FM/AM DC values and signals, with peak detection option
- I^2S-bus interface for a feature extension (e.g. Dolby surround) with matrix, level adjust and mute.

1.3 Analog audio section

- Analog crossbar switch with inputs for mono and stereo (also applicable as SCART 3 input), SCART 1 input/output, SCART 2 input/output and line output
- User defined full-level/–3 dB scaling for SCART outputs
- Output selection of mono, stereo, dual A/B, dual A or dual B
- 20 kHz bandwidth for SCART-to-SCART copies
- Standby mode with functionality for SCART copies
- Dual audio digital-to-analog converter from DSP to analog crossbar switch, bandwidth 15 kHz
- Dual audio ADC from analog inputs to DSP
- Two dual audio Digital-to-Analog Converters (DACs) for loudspeaker (Main) and headphone (Auxiliary) outputs; also applicable for L, R, C and S in the Dolby Pro Logic mode with feature extension.

2 GENERAL DESCRIPTION

The TDA9875A is a single-chip Digital TV Sound Processor (DTVSP) for analog and digital multi-channel sound systems in TV sets and satellite receivers.

2.1 Supported standards

The multistandard/multi-stereo capability of the TDA9875A is mainly of interest in Europe, but also in Hong Kong/Peoples Republic of China and South East Asia. This includes B/G, D/K, I, M and L standard. In other application areas there exists only subsets of those standard combinations otherwise only single standards are transmitted.

M standard is transmitted in Europe by the American Forces Network (AFN) with European channel spacing (7 MHz VHF, 8 MHz UHF) and monaural sound.

The AM sound of L/L' standard is normally demodulated in the 1st sound IF. The resulting AF signal has to be entered into the mono audio input of the TDA9875A. A second possibility is to use the internal AM demodulator stage, however this gives limited performance.

Korea has a stereo sound system similar to Europe and is supported by the TDA9875A. Differences include deviation, modulation contents and identification. It is based on M standard.

An overview of the supported standards and sound systems and their key parameters is given in Table 1.

The analog multi-channel sound systems (A2, A2+ and A2*) are sometimes also named 2CS (2 carrier systems).

2.1.1 ANALOG 2-CARRIER SYSTEMS

Table 1 Frequency modulation

STANDARD	SOUND SYSTEM	CARRIER FREQUENCY (MHz)	FM DEVIATION (kHz) NOM./MAX./OVER	MODULATION		BANDWIDTH/ DE-EMPHASIS (kHz/μs)
				SC1	SC2	
M	mono	4.5	15/25/50	mono	–	15/75
M	A2+	4.5/4.724	15/25/50	$\frac{1}{2}$(L + R)	$\frac{1}{2}$(L – R)	15/75 (Korea)
B/G	A2	5.5/5.742	27/50/80	$\frac{1}{2}$(L + R)	R	15/50
I	mono	6.0	27/50/80	mono	–	15/50
D/K	A2	6.5/6.742	27/50/80	$\frac{1}{2}$(L + R)	R	15/50
D/K	A2*	6.5/6.258	27/50/80	$\frac{1}{2}$(L + R)	R	15/50

Table 2 Identification for A2 systems

PARAMETER	A2/A2*	A2+ (KOREA)
Pilot frequency	54.6875 kHz = 3.5 × line frequency	55.0699 kHz = 3.5 × line frequency
Stereo identification frequency	$117.5\ \text{Hz} = \frac{\text{line frequency}}{133}$	$149.9\ \text{Hz} = \frac{\text{line frequency}}{105}$
Dual identification frequency	$274.1\ \text{Hz} = \frac{\text{line frequency}}{57}$	$276.0\ \text{Hz} = \frac{\text{line frequency}}{57}$
AM modulation depth	50%	50%

2.1.2 2-CARRIER SYSTEMS WITH NICAM

Table 3 NICAM

STANDARD	SC1				SC2 (MHz) NICAM	DE-EMPHASIS	ROLL-OFF (%)	NICAM CODING
	FREQUENCY (MHz)	TYPE	MODULATION					
			INDEX (%) NOM./MAX.	DEVIATION (kHz) NOM./MAX.				
B/G	5.5	FM	–	27/50	5.85	J17	40	note 1
I	6.0	FM	–	27/50	6.552	J17	100	note 1
D/K	6.5	FM	–	27/50	5.85	J17	40	note 2
L	6.5	AM	54/100	–	5.85	J17	40	note 1

Notes

1. See *“EBU specification”* or equivalent specification.
2. Not yet defined.

2.1.3 SATELLITE SYSTEMS

An important specification for satellite TV reception is the *"Astra specification"*. The TDA9875A is suited for the reception of Astra and other satellite signals.

Table 4 FM satellite sound

CARRIER TYPE	CARRIER FREQUENCY (MHz)	MODULATION INDEX	MAXIMUM FM DEVIATION (kHz)	MODULATION	BANDWIDTH/ DE-EMPHASIS (kHz/µs)
Main	6.50(1)	0.26	85	mono	15/50(1)
Sub	7.02/7.20	0.15	50	m/st/d(2)	15/adaptive(3)
Sub	7.38/7.56	0.15	50	m/st/d(2)	15/adaptive(3)
Sub	7.74/7.92	0.15	50	m/st/d(2)	15/adaptive(3)
Sub	8.10/8.28	0.15	50	m/st/d(2)	15/adaptive(3)

Notes

1. For other satellite systems, frequencies of, for example, 5.80, 6.60 or 6.65 MHz can also be received. A de-emphasis of 60 µs, or in accordance with J17, is available.
2. m/st/d = mono or stereo or dual language sound.
3. Adaptive de-emphasis = compatible to transmitter specification.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9875A	SDIP64	plastic shrink dual in-line package; 64 leads (750 mil)	SOT274-1

4 BLOCK DIAGRAM

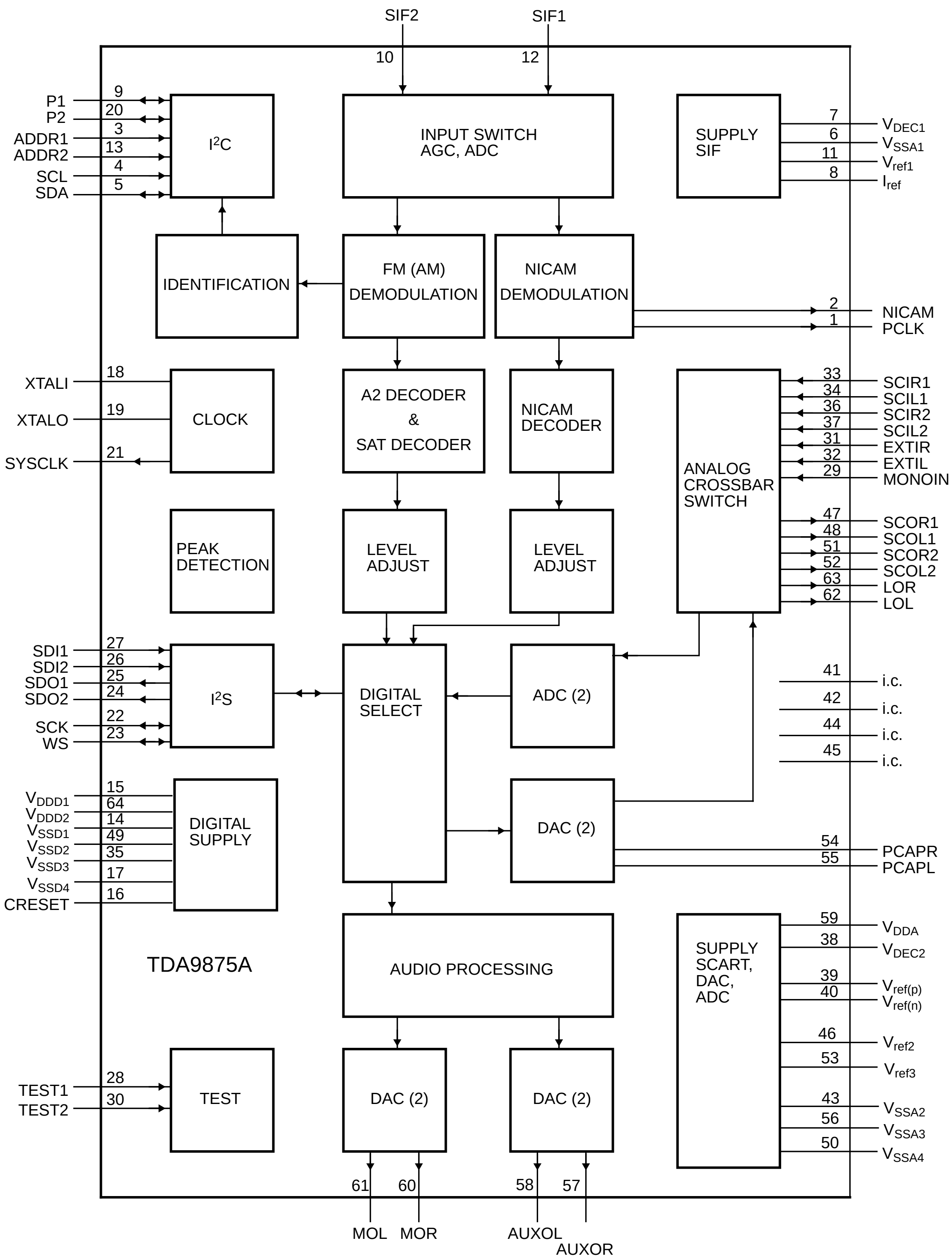


Fig.1 Block diagram.

5 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
PCLK	1	O	NICAM clock output at 728 kHz
NICAM	2	O	serial NICAM data output at 728 kHz
ADDR1	3	I	first I^2C-bus slave address modifier
SCL	4	I	I^2C-bus clock
SDA	5	I/O	I^2C-bus data
V_{SSA1}	6	supply	supply ground 1; analog front-end circuitry
V_{DEC1}	7	–	positive power supply voltage 1 decoupling; analog front-end circuitry
I_{ref}	8	–	resistor for reference current generator; analog front-end circuitry
P1	9	I/O	first general purpose I/O pin
SIF2	10	I	sound IF input 2
V_{ref1}	11	–	reference voltage; analog front-end circuitry
SIF1	12	I	sound IF input 1
ADDR2	13	I	second I^2C-bus slave address modifier
V_{SSD1}	14	supply	supply ground 1; digital circuitry
V_{DDD1}	15	supply	digital supply voltage 1; digital circuitry
CRESET	16	–	capacitor for power-on reset
V_{SSD4}	17	supply	supply ground 4; digital circuitry
XTALI	18	I	crystal oscillator input
XTALO	19	O	crystal oscillator output
P2	20	I/O	second general purpose I/O pin
SYSCLK	21	O	system clock output
SCK	22	I/O	I^2S-bus clock
WS	23	I/O	I^2S-bus word select
SDO2	24	O	I^2S-bus data output 2
SDO1	25	O	I^2S-bus data output 1
SDI2	26	I	I^2S-bus data input 2
SDI1	27	I	I^2S-bus data input 1
TEST1	28	I	first test pin; connected to V_{SSD1} for normal operation
MONOIN	29	I	audio mono input
TEST2	30	I	second test pin; connected to V_{SSD1} for normal operation
EXTIR	31	I	external audio input right channel
EXTIL	32	I	external audio input left channel
SCIR1	33	I	SCART 1 input right channel
SCIL1	34	I	SCART 1 input left channel
V_{SSD3}	35	supply	supply ground 3; digital circuitry
SCIR2	36	I	SCART 2 input right channel
SCIL2	37	I	SCART 2 input left channel
V_{DEC2}	38	–	positive power supply voltage 2 decoupling; audio analog-to-digital converter circuitry
$V_{ref(p)}$	39	–	positive reference voltage; audio analog-to-digital converter circuitry

SYMBOL	PIN	I/O	DESCRIPTION
$V_{ref(n)}$	40	–	reference voltage ground; audio analog-to-digital converter circuitry
i.c.	41	–	internally connected; note 1
i.c.	42	–	internally connected; note 2
V_{SSA2}	43	supply	supply ground 2; audio analog-to-digital converter circuitry
i.c.	44	–	internally connected; note 2
i.c.	45	–	internally connected; note 1
V_{ref2}	46	–	reference voltage; audio analog-to-digital converter circuitry
SCOR1	47	O	SCART 1 output right channel
SCOL1	48	O	SCART 1 output left channel
V_{SSD2}	49	supply	supply ground 2; digital circuitry
V_{SSA4}	50	supply	supply ground 4; audio operational amplifier circuitry
SCOR2	51	O	SCART 2 output right channel
SCOL2	52	O	SCART 2 output left channel
V_{ref3}	53	–	reference voltage; audio digital-to-analog converter and operational amplifier circuitry
PCAPR	54	–	post-filter capacitor pin right channel, audio digital-to-analog converter
PCAPL	55	–	post-filter capacitor pin left channel, audio digital-to-analog converter
V_{SSA3}	56	supply	supply ground 3; audio digital-to-analog converter circuitry
AUXOR	57	O	headphone (Auxiliary) output right channel
AUXOL	58	O	headphone (Auxiliary) output left channel
V_{DDA}	59	supply	positive analog power supply voltage; analog circuitry
MOR	60	O	loudspeaker (Main) output right channel
MOL	61	O	loudspeaker (Main) output left channel
LOL	62	O	line output left channel
LOR	63	O	line output right channel
V_{DDD2}	64	supply	digital supply voltage 2; digital circuitry

Notes

1. Test pin, CMOS level input, pull-up resistor, can be connected to V_{SS}.
2. Test pin, CMOS 3-state stage, can be connected to V_{SS}.

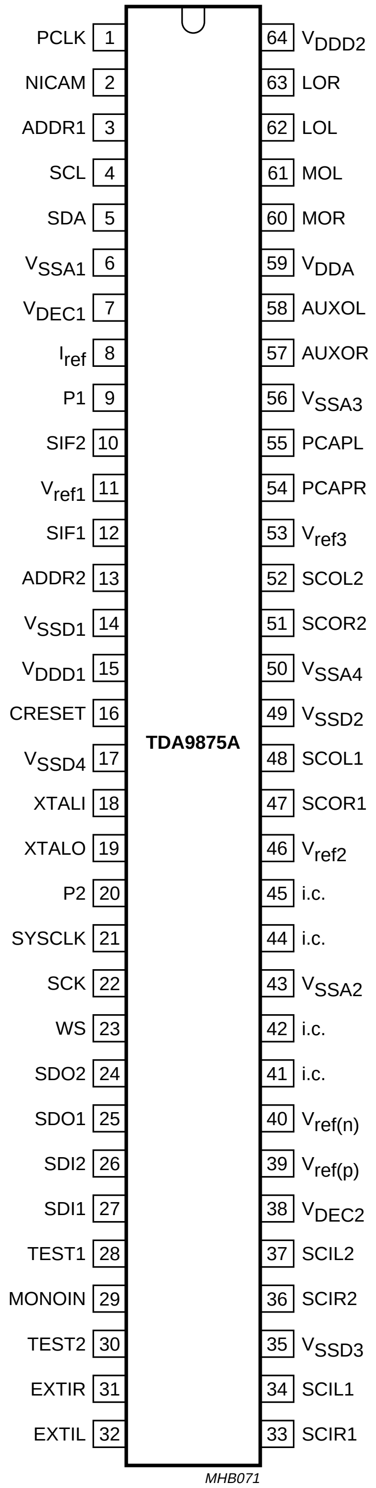


Fig.2 Pin configuration.

6 FUNCTIONAL DESCRIPTION

6.1 Description of the demodulator and decoder section

6.1.1 SIF INPUT

Two input pins are provided, SIF1 e.g. for terrestrial TV and SIF2 e.g. for a satellite tuner. For higher SIF signal levels the SIF input can be attenuated with an internal switchable −10 dB resistor divider. As no specific filters are integrated, both inputs have the same specification giving flexibility in application. The selected signal is passed through an AGC circuit and then digitized by an 8-bit ADC operating at 24.576 MHz.

6.1.2 AGC

The gain of the AGC amplifier is controlled from the ADC output by means of a digital control loop employing hysteresis. The AGC has a fast attack behaviour to prevent ADC overloads and a slow decay behaviour to prevent AGC oscillations. For AM demodulation the AGC must be switched off. When switched off, the control loop is reset and fixed gain settings can be chosen from Table 15 (subaddress 0).

The AGC can be controlled via the I^2C-bus. Details can be found in the I^2C-bus register definitions (see Chapter 10).

6.1.3 MIXER

The digitized input signal is fed to the mixers, which mix one or both input sound carriers down to zero IF. A 24-bit control word for each carrier sets the required frequency. Access to the mixer control word registers is via the I^2C-bus. When receiving NICAM programs, a feedback signal is added to the control word of the second carrier mixer to establish a carrier-frequency loop.

6.1.4 FM AND AM DEMODULATION

An FM or AM input signal is fed via a band-limiting filter to a demodulator that can be used for either FM or AM demodulation. Apart from the standard (fixed) de-emphasis characteristic, an adaptive de-emphasis is available for encoded satellite programs. A stereo decoder recovers the left and right signal channels from the demodulated sound carriers. Both the European and Korean stereo systems are supported.

6.1.5 FM IDENTIFICATION

The identification of the FM sound mode is performed by AM synchronous demodulation of the pilot signal and narrow-band detection of the identification frequencies. The result is available via the I^2C-bus interface. A selection can be made via the I^2C-bus for B/G, D/K and M standard and for three different modes that represent different trade-offs between speed and reliability of identification.

6.1.6 NICAM DEMODULATION

The NICAM signal is transmitted in a DQPSK code at a bit rate of 728 kbit/s. The NICAM demodulator performs DQPSK demodulation and feeds the resulting bitstream and clock signal onto the NICAM decoder and, for evaluation purposes, to PCLK (pin 1) and NICAM (pin 2).

A timing loop controls the frequency of the crystal oscillator to lock the sampling rate to the symbol timing of the NICAM data.

6.1.7 NICAM DECODER

The device performs all decoding functions in accordance with the *“EBU NICAM 728 specification”*. After locking to the frame alignment word, the data is descrambled by applying the defined pseudo-random binary sequence; the device will then synchronize to the periodic frame flag bit C0.

The status of the NICAM decoder can be read out from the NICAM status register by the user (see the I^2C-bus register description in Section 10.4.2). The OSB bit indicates that the decoder has locked to the NICAM data. The VDSP bit indicates that the decoder has locked to the NICAM data and that the data is valid sound data. The C4 bit indicates that the sound conveyed by the FM mono channel is identical to the sound conveyed by the NICAM channel. The error byte contains the number of sound sample errors, resulting from parity checking, that occurred in the past 128 ms period. The Bit Error Rate (BER) can be calculated using the following equation;

$$\mathrm{BER} = \frac{\text{bit errors}}{\text{total bits}} \approx \text{error byte} \times 1.74 \times 10^{-5}$$

6.1.8 NICAM AUTO-MUTE

This function is enabled by setting bit AMUTE LOW subaddress 14 (see Section 10.3.11). Upper and lower error limits may be defined by writing appropriate values to two registers in the I^{2}C-bus section (subaddresses 16 and 17; see Sections 10.3.13 and 10.3.14). When the number of errors in a 128 ms period exceeds the upper error limit the auto-mute function will switch the output sound from NICAM to whatever sound is on the first sound carrier (FM or AM). When the error count is smaller than the lower error limit the NICAM sound is restored.

The auto-mute function can be disabled by setting bit AMUTE HIGH. In this condition clicks become audible when the error count increases; the user will hear a signal of degrading quality.

A decision to enable/disable the auto-muting is taken by the microcontroller based on an interpretation of the application control bits C1, C2, C3 and C4 and, possibly, any additional strategy implemented by the set maker in the microcontroller software.

For NICAM L applications, it is recommended to demodulate AM sound in the first sound IF and connect the audio signal to the mono input of the TDA9875A. By setting the AMSEL bit subaddress 14 (see Section 10.3.11), the auto-mute function will switch to the audio ADC instead of switching to the first sound carrier. The ADC source selector subaddress 23 (see Section 10.3.20) should be set to mono input, where the AM sound signal should be connected.

6.1.9 CRYSTAL OSCILLATOR

The digital-controlled crystal oscillator (DCXO) is illustrated in Fig.8 (see Chapter 12). The circuitry of the DCXO is fully integrated, only the external 24.576 MHz crystal is needed.

6.1.10 TEST PINS

Both test pins are active HIGH, in normal operation of the device they are wired to V_{SSD1}. Test functions are for manufacturing tests only and are not available to customers. Without external circuitry these pads are pulled down to LOW level with internal resistors.

6.1.11 POWER FAIL DETECTOR

The power fail detector monitors the internal power supply for the digital part of the device. If the supply has temporary been lower than the specified lower limit, the power-on reset bit POR, transmitter register subaddress 0 (see Section 10.4.1), will be set to HIGH. The CLRPOR bit, slave register subaddress 1 (see Section 10.3.2), resets the power-on reset flip-flop to LOW. If this is detected, an initialization of the TDA9875A has to be carried out to ensure reliable operation.

6.2 Description of the DSP

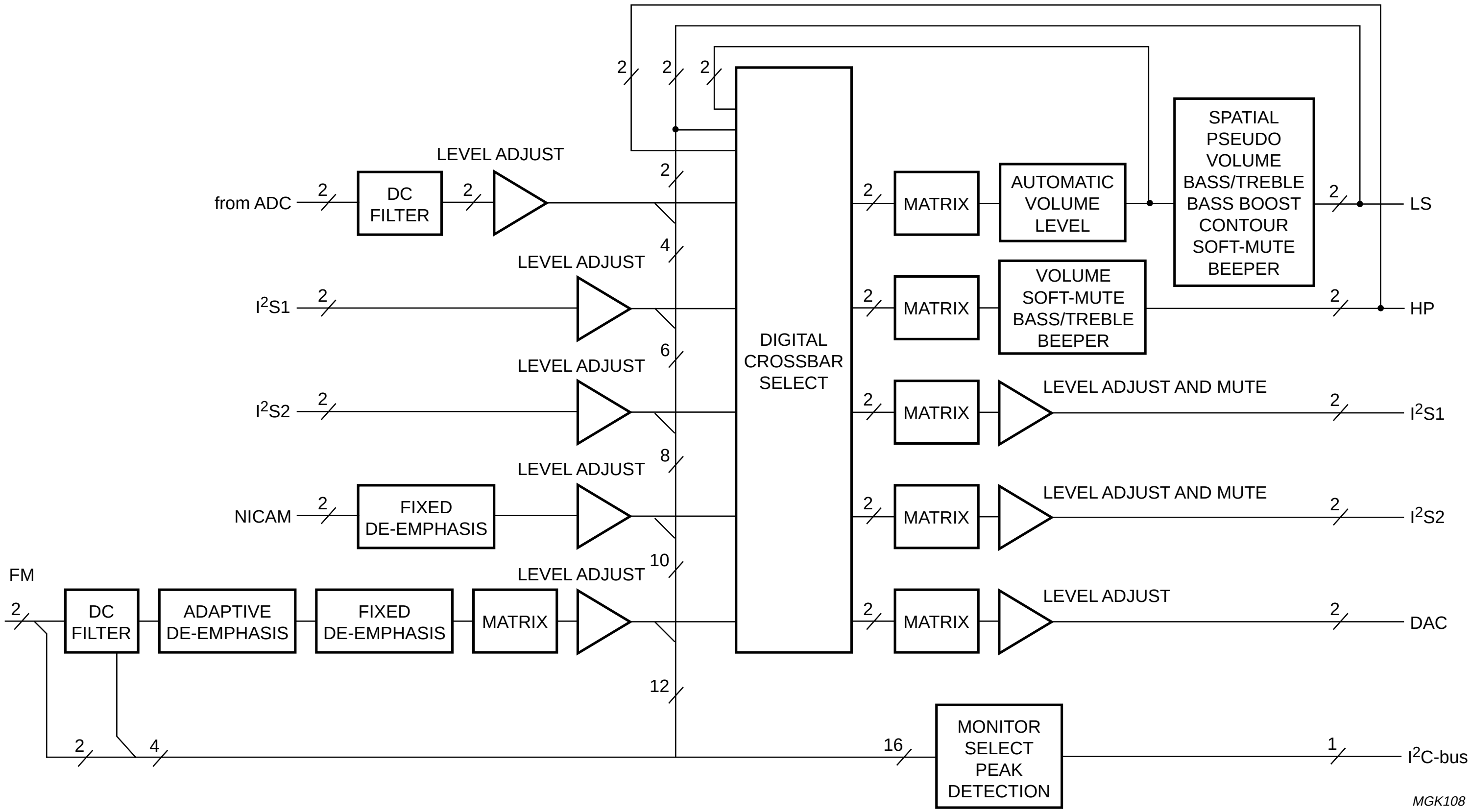


Fig.3 DSP data flow diagram.

6.2.1 LEVEL SCALING

All input channels to the digital crossbar switch (except for the loudspeaker feedback path) are equipped with a level adjust facility to change the signal level in a range of ±15 dB. It is recommended to scale all input channels to be 15 dB below full scale (–15 dB full scale) under nominal conditions.

6.2.2 NICAM PATH

The NICAM path has a switchable J17 de-emphasis.

6.2.3 FM (AM) PATH

A high-pass filter suppresses DC offsets from the FM demodulator due to carrier frequency offsets and supplies the monitor/peak function with DC values and an unfiltered signal, e.g. for the purpose of carrier detection.

The de-emphasis function offers fixed settings for the supported standards (50 µs, 60 µs, 75 µs and J17).

An adaptive de-emphasis is available for Wegener-Panda 1 encoded programs.

A matrix performs the dematrixing of the A2 stereo, dual and mono signals.

6.2.4 NICAM AUTO-MUTE

If NICAM B/G, I, D/K is received, the auto-mute is enabled and the signal quality becomes poor, the digital crossbar switch switches automatically to FM and switches the matrix to channel 1. The automatic switching depends on the NICAM bit error rate.
The auto-mute function can be disabled via the I^{2}C-bus.

For NICAM L applications, it is recommended to demodulate AM sound in the first sound IF and connect the audio signal to the mono input of the TDA9875A. By setting the AMSEL bit subaddress 14 (see Section 10.3.11), the auto-mute function will switch to the audio ADC instead of switching to the first sound carrier. The ADC source selector subaddress 23 (see Section 10.3.20) should be set to mono input, where the AM sound signal should be connected.

6.2.5 MONITOR

This function provides data words from a number of locations of the signal processing paths to the I^{2}C-bus interface (2 data bytes). Signal sources include the FM demodulator outputs, most inputs to the digital crossbar switch and the outputs of the ADC. Source selection and data read-out is performed via the I^{2}C-bus.

Optionally, the peak value can be measured instead of simply taking samples. The internally stored peak value is reset to zero when the data is read via the I^{2}C-bus.
The monitor function may be used, for example, for signal level measurements or carrier detection.

6.2.6 LOUDSPEAKER (MAIN) CHANNEL

The matrix provides the following functions; forced mono, stereo, channel swap, channel 1, channel 2 and spatial effects.

There are fixed coefficient sets for spatial settings of 30%, 40% and 52%.

The Automatic Volume Level (AVL) function provides a constant output level of –23 dB full scale for input levels between 0 and –29 dB full scale. There are some fixed decay time constants to choose from, i.e. 2, 4 and 8 seconds.

Pseudo stereo is based on a phase shift in one channel via a 2nd-order all-pass filter. There are fixed coefficient sets to provide 90 degrees phase shift at frequencies of 150, 200 and 300 Hz.

Volume is controlled individually for each channel ranging from +24 to –83 dB with 1 dB resolution. There is also a mute position. For the purpose of a simple control software in the microcontroller, the decimal number that is sent as an I^{2}C-bus data byte for volume control is identical to the volume setting in dBs (e.g. the I^{2}C-bus data byte +10 sets the new volume value to +10 dB).

Balance can be realized by independent control of the left and right channel volume settings.

Contour is adjustable between 0 and +18 dB with 1 dB resolution. This function is linked to the volume setting by means of microcontroller software.

Bass is adjustable between +15 and –12 dB with 1 dB resolution and treble is adjustable between ±12 dB with 1 dB resolution.

For the purpose of a simple control software in the microcontroller, the decimal number that is sent as an I^{2}C-bus data byte for contour, bass or treble is identical to the new contour, bass or treble setting in dBs (e.g. the I^{2}C-bus data byte +8 sets the new value to +8 dB).

Extra bass boost is provided up to 20 dB with 2 dB resolution. The implemented coefficient set serves merely as an example on how to use this filter.

The beeper provides tones in a range from approximately 400 Hz to 30 kHz. The frequency can be selected via the I^{2}C-bus. The beeper output signal is added to the loudspeaker and headphone channel signals. The beeper volume is adjustable with respect to full scale between 0 and –93 dB with 3 dB resolution. The beeper is not effected by mute.

Soft-mute provides a mute ability in addition to volume control with a well defined time (32 ms) after which the soft-mute is completed. A smooth fading is achieved by a cosine masking.

6.2.7 HEADPHONE (AUXILIARY) CHANNEL

The matrix provides the following functions; forced mono, stereo, channel swap, channel 1 and channel 2 (or C and S in Dolby Surround Pro Logic mode).

Volume is controlled individually for each channel in a range from +24 to –83 dB with 1 dB resolution. There is also a mute position. For the purpose of a simple control software in the microcontroller, the decimal number that is sent as an I^2C-bus data byte for volume control is identical to the volume setting in dB (e.g. the I^2C-bus data byte +10 sets the new volume value to +10 dB).

Balance can be realized by independent control of the left and right channel volume settings.

Bass is adjustable between +15 and –12 dB with 1 dB resolution and treble is adjustable between ±12 dB with 1 dB resolution.

For the purpose of a simple control software in the microcontroller, the decimal number that is sent as an I^2C-bus data byte for bass or treble is identical to the new bass or treble setting in dB (e.g. the I^2C-bus data byte +8 sets the new value to +8 dB).

The beeper provides tones in a range from approximately 400 Hz to 30 kHz. The frequency can be selected via the I^2C-bus. The beeper output signal is added to the loudspeaker and headphone channel signals. The beeper volume is adjustable with respect to full scale between 0 and –93 dB with 3 dB resolution. The beeper is not effected by mute.

Soft-mute provides a mute ability in addition to volume control with a well defined time (32 ms) after which the soft-mute is completed. A smooth fading is achieved by a cosine masking.

6.2.8 FEATURE INTERFACE

The feature interface comprises two I^2S-bus input/output ports and a system clock output. Each I^2S-bus port is equipped with level adjust facilities that can change the signal level in a range of ±15 dB with 1 dB resolution. Outputs can be disabled to improve EMC performance.

The I^2S-bus output matrix provides the following functions; forced mono, stereo, channel swap, channel 1 and channel 2.

One example of how the feature interface can be used in a TV set is to connect an external Dolby Surround Pro Logic DSP, such as the SAA7710, to the I^2S-bus ports. Outputs must be enabled and a suitable master clock signal for the DSP can be taken from pin SYSCLK.
A stereo signal from any source will be output on one of the I^2S-bus serial data outputs and the four processed signal channels will be entered at both I^2S-bus serial data inputs. Left and right could then be output to the power amplifiers via the Main channel, centre and surround via the Auxiliary channel.

6.2.9 CHANNEL FROM THE AUDIO ANALOG-TO-DIGITAL CONVERTER

The signal level at the output of the ADC can be adjusted in a range of ±15 dB with 1 dB resolution. The audio ADC itself is scaled to a gain of –6 dB.

6.2.10 CHANNEL TO THE ANALOG CROSSBAR PATH

Level adjust with control positions 0 dB, +3 dB, +6 dB and +9 dB.

6.2.11 DIGITAL CROSSBAR SWITCH (see Fig.6)

Input channels to the crossbar switch are from the audio ADC, I^2S1, I^2S2, FM path, NICAM path and from the loudspeaker channel path after matrix and AVL.

Output channels comprise loudspeaker, headphone, I^2S1, I^2S2 and the audio DACs for line output and SCART.

The I^2S1 and I^2S2 outputs also provide digital outputs from the loudspeaker and headphone channels, but without the beeper signals.

6.2.12 GENERAL

There are a number of functions that can provide signal gain, e.g. volume, bass and treble control. Great care has to be taken when using gain with large input signals in order not to exceed the maximum possible signal swing, which would cause severe signal distortion. The nominal signal level of the various signal sources to the digital crossbar switch should be 15 dB below digital full scale (–15 dB full scale). This means that a volume setting of, say, +15 dB would just produce a full scale output signal and not cause clipping, if the signal level is nominal.

Sending illegal data patterns via the I^{2}C-bus will not cause any changes of the current setting for the volume, bass, treble, bass boost and level adjust functions.

6.2.13 EXPERT MODE

The TDA9875A provides a special expert mode that gives direct write access to the internal Coefficient RAM (CRAM) of the DSP. It can be used to create user-defined characteristics, such as a tone control with different corner frequencies or special boost/cut characteristics to correct the low-frequency loudspeaker and/or cabinet frequency responses by means of the bass boost filter. However, this mode must be used with great care.

More information on the functions of this device, such as the number of coefficients per function, their default values, memory addresses, etc., can be made available on request.

6.2.14 OVERVIEW OF DSP FUNCTIONS

Table 5 Overview of DSP functions

FUNCTION	EXPERT MODE	PARAMETER	VALUE	UNIT
Bass control for loudspeaker and headphone output	yes	control range	–12 to +15	dB
		resolution	1	dB
		resolution at frequency	40	Hz
Treble control for loudspeaker and headphone output	yes	control range	–12 to +12	dB
		resolution	1	dB
		resolution at frequency	14	kHz
Contour for loudspeaker output	yes	control range	0 to +18	dB
		resolution	1	dB
		resolution at frequency	40	Hz
Bass boost for loudspeaker output	yes	control range	0 to +20	dB
		resolution	2	dB
		resolution at frequency	20	Hz
		corner frequency	350	Hz
Volume control for each separate channel in loudspeaker and headphone output	no	control range	–83 to +24	dB
		resolution	1	dB
		mute position at step	10101100	
Soft-mute for loudspeaker and headphone output	no	processing time	32	ms
Spatial effects	yes	anti-phase crosstalk positions	30, 40 and 52	%
Pseudo stereo	yes	90 degree phase shift at frequency	150, 200 and 300	Hz
Beeper additional to the signal in the loudspeaker and headphone channel	yes	beep frequencies	see Section 10.3.38	
		control range	0 to –93	dB
		resolution	3	dB
		mute position at step	00100000	
AVL	yes	step width	quasi continuously	
		AVL output level for an input level between 0 and –29 dB full scale	–23	dBFS
		attack time	10	ms
		decay time constant	2, 4 and 8	s

FUNCTION	EXPERT MODE	PARAMETER	VALUE	UNIT
General	no	–3 dB lower corner frequency of DSP	10	Hz
		–1 dB bandwidth of DSP	14.5	kHz
Level adjust I^2S1 and I^2S2 inputs	yes	control range	–15 to +15	dB
		resolution	1	dB
Level adjust I^2S1 and I^2S2 outputs	yes	control range	–15 to +15	dB
		resolution	1	dB
		mute position at step	00010000	
Level adjust analog crossbar path	no	control positions	0, 3, 6 and 9	dB
Level adjust audio ADC outputs	yes	control range	+15 to –15	dB
		resolution	1	dB
Level adjust NICAM path	yes	control range	+15 to –15	dB
		resolution	1	dB
Level adjust FM path	yes	control range	+15 to –15	dB
		resolution	1	dB

6.3 Description of the analog audio section

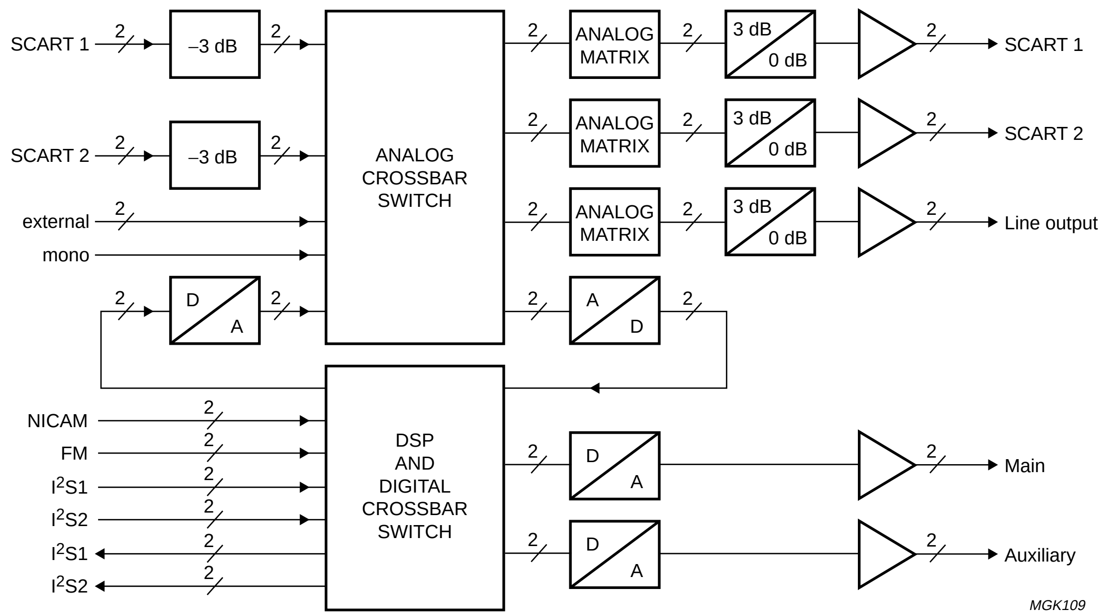


Fig.4 Block diagram for the audio section.

6.3.1 ANALOG CROSSBAR SWITCH AND ANALOG MATRIX (see also Fig.6)

There are a number of analog input and output ports with the TDA9875A. Analog source selector switches are employed to provide the desired analog signal routing capability. The analog signal routing is performed by the analog crossbar switch section. A dual audio ADC provides the connection to the DSP section and a dual audio DAC provides the connection from the DSP section to the analog crossbar switch. The digital signal routing is performed by a digital crossbar switch.

The basic signal routing philosophy of the TDA9875A is that each switch handles two signal channels at the same time, e.g. left and right, language A and B, directly at the source.

Each source selector switch is followed by an analog matrix to perform further selection tasks, such as putting a signal from one input channel, say language A, to both output channels or for swapping left and right channels. The analog matrix provides the functions given in Table 6 (see also Fig.5).

Table 6 Analog matrix functions

MODE	MATRIX OUTPUT	
	LEFT OUTPUT	**RIGHT OUTPUT**
1	left input	right input
2	right input	left input
3	left input	left input
4	right input	right input

Fig.5 Analog matrix.

All switches and matrices are controlled via the I^{2}C-bus.

6.3.2 SCART INPUTS

The SCART specification allows for a signal level of up to 2 V (rms). Because of signal handling limitations, due to the 5 V supply voltage of the TDA9875A, it is necessary to have fixed 3 dB attenuators at the SCART inputs to obtain a 2 V input. This results in a –3 dB SCART-to-SCART copy gain. If 0 dB copy gain is preferred (with maximum 1.4 V input), there are +3 dB/0 dB amplifiers at the outputs of SCART 1 and SCART 2 and at the line output.

The input attenuator is realized by an external series resistor in combination with the input impedance, both of which form a voltage divider. With this voltage divider the maximum SCART signal level of 2 V (rms) is scaled down to 1.4 V (rms) at the input pin.

6.3.3 EXTERNAL AND MONO INPUTS

The 3 dB input attenuators are not required for the external and mono inputs, because those signal levels are under control of the TV designer. The maximum allowed input level is 1.4 V (rms). By adding external series resistors, the external inputs can be used as an additional SCART input.

6.3.4 SCART OUTPUTS

The SCART outputs employ amplifiers with two gain settings. The gain can be set to +3 dB or to 0 dB via the I^{2}C-bus. The +3 dB position is needed to compensate for the 3 dB attenuation at the SCART inputs should SCART-to-SCART copies with 0 dB gain be preferred [under the condition of 1.4 V (rms) maximum input level]. The 0 dB position is needed, for example, for an external-to-SCART copy with 0 dB gain.

6.3.5 LINE OUTPUT

The line output can provide an unprocessed copy of the audio signal in the loudspeaker channels. This can be either an external signal that comes from the dual audio ADC, or a signal from an internal digital audio source that comes from the dual audio DAC. The line output employs amplifiers with two gain settings. The +3 dB position is needed to compensate for the attenuation at the SCART inputs, while the 0 dB position is needed, for example, for non-attenuated external or internal digital signals (see Section 6.3.4).

6.3.6 LOUDSPEAKER (MAIN) AND HEADPHONE (AUXILIARY) OUTPUTS

Signals from any audio source can be applied to the loudspeaker and to the headphone output channels via the digital crossbar switch and the DSP.

6.3.7 DUAL AUDIO DAC

The TDA9875A contains three dual audio DACs, one for the connection from the DSP to the analog crossbar switch section and two for the loudspeaker and headphone outputs. Each of the three dual low-noise high-dynamic range DACs consists of two 15-bit DACs with current outputs, followed by a buffer operational amplifier.
The audio DACs operate with four-fold oversampling and noise shaping.

6.3.8 DUAL AUDIO ADC

There is one dual audio ADC in the TDA9875A for the connection of the analog crossbar switch section to the DSP. The dual audio ADC consists of two bitstream 3rd-order sigma-delta audio ADCs and a high-order decimation filter.

6.3.9 STANDBY MODE

The standby mode (subaddress 1, bit 5) disables most functions and reduces power dissipation. The analog crossbar switch and the SCART section remains operational and can be controlled by the I^2C-bus to support copying of analog signals from SCART-to-SCART.

Unused internal registers may lose their information in standby mode. Therefore, the device needs to be initialized on returning to normal operation. This can be accomplished in the same way as after a power-on reset.

6.3.10 SUPPLY GROUND

The different supply grounds V_{SSX} are internally connected via substrate. Thus it is recommended to connect all ground pins externally close to the pins by a copper plane.

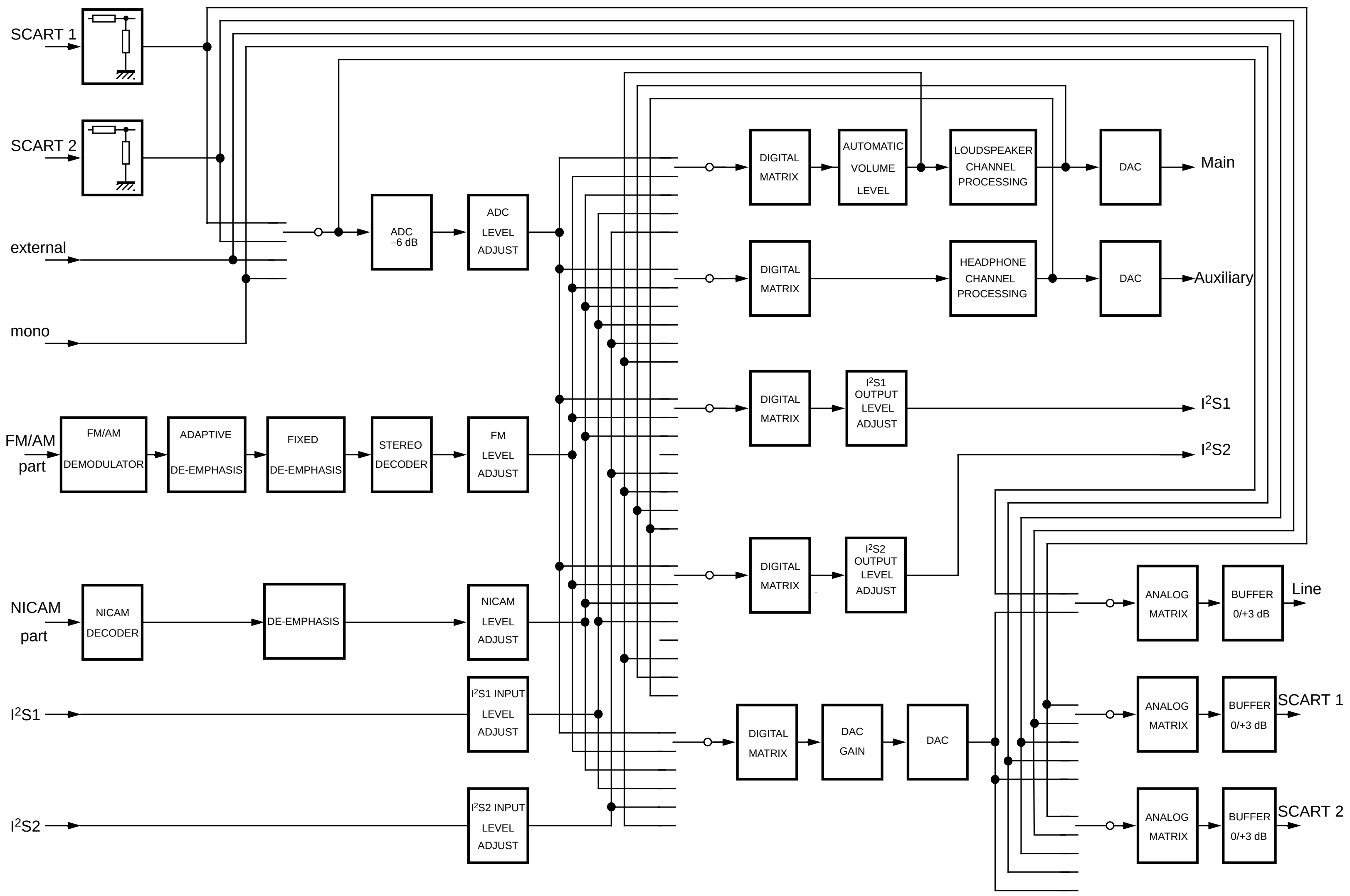


Fig.6 Audio signal flow diagram.

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	DC supply voltage		–0.5	+6.0	V
ΔV_{DD}	voltage differences between two V_{DD} pins		–	550	mV
$I_{i/o(max)}$	maximum input/output voltage		–0.5	V_{DD} + 0.5	V
I_{DDD}, I_{SSD}	DC V_{DD} or V_{SS} current per digital supply pin		–	±180	mA
$I_{lu(prot)}$	latch-up protection current		100	–	mA
P_{tot}	total power dissipation		–	1.2	W
T_{stg}	storage temperature		–55	+125	°C
T_{amb}	operating ambient temperature		–20	+70	°C
V_{es}	electrostatic handling	note 1	2000	–	V
		note 2	200	–	V

Notes

1. Human body model: C = 100 pF; R = 1.5 kΩ.
2. Machine model: C = 200 pF; L = 0.75 µH; R = 0 Ω.

8 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W

9 CHARACTERISTICS

$V_{SIF(p-p)}$ = 300 mV; AGCOFF = 0; AGCSLOW = 0; AGCLEV = 0; level and gain setting in accordance with note 3; V_{DD} = 5 V; T_{amb} = 25 °C; settings in accordance with B/G standard; FM deviation ±50 kHz; f_{mod} = 1 kHz; FM sound parameters in accordance with system A2; NICAM in accordance with *"EBU specification"*; 1 kΩ measurement source resistance for AF inputs; unless otherwise specified; with external components of Fig.8.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDD1}	digital supply voltage 1		4.75	5.0	5.5	V
V_{SSD1}	digital supply ground 1	note 1	–	0.0	–	V
I_{DDD1}	digital supply current 1	V_{DDD1} = 5.0 V	58	73	88	mA
V_{DDD2}	digital supply voltage 2		4.75	5.0	5.5	V
V_{SSD2}	digital supply ground 2	note 1	–	0.0	–	V
I_{DDD2}	digital supply current 2	V_{DDD2} = 5.0 V; SYSCLOCK off	0.1	0.4	2	mA
V_{SSD3}	digital supply ground 3	note 1	–	0.0	–	V
V_{SSD4}	digital supply ground 4	note 1	–	0.0	–	V
V_{DDA}	analog supply voltage		4.75	5.0	5.5	V
I_{DDA}	analog supply current for DAC part	V_{DDA} = 5.0 V; digital silence	44	56	68	mA
V_{SSA1}	analog ground for analog front-end	note 1	–	0.0	–	V
V_{SSA2}	analog ground for audio ADC part	note 1	–	0.0	–	V
V_{SSA3}	analog ground for audio DAC part	note 1	–	0.0	–	V
V_{SSA4}	analog ground for SCART		–	0.0	–	V
Demodulator supply decoupling and references						
V_{DEC1}	analog supply decoupling voltage for demodulator part		3.0	3.3	3.6	V
V_{ref1}	analog reference voltage for demodulator part		–	2	–	V
$I_{ref1(sink)}$	V_{ref1} sink current		–	200	–	μA
Audio supply decoupling and references						
V_{DEC2}	analog supply decoupling voltage for audio ADC part		3.0	3.3	3.6	V
V_{ref2}	reference voltage for audio ADCs	referenced to V_{DEC2}/V_{SSA2}	–	50	–	%
$Z_{Vref2\text{-}VDEC2}$	impedance V_{ref2} to V_{DEC2}		–	20	–	kΩ
$Z_{Vref2\text{-}VSSA2}$	impedance V_{ref2} to V_{SSA2}		–	20	–	kΩ
V_{ref3}	reference voltage for audio DAC and operational amplifier	referenced to V_{DDA}/V_{SSA3}	–	50	–	%
$Z_{Vref3\text{-}VDDA}$	impedance V_{ref3} to V_{DDA}		–	20	–	kΩ
$Z_{Vref3\text{-}VSSA3}$	impedance V_{ref3} to V_{SSA3}		–	20	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power fail detector						
$V_{rst(pd)}$	power fail threshold level		–	3.9	–	V
Digital inputs and outputs						
INPUTS						
CMOS level input, pull-down (pins TEST1 and TEST2)						
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DDD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDD}$	–	–	V
C_i	input capacitance		–	–	10	pF
Z_i	input impedance		–	50	–	kΩ
CMOS level input, hysteresis, pull-up (pin CRESET)						
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DDD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDD}$	–	–	V
V_{hys}	hysteresis voltage		–	1.3	–	V
C_i	input capacitance		–	–	10	pF
Z_i	input impedance		–	50	–	kΩ
INPUTS/OUTPUTS						
I^2C-bus level input with Schmitt trigger, open-drain output stage, 400 kHz I^2C operation and level (pins SCL and SDA)						
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DDD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDD}$	–	–	V
V_{hys}	hysteresis voltage		–	$0.05V_{DDD}$	–	V
I_{LI}	input leakage current		–	–	±10	μA
C_i	input capacitance		–	–	10	pF
V_{OL}	LOW-level output voltage		–	–	0.6	V
C_L	load capacitance		–	–	400	pF
TTL/CMOS level, 4 mA 3-state output stage, pull-up (pins PCLK, NICAM, ADDR1, ADDR2, P1, P2, SCK, WS, SDO1, SDO2, SDI1 and SDI2)						
V_{IL}	LOW-level input voltage		–	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	–	V
C_i	input capacitance		–	–	10	pF
V_{OL}	LOW-level output voltage		–	–	0.4	V
V_{OH}	HIGH-level output voltage		2.4	–	–	V
C_L	load capacitance		–	–	100	pF
Z_i	input impedance		–	50	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
OUTPUTS						
CMOS level output, 4 mA 3-state output stage, slew rate controlled (pin SYSCLK)						
V_{OL}	LOW-level output voltage		–	–	$0.3V_{DDD}$	V
V_{OH}	HIGH-level output voltage		$0.7V_{DDD}$	–	–	V
C_L	load capacitance		–	–	100	pF
I_{LIZ}	3-state leakage current	V_i = 0 to V_{DDD}	–	–	±10	μA
SIF1 and SIF2 analog inputs						
$V_{SIFmax(p-p)}$	maximum composite SIF input voltage for clipping (peak-to-peak value)	SIF input level adjust 0 dB	–	941	–	mV
		SIF input level adjust –10 dB	–	2976	–	mV
$V_{SIFmin(p-p)}$	minimum composite SIF input voltage for lower limit of AGC (peak-to-peak value)	SIF input level adjust 0 dB	–	59	–	mV
		SIF input level adjust –10 dB	–	188	–	mV
AGC	AGC range		–	24	–	dB
f_i	input frequency		4	–	9.2	MHz
R_i	input resistance	AGCLEV = 0	10	–	–	kΩ
C_i	input capacitance		–	7.5	11	pF
Δf_{FM}	FM deviation	B/G standard; THD < 1%	±100	–	–	kHz
$\Delta f_{FM(FS)}$	FM deviation full scale level	terrestrial FM; level adjust 0 dB	±150	–	–	kHz
C/N_{FM}	FM carrier C/N_c ratio	N_{FM} bandwidth = 6 MHz; white noise for S/N = 40 dB; *"CCIR468"*; quasi peak	–	77	–	$\frac{dB_{FM}}{Hz}$
C/N_N	NICAM carrier C/N_c ratio	N_c bandwidth = 6 MHz; bit error rate = 10^{-3}; white noise	–	66	–	$\frac{dB_N}{Hz}$
α_{ct}	crosstalk attenuation SIF1 to SIF2	f_i = 4 to 9.2 MHz; note 2	50	–	–	dB
Demodulator performance; note 3						
THD + N	total harmonic distortion plus noise	from FM source to any output; V_o = 1 V (rms) with low-pass filter	–	0.3	0.5	%
		from NICAM source to any output; V_o = 1 V (rms) with low-pass filter	–	0.1	0.3	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N	signal-to-noise ratio	SC1 from FM source to any output; V_o = 1 V (rms); *"CCIR468"*; quasi peak	64	70	–	dB
		SC2 from FM source to any output; V_o = 1 V (rms); *"CCIR468"*; quasi peak	60	66	–	dB
		NICAM source; V_o = 1 V (rms)	NICAM in accordance with *"EBU specification"*; note 4			
B_{-3}	–3 dB bandwidth	from FM source to any output	14.5	15	–	kHz
		from NICAM source to any output	14.5	15	–	kHz
FR	frequency response 20 Hz to 14 kHz	from FM or NICAM to any output; f_{ref} = 1 kHz; inclusive pre-emphasis and de-emphasis	–	±2	–	dB
$\alpha_{cs(dual)}$	dual signal channel separation	note 5	65	70	–	dB
$\alpha_{cs(stereo)}$	stereo channel separation	note 6	40	45	–	dB
α_{AM}	AM suppression for FM	AM: 1 kHz, 30% modulation; reference: 1 kHz, 50 kHz deviation	50	–	–	dB
S/N_{AM}	AM demodulation	SIF level 100 mV (rms); 54% AM; 1 kHz AF; *"CCIR468"*; quasi peak	36	45	–	dB
Identification for FM systems						
mod_p	pilot modulation for identification		25	50	75	%
C/N_p	pilot sideband C/N for identification start		–	27	–	$\frac{dB}{Hz}$
f_{ident}	identification window	B/G stereo				
		slow mode	116.85	–	118.12	Hz
		medium mode	116.11	–	118.89	Hz
		fast mode	114.65	–	120.46	Hz
		B/G dual				
		slow mode	273.44	–	274.81	Hz
		medium mode	272.07	–	276.20	Hz
		fast mode	270.73	–	277.60	Hz
$t_{ident(on)}$	total identification time ON	slow mode	–	–	2	s
		medium mode	–	–	1	s
		fast mode	–	–	0.5	s
$t_{ident(off)}$	total identification time OFF	slow mode	–	–	2	s
		medium mode	–	–	1	s
		fast mode	–	–	0.5	s

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog audio inputs						
MONO INPUT AND EXTERNAL INPUT						
$V_{i(nom)(rms)}$	nominal level input voltage (rms value)	note 3	–	500	–	mV
$V_{i(clip)(rms)}$	clipping level input voltage (rms value)	THD < 3%; note 7	1250	1400	–	mV
R_i	input resistance	note 7	28	35	42	kΩ
SCART INPUTS						
$V_{i(nom)(rms)}$	nominal level input voltage at input pin (rms value)	–3 dB divider with external 15 kΩ resistor; notes 3 and 8	–	350	–	mV
$V_{i(clip)(rms)}$	clipping level input voltage at input pin (rms value)	–3 dB divider with external 15 kΩ resistor; THD < 3%; notes 7 and 8	1250	1400	–	mV
R_i	input resistance	note 7	28	35	42	kΩ
Analog audio outputs						
LOUDSPEAKER (MAIN) AND HEADPHONE (AUXILIARY) OUTPUTS						
$V_{o(clip)(rms)}$	clipping level output voltage (rms value)	THD < 3%	1250	1400	–	mV
R_o	output resistance		150	250	375	Ω
$R_{L(AC)}$	AC load resistance		10	–	–	kΩ
$R_{L(DC)}$	DC load resistance		10	–	–	kΩ
C_L	output load capacitance		–	10	12	nF
$V_{offset(DC)}$	static DC offset voltage		–	30	70	mV
α_{mute}	mute suppression	nominal input signal from any source; f_i = 1 kHz; note 3	80	–	–	dB
$G_{ro(main,aux)}$	roll-off gain at 14.5 kHz for Main and Auxiliary channels	from any source	–3	–2	–	dB
$PSRR_{main,aux}$	power supply ripple rejection for Main and Auxiliary channels	f_{ripple} = 70 Hz; V_{ripple} = 100 mV (peak); C_{Vref} = 47 μF; signal from I^2S-bus	40	45	–	dB
SCART OUTPUTS AND LINE OUTPUT						
$V_{o(nom)(rms)}$	nominal level output voltage (rms value)	+3 dB amplification; note 3	–	500	–	mV
$V_{o(clip)(rms)}$	clipping level output voltage (rms value)	THD < 3%	1250	1400	–	mV
R_o	output resistance		150	250	375	Ω
$R_{L(AC)}$	AC load resistance		10	–	–	kΩ
$R_{L(DC)}$	DC load resistance		10	–	–	kΩ
C_L	output load capacitance		–	–	2.5	nF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{offset(DC)}$	static DC offset voltage	output amplifiers at +3 dB position	–	30	50	mV
α_{mute}	mute suppression	nominal input signal from any source; f_i = 1 kHz; note 3	80	–	–	dB
B	bandwidth	from SCART, external and mono sources; –3 dB bandwidth	20	–	–	kHz
		from DSP sources; –3 dB bandwidth	14.5	–	–	kHz
PSRR	power supply ripple rejection	f_{ripple} = 70 Hz; V_{ripple} = 100 mV (peak); C_{Vref} = 47 μF; signal from I²S-bus	40	45	–	dB
Audio performance						
THD + N	total harmonic distortion plus noise	$V_i = V_o$ = 1 V (rms); f_i = 1 kHz; bandwidth 20 Hz to 15 kHz; note 9				
		from any analog audio input to I²S-bus	–	0.1	0.3	%
		from I²S-bus to any analog audio output	–	0.1	0.3	%
		SCART-to-SCART copy	–	0.1	0.3	%
		SCART-to-Main copy	–	0.2	0.5	%
S/N	signal-to-noise ratio	reference voltage V_o = 1.4 V (rms); f_i = 1 kHz; *“CCIR468”*; quasi peak; note 9				
		from any analog audio input to I²S-bus	73	77	–	dB
		from I²S-bus to any analog audio output	78	85	–	dB
		SCART-to-SCART copy	78	85	–	dB
		SCART-to-Main copy	73	77	–	dB
α_{ct}	crosstalk attenuation	between any analog input pairs; f_i = 1 kHz	70	–	–	dB
		between any analog output pairs; f_i = 10 kHz	65	–	–	dB
α_{cs}	channel separation	between left and right of any input pair	65	–	–	dB
		between left and right of any output pair	60	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
G_A	gain from SCART-to-SCART with –3 dB input voltage divider	output amplifier in +3 dB position; R_{ext} = 15 kΩ ±10%	–1.5	0	+1.1	dB
		output amplifier in 0 dB position; R_{ext} = 15 kΩ ±10%	–4.5	–3.0	–1.9	dB
Crystal specification (fundamental mode)						
f_{xtal}	crystal frequency		–	24.576	–	MHz
C_L	load capacitance		–	20	–	pF
C_1	series capacitance		–	20	–	fF
C_0	parallel capacitance		–	–	7	pF
Φ_{pull}	pulling sensitivity	C_L changed from 18 to 16 pF	–	25	–	$\frac{10^{-6}}{pF}$
R_R	equivalent series resistance	at nominal frequency	–	–	30	Ω
R_N	equivalent series resistance of unwanted mode		$2R_R$	–	–	Ω
ΔT	temperature range		–20	+25	+70	°C
X_J	adjustment tolerance		–	–	±30	10^{-6}
X_D	drift	across temperature range	–	–	±30	10^{-6}
X_A	ageing		–	–	±5	$\frac{10^{-6}}{year}$

Notes to the characteristics

1. All analog and digital supply ground pins are connected internally.
2. Set demodulator to AM mode. Apply an AM carrier (with 1 kHz and 100%) to one channel. Check AGC step. Switch AGC off and set AGC to the gain step found. Measure the 1 kHz signal level of this channel and take it as a reference. Switch to the other SIF input to which no signal is connected and which is terminated with 50 Ω. Measure now the 1 kHz crosstalk signal level. The SIF source resistance should be low (50 Ω).
3. Definitions of levels and level setting:
   The full-scale level for analog audio signals is V_{FS} = 1.4 V (rms). The nominal level at the digital crossbar switch is defined at –15 dBFS.
   Nominal audio input levels:
   extern, mono: 500 mV (rms); –9 dBFS.
   See also Tables 7 and 8.
4. Audio performance is limited by the dynamic range of the NICAM728 system. Due to compansion, the quantization noise is never lower than –62 dB (unweighted rms) with respect to the input level.
5. FM source; in dual mode only A (respectively B) signal modulated; measured at B (respectively A) channel output; V_o = 1 V (rms) of modulated channel.
6. FM source; in stereo mode only L (respectively R) signal modulated; measured at R (respectively L) channel output; V_o = 1 V (rms) of modulated channel. The stereo channel separation may be limited by adjustment tolerances of the transmitter.
7. If the supply voltage for the TDA9875A is switched off, because of the ESD protection circuitry, all audio input pins are short-circuited. To avoid a short-circuit at the SCART inputs a 15 kΩ resistor (–3 dB divider) has to be used.
8. The SCART specification allows a signal level of up to 2 V (rms). Because of signal handling limitations due to the 5 V supply voltage for the TDA9875A, there is a need for fixed 3 dB attenuators at the SCART inputs. To achieve SCART-to-SCART copies with 0 dB gain, there are +3 dB/0 dB amplifiers at the outputs of SCART 1 and SCART 2 and at the line output. The attenuator is realized by an internal resistor that works together with an external series resistor as a voltage divider. With this voltage divider the maximum SCART input signal level of 2 V (rms) is scaled down to 1.4 V (rms) at the input pin. To avoid clipping, the +3 dB gain must not be used if the SCART input signal is larger than 1.4 V (rms).
9. ADC level adjust = +6 dB, all other level adjusts = 0 dB, if external –3 dB divider is used set output buffer gain to +3 dB, tone control to 0 dB, AVL off and volume control to 0 dB.

Table 7 Level setting FM, AM and NICAM

0 dBFS = 1.4 V (rms), FS means full scale; note 1.

STANDARD	MODE	TRANSMITTER NOMINAL MODULATION DEPTH	NOMINAL LEVEL AT DEMODULATOR OUTPUT	CARRIER	FREQUENCY	MODE	IDENTIFICATION	DE-EMPHASIS	FM/ NICAM LEVEL ADJUST
M	2 channel	15 kHz deviation	–24 dBFS; note 2	1	4.5 MHz	FM	–	75 µs	+9 dB
				2	4.724 MHz	FM	on	75 µs	+9 dB
B/G	2 channel	27 kHz deviation	–19 dBFS	1	5.5 MHz	FM	–	50 µs	+4 dB
				2	5.742 MHz	FM	on	50 µs	+4 dB
B/G	NICAM	–11.2 dBFS	–18 dBFS	1	5.5 MHz	FM	–	50 µs	+4 dB
				2	5.85 MHz	NICAM	off	J17	+3 dB
I	NICAM	–15.8 dBFS	–23 dBFS	1	6.0 MHz	FM	–	50 µs	+4 dB
				2	6.552 MHz	NICAM	off	J17	+8 dB
D/K	2 channel	27 kHz deviation	–19 dBFS	1	6.5 MHz	FM	–	50 µs	+4 dB
				2	6.742 MHz	FM	on	50 µs	+4 dB
D/K	2 channel	27 kHz deviation	–19 dBFS	1	6.5 MHz	FM	–	50 µs	+4 dB
				2	6.25 MHz	FM	on	50 µs	+4 dB
D/K	2 channel	27 kHz deviation	–19 dBFS	1	6.5 MHz	FM	–	50 µs	+4 dB
				2	5.742 MHz	FM	on	50 µs	+4 dB
D/K	NICAM	–11.2 dBFS	–18 dBFS	1	6.5 MHz	FM	–	50 µs	+4 dB
				2	5.85 MHz	NICAM	off	J17	+3 dB
L/L accent	NICAM	54% AM	–19 dBFS	1	6.5 MHz	AM	–	50 µs	+5 dB
				2	5.85 MHz	NICAM	off	J17	+3 dB

Notes

1. Nominal level at digital crossbar is defined at –15 dBFS. DAC gain setting 6 dB. Output buffer setting 0 dB. Nominal SCART output level 500 mV (rms).
2. For stereo signals the output level is 6 dB lower. The level adjust has to be increased by 6 dB.

–

Table 8 Level setting SAT FM

0 dBFS = 1.4 V (rms), FS means full scale.

SOURCE	TRANSMITTER MAXIMUM MODULATION DEPTH	NOMINAL LEVEL AT DEMODULATOR OUTPUT	FM LEVEL ADJUST SETTING	MAXIMUM LEVEL AT CROSSBAR	DAC GAIN SETTING	OUTPUT BUFFER	NOMINAL SCART OUTPUT VOLTAGE
SAT FM, stereo	50 kHz deviation	–13 dBFS	4 dB	–9 dBFS	6 dB	0 dB	1 V (rms)
SAT FM, mono	85 kHz deviation	–9 dBFS	0 dB				

10 I^{2}C-BUS CONTROL

10.1 Introduction

The TDA9875A is fully controlled via the I^{2}C-bus. Control is exercised by writing data to one or more internal registers. Status information can be read from an array of registers to enable the controlling microcontroller determine whether any action is required.

The device has an I^{2}C-bus slave transceiver, in accordance with the fast-mode specification, with a maximum speed of 400 kbits/s. Information concerning the I^{2}C-bus can be found in brochure *"I^{2}C-bus and how to use it"* (order number 9398 393 40011). To avoid conflicts in a real application with other ICs providing similar or complementary functions, there are four possible slave addresses available which can be selected by pins ADDR1 and ADDR2 (see Table 9).

Table 9 Possible slave addresses

ADDR2	ADDR1	SLAVE ADDRESS A6 TO A0
0	0	1 0 1 1 0 0 0
0	1	1 0 1 1 0 0 1
1	0	1 0 1 1 0 1 0
1	1	1 0 1 1 0 1 1

The I^{2}C-bus interface remains operational in the standby mode of the TDA9875A to allow control of the analog source selectors with regard to SCART-to-SCART copying.

The device will not respond to a 'general call' on the I^{2}C-bus, i.e. when a slave address of 0000000 is sent by a master.

The data transmission between the microcontroller and the other I^{2}C-bus controlled ICs is not disturbed when the supply voltage of the TDA9875A is not connected.

10.2 Power-up state

At power-up the device is in the following state:

- All outputs muted
- No sound carrier frequency loaded
- General-purpose I/O pins ready for input (HIGH)
- Input SIF1 selected with:
  - AGC on
  - Small hysteresis
  - SIF input level shift 0 dB.
- Demodulators for both sound carriers set to FM with:
  - Identification for B/G, D/K, response time 1 s
  - Level adjust set to 0 dB
  - De-emphasis 50 µs
  - Matrix set to mono.
- Main channel set to FM input with:
  - Spatial off
  - Pseudo off
  - AVL off
  - Volume mute
  - Bass flat
  - Treble flat
  - Contour off
  - Bass boost flat.
- Auxiliary channel set to FM input with:
  - Volume mute
  - Bass flat
  - Treble flat.
- Feature interface all outputs off
- Beeper off
- Monitoring of carrier 1 FM demodulator DC output.

After power-up a device initialization has to be performed via the I^{2}C-bus to put the TDA9875A into the proper mode of operation, in accordance with the desired TV standard, audio control settings, etc.

10.3 Slave receiver mode

As a slave receiver, the TDA9875A provides 46 registers for storing commands and data. These registers are accessed via so-called subaddresses. A subaddress can be thought of as a pointer to an internal memory location.

Table 10 I^2C-bus; slave address, subaddress and data format

S	SLAVE ADDRESS	0	ACK	SUBADDRESS	ACK	DATA	ACK	P

Table 11 Explanation of Table 10

BIT	FUNCTION
S	START condition
SLAVE ADDRESS	7-bit device address
0	data direction bit (write to device)
ACK	acknowledge by slave
SUBADDRESS	address of register to write to
DATA	data byte to be written into register
P	STOP condition

It is allowed to send more than one data byte per transmission to the TDA9875A. In this event, the subaddress is automatically incremented after each data byte, resulting in storing the sequence of data bytes at successive register locations, starting at SUBADDRESS. A transmission can start at any valid subaddress. Each byte is acknowledged with ACK (acknowledge).

There is no ‘wrap-around’ of subaddresses.

Commands and data are processed as soon as they have been completely received. Functions requiring more than one byte will, thus, be executed only after all bytes for that function have been received. If the transmission is terminated (STOP condition) before all bytes have been received, the incomplete data for that function are ignored.

Table 12 Format for a transmission employing auto-increment of subaddresses

S	SLAVE ADDRESS	0	ACK	SUBADDRESS	ACK	DATA BYTE A(1)	DATA	ACK	P

Note

1. n data bytes with auto-increment of subaddresses.

Data patterns sent to the various subaddresses are not checked for being illegal or not at that address, except for the functions of volume, bass, treble control, bass boost and level adjust.

Detection of a STOP condition without a preceding acknowledge bit is regarded as a bus error. The last operation will not then be executed.

Table 13 Overview of the slave receiver registers

SUBADDRESS (DECIMAL)	DATA								FUNCTION
	MSB							LSB	
0	0	0	s	g	g	g	g	g	AGC level shift, AGC gain selection
1	c	c	c	c	c	c	c	c	general configuration
2	p	0	0	m	m	s	s	s	monitor select, peak detector on/off
3	f	f	f	f	f	f	f	f	carrier 1 frequency; MS part
4	f	f	f	f	f	f	f	f	carrier 1 frequency
5	f	f	f	f	f	f	f	f	carrier 1 frequency; LS part
6	f	f	f	f	f	f	f	f	carrier 2 frequency; MS part
7	f	f	f	f	f	f	f	f	carrier 2 frequency
8	f	f	f	f	f	f	f	f	carrier 2 frequency; LS part
9	c	c	c	c	c	c	c	c	demodulator configuration
10	d	d	d	d	d	d	d	d	FM de-emphasis
11	0	0	0	0	0	m	m	m	FM matrix
12	0	0	0	l	l	l	l	l	channel 1 output level adjust
13	0	0	0	l	l	l	l	l	channel 2 output level adjust
14	t	t	0	c	0	c	c	c	NICAM configuration
15	0	0	0	l	l	l	l	l	NICAM output level adjust
16	l	l	l	l	l	l	l	l	NICAM lower error limit
17	u	u	u	u	u	u	u	u	NICAM upper error limit
18	m	m	m	m	m	m	m	m	audio mute control
19	g	m	m	m	g	s	s	s	DAC output select
20	0	g	m	m	0	s	s	s	SCART 1 output select
21	0	g	m	m	0	s	s	s	SCART 2 output select
22	0	g	m	m	0	0	0	s	line output select
23	s	s	s	l	l	l	l	l	ADC output select
24	0	m	m	m	0	s	s	s	Main channel select
25	0	0	s	s	p	p	a	a	audio effects (AVL, pseudo, spatial)
26	v	v	v	v	v	v	v	v	volume control, Main left
27	v	v	v	v	v	v	v	v	volume control, Main right
28	0	0	0	c	c	c	c	c	contour control, Main
29	0	0	0	b	b	b	b	b	bass control, Main
30	0	0	0	t	t	t	t	t	treble control, Main
31	0	m	m	m	0	s	s	s	Auxiliary channel select
32	v	v	v	v	v	v	v	v	volume control, Auxiliary left
33	v	v	v	v	v	v	v	v	volume control, Auxiliary right
34	0	0	0	b	b	b	b	b	bass control, Auxiliary
35	0	0	0	t	t	t	t	t	treble control, Auxiliary
36	0	0	0	c	c	c	c	c	feature interface configuration
37	0	m	m	m	0	s	s	s	I^2S1 output select

SUBADDRESS (DECIMAL)	DATA								FUNCTION
	MSB							LSB	
38	0	0	0	i	i	i	i	i	I^2S1 input level adjust
39	0	0	0	o	o	o	o	o	I^2S1 output level adjust
40	0	m	m	m	0	s	s	s	I^2S2 output select
41	0	0	0	i	i	i	i	i	I^2S2 input level adjust
42	0	0	0	o	o	o	o	o	I^2S2 output level adjust
43	0	0	0	0	0	f	f	f	beeper frequency
44	0	0	v	v	v	v	v	v	beeper volume, Main and Auxiliary
45	b	b	b	b	b	b	b	b	bass boost, Main left and right

The following sub-sections provide a detailed description of the slave receiver registers:

10.3.1 AGC GAIN REGISTER

10.3.1.1 Description

If the automatic gain control function is switched off in the general configuration register, the contents of this register will define a fixed gain of the AGC stage. The input voltages given are meant to generate a full scale output from the SIF ADC. If automatic gain control is on, the AGCGAIN setting is ignored. After switching off the automatic gain control function, the latest gain control setting is copied to the AGC gain register. If the AGC input level shift bit AGCLEV is set to HIGH the input signal is scaled with –10 dB. The AGCLEV bit is also active if the automatic gain function is enabled.

It should be noted that the input voltages should be considered as approximate target values.

Table 14 Description of the AGC gain register

BIT	NAME	DESCRIPTION
7 (MSB)	–	Set to logic 0
6	–	Set to logic 0
5	AGCLEV	If the AGC input level shift bit AGCLEV is set to HIGH the input signal is scaled with –10 dB. The AGCLEV bit is also active if the automatic gain function is enabled.
4	AGCGAIN	If the automatic gain control function is switched off in the general configuration register, the contents of this register will define a fixed gain of the AGC stage.
3		
2		
1		
0 (LSB)		

10.3.1.2 Definition

Table 15 Subaddress 0

MSB							LSB	AGC GAIN (dB)	SIF INPUT VOLTAGE (mV (p-p))
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**		
0	0	0/1	1	1	1	1	1	0.0	941/2976
0	0	0/1	1	1	1	1	0	0.8	861/2723
0	0	0/1	1	1	1	0	1	1.5	788/2490
0	0	0/1	1	1	1	0	0	2.3	720/2278
0	0	0/1	1	1	0	1	1	3.1	659/2084
0	0	0/1	1	1	0	1	0	3.9	603/1906
0	0	0/1	1	1	0	0	1	4.6	551/1744
0	0	0/1	1	1	0	0	0	5.4	504/1595
0	0	0/1	1	0	1	1	1	6.2	461/1459
0	0	0/1	1	0	1	1	0	7.0	422/1334
0	0	0/1	1	0	1	0	1	7.7	386/1221
0	0	0/1	1	0	1	0	0	8.5	353/1117
0	0	0/1	1	0	0	1	1	9.3	323/1021
0	0	0/1	1	0	0	1	0	10.1	295/934
0	0	0/1	1	0	0	0	1	10.8	270/855
0	0	0/1	1	0	0	0	0	11.6	247/782
0	0	0/1	0	1	1	1	1	12.4	226/715
0	0	0/1	0	1	1	1	0	13.2	207/654
0	0	0/1	0	1	1	0	1	13.9	189/598
0	0	0/1	0	1	1	0	0	14.7	173/547
0	0	0/1	0	1	0	1	1	15.5	158/501
0	0	0/1	0	1	0	1	0	16.3	145/458
0	0	0/1	0	1	0	0	1	17.0	132/419
0	0	0/1	0	1	0	0	0	17.8	121/383
0	0	0/1	0	0	1	1	1	18.6	111/350
0	0	0/1	0	0	1	1	0	19.4	101/321
0	0	0/1	0	0	1	0	1	20.1	93/293
0	0	0/1	0	0	1	0	0	20.9	85/268
0	0	0/1	0	0	0	1	1	21.7	78/245
0	0	0/1	0	0	0	1	0	22.5	71/224
0	0	0/1	0	0	0	0	1	23.2	65/205
0	0	0/1	0	0	0	0	0	24.0	59/188(note 1)

Note

1. The default setting at power-up is 00000000.

10.3.2 GENERAL CONFIGURATION REGISTER

10.3.2.1 Description

Table 16 Description of Table 17

NAME	HIGH/LOW	FUNCTION
SIFSEL	HIGH	Selects pin SIF2 for input (recommended for satellite tuner).
	LOW	Pin SIF1 (terrestrial TV) is selected.
AGCOFF	HIGH	Forces the AGC block to a fixed gain as defined in the AGC gain register.
	LOW	The automatic gain control function is enabled and the contents of the AGC gain register is ignored.
AGCSLOW	HIGH	A longer decay time is selected for input signals with strong video modulation (intercarrier). This bit only has an effect when bit AGCOFF = 0.
	LOW	Selects normal attack and decay times for the AGC.
CLRPOR	HIGH	Resets the power fail detector to LOW.
	LOW	This bit is automatically reset to LOW after bit POR in the device status register has been reset.
INIT	HIGH	Causes initialization of TDA9875A to its default settings. This has the same effect as a power-on reset. If there is a conflict between the default settings and any bit set HIGH in this register, the bits of this register have priority over the corresponding default setting.
	LOW	This bit is automatically reset to LOW after initialization. When set LOW, the TDA9875A is in its normal mode of operation.
STDBY	HIGH	Puts the TDA9875A into the standby mode. Most functions are disabled and power dissipation is somewhat reduced, but the analog selectors/matrices remain operational to support analog copying from SCART-to-SCART.
	LOW	The TDA9875A is in its normal mode of operation. On return from standby mode, the device is in its power-on reset mode and needs to be re-initialized.
P1OUT, P2OUT	–	These bits control the general purpose input/output pins. The contents of these bits is written directly to the corresponding pins. If input is desired, the bits must be set HIGH to allow the pins to be pulled LOW externally. Input from the pins is reflected in the device status register (see Section 10.4, subaddress 0). P1OUT is recommended to be used for switching an SIF trap for the adjacent picture carrier in designs that employ such a trap.

10.3.2.2 Definition

Table 17 Subaddress 1 (note 1)

BIT	NAME	DESCRIPTION
7 (MSB)	P2OUT	general purpose I/O pin 2
6	P1OUT	general purpose I/O pin 1
5	STDBY	standby mode on/off
4	INIT	initialize to defaults (as reset)
3	CLRPOR	clear power-on reset flip-flop
2	AGCSLOW	AGC decay time
1	AGCOFF	AGC on/off
0 (LSB)	SIFSEL	SIF input select

Note

1. The default setting at power-up is 11000000.

10.3.3 MONITOR SELECT REGISTER

10.3.3.1 Description

This register is used to define the signal source, the level of which is to be monitored, and if the peak level is to be monitored. Peak level refers to the magnitude of the maximum excursion of a signal. Data can be read-out in the I^{2}C-bus slave transmitter mode (see Section 10.4, subaddresses 5 and 6).

Audio magnitude/phase is related to the FM demodulator output. Phase information is provided, when it operates in FM mode, while magnitude is supplied in AM mode.

Table 18 Description of bit PEAKMON

NAME	HIGH/LOW	FUNCTION
PEAKMON	HIGH	selects the peak level of a source to be monitored
	LOW	the last sample will be supplied

10.3.3.2 Definition

Table 19 Subaddress 2 (note 1)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
PEAKMON	0	0	see Table 21		see Table 20		

Note

1. The default setting at power-up is 00000000.

Table 20 Signal source (note 1)

B2	B1	B0	SIGNAL SOURCE
0	0	0	DC output of FM demodulator
0	0	1	audio magnitude/phase, FM demodulator output
0	1	0	crossbar input from FM/AM channel
0	1	1	crossbar input from NICAM channel
1	0	0	crossbar input from I^{2}S1 channel
1	0	1	crossbar input from I^{2}S2 channel
1	1	0	crossbar input from audio ADC channel
1	1	1	input to Main channel DAC (without beeper)

Note

1. The term ‘crossbar’ refers to the digital selector, where level-adjusted signals from various sources are available.

Table 21 Monitor output

B4	B3	MONITOR OUTPUT
0	0	$\frac{\text{L input} + \text{R input}}{2}$
0	1	L input (channel 1, respectively)
1	0	R input (channel 2, respectively)

10.3.3.3 Note

By reading out level read-out registers (subaddresses 5 and 6, see Section 10.4), the current peak level will be reset.

10.3.4 CARRIER 1 FREQUENCY REGISTER

10.3.4.1 Description

The three bytes together constitute a 24-bit frequency control word to represent the sound carrier (i.e. mixer) frequency in accordance with the following formula:

$$\text{data} = \frac{f_{mix}}{f_{clk}} \times 2^{24}$$

Where:

data = 24-bit frequency control word.

f_{mix} = desired sound carrier frequency.

f_{clk} = 12.288 MHz (clock frequency of mixer).

2^{24} = 16777216 (number of steps in a 24-bit word size).

Example: A 5.5 MHz sound carrier frequency will be generated by sending the following sequence of data bytes to the TDA9875A (data = 7509333 in decimal notation or 729555 in hex): 01110010 10010101 01010101.

As three bytes are required to define a carrier frequency, execution of this command starts only after all bytes have been received. If an error occurs, e.g. a premature STOP condition, partial data for this function is ignored.

The default setting at power-up is 00000000 for all three bytes.

10.3.4.2 Definition

Most significant part at subaddress 3.

Table 22 Subaddresses 3 to 5

BIT	SUBADDRESSES
7 (MSB)	3
6	
5	
4	
3	
2	
1	
0	
7	4
6	
5	
4	
3	
2	
1	
0	
7	5
6	
5	
4	
3	
2	
1	
0 (LSB)	

10.3.5 CARRIER 2 FREQUENCY REGISTER

10.3.5.1 Description

Same as for sound carrier 1.

If the carrier 2 frequency register is used, it will be for either the second FM sound carrier of a terrestrial or satellite FM program or the NICAM sound carrier.

10.3.5.2 Definition

Subaddresses 6 to 8.

Same as for sound carrier 1, except for subaddresses used.

10.3.6 DEMODULATOR CONFIGURATION REGISTER

10.3.6.1 Description

Table 23 Description of subaddress 9 (notes 1 and 2)

NAME	HIGH/LOW	FUNCTION
CH1MODE	HIGH	selects the hardware for the first sound carrier to operate in AM mode
	LOW	FM mode is assumed. This applies to both terrestrial and satellite FM reception.
FILTBW0, FILTBW1	–	selects the filter bandwidth for channel 1 and channel 2 in accordance with Table 26
CH2MOD0, CH2MOD1	–	These bits control the hardware for the second sound carrier in accordance with the truth Table 25. The NICAM mode employs a wider bandwidth of the decimation filters than the FM mode.
IDAREA	HIGH	selects FM identification frequencies in accordance with the specification for Korea
	LOW	frequencies for Europe are selected (B/G and D/K standard)
IDMOD0, IDMOD1	–	These bits define the response time after which a sound mode identification result may be expected. The longer the time, the more reliable the identification.

Notes

1. It is recommended to switch the FM sound mode identification off whenever the received program is not a terrestrial 2-carrier sound.
2. Switching the identification off will reset the associated hardware to a defined state.

10.3.6.2 Definition

Table 24 Subaddress 9 (note 1; see Table 23)

BIT	NAME	DESCRIPTION
7 (MSB)	IDMOD1	response time for FM sound mode identification
6	IDMOD0	
5	IDAREA	application area for FM identification
4	FILTBW1	selects filter bandwidth in accordance with Table 26
3	CH2MOD1	channel 2 receive mode
2	CH2MOD0	
1	FILTBW0	selects filter bandwidth in accordance with Table 26
0 (LSB)	CH1MODE	channel 1 receive mode

Note

1. The default setting at power-up is 00000000.

Table 25 Channel 2 receive mode (see Table 24)

B3	B2	CHANNEL 2
0	0	FM
0	1	AM
1	0	NICAM

Table 26 Filter bandwidth channel 1/channel 2 (see Table 24)

B4	B1	FILTER BANDWIDTH CH1/CH2	FILTER MODES
0	0	narrow/narrow	recommended for nominal terrestrial broadcast conditions and SAT with 2 carriers
0	1	extra wide/narrow	recommended only for high-deviation SAT mono carriers (e.g. obsolete main channel on Astra)
1	0	medium/medium	recommended for moderately overmodulated broadcast conditions
1	1	wide/wide	recommended for strongly overmodulated broadcast conditions

Table 27 Identification mode (see Table 24)

B7	B6	IDENT MODE
0	0	slow
0	1	medium
1	0	fast
1	1	off/reset

10.3.7 FM DE-EMPHASIS REGISTER

10.3.7.1 Description

This register is used to select the proper de-emphasis characteristics as appropriate for the standard of the received carrier. Bits B3 to B0 apply to sound carrier 1, bits B7 to B4 apply to sound carrier 2. In the event of A2 reception, both groups must be set to the same characteristics.

10.3.7.2 Definition

Table 28 Subaddress 10 (note 1)

BIT	NAME	DESCRIPTION
7 (MSB)	ADEEM2	adaptive de-emphasis on/off
6		time constant selection for FM de-emphasis
5		
4		
3	ADEEM1	adaptive de-emphasis on/off
2		time constant selection for FM de-emphasis
1		
0 (LSB)		

Note

1. The default setting at power-up is 00000000.

Table 29 De-emphasis

B6, B2	B5, B1	B4, B0	DE-EMPHASIS
0	0	0	50 μs (Europe)
0	0	1	60 μs
0	1	0	75 μs (M standard)
0	1	1	J17
1	0	0	off

Table 30 Description of bits ADEEM1 and ADEEM2 (note 1)

NAME	HIGH/LOW	FUNCTION
ADEEM1, ADEEM2	HIGH	Activates the adaptive de-emphasis function, which is required for certain satellite FM channels. The standard FM de-emphasis must then be set to 75 μs.
	LOW	the adaptive de-emphasis is off

Note

1. The FM de-emphasis gain is 0 dB at 40 Hz.

10.3.8 FM MATRIX REGISTER

10.3.8.1 Description

This register is used to select the proper dematrixing characteristics as appropriate for the standard of the received carrier and the related sound mode identification.

10.3.8.2 Definition

Table 31 Subaddress 11 (note 1)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	see Table 32		

Note

1. The default setting at power-up is 00000000.

Table 32 Description of Subaddress 11 (bits B2 to B0)

B2	B1	B0	L OUTPUT	R OUTPUT	MODE
0	0	0	CH1 input; note 1	CH1 input; note 1	mono 1
0	0	1	CH2 input; note 2	CH2 input; note 2	mono 2
0	1	0	CH1 input; note 1	CH2 input; note 2	dual
0	1	1	CH2 input; note 2	CH1 input; note 1	dual swapped
1	0	0	$2\mathrm{CH1\ input} - \mathrm{CH2\ input}$	CH2 input; note 2	stereo Europe
1	0	1	$\frac{\mathrm{CH1\ input} + \mathrm{CH2\ input}}{2}$	$\frac{\mathrm{CH1\ input} - \mathrm{CH2\ input}}{2}$	stereo Korea; note 3

Notes

1. CH1: audio signal from FM channel 1.
2. CH2: audio signal from FM channel 2.
3. See Table 7. For stereo Korea the dematrix applies 6 dB attenuation

10.3.9 FM CHANNEL 1 LEVEL ADJUST REGISTER

10.3.9.1 Description

This register is used to correct for standard and station-dependent differences of signal levels. Table 33 applies to sound carrier 1.

10.3.9.2 Definition

Table 33 Subaddress 12

MSB							LSB	GAIN SETTING (dB)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0 (note 1)
0	0	0	1	1	1	1	1	–1
0	0	0	1	1	1	1	0	–2
0	0	0	1	1	1	0	1	–3
0	0	0	1	1	1	0	0	–4
0	0	0	1	1	0	1	1	–5
0	0	0	1	1	0	1	0	–6
0	0	0	1	1	0	0	1	–7
0	0	0	1	1	0	0	0	–8
0	0	0	1	0	1	1	1	–9
0	0	0	1	0	1	1	0	–10
0	0	0	1	0	1	0	1	–11
0	0	0	1	0	1	0	0	–12
0	0	0	1	0	0	1	1	–13
0	0	0	1	0	0	1	0	–14
0	0	0	1	0	0	0	1	–15
0	0	0	1	0	0	0	0	mute

Note

1. The default setting at power-up is 00000000.

10.3.10 FM CHANNEL 2 LEVEL ADJUST REGISTER

10.3.10.1 Description

This register is used to correct for standard and station-dependent differences of signal levels. Table 34 applies to sound carrier 2 in its FM and AM modes. In the event of A2, channels 1 and 2 should be adjusted to the same level.

10.3.10.2 Definition

Table 34 Subaddress 13

MSB							LSB	GAIN SETTING (dB)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0 (note 1)
0	0	0	1	1	1	1	1	–1
0	0	0	1	1	1	1	0	–2
0	0	0	1	1	1	0	1	–3
0	0	0	1	1	1	0	0	–4
0	0	0	1	1	0	1	1	–5
0	0	0	1	1	0	1	0	–6
0	0	0	1	1	0	0	1	–7
0	0	0	1	1	0	0	0	–8
0	0	0	1	0	1	1	1	–9
0	0	0	1	0	1	1	0	–10
0	0	0	1	0	1	0	1	–11
0	0	0	1	0	1	0	0	–12
0	0	0	1	0	0	1	1	–13
0	0	0	1	0	0	1	0	–14
0	0	0	1	0	0	0	1	–15
0	0	0	1	0	0	0	0	mute

Note

1. The default setting at power-up is 00000000.

10.3.11 NICAM CONFIGURATION REGISTER

10.3.11.1 Description

Table 35 Description of Table 36 (notes 1 and 2)

NAME	HIGH/LOW	FUNCTION
AMUTE	HIGH	Automatic muting is disabled. This bit has only an effect when the second sound carrier is set to NICAM.
	LOW	enables the automatic switching between NICAM and the program on the first sound carrier (i.e. FM mono or AM), dependent on the NICAM bit error rate
NDEEM	HIGH	switches the NICAM J17 de-emphasis off
	LOW	switches the NICAM J17 de-emphasis on
AMSEL	HIGH	The auto-mute function will switch the output sound from NICAM L to the ADC output select register. With the ADC output select register the wanted signal source, e.g. the mono input, can be pre-set (subaddress 23, see Section 10.3.20). This is useful, if the AM sound NICAM L systems is demodulated externally.
	LOW	The auto-mute function will switch the output sound from NICAM L to the AM program on the internal first sound carrier.
DOUTEN	HIGH	enables the output of the NICAM serial data stream from the DQPSK demodulator and of the associated clock, PCLK
	LOW	both outputs will be 3-stated
DCXOTEST	HIGH	DCXO test mode on (available only during FM mode); note 3
	LOW	DCXO normal mode
DCXOPULL	HIGH	during DCXO test mode set to lower DCXO frequency
	LOW	during DCXO test mode set to higher DCXO frequency

Notes

1. The decision of whether auto-muting is permitted shall be taken by the controlling microcontroller based on information contained in the TDA9875A’s status registers. Thus, it depends on the strategy implemented in the software whether the auto-mute function is in accordance with *“NICAM 728 ETS Revised for Data Applications”* or any other preference.
2. The NICAM de-emphasis gain is 0 dB at 40 Hz.
3. The DCXO test mode is intended for checking the DCXO control range with the actually used PCB layout and crystal type. During normal operation, the DCXO test mode should not be used.

10.3.11.2 Definition

Table 36 Subaddress 14 (note 1)

BIT	NAME	DESCRIPTION
7 (MSB)	DCXOPULL	selects DCXO lower/upper test frequency
6	DCXOTEST	selects DCXO test mode (available only during FM mode)
5	0	set logic to 0
4	DOUTEN	data output enable
3	0	set logic to 0
2	AMSEL	selects auto-muting signal source
1	NDEEM	de-emphasis on/off
0 (LSB)	AMUTE	auto-muting on/off

Note

1. The default setting at power-up is 00000000.

10.3.12 NICAM LEVEL ADJUST REGISTER

10.3.12.1 Description

This register is used to correct for standard and station-dependent differences of signal levels. Table 37 applies to both NICAM sound outputs.

10.3.12.2 Definition

Table 37 Subaddress 15

MSB							LSB	GAIN SETTING (dB)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0 (note 1)
0	0	0	1	1	1	1	1	–1
0	0	0	1	1	1	1	0	–2
0	0	0	1	1	1	0	1	–3
0	0	0	1	1	1	0	0	–4
0	0	0	1	1	0	1	1	–5
0	0	0	1	1	0	1	0	–6
0	0	0	1	1	0	0	1	–7
0	0	0	1	1	0	0	0	–8
0	0	0	1	0	1	1	1	–9
0	0	0	1	0	1	1	0	–10
0	0	0	1	0	1	0	1	–11
0	0	0	1	0	1	0	0	–12
0	0	0	1	0	0	1	1	–13
0	0	0	1	0	0	1	0	–14
0	0	0	1	0	0	0	1	–15
0	0	0	1	0	0	0	0	mute

Note

1. The default setting at power-up is 00000000.

10.3.13 NICAM LOWER ERROR LIMIT REGISTER

10.3.13.1 Description

When the auto-mute function is enabled (bit AMUTE in the NICAM configuration register) and the NICAM bit error count is lower than the value contained in this register, the NICAM signal is reselected for reproduction, see Section 10.3.14.

10.3.13.2 Definition

Table 38 Subaddress 16 (notes 1 and 2)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0

Notes

1. The default setting at power-up is 00010100.
2. The lower bit error rate limit $\cong$ subaddress 16 $\times$ 1.74 $\times$ 10^{-5}.

10.3.14 NICAM UPPER ERROR LIMIT REGISTER

10.3.14.1 Description

When the auto-mute function is enabled (bit AMUTE in the NICAM configuration register) and the NICAM bit error count is higher than the value contained in this register, the signal of the first sound carrier (i.e. FM mono or AM sound) or the external mono input (depending on bit AMSEL and ADC output selection) is selected for reproduction.

The difference between upper and lower error limit constitutes a hysteresis to avoid frequent switching between NICAM and the program on the first sound carrier.

10.3.14.2 Definition

Table 39 Subaddress 17 (notes 1 and 2)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0

Notes

1. The default setting at power-up is 01010000.
2. The upper bit error rate limit $\cong$ subaddress 17 $\times$ 1.74 $\times$ 10^{-5}.

10.3.15 AUDIO MUTE CONTROL REGISTER

10.3.15.1 Description

When any of these bits are set HIGH, the corresponding pair of output channels will be muted. A LOW bit allows normal signal output.

There is a soft-mute facility for the Main and Auxiliary output channels to provide click-free muting independent of the volume control. This is switched on/off by bits MUTMAIN and MUTAUX.

10.3.15.2 *Definition*

Table 40 Subaddress 18 (note 1)

BIT	NAME	DESCRIPTION
7 (MSB)	MUTI^{2}S2	mute I^{2}S2 outputs
6	MUTI^{2}S1	mute I^{2}S1 outputs
5	MUTDAC	mute internal DAC
4	MUTLINE	mute line outputs
3	MUTSC2	mute SCART 2 outputs
2	MUTSC1	mute SCART 1 outputs
1	MUTAUX	mute Auxiliary outputs
0 (LSB)	MUTMAIN	mute Main channels

Note

1. The default setting at power-up is 11111111.

10.3.16 DAC OUTPUT SELECT REGISTER

10.3.16.1 *Description*

This register is used to define both the signal source to be entered into the DAC and the mode of the digital matrix for signal selection. The DAC is used for signal output from digital sources at analog outputs.

The bits DACGAIN1 and DACGAIN2 can introduce some extra gain at the input to the DAC. DACGAIN1 adds 3 dB and DACGAIN2 adds 6 dB of gain, respectively.

The two combinations of FM and NICAM apply to the (rare) condition that three different languages are being broadcast in an FM + NICAM system. They allow for a two-out-of-three selection for external use, such as recording.

10.3.16.2 *Definition*

Table 41 Subaddress 19 (note 1)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
DACGAIN2(2)	see Table 43			DACGAIN1(2)	see Table 42		

Notes

1. The default setting at power-up is 00000000.
2. See Table 44.

Table 42 Signal source left and right

B2	B1	B0	SIGNAL SOURCE	
			LEFT	RIGHT
0	0	0	FM left	FM right
0	0	1	NICAM left	NICAM right
0	1	0	I^2S1 left	I^2S1 right
0	1	1	I^2S2 left	I^2S2 right
1	0	0	ADC left	ADC right
1	0	1	AVL left	AVL right
1	1	0	FM mono	NICAM M1
1	1	1	FM mono	NICAM M2

Table 43 Bits B6 to B4

B6	B5	B4	L OUTPUT	R OUTPUT
0	0	0	L input	R input
0	0	1	L input	L input
0	1	0	R input	R input
0	1	1	R input	L input
1	0	0	$\frac{L+R}{2}$	$\frac{L+R}{2}$

Table 44 Description of bits DACGAIN1 and DACGAIN2

B7	B3	GAIN (dB)
0	0	0
0	1	3
1	0	6
1	1	9

10.3.17 SCART 1 OUTPUT SELECT REGISTER

10.3.17.1 Description

This register is used to define both the signal source to be output at SCART 1 and the output channel selector mode.

10.3.17.2 Definition

Table 45 Subaddress 20 (note 1)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
0	SC1GAIN(2)	see Table 47		0	see Table 46		

Notes

1. The default setting at power-up is 00000001.
2. See Table 48.

Table 46 Signal source

B2	B1	B0	SIGNAL SOURCE
0	0	0	SCART 1 input
0	0	1	SCART 2 input
0	1	0	external input
0	1	1	mono input
1	0	0	DAC input

Table 47 Bits B5 and B4

B5	B4	L OUTPUT	R OUTPUT
0	0	L input	R input
0	1	L input	L input
1	0	R input	R input
1	1	R input	L input

Table 48 Description of bit SC1GAIN

NAME	HIGH/LOW	FUNCTION
SC1GAIN	HIGH	Activates the 3 dB gain stage at the SCART 1 output buffers. As any SCART input passes a 3 dB attenuator, this gain stage can be used to compensate that attenuation, resulting in a 0 dB insertion loss when copying from SCART 2 input to SCART 1 output. However, that gain must be used with great care, as it will cause signal clipping at high input levels.
	LOW	The audio signal will be output unchanged (0 dB gain).

10.3.18 SCART 2 OUTPUT SELECT REGISTER

10.3.18.1 Description

This register is used to define both the signal source to be output at SCART 2 and the output channel selector mode.

10.3.18.2 Definition

Table 49 Subaddress 21 (note 1)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
0	SC2GAIN(2)	see Table 51		0	see Table 50		

Notes

1. The default setting at power-up is 00000000.
2. See Table 52.

Table 50 Signal source

B2	B1	B0	SIGNAL SOURCE
0	0	0	SCART 1 input
0	0	1	SCART 2 input
0	1	0	external input
0	1	1	mono input
1	0	0	DAC input

Table 51 Bits B5 and B4

B5	B4	L OUTPUT	R OUTPUT
0	0	L input	R input
0	1	L input	L input
1	0	R input	R input
1	1	R input	L input

Table 52 Description of bit SC2GAIN

NAME	HIGH/LOW	FUNCTION
SC2GAIN	HIGH	Activates the 3 dB gain stage at the SCART 2 output buffers. As any SCART input passes a 3 dB attenuator, this gain stage can be used to compensate that attenuation, resulting in a 0 dB insertion loss when copying from SCART 1 input to SCART 2 output. However, that gain must be used with great care, as it will cause signal clipping at high input levels.
	LOW	The audio signal will be output unchanged (0 dB gain).

10.3.19 LINE OUTPUT SELECT REGISTER

10.3.19.1 Description

By definition, the line output conveys the same signal as the Main (loudspeaker) channel, but in a non-processed form. This register is used to characterize the signal to be output at the line output and define the output channel selector mode.

10.3.19.2 Definition

Table 53 Subaddress 22 (note 1)

BIT	NAME	DESCRIPTION
7 (MSB)	–	set to logic 0
6	LINGAIN	line output gain on/off; see Table 55
5		see Table 54
4		
3	–	set to logic 0
2	–	set to logic 0
1	–	set to logic 0
0 (LSB)	LINSEL	select source for line output; see Table 55

Note

1. The default setting at power-up is 00000000.

Table 54 Bits B5 and B4

B5	B4	L OUTPUT	R OUTPUT
0	0	L input	R input
0	1	L input	L input
1	0	R input	R input
1	1	R input	L input

Table 55 Description of bits LINSEL and LINGAIN

NAME	HIGH/LOW	FUNCTION
LINSEL	HIGH	Specifies that a signal from an analog source is being processed in the Main channel. Analog signal sources comprise SCART 1 input, SCART 2 input, external input and mono input, i.e. any input to the ADC.
	LOW	Specifies that a signal from a digital source is being processed in the Main channel. Digital signal sources comprise FM, NICAM, I^2S1 input and I^2S2 input.
LINGAIN	HIGH	Activates the 3 dB gain stage at the line output buffers.
	LOW	The audio signal will be output unchanged (0 dB gain).

10.3.20 ADC OUTPUT SELECT REGISTER

10.3.20.1 Description

This register is used to define the signal source for the ADC. There is no output channel selector, because all digital signal sinks of the ADC have their own matrix. Instead, a level adjustment facility for the ADC output is provided.

10.3.20.2 Definition

Table 56 Subaddress 23 (note 1)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
see Table 57			see Table 58				

Note

1. The default setting at power-up is 00000000.

Table 57 Signal source

B7	B6	B5	SIGNAL SOURCE
0	0	0	SCART 1 input
0	0	1	SCART 2 input
0	1	0	external input
0	1	1	mono input

Table 58 ADC level adjust (note 1)

B4	B3	B2	B1	B0	GAIN SETTING (dB)
0	1	1	1	1	+15
0	1	1	1	0	+14
0	1	1	0	1	+13
0	1	1	0	0	+12
0	1	0	1	1	+11
0	1	0	1	0	+10
0	1	0	0	1	+9
0	1	0	0	0	+8
0	0	1	1	1	+7
0	0	1	1	0	+6
0	0	1	0	1	+5
0	0	1	0	0	+4
0	0	0	1	1	+3
0	0	0	1	0	+2
0	0	0	0	1	+1
0	0	0	0	0	0
1	1	1	1	1	–1
1	1	1	1	0	–2
1	1	1	0	1	–3
1	1	1	0	0	–4
1	1	0	1	1	–5
1	1	0	1	0	–6
1	1	0	0	1	–7
1	1	0	0	0	–8
1	0	1	1	1	–9
1	0	1	1	0	–10
1	0	1	0	1	–11
1	0	1	0	0	–12
1	0	0	1	1	–13
1	0	0	1	0	–14
1	0	0	0	1	–15
1	0	0	0	0	mute

Note

1. If the ADC level adjust is set to 0 dB a full-scale input signal to the ADC results into a level of –6 dB full-scale at the digital x-bar.

10.3.21 MAIN CHANNEL SELECT REGISTER

10.3.21.1 Description

This register is used to define both the signal source to be processed in the Main (loudspeaker) channel and the mode of the digital matrix for signal selection.

10.3.21.2 Definition

Table 59 Subaddress 24 (note 1)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
0	see Table 61			0	see Table 60		

Note

1. The default setting at power-up is 00000000.

Table 60 Signal source

B2	B1	B0	SIGNAL SOURCE
0	0	0	FM input
0	0	1	NICAM input
0	1	0	I^2S1 input
0	1	1	I^2S2 input
1	0	0	ADC input

Table 61 Bits B6 to B4

B6	B5	B4	L OUTPUT	R OUTPUT
0	0	0	L input	R input
0	0	1	L input	L input
0	1	0	R input	R input
0	1	1	R input	L input
1	0	0	$\frac{L + R}{2}$	$\frac{L + R}{2}$

10.3.22 AUDIO EFFECTS REGISTER

10.3.22.1 Definition

Table 62 Subaddress 25 (note 1; see Table 66)

MSB							**LSB**
B7	B6	B5	B4	B3	B2	B1	B0
0	0	SPATIAL1(2)	SPATIAL0(2)	PSEUDO1(3)	PSEUDO0(3)	AVL1(4)	AVL0(4)

Notes

1. The default setting at power-up is 00000000.
2. See Table 65.
3. See Table 64.
4. See Table 63.

Table 63 AVL control mode

B1	**B0**	**AVL MODE**
0	0	off/reset
0	1	short decay
1	0	medium decay
1	1	long decay

Table 64 Pseudo control setting

B3	**B2**	**PSEUDO SETTING (Hz)**
0	0	off
0	1	300
1	0	200
1	1	150

Table 65 Spatial control setting

B5	**B4**	**SPATIAL SETTING (%)**
0	0	off
0	1	30
1	0	40
1	1	52

Table 66 Description of Table 62 (notes 1, 2 and 3)

NAME	FUNCTION
AVL0, AVL1	these bits set the mode of operation of the automatic volume level control function at the entrance to the Main (loudspeaker) channel
PSEUDO0, PSEUDO1	These bits set the amount of the effect function (pseudo stereo) for mono signals in the Main channel. This function should be activated only in accordance with the result of the sound mode identification.
SPATIAL0, SPATIAL1	These bits set the amount of the effect function (stereo base width expansion) for stereo signals in the Main channel. This function should be activated only in accordance with the result of the sound mode identification.

Notes

1. Switching the AVL off will reset the associated hardware to a defined state.
2. When the signal source for the Main channel is changed while the AVL is on, the AVL needs to be reset in order to avoid excessive settling times. This can be achieved by switching the AVL off and on again.
3. The pseudo stereo function is based on an all-pass filter. A 90 degrees phase shift occurs at the frequencies stated in Table 64. There is a gain of 3 dB in the left audio channel.

10.3.23 VOLUME CONTROL REGISTERS (MAIN)

10.3.23.1 Description

These two registers control the volume setting of the Main (loudspeaker) channel. The register at subaddress 26 applies to the left channel signal, while the register at subaddress 27 applies to the right channel signal.

Balance control is exercised by offsetting the left and right channel volume settings.

10.3.23.2 Definition

Table 67 Subaddresses 26 and 27

MSB							LSB	VOLUME SETTING (dB)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	1	1	0	0	0	+24
0	0	0	1	0	1	1	1	+23
0	0	0	1	0	1	1	0	+22
0	0	0	1	0	1	0	1	+21
0	0	0	1	0	1	0	0	+20
0	0	0	1	0	0	1	1	+19
0	0	0	1	0	0	1	0	+18
0	0	0	1	0	0	0	1	+17
0	0	0	1	0	0	0	0	+16
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	–1
1	1	1	1	1	1	1	0	–2
1	1	1	1	1	1	0	1	–3
1	1	1	1	1	1	0	0	–4
1	1	1	1	1	0	1	1	–5
1	1	1	1	1	0	1	0	–6
1	1	1	1	1	0	0	1	–7
1	1	1	1	1	0	0	0	–8
1	1	1	1	0	1	1	1	–9
1	1	1	1	0	1	1	0	–10
1	1	1	1	0	1	0	1	–11
1	1	1	1	0	1	0	0	–12

MSB							LSB	VOLUME SETTING (dB)
B7	B6	B5	B4	B3	B2	B1	B0	
1	1	1	1	0	0	1	1	–13
1	1	1	1	0	0	1	0	–14
1	1	1	1	0	0	0	1	–15
1	1	1	1	0	0	0	0	–16
1	1	1	0	1	1	1	1	–17
1	1	1	0	1	1	1	0	–18
1	1	1	0	1	1	0	1	–19
1	1	1	0	1	1	0	0	–20
1	1	1	0	1	0	1	1	–21
1	1	1	0	1	0	1	0	–22
1	1	1	0	1	0	0	1	–23
1	1	1	0	1	0	0	0	–24
1	1	1	0	0	1	1	1	–25
1	1	1	0	0	1	1	0	–26
1	1	1	0	0	1	0	1	–27
1	1	1	0	0	1	0	0	–28
1	1	1	0	0	0	1	1	–29
1	1	1	0	0	0	1	0	–30
1	1	1	0	0	0	0	1	–31
1	1	1	0	0	0	0	0	–32
1	1	0	1	1	1	1	1	–33
1	1	0	1	1	1	1	0	–34
1	1	0	1	1	1	0	1	–35
1	1	0	1	1	1	0	0	–36
1	1	0	1	1	0	1	1	–37
1	1	0	1	1	0	1	0	–38
1	1	0	1	1	0	0	1	–39
1	1	0	1	1	0	0	0	–40
1	1	0	1	0	1	1	1	–41
1	1	0	1	0	1	1	0	–42
1	1	0	1	0	1	0	1	–43
1	1	0	1	0	1	0	0	–44
1	1	0	1	0	0	1	1	–45
1	1	0	1	0	0	1	0	–46
1	1	0	1	0	0	0	1	–47
1	1	0	1	0	0	0	0	–48
1	1	0	0	1	1	1	1	–49
1	1	0	0	1	1	1	0	–50
1	1	0	0	1	1	0	1	–51

MSB							LSB	VOLUME SETTING (dB)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
1	1	0	0	1	1	0	0	–52
1	1	0	0	1	0	1	1	–53
1	1	0	0	1	0	1	0	–54
1	1	0	0	1	0	0	1	–55
1	1	0	0	1	0	0	0	–56
1	1	0	0	0	1	1	1	–57
1	1	0	0	0	1	1	0	–58
1	1	0	0	0	1	0	1	–59
1	1	0	0	0	1	0	0	–60
1	1	0	0	0	0	1	1	–61
1	1	0	0	0	0	1	0	–62
1	1	0	0	0	0	0	1	–63
1	1	0	0	0	0	0	0	–64
1	0	1	1	1	1	1	1	–65
1	0	1	1	1	1	1	0	–66
1	0	1	1	1	1	0	1	–67
1	0	1	1	1	1	0	0	–68
1	0	1	1	1	0	1	1	–69
1	0	1	1	1	0	1	0	–70
1	0	1	1	1	0	0	1	–71
1	0	1	1	1	0	0	0	–72
1	0	1	1	0	1	1	1	–73
1	0	1	1	0	1	1	0	–74
1	0	1	1	0	1	0	1	–75
1	0	1	1	0	1	0	0	–76
1	0	1	1	0	0	1	1	–77
1	0	1	1	0	0	1	0	–78
1	0	1	1	0	0	0	1	–79
1	0	1	1	0	0	0	0	–80
1	0	1	0	1	1	1	1	–81
1	0	1	0	1	1	1	0	–82
1	0	1	0	1	1	0	1	–83
1	0	1	0	1	1	0	0	mute (note 1)

Note

1. The default setting at power-up is 10101100.

10.3.24 CONTOUR CONTROL REGISTER

10.3.24.1 Description

This register is used to apply the contour or loudness function (physiological volume control) to the left and right signal channels of the Main channel by means of an extra bass boost. The gain setting must be chosen in accordance with the volume control setting for the Main channel. For example, the contour gain could be incremented for every 5 dB, or so, of decrease of the volume setting. This needs to be done by the microcontroller. The 0 dB contour setting is equal to contour off.

10.3.24.2 Definition

Table 68 Subaddress 28

MSB							LSB	CONTOUR GAIN (dB)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	1	0	0	1	0	18
0	0	0	1	0	0	0	1	17
0	0	0	1	0	0	0	0	16
0	0	0	0	1	1	1	1	15
0	0	0	0	1	1	1	0	14
0	0	0	0	1	1	0	1	13
0	0	0	0	1	1	0	0	12
0	0	0	0	1	0	1	1	11
0	0	0	0	1	0	1	0	10
0	0	0	0	1	0	0	1	9
0	0	0	0	1	0	0	0	8
0	0	0	0	0	1	1	1	7
0	0	0	0	0	1	1	0	6
0	0	0	0	0	1	0	1	5
0	0	0	0	0	1	0	0	4
0	0	0	0	0	0	1	1	3
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0 (note 1)

Note

1. The default setting at power-up is 00000000.

10.3.25 BASS CONTROL REGISTER (MAIN)

10.3.25.1 Description

This register is used to apply bass control to the left and right signal channels of the Main channel.

10.3.25.2 Definition

Table 69 Subaddress 29

MSB							LSB	BASS SETTING (dB)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0 (note 1)
0	0	0	1	1	1	1	1	–1
0	0	0	1	1	1	1	0	–2
0	0	0	1	1	1	0	1	–3
0	0	0	1	1	1	0	0	–4
0	0	0	1	1	0	1	1	–5
0	0	0	1	1	0	1	0	–6
0	0	0	1	1	0	0	1	–7
0	0	0	1	1	0	0	0	–8
0	0	0	1	0	1	1	1	–9
0	0	0	1	0	1	1	0	–10
0	0	0	1	0	1	0	1	–11
0	0	0	1	0	1	0	0	–12

Note

1. The default setting at power-up is 00000000.

10.3.26 Treble control register (main)

10.3.26.1 Description

This register is used to apply treble control to the left and right signal channels of the Main channel.

10.3.26.2 Definition

Table 70 Subaddress 30

MSB							**LSB**	**TREBLE SETTING (dB)**
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0 (note 1)
0	0	0	1	1	1	1	1	–1
0	0	0	1	1	1	1	0	–2
0	0	0	1	1	1	0	1	–3
0	0	0	1	1	1	0	0	–4
0	0	0	1	1	0	1	1	–5
0	0	0	1	1	0	1	0	–6
0	0	0	1	1	0	0	1	–7
0	0	0	1	1	0	0	0	–8
0	0	0	1	0	1	1	1	–9
0	0	0	1	0	1	1	0	–10
0	0	0	1	0	1	0	1	–11
0	0	0	1	0	1	0	0	–12

Note

1. The default setting at power-up is 00000000.

10.3.27 AUXILIARY CHANNEL SELECT REGISTER

10.3.27.1 Description

This register is used to define both the signal source to be processed in the Auxiliary (headphone) channel and the mode of the digital matrix for signal selection.

10.3.27.2 Definition

Table 71 Subaddress 31 (note 1)

MSB							**LSB**
B7	B6	B5	B4	B3	B2	B1	B0
0	see Table 73			0	see Table 72		

Note

1. The default setting at power-up is 00000000.

Table 72 Signal source

B2	**B1**	**B0**	**SIGNAL SOURCE**
0	0	0	FM input
0	0	1	NICAM input
0	1	0	I^2S1 input
0	1	1	I^2S2 input
1	0	0	ADC input
1	0	1	AVL input

Table 73 Bits B6 to B4

B6	**B5**	**B4**	**L OUTPUT**	**R OUTPUT**
0	0	0	L input	R input
0	0	1	L input	L input
0	1	0	R input	R input
0	1	1	R input	L input
1	0	0	$\frac{L + R}{2}$	$\frac{L + R}{2}$

10.3.28 VOLUME CONTROL REGISTERS (AUXILIARY)

10.3.28.1 Description

These two registers control the volume setting of the Auxiliary (headphone) channel. The register at subaddress 32 applies to the left channel signal, while the register at subaddress 33 applies to the right channel signal.

Balance control is exercised by offsetting the left and right channel volume settings.

10.3.28.2 Definition

Table 74 Subaddresses 32 and 33

MSB							LSB	VOLUME SETTING (dB)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	1	1	0	0	0	+24
0	0	0	1	0	1	1	1	+23
0	0	0	1	0	1	1	0	+22
0	0	0	1	0	1	0	1	+21
0	0	0	1	0	1	0	0	+20
0	0	0	1	0	0	1	1	+19
0	0	0	1	0	0	1	0	+18
0	0	0	1	0	0	0	1	+17
0	0	0	1	0	0	0	0	+16
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	–1
1	1	1	1	1	1	1	0	–2
1	1	1	1	1	1	0	1	–3
1	1	1	1	1	1	0	0	–4
1	1	1	1	1	0	1	1	–5
1	1	1	1	1	0	1	0	–6
1	1	1	1	1	0	0	1	–7
1	1	1	1	1	0	0	0	–8
1	1	1	1	0	1	1	1	–9
1	1	1	1	0	1	1	0	–10
1	1	1	1	0	1	0	1	–11
1	1	1	1	0	1	0	0	–12
1	1	1	1	0	0	1	1	–13
1	1	1	1	0	0	1	0	–14

MSB							LSB	VOLUME SETTING (dB)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
1	1	1	1	0	0	0	1	–15
1	1	1	1	0	0	0	0	–16
1	1	1	0	1	1	1	1	–17
1	1	1	0	1	1	1	0	–18
1	1	1	0	1	1	0	1	–19
1	1	1	0	1	1	0	0	–20
1	1	1	0	1	0	1	1	–21
1	1	1	0	1	0	1	0	–22
1	1	1	0	1	0	0	1	–23
1	1	1	0	1	0	0	0	–24
1	1	1	0	0	1	1	1	–25
1	1	1	0	0	1	1	0	–26
1	1	1	0	0	1	0	1	–27
1	1	1	0	0	1	0	0	–28
1	1	1	0	0	0	1	1	–29
1	1	1	0	0	0	1	0	–30
1	1	1	0	0	0	0	1	–31
1	1	1	0	0	0	0	0	–32
1	1	0	1	1	1	1	1	–33
1	1	0	1	1	1	1	0	–34
1	1	0	1	1	1	0	1	–35
1	1	0	1	1	1	0	0	–36
1	1	0	1	1	0	1	1	–37
1	1	0	1	1	0	1	0	–38
1	1	0	1	1	0	0	1	–39
1	1	0	1	1	0	0	0	–40
1	1	0	1	0	1	1	1	–41
1	1	0	1	0	1	1	0	–42
1	1	0	1	0	1	0	1	–43
1	1	0	1	0	1	0	0	–44
1	1	0	1	0	0	1	1	–45
1	1	0	1	0	0	1	0	–46
1	1	0	1	0	0	0	1	–47
1	1	0	1	0	0	0	0	–48
1	1	0	0	1	1	1	1	–49
1	1	0	0	1	1	1	0	–50
1	1	0	0	1	1	0	1	–51
1	1	0	0	1	1	0	0	–52
1	1	0	0	1	0	1	1	–53
1	1	0	0	1	0	1	0	–54
1	1	0	0	1	0	0	1	–55

MSB							LSB	VOLUME SETTING (dB)
B7	B6	B5	B4	B3	B2	B1	B0	
1	1	0	0	1	0	0	0	–56
1	1	0	0	0	1	1	1	–57
1	1	0	0	0	1	1	0	–58
1	1	0	0	0	1	0	1	–59
1	1	0	0	0	1	0	0	–60
1	1	0	0	0	0	1	1	–61
1	1	0	0	0	0	1	0	–62
1	1	0	0	0	0	0	1	–63
1	1	0	0	0	0	0	0	–64
1	0	1	1	1	1	1	1	–65
1	0	1	1	1	1	1	0	–66
1	0	1	1	1	1	0	1	–67
1	0	1	1	1	1	0	0	–68
1	0	1	1	1	0	1	1	–69
1	0	1	1	1	0	1	0	–70
1	0	1	1	1	0	0	1	–71
1	0	1	1	1	0	0	0	–72
1	0	1	1	0	1	1	1	–73
1	0	1	1	0	1	1	0	–74
1	0	1	1	0	1	0	1	–75
1	0	1	1	0	1	0	0	–76
1	0	1	1	0	0	1	1	–77
1	0	1	1	0	0	1	0	–78
1	0	1	1	0	0	0	1	–79
1	0	1	1	0	0	0	0	–80
1	0	1	0	1	1	1	1	–81
1	0	1	0	1	1	1	0	–82
1	0	1	0	1	1	0	1	–83
1	0	1	0	1	1	0	0	mute (note 1)

Note

1. The default setting at power-up is 10101100.

10.3.29 BASS CONTROL REGISTER (AUXILIARY)

10.3.29.1 Description

This register is used to apply bass control to the left and right signal channels of the Auxiliary channel.

10.3.29.2 Definition

Table 75 Subaddress 34

MSB							LSB	BASS SETTING (dB)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0 (note 1)
0	0	0	1	1	1	1	1	–1
0	0	0	1	1	1	1	0	–2
0	0	0	1	1	1	0	1	–3
0	0	0	1	1	1	0	0	–4
0	0	0	1	1	0	1	1	–5
0	0	0	1	1	0	1	0	–6
0	0	0	1	1	0	0	1	–7
0	0	0	1	1	0	0	0	–8
0	0	0	1	0	1	1	1	–9
0	0	0	1	0	1	1	0	–10
0	0	0	1	0	1	0	1	–11
0	0	0	1	0	1	0	0	–12

Note

1. The default setting at power-up is 00000000.

10.3.30 TREBLE CONTROL REGISTER (AUXILIARY)

10.3.30.1 Description

This register is used to apply treble control to the left and right signal channels of the Auxiliary channel.

10.3.30.2 Definition

Table 76 Subaddress 35

MSB							LSB	TREBLE SETTING (dB)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
X	X	X	0	1	1	0	0	+12
X	X	X	0	1	0	1	1	+11
X	X	X	0	1	0	1	0	+10
X	X	X	0	1	0	0	1	+9
X	X	X	0	1	0	0	0	+8
X	X	X	0	0	1	1	1	+7
X	X	X	0	0	1	1	0	+6
X	X	X	0	0	1	0	1	+5
X	X	X	0	0	1	0	0	+4
X	X	X	0	0	0	1	1	+3
X	X	X	0	0	0	1	0	+2
X	X	X	0	0	0	0	1	+1
X	X	X	0	0	0	0	0	0 (note 1)
X	X	X	1	1	1	1	1	–1
X	X	X	1	1	1	1	0	–2
X	X	X	1	1	1	0	1	–3
X	X	X	1	1	1	0	0	–4
X	X	X	1	1	0	1	1	–5
X	X	X	1	1	0	1	0	–6
X	X	X	1	1	0	0	1	–7
X	X	X	1	1	0	0	0	–8
X	X	X	1	0	1	1	1	–9
X	X	X	1	0	1	1	0	–10
X	X	X	1	0	1	0	1	–11
X	X	X	1	0	1	0	0	–12

Note

1. The default setting at power-up is 00000000.

10.3.31 FEATURE INTERFACE CONFIGURATION REGISTER

10.3.31.1 Definition

Table 77 Subaddress 36 (note 1)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	SYSCL1(2)	SYSCL0(2)	SYSOUT(3)	I^{2}SFORM(4)	I^{2}SOUT(5)

Notes

1. The default setting at power-up is 00000000.
2. System clock frequency select; see Table 78.
3. System clock output on/off; see Table 79.
4. Serial output format; see Table 79.
5. I^{2}S-bus outputs on/off; see Table 79.

Table 78 System clock frequency select

B4	B3	SYSCLK OUTPUT	FREQUENCY (MHz)
0	0	$256f_s$	8.192
0	1	$384f_s$	12.288
1	0	$512f_s$	16.384; note 1
1	1	$768f_s$	24.576

Note

1. With 16.384 MHz, the duty cycle is 33% : 67%.

Table 79 Description of Table 77

NAME	HIGH/LOW	FUNCTION
I^{2}SOUT	HIGH	Enables the output of serial audio data (2 pins) plus serial bit clock and word select in a format determined by the I^{2}SFORM bit. The TDA9875A is then an I^{2}S-bus master.
	LOW	the outputs mentioned will be 3-stated, thereby improving the EMC performance
I^{2}SFORM	HIGH	an MSB-aligned, MSB-first output format is selected, i.e. a level change at the word select pin indicates the beginning of a new audio sample
	LOW	the standard I^{2}S-bus output format is selected
SYSOUT	HIGH	enables the output of a system (or master) clock signal at pin SYSCLK
	LOW	the output will be off, thereby improving the EMC performance

10.3.32 I^2S1 OUTPUT SELECT REGISTER

10.3.32.1 Description

This register is used to define both the signal source to be output at I^2S1 and the mode of the digital matrix for signal selection.

10.3.32.2 Definition

Table 80 Subaddress 37 (note 1)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
0	see Table 82			0	see Table 81		

Note

1. The default setting at power-up is 00000000.

Table 81 Signal source (note 1)

B2	B1	B0	SIGNAL SOURCE
0	0	0	FM output
0	0	1	NICAM output
0	1	0	I^2S1 input
0	1	1	I^2S2 input
1	0	0	ADC output
1	0	1	AVL output
1	1	0	Auxiliary output
1	1	1	Main output

Note

1. The Main and Auxiliary channel outputs will not contain the beeper signal.

Table 82 Bits B6 to B4

B6	B5	B4	L OUTPUT	R OUTPUT
0	0	0	L input	R input
0	0	1	L input	L input
0	1	0	R input	R input
0	1	1	R input	L input
1	0	0	$\frac{L+R}{2}$	$\frac{L+R}{2}$

10.3.33 I²S1 INPUT LEVEL ADJUST REGISTER

10.3.33.1 Description

This register is used to adjust the input level at the I²S1 interface. Left and right signal channel are treated identically.

10.3.33.2 Definition

Table 83 Subaddress 38

MSB							LSB	GAIN SETTING (dB)
B7	B6	B5	B4	B3	B2	B1	B0	
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0 (note 1)
0	0	0	1	1	1	1	1	–1
0	0	0	1	1	1	1	0	–2
0	0	0	1	1	1	0	1	–3
0	0	0	1	1	1	0	0	–4
0	0	0	1	1	0	1	1	–5
0	0	0	1	1	0	1	0	–6
0	0	0	1	1	0	0	1	–7
0	0	0	1	1	0	0	0	–8
0	0	0	1	0	1	1	1	–9
0	0	0	1	0	1	1	0	–10
0	0	0	1	0	1	0	1	–11
0	0	0	1	0	1	0	0	–12
0	0	0	1	0	0	1	1	–13
0	0	0	1	0	0	1	0	–14
0	0	0	1	0	0	0	1	–15
0	0	0	1	0	0	0	0	mute

Note

1. The default setting at power-up is 00000000.

10.3.34 I^2S1 OUTPUT LEVEL ADJUST REGISTER

10.3.34.1 Description

This register is used to adjust the output level at the I^2S1 interface. Left and right signal channel are treated identically.

10.3.34.2 Definition

Table 84 Subaddress 39

MSB							LSB	GAIN SETTING (dB)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0 (note 1)
0	0	0	1	1	1	1	1	–1
0	0	0	1	1	1	1	0	–2
0	0	0	1	1	1	0	1	–3
0	0	0	1	1	1	0	0	–4
0	0	0	1	1	0	1	1	–5
0	0	0	1	1	0	1	0	–6
0	0	0	1	1	0	0	1	–7
0	0	0	1	1	0	0	0	–8
0	0	0	1	0	1	1	1	–9
0	0	0	1	0	1	1	0	–10
0	0	0	1	0	1	0	1	–11
0	0	0	1	0	1	0	0	–12
0	0	0	1	0	0	1	1	–13
0	0	0	1	0	0	1	0	–14
0	0	0	1	0	0	0	1	–15
0	0	0	1	0	0	0	0	mute

Note

1. The default setting at power-up is 00000000.

10.3.35 I^2S2 OUTPUT SELECT REGISTER

10.3.35.1 Description

This register is used to define both the signal source to be output at I^2S2 and the mode of the digital matrix for signal selection.

10.3.35.2 Definition

Table 85 Subaddress 40 (note 1)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
0	see Table 87			0	see Table 86		

Note

1. The default setting at power-up is 00000000.

Table 86 Signal source (note 1)

B2	B1	B0	SIGNAL SOURCE
0	0	0	FM output
0	0	1	NICAM output
0	1	0	I^2S1 input
0	1	1	I^2S2 input
1	0	0	ADC output
1	0	1	AVL output
1	1	0	Auxiliary output
1	1	1	Main output

Note

1. The Main and Auxiliary channel outputs will not contain the beeper signal.

Table 87 Bits B6 to B4

B6	B5	B4	L OUTPUT	R OUTPUT
0	0	0	L input	R input
0	0	1	L input	L input
0	1	0	R input	R input
0	1	1	R input	L input
1	0	0	$\frac{L+R}{2}$	$\frac{L+R}{2}$

10.3.36 I^2S2 INPUT LEVEL ADJUST REGISTER

10.3.36.1 Description

This register is used to adjust the input level at the I^2S2 interface. Left and right signal channel are treated identically.

10.3.36.2 Definition

Table 88 Subaddress 41

MSB							LSB	GAIN SETTING (dB)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0 (note 1)
0	0	0	1	1	1	1	1	–1
0	0	0	1	1	1	1	0	–2
0	0	0	1	1	1	0	1	–3
0	0	0	1	1	1	0	0	–4
0	0	0	1	1	0	1	1	–5
0	0	0	1	1	0	1	0	–6
0	0	0	1	1	0	0	1	–7
0	0	0	1	1	0	0	0	–8
0	0	0	1	0	1	1	1	–9
0	0	0	1	0	1	1	0	–10
0	0	0	1	0	1	0	1	–11
0	0	0	1	0	1	0	0	–12
0	0	0	1	0	0	1	1	–13
0	0	0	1	0	0	1	0	–14
0	0	0	1	0	0	0	1	–15
0	0	0	1	0	0	0	0	mute

Note

1. The default setting at power-up is 00000000.

10.3.37 I^{2}S2 OUTPUT LEVEL ADJUST REGISTER

10.3.37.1 Description

This register is used to adjust the output level at the I^{2}S2 interface. Left and right signal channel are treated identically.

10.3.37.2 Definition

Table 89 Subaddress 42

MSB							LSB	GAIN SETTING (dB)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0 (note 1)
0	0	0	1	1	1	1	1	–1
0	0	0	1	1	1	1	0	–2
0	0	0	1	1	1	0	1	–3
0	0	0	1	1	1	0	0	–4
0	0	0	1	1	0	1	1	–5
0	0	0	1	1	0	1	0	–6
0	0	0	1	1	0	0	1	–7
0	0	0	1	1	0	0	0	–8
0	0	0	1	0	1	1	1	–9
0	0	0	1	0	1	1	0	–10
0	0	0	1	0	1	0	1	–11
0	0	0	1	0	1	0	0	–12
0	0	0	1	0	0	1	1	–13
0	0	0	1	0	0	1	0	–14
0	0	0	1	0	0	0	1	–15
0	0	0	1	0	0	0	0	mute

Note

1. The default setting at power-up is 00000000.

10.3.38 BEEPER FREQUENCY CONTROL REGISTER

10.3.38.1 Description

This register is used to select from sample beeper oscillator frequencies. The beeper output signal is added to the Main and Auxiliary channel output DAC.

Due to the frequency response of the audio DACs upsampling filters, the 25 kHz beep is approximately 5 dB louder than the 390 Hz beep.

10.3.38.2 Definition

Table 90 Subaddress 43 (note 1)

MSB							LSB	GENERATED FREQUENCY (Hz)
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	0	0	1	1	1	25000
0	0	0	0	0	1	1	0	7040
0	0	0	0	0	1	0	1	3580
0	0	0	0	0	1	0	0	1770
0	0	0	0	0	0	1	1	1270
0	0	0	0	0	0	1	0	900
0	0	0	0	0	0	0	1	640
0	0	0	0	0	0	0	0	390

Note

1. The default setting at power-up is 00000000.

10.3.39 BEEPER VOLUME CONTROL REGISTER

10.3.39.1 Description

This register is used to set the beeper volume. The gain setting is relative to digital full scale at the input to the Main and Auxiliary channel output DACs. The beeper volume is independent of any other volume setting.

The beeper signal is added to the Main and Auxiliary channel output signals in the $2 \times f_s$ domain. The beeper volume should be set with great care, when the audio signals in the Main and Auxiliary channels are close to digital full scale, to avoid output signal distortion due to overload.

10.3.39.2 Definition

Table 91 Subaddress 44

MSB							**LSB**	**GAIN SETTING (dB)**
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	0	0	0	0	0	0
0	0	1	1	1	1	1	1	–3
0	0	1	1	1	1	1	0	–6
0	0	1	1	1	1	0	1	–9
0	0	1	1	1	1	0	0	–12
0	0	1	1	1	0	1	1	–15
0	0	1	1	1	0	1	0	–18
0	0	1	1	1	0	0	1	–21
0	0	1	1	1	0	0	0	–24
0	0	1	1	0	1	1	1	–27
0	0	1	1	0	1	1	0	–30
0	0	1	1	0	1	0	1	–33
0	0	1	1	0	1	0	0	–36
0	0	1	1	0	0	1	1	–39
0	0	1	1	0	0	1	0	–42
0	0	1	1	0	0	0	1	–45
0	0	1	1	0	0	0	0	–48
0	0	1	0	1	1	1	1	–51
0	0	1	0	1	1	1	0	–54
0	0	1	0	1	1	0	1	–57
0	0	1	0	1	1	0	0	–60
0	0	1	0	1	0	1	1	–63
0	0	1	0	1	0	1	0	–66
0	0	1	0	1	0	0	1	–69
0	0	1	0	1	0	0	0	–72
0	0	1	0	0	1	1	1	–75
0	0	1	0	0	1	1	0	–78
0	0	1	0	0	1	0	1	–81
0	0	1	0	0	1	0	0	–84
0	0	1	0	0	0	1	1	–87
0	0	1	0	0	0	1	0	–90
0	0	1	0	0	0	0	1	–93
0	0	1	0	0	0	0	0	mute (note 1)

Note

1. The default setting at power-up is 00100000.

10.3.40 BASS BOOST CONTROL REGISTER

10.3.40.1 Description

This register is used to select from a few sample bass boost settings to modify the frequency characteristics of the Main channel (shelving filter). Bits B3 to B0 apply to the left channel, bits B7 to B4 apply to the right channel. This function must be used with care in order to avoid clipping distortion at high volume settings.

More sophisticated control of the bass boost filter can be exercised in the expert mode (see Section 10.5). The user then has full control over this 2nd-order filter and can, within limits, realize bass equalizers with arbitrary centre frequencies, Q factors and boost/cut settings.

10.3.40.2 Definition

Table 92 Subaddress 45 (note 1; see Table 93)

MSB							**LSB**
B7	B6	B5	B4	B3	B2	B1	B0

Note

1. The default setting at power-up is 00000000.

Table 93 Gain setting

B7, B3	**B6, B2**	**B5, B1**	**B4, B0**	**GAIN SETTING (dB)**	**CORNER FREQUENCY (Hz)**
1	0	1	0	20	350
1	0	0	1	18	350
1	0	0	0	16	350
0	1	1	1	14	350
0	1	1	0	12	350
0	1	0	1	10	350
0	1	0	0	8	350
0	0	1	1	6	350
0	0	1	0	4	350
0	0	0	1	2	350
0	0	0	0	0	350

10.4 Slave transmitter mode

As a slave transmitter, the TDA9875A provides 13 registers with status information and data, a part of which is for Philips internal purposes only. These registers can be accessed by means of subaddresses.

Table 94 General format for reading data from the TDA9875A

S	SLAVE ADDRESS	0	ACK	SUBADDRESS	ACK	Sr	SLAVE ADDRESS	1	ACK	DATA	NAm	P

Table 95 Explanation of Tables 94 and 96

BIT	FUNCTION
S	START condition
SLAVE ADDRESS	7-bit device address
0	data direction bit (write to device)
ACK	acknowledge (by the slave)
SUBADDRESS	address of register to read from
Sr	repeated START condition
1	data direction bit (read from device)
DATA	data byte read from register
NAm	not acknowledge (by the master)
Am	acknowledge (by the master)
P	STOP condition

Reading of data can start at any valid subaddress. It is allowed to read more than 1 data byte per transmission from the TDA9875A. In this situation, the subaddress is automatically incremented after each data byte, which results in reading the sequence of data bytes from successive register locations, starting at SUBADDRESS.

Table 96 Format of a transmission using automatic incrementing of subaddresses

S	SLAVE ADDRESS	0	ACK	SUBADDRESS	ACK	Sr	SLAVE ADDRESS	1	ACK	DATA BYTE Am(1)	DATA	NAm	P

Note

1. n data bytes with auto-increment of subaddresses.

Each data byte in a read sequence, except for the last one, is acknowledged with Am (acknowledge by the master). The subaddresses ‘wrap around’ from decimal 255 to 0. If an attempt is made to read from a non-existing subaddress, the device will send a data pattern of all ones, i.e. FF in hexadecimal notation.

Table 97 Overview of the slave transmitter registers (note 1)

SUBADDRESS (DECIMAL)	DATA								FUNCTION
	MSB							LSB	
0	s	s	s	s	s	s	s	s	device status (power-on, identification, etc.)
1	s	s	s	s	s	s	s	s	NICAM status
2	e	e	e	e	e	e	e	e	NICAM error count
3	d	d	d	d	d	d	d	d	additional data (LSB)
4	c	c	X	c	c	d	d	d	additional data (MSB)
5	l	l	l	l	l	l	l	l	level read-out (MSB)
6	l	l	l	l	l	l	l	l	level read-out (LSB)
7	X	X	X	c	c	c	c	c	SIF level
251	a	a	a	a	a	a	a	a	test register 3; note 2
252	a	a	a	a	a	a	a	a	test register 2; note 2
253	a	a	a	a	a	a	a	a	test register 1; note 2
254	d	d	d	d	d	d	d	d	device identification code
255	s	s	s	s	s	s	s	s	software identification code

Notes

1. X indicates a bit that has not been assigned to a function. This bit is reserved for future extensions.
2. Registers from subaddress 251 to 255 are for Philips internal purposes only. They are considered as a set of registers for the identification of individual members and some key parameters in a family of devices.

A detailed description of the slave transmitter registers is given in below:

10.4.1 DEVICE STATUS REGISTER

10.4.1.1 Description

Table 98 Description of Table 99

NAME	HIGH/LOW	FUNCTION
POR	–	The power supply for the digital part of the device, V_{DDD2}, has temporarily been lower than the specified lower limit. If this is detected an initialization of the TDA9875A has to be carried out to ensure reliable operation.
IDSTE	–	this bit is HIGH if an FM stereo signal has been identified
IDDUA	–	This bit is HIGH if an FM dual-language signal has been identified. When neither IDSTE nor IDDUA are set, the received signal has to be assumed to be FM mono.
VDSP	HIGH	indicates that digital transmission is a sound source (NICAM)
	LOW	the transmission is either data or currently undefined format (NICAM)
AMSTAT	–	if this bit is HIGH, it indicates that the auto-muting function has switched from NICAM to the program of the first sound carrier (i.e. FM mono or AM in NICAM L systems) or to the ADC (depending on bit AMSEL)
RSSF	HIGH	This bit is a copy of the C4 bit in the NICAM status register. It indicates that the FM (or AM for standard L) sound matches the digital transmission and auto-muting should be enabled.
	LOW	auto-muting should be disabled, as analog and digital sound are different
P1IN, P2IN	–	these bits reflect the status of the corresponding general purpose port pins, see Section 10.3.2

10.4.1.2 Definition

Table 99 Subaddress 0

BIT	NAME	DESCRIPTION
7 (MSB)	P2IN	input from port 2
6	P1IN	input from port 1
5	RSSF	reserve sound switching flag
4	AMSTAT	auto-mute status
3	VDSP	identification of NICAM sound
2	IDDUA	identification of FM dual sound
1	IDSTE	identification of FM stereo
0 (LSB)	POR	power fail bit

10.4.2 NICAM STATUS REGISTER

10.4.2.1 Description

Table 100 Description of Table 101

NAME	HIGH/LOW	FUNCTION
D/SB	–	if this bit is HIGH it indicates dual mono mode
S/MB	–	if this bit is HIGH it indicates stereo mode
CFC	–	if this bit is HIGH, it indicates a configuration change at the 16 frame (C0) boundary
OSB	HIGH	indicates that the device has both frame and C0 (16 frame) synchronization
	LOW	the audio output from the NICAM part should be digital silence
C1, C2, C3, C4	–	these bits correspond to the control bits C1 to C4 in the NICAM transmission

10.4.2.2 Definition

Table 101 Subaddress 1

BIT	NAME	DESCRIPTION
7 (MSB)	C4	NICAM application control bits
6	C3	
5	C2	
4	C1	
3	OSB	synchronization bit
2	CFC	configuration change
1	S/MB	identification of NICAM stereo
0 (LSB)	D/SB	identification of NICAM dual mono

10.4.2.3 Notes

The TDA9875A does not support the Extended Control Modes. Therefore, the program of the first sound carrier (i.e. FM mono or AM) is selected for reproduction in case bit C3 is set HIGH, independent of bit AMUTE in the NICAM configuration register being set or not.

When a NICAM transmitter is switched off, the device will lose synchronization. In this situation the program of the first sound carrier is selected for reproduction, independent of bit AMUTE being set or not.

10.4.3 NICAM ERROR COUNT REGISTER

10.4.3.1 Description

Bits B7 to B0 contain the number of errors occurring in the previous 128 ms period. The register is updated every 128 ms.

10.4.3.2 Definition

Table 102 Subaddress 2

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0

10.4.4 ADDITIONAL DATA REGISTERS

10.4.4.1 *Description*

These two bytes provide information on the additional data bits.

10.4.4.2 *Definition*

Table 103 Subaddress 3

BIT	NAME
7 (MSB)	AD7
6	AD6
5	AD5
4	AD4
3	AD3
2	AD2
1	AD1
0 (LSB)	AD0

Table 104 Subaddress 4

BIT	NAME
7 (MSB)	OVW
6	SAD
5	X (don't care)
4	CI1
3	CI2
2	AD10
1	AD9
0 (LSB)	AD8

Table 105 Description of Tables 103 and 104

NAME	HIGH/LOW	FUNCTION
AD10 to AD0	–	comprise the additional data word
CI1, CI2	–	these are CI bits decoded by majority logic from the parity checks of the last ten samples in a frame
SAD	HIGH	new additional data is written into the IC
	LOW	reset, when the additional data bits are read
OVW	–	if this bit is HIGH, new additional data bits are written to the IC without the previous bits being read

10.4.5 LEVEL READ-OUT REGISTERS

10.4.5.1 Description

These two bytes constitute a word that provides data from a location that has been specified with the monitor select register. The most significant byte of the data is stored at subaddress 5.

If peak-level monitoring has been selected, the peak-level monitoring register is cleared and monitoring resumes after its contents has been transferred to these two bytes.

10.4.5.2 Definition

Table 106 Subaddress 5

BIT
7 (most significant bit or sign bit)
6
5
4
3
2
1
0

Table 107 Subaddress 6

BIT
7
6
5
4
3
2
1
0 (least significant bit)

10.4.6 SIF LEVEL REGISTER

10.4.6.1 Description

When the SIF AGC is on, bits B4 to B0 of this register contain a number that gives an indication of the SIF input level. That number corresponds to the AGC gain register setting (see Section 10.3, subaddress 0).

When the SIF AGC is off, this register returns the contents of the AGC gain register.

10.4.6.2 Definition

Table 108 Subaddress 7

MSB							**LSB**
B7	B6	B5	B4	B3	B2	B1	B0

10.4.7 TEST REGISTER 3

10.4.7.1 Description

This register contains, as a binary number, the highest memory address used for the Coefficient RAM (CRAM, expert mode).

10.4.7.2 Definition

Table 109 Subaddress 251

MSB							**LSB**
B7	B6	B5	B4	B3	B2	B1	B0
0	1	1	1	1	1	1	1

10.4.8 TEST REGISTER 2

10.4.8.1 Description

This register contains, as a binary number, the highest subaddress used for slave receiver registers.

10.4.8.2 Definition

Table 110 Subaddress 252

MSB							**LSB**
B7	B6	B5	B4	B3	B2	B1	B0
0	0	1	0	1	1	0	1

10.4.9 TEST REGISTER 1

10.4.9.1 Description

This register contains, as a binary number, the highest subaddress used for slave transmitter (status) registers.

10.4.9.2 Definition

Table 111 Subaddress 253

MSB							**LSB**
B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	1	1	1

10.4.10 DEVICE IDENTIFICATION CODE

10.4.10.1 Description

There will be several devices in the digital TV sound processor family. This byte is used to identify the individual family members.

10.4.10.2 Definition

Table 112 Subaddress 254

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	1	0

10.4.11 SOFTWARE IDENTIFICATION CODE

10.4.11.1 Description

It is likely that during the life time of this family of devices several versions of the DSP software will be made, e.g., to accommodate new application concepts, respond to customer wishes, etc. This byte is used to identify the different releases.

10.4.11.2 Definition

Table 113 Subaddress 255

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	1	0

10.5 Expert mode

In addition to the slave receiver and slave transmitter modes previously described, there is a special ‘expert’ mode that gives direct write access to the internal CRAM of the DSP.

In this mode, transferred data contain 12-bit-wide coefficients. As those coefficients bypass on-chip coefficient look-up tables for many functions, they directly influence the processing of signals within the DSP.

This mode must be used with great care. It can be used to create user-defined characteristics, such as a tone control with different corner frequencies or special boost/cut characteristics to correct the low-frequency loudspeaker and/or cabinet frequency responses.

Table 114 General format for entering the expert mode and writing coefficients into the TDA9875A

S	SLAVE ADDRESS	0	ACK	10000000	ACK	CRAM ADDRESS	ACK	DATA	ACK	DATA	ACK	P

Table 115 Explanation of Table 114

BIT	FUNCTION
S	START condition
SLAVE ADDRESS	7-bit device address
0	data direction bit (write to device)
ACK	acknowledge
10000000	pattern to enter the expert mode
CRAM ADDRESS	start address of coefficient RAM to write to
DATA	data byte containing part of a coefficient
P	STOP condition

As the coefficients do not fit into one data byte, they have to be split and arranged (see Table 116). The most significant bit is transferred first.

Table 116 General format (notes 1, 2 and 3)

BYTE	DATA								DESCRIPTION
1. data byte	a	a	a	a	a	a	a	a	2 MST of 1st coefficient
2. data byte	a	a	a	a	X	X	X	X	1 LST of 1st coefficient

Notes

1. X = don’t care.
2. MST = most significant third.
3. LST = least significant third.

The general format described in Table 116 shows the minimum number of data bytes required, i.e. two bytes for the transfer of a single coefficient.

Should more than one coefficient be sent, then the CRAM address will be automatically incremented after each coefficient, resulting in writing the sequence of coefficients into successive memory locations, starting at CRAM ADDRESS. A transmission can start with any valid CRAM address. If two coefficients are to be transferred, they are arranged as shown in Table 117.

Table 117 Transfer of two coefficients

BYTE	DATA								DESCRIPTION
1 data byte	a	a	a	a	a	a	a	a	2 MST of 1st coefficient
2 data byte	a	a	a	a	b	b	b	b	1 LST of 1st coefficient + 1 MST of 2nd coefficient
3 data byte	b	b	b	b	b	b	b	b	2 LST of 2nd coefficient

With any odd number of coefficients to be transferred, the least significant nibble of the last byte is regarded as containing don’t care data.

As the transfer of coefficients cannot be accomplished within one audio sample period, it is necessary that received coefficients be buffered and made active all at the same time to avoid audio signal transients. The receive buffer is designed to store up to 8 coefficients in addition to the CRAM address. Each byte that fits into the buffer is acknowledged with ACK (acknowledge). If an attempt is made to write more coefficients than the buffer can store, the device acknowledges with NACK (not acknowledge) and any further coefficients are ignored. Coefficients that are already in the receive buffer remain intact.

An expert mode transfer ends when the I^2C-bus STOP condition or a repeated START condition has been detected. Only those coefficients that have been received during the last transmission will then be copied from the buffer to the CRAM.

To make efficient and correct use of the expert mode, it is recommended to transfer all coefficients for any one function in a single transmission.

There is no checking of memory addresses and the automatic incrementing of addresses does not stop at the highest used CRAM address. The user of this expert mode must be fully acquainted with the relevant procedures.

More information concerning the functions of this device, such as the number of coefficients per function, their default values, memory addresses, etc., can be supplied on request at a later date.

11 I^2S-BUS DESCRIPTION

The feature interface of the TDA9875A contains two serial audio inputs and outputs and associated clock signals. It can be used to supply, for example, audio signals from received TV programs to a digital audio output device (AES/EBU format), or import serial audio signals from other sources for reproduction through the TV set’s loudspeaker and/or headphone channels. Apart from such simple data input or output, it is also possible to run audio signals through an external DSP, which performs some additional functions, such as room simulation, Dolby Surround Pro Logic etc. and feed those signals back into the loudspeaker and/or headphone channels of the TDA9875A.

Two serial audio formats are supported at the feature interface, i.e. the I^{2}S-bus format and a very similar MSB-aligned format. The difference is illustrated in Fig.7.

In both formats the left audio channel of a stereo sample pair is output first and is placed on the serial data line (SDI for input, SDO for output) when the word select line (WS) is LOW. Data is written at the trailing edge of SCK and read at the leading edge of SCK. The most significant bit is sent first.

At power-up, the outputs of the feature interface are 3-stated to reduce EMC and allow for combinations with other ICs. If output is desired, it has to be activated by means of an I^{2}C-bus command.

When the output is enabled, the serial audio data can be taken from pins SDO1 and SDO2. Depending on the signal source, switch and matrix positions, the output can be either mono, stereo or dual language sound on either output.

The word select output is clocked with the audio sample frequency at 32 kHz. The serial clock output (SCK) is clocked at a frequency of 2.048 MHz. This means, that there are 64 clock pulses per pair of stereo output samples, or 32 clock pulses per sample. Depending again on the signal source, the number of significant bits on the serial data outputs, SDO1 and SDO2, is between 14 and 18.

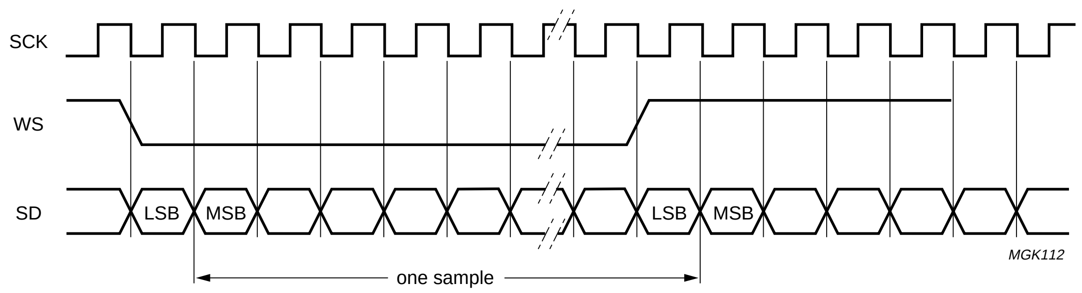
Apart from just feeding a digital audio device, such as a DAC or an AES/EBU transmitter, the serial data outputs can be connected directly to the serial inputs (loop-back connection) or first to an external device, e.g. a feature DSP such as the SAA7710 and then back to the serial inputs. In all of these configurations, the SCK and WS clocks will be generated by the TDA9875A, which then is the I^{2}S-bus master.

The serial data inputs, SDI1 and SDI2, are active at all times, independent of the serial data outputs being on or off.
When the serial data outputs are off (either after power-up or via the appropriate I^{2}C-bus command) serial data and clocks WS and SCK from a separate digital audio source can be fed into the TDA9875A, be processed and output in accordance with internal selector positions, provided that the following criteria are met:

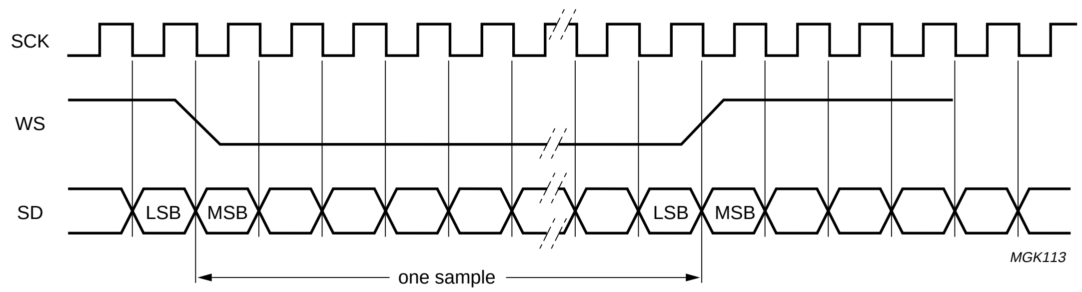
- 32 kHz audio sample frequency
- 32 clock bits per sample
- External timing and data synchronized to TDA9875A.

In such cases, the external source is the I^{2}S-bus master and the TDA9875A is the I^{2}S-bus slave.

To support synchronization of external devices or as a master clock for them, a system clock output, SYSCLK, is available from the TDA9875A. At power-up it is off. It can be enabled and the output frequency set via an I^{2}C-bus command. Available output frequencies are 8.192, 12.288, 16.384 and 24.576 MHz.



a. I²S-bus format.



b. MSB-aligned format.

Fig.7 Serial audio interface formats.

12 EXTERNAL COMPONENTS

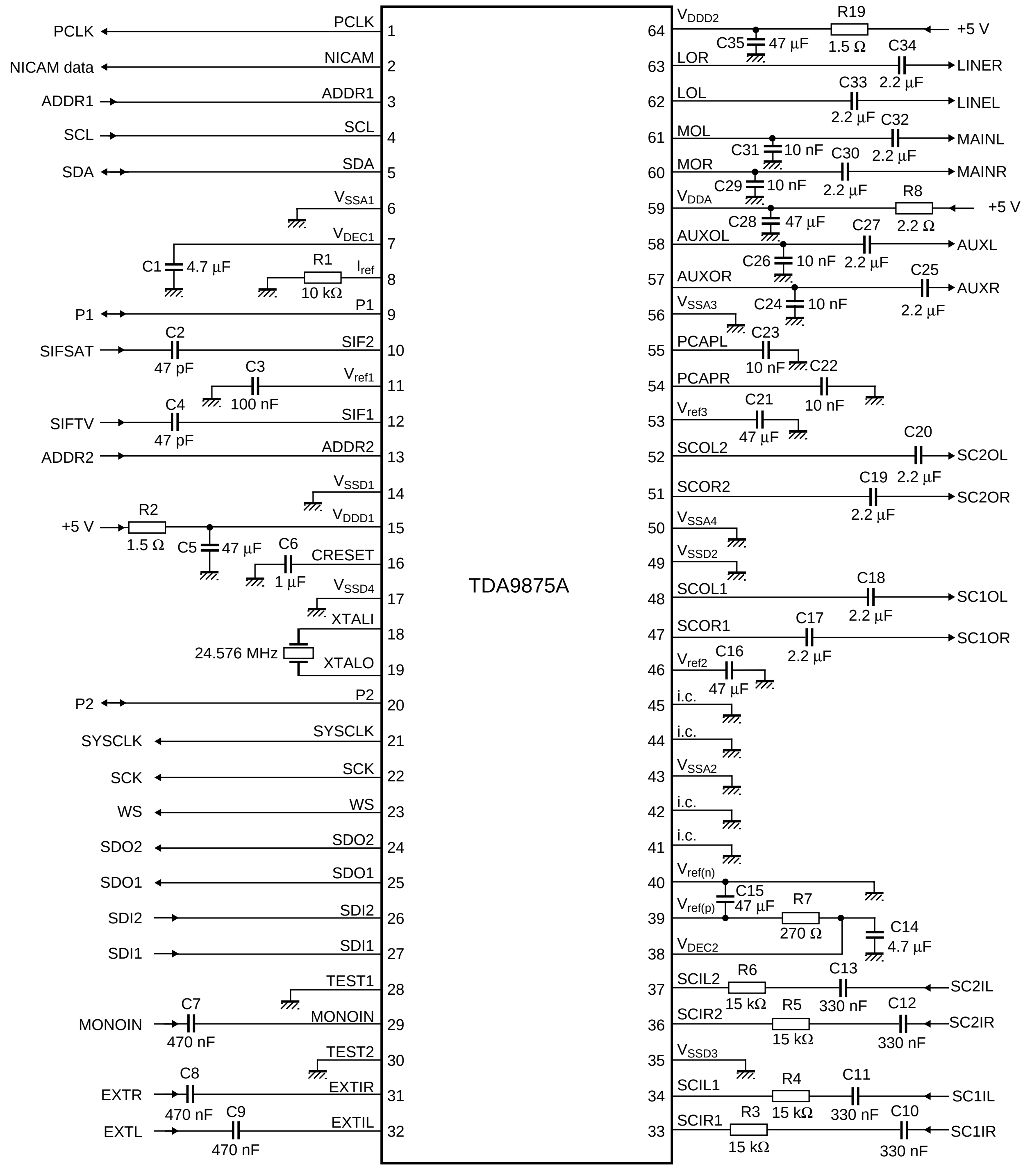
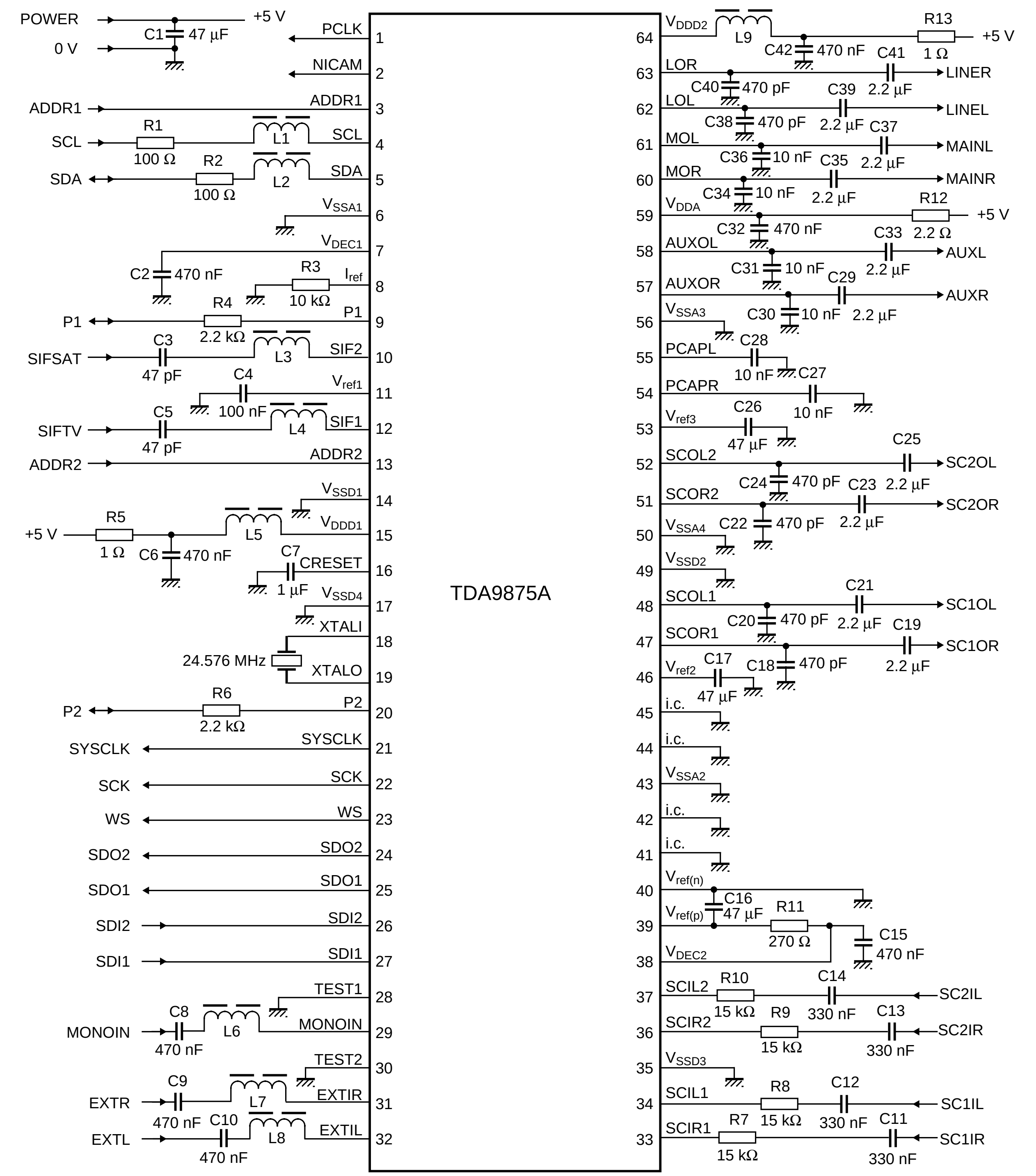


Fig.8 Schematic for measurements.

13 APPLICATION CIRCUITRY

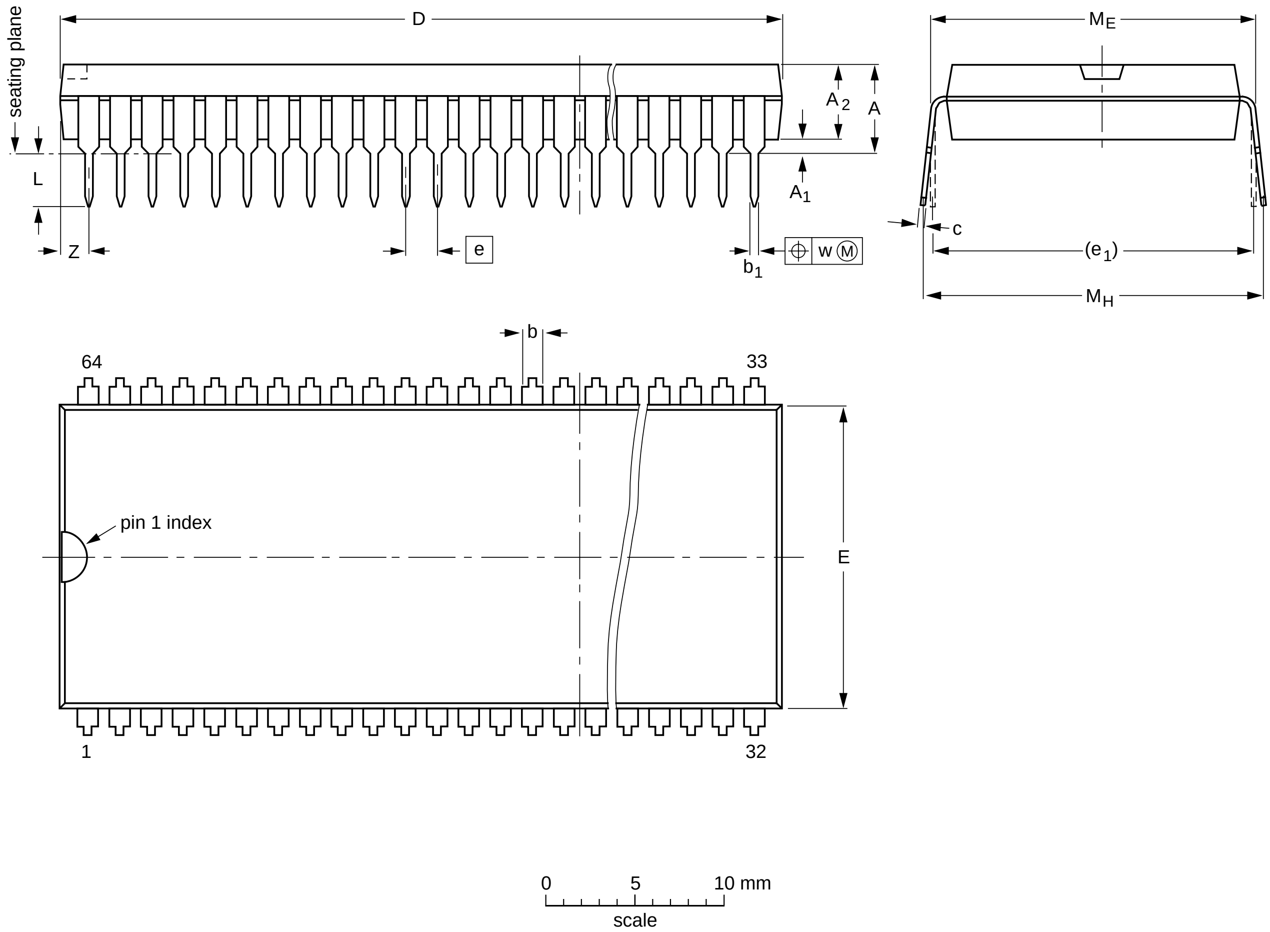


note: L's are ferrite beads.

Fig.9 Schematic for application.

14 PACKAGE OUTLINE

SDIP64: plastic shrink dual in-line package; 64 leads (750 mil) **SOT274-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.84	0.51	4.57	1.3 0.8	0.53 0.40	0.32 0.23	58.67 57.70	17.2 16.9	1.778	19.05	3.2 2.8	19.61 19.05	20.96 19.71	0.18	1.73

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT274-1						~~92-10-13~~ 95-02-04

15 SOLDERING

15.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *“IC Package Databook”* (order code 9398 652 90011).

15.2 Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

15.3 Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

16 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

17 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

18 PURCHASE OF PHILIPS I^2C COMPONENTS

Purchase of Philips I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C system provided the system conforms to the I^2C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,
Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax.+381 11 635 777

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

Printed in The Netherlands 545104/1200/01/pp96 Date of release: 1998 Aug 13 Document order number: 9397 750 03004

Let's make things better.

Philips
Semiconductors

PHILIPS