INTEGRATED CIRCUITS

# DATA SHEET

# TDA8793

## 8-bit, low-power, 3 V, 100 Msps, analog-to-digital converter

Objective specification
File under Integrated Circuits, IC02

1998 May 14

Philips Semiconductors

PHILIPS

# 8-bit, low-power, 3 V, 100 Msps, analog-to-digital converter

# TDA8793

## FEATURES

- 8-bit low-power ADC (170 mW typical)
- 2.7 to 3.6 V operation
- Sampling rate up to 100 Msps
- Track-and-hold circuit
- CMOS/TTL compatible digital inputs and outputs
- Internal references
- Power-down mode; 5 mW.

## GENERAL DESCRIPTION

The TDA8793 is an 8-bit low-power Analog-to-Digital Converter (ADC) which includes a track-and-hold circuit and an internal reference. The device converts an analog input signal, up to 100 MHz, into 8-bit binary codes at a maximum sample rate of 100 Msps. All digital inputs and output are TTL/CMOS compatible.

The power-down mode enables the device power consumption to be reduced to 5 mW.

## APPLICATIONS

- Radio communications
- Digital data storage read channels
- Medical imaging
- Digital instrumentation.

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{CCA}$ | analog supply voltage | | 2.7 | 3.0 | 3.6 | V |
| $V_{CCD}$ | digital supply voltage | | 2.7 | 3.0 | 3.6 | V |
| $V_{CCO}$ | output stages supply voltage | | 2.7 | 3.0 | 3.6 | V |
| $I_{CCA}$ | analog supply current | | – | 40 | – | mA |
| $I_{CCD}$ | digital supply current | | – | 16 | – | mA |
| $I_{CCO}$ | output stages supply current | | – | 0.1 | – | mA |
| INL | integral non linearity | ramp input; $f_{CLK}$ = 100 MHz; $V_{CCA} = V_{CCD}$ = 3 V | – | ±1 | tbf | LSB |
| DNL | differential non-linearity | ramp input; $f_{CLK}$ = 100 MHz; $V_{CCA} = V_{CCD}$ = 3 V | – | ±0.75 | tbf | LSB |
| $f_{CLK(max)}$ | maximum clock input frequency | | 100 | – | – | MHz |
| $P_{tot}$ | total power dissipation | $V_{CC}$ = 3 V | – | tbf | – | mW |

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| TDA8793 | LQFP32 | plastic low profile quad flat package; 32 leads; body 5 × 5 × 1.4 mm | SOT401-1 |

## BLOCK DIAGRAM

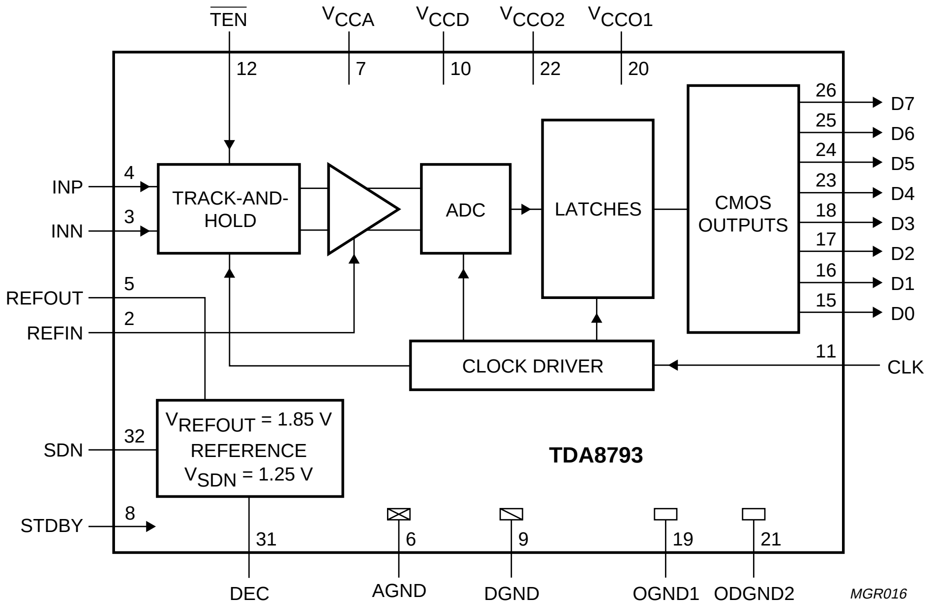



Fig.1 Block diagram.

# 8-bit, low-power, 3 V, 100 Msps, analog-to-digital converter

# TDA8793

## PINNING

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| n.c. | 1 | not connected |
| REFIN | 2 | reference input for ADC |
| INN | 3 | negative input |
| INP | 4 | positive input |
| REFOUT | 5 | reference for AC coupling |
| AGND | 6 | analog ground |
| $V_{CCA}$ | 7 | analog supply voltage |
| STDBY | 8 | standby mode input; (active HIGH) |
| DGND | 9 | digital ground |
| $V_{CCD}$ | 10 | digital supply voltage |
| CLK | 11 | clock input |
| $\overline{TEN}$ | 12 | track enable input; (active LOW) |
| n.c. | 13 | not connected |
| n.c. | 14 | not connected |
| D0 | 15 | data output bit 0 (LSB) |
| D1 | 16 | data output bit 1 |

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| D2 | 17 | data output bit 2 |
| D3 | 18 | data output bit 3 |
| OGND1 | 19 | output ground 1 |
| $V_{CCO1}$ | 20 | output supply voltage 1 |
| OGND2 | 21 | output ground 2 |
| $V_{CCO2}$ | 22 | output supply voltage 2 |
| D4 | 23 | data output bit 4 |
| D5 | 24 | data output bit 5 |
| D6 | 25 | data output bit 6 |
| D7 | 26 | data output bit 7 (MSB) |
| n.c | 27 | not connected |
| n.c | 28 | not connected |
| n.c | 29 | not connected |
| n.c | 30 | not connected |
| DEC | 31 | decoupling |
| SDN | 32 | stabilized decoupling node |

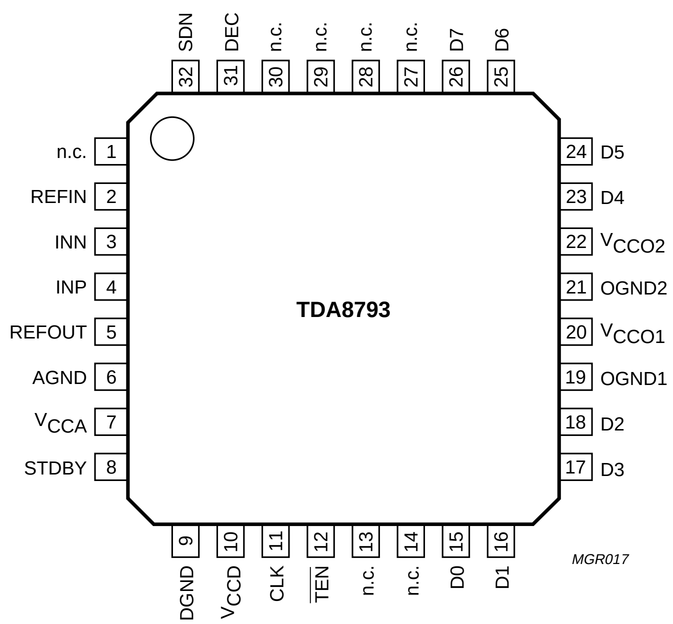



Fig.2 Pin configuration.

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{CCA}$ | analog supply voltage | | –0.3 | +7.0 | V |
| $V_{CCD}$ | digital supply voltage | | –0.3 | +7.0 | V |
| $V_{CCO}$ | output stages supply voltage | | –0.3 | +7.0 | V |
| $\Delta V_{CC}$ | supply voltage differences between: | | | | |
| | $V_{CCA}$ and $V_{CCD}$ | | –1.0 | +1.0 | V |
| | $V_{CCO}$ and $V_{CCD}$ | | –1.0 | +1.0 | V |
| | $V_{CCA}$ and $V_{CCO}$ | | –1.0 | +1.0 | V |
| $V_{INP, INN}$ | input voltage range | referenced to AGND | –0.3 | +7.0 | V |
| $I_O$ | output current | | – | 10 | mA |
| $T_{stg}$ | storage temperature | | –55 | +150 | °C |
| $T_{amb}$ | operating ambient temperature | | 0 | 70 | °C |
| $T_j$ | junction temperature | | – | – | °C |

## HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

## THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| $R_{th\ j\text{-}a}$ | thermal resistance from junction to ambient | in free air | 94 | °C/W |

## CHARACTERISTICS

$V_{CCA}$ = $V_7$ to $V_6$ = 2.7 to 3.6 V; $V_{CCD}$ = $V_{10}$ to $V_9$ = 2.7 to 3.6 V; $V_{CCO}$ = $V_{20}$ (or $V_{22}$) to $V_{19}$ (or $V_{21}$) = 2.7 to 3.6 V; AGND to DGND and OGND shorted together; $V_{CCA}$ to $V_{CCD}$ = –0.15 to +0.15 V; $V_{CCD}$ to $V_{CCO}$ = –0.15 to +0.15 V; $V_{CCA}$ to $V_{CCO}$ = –0.15 to +0.15 V; $T_{amb}$ = 0 to 70 °C; typical values measured at $V_{CCA}$ = $V_{CCD}$ = $V_{CCO}$ = 3.0 V and $T_{amb}$ = 25 °C unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| $V_{CCA}$ | analog supply voltage | | 2.7 | 3.0 | 3.6 | V |
| $V_{CCD}$ | digital supply voltage | | 2.7 | 3.0 | 3.6 | V |
| $V_{CCO}$ | output stages supply voltage | | 2.7 | 3.0 | 3.6 | V |
| $I_{CCA}$ | analog supply current | | – | 40 | – | mA |
| $I_{CCD}$ | digital supply current | | – | 16 | – | mA |
| $I_{CCO}$ | output stages supply current | $f_i$ = ramp input | – | 0.1 | – | mA |
| | | $f_i$ = 50 MHz | – | tbf | – | mA |
| **Internal reference (SDN pin);** note 1 | | | | | | |
| $V_{ref}$ | reference voltage | | – | 1.25 | – | V |
| $V_{reg}$ | line regulation voltage | 2.7 < $V_{CCA}$ < 3.6 V | – | 2 | – | mV |
| TC | temperature coefficient | | – | tbf | – | ppm/K |
| $I_L$ | load current | | –500 | – | – | μA |
| **Internal reference (pin REFOUT)** | | | | | | |
| $V_{o(ref)}$ | reference voltage | | – | 1.85 | – | V |
| $V_{o(reg)}$ | line regulation voltage | 2.7 < $V_{CCA}$ < 3.6 V | – | 3 | – | mV |
| TC | temperature coefficient | | – | tbf | – | ppm/K |
| $I_L$ | load current | | –500 | – | – | μA |
| **Clock input (pin CLK);** note 2 | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | 0 | – | 0.8 | V |
| $V_{IH}$ | HIGH-level input voltage | | 2 | – | $V_{CCD}$ | V |
| $I_{IL}$ | LOW-level input current | $V_{CLK}$ = 0 | –2 | – | +2 | μA |
| $I_{IH}$ | HIGH-level input current | $V_{CLK}$ = $V_{CCD}$ | – | – | 5 | μA |
| $t_r$ | clock rise time | | 0.75 | – | tbf | ns |
| $t_f$ | clock fall time | | 0.75 | – | tbf | ns |
| $Z_i$ | input impedance | $f_{CLK}$ = 100 MHz | – | tbf | – | kΩ |
| $C_i$ | input capacitance | $f_{CLK}$ = 100 MHz | – | 2 | – | pf |
| **Standby input (pin STDBY);** see Table 1 | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | 0 | – | 0.8 | V |
| $V_{IH}$ | HIGH-level input voltage | | 2 | – | $V_{CCD}$ | V |
| $I_{IL}$ | LOW-level input current | $V_{CLK}$ = 0 | –5 | – | – | μA |
| $I_{IH}$ | HIGH-level input current | $V_{CLK}$ = $V_{CCD}$ | – | – | 5 | μA |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Track enable input (pin $\overline{TEN}$);** see Table 2 | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | 0 | – | 0.8 | V |
| $V_{IH}$ | HIGH-level input voltage | | 2 | – | $V_{CCD}$ | V |
| $I_{IL}$ | LOW-level input current | $V_{CLK} = 0$ | –5 | – | – | μA |
| $I_{IH}$ | HIGH-level input current | $V_{CLK} = V_{CCD}$ | – | – | 5 | μA |
| **Pins INP and INN (analog input voltage referenced to AGND); $V_{REFIN}$ = 1.25 V;** see Table 3 | | | | | | |
| $V_{i(p-p)}$ | input voltage range (peak-to-peak value) | $V_i = V_{INP} - V_{INN}$; $T_{amb} = 25$ °C | 0.95 | 1 | 1.05 | V |
| $\Delta T_{CI}$ | input voltage range drift | | – | tbf | – | ppm/K |
| $V_{i(os)}$ | input offset voltage | output code = 127 | tbf | tbf | tbf | mV |
| $Z_i$ | input impedance | $f_{CLK}$ = 50 MHz | – | tbf | – | kΩ |
| $C_i$ | input capacitance | $f_{CLK}$ = 50 MHz | – | 2 | – | pf |
| $I_{IL}$ | LOW-level input current | $V_{INP} = V_{REFOUT} - 0.5$; $V_{INP} = V_{REFOUT} + 0.5$ | –1 | – | – | μA |
| $I_{IH}$ | HIGH-level input current | $V_{INP} = V_{REFOUT} - 0.5$; $V_{INP} = V_{REFOUT} + 0.5$ | – | – | 40 | μA |
| **Voltage controlled regulator input pin $V_{REFIN}$ (referenced to AGND);** see note 3 | | | | | | |
| $V_{i(ref)}$ | reference voltage | | tbf | 1.25 | tbf | V |
| $I_{i(ref)}$ | input current on pin $V_{REFIN}$ | | – | tbf | – | μA |
| **Outputs; ADC data outputs** | | | | | | |
| $V_{OL}$ | LOW-level output voltage | $I_O$ = 1 mA | – | – | 0.5 | V |
| $V_{OH}$ | HIGH-level output voltage | $I_O$ = –0.4 mA | $V_{CC} - 0.5$ | – | $V_{CCD}$ | V |
| $C_L$ | output load capacitance | | – | – | 10 | pF |
| $\delta v/\delta t$ | slew rate | 10 to 90%; $C_L$ = 10 pF | – | tbf | – | V/ns |
| **Switching characteristics;** see note 2 and Table 1 | | | | | | |
| $f_{CLK(min)}$ | minimum clock frequency | track = LOW | – | – | tbf | MHz |
| | | track = HIGH | – | – | tbf | kHz |
| $f_{CLK(max)}$ | maximum clock frequency | | 100 | – | – | MHz |
| $t_{W(CLKH)}$ | clock pulse width HIGH | | 4 | – | – | ns |
| $t_{W(CLKL)}$ | clock pulse width LOW | | 4 | – | – | ns |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Analog signal processing;** see note 3 | | | | | | |
| INL | integral non-linearity | ramp input; $f_{CLK}$ = 100 MHz; $V_{CCA}$ = $V_{CCD}$ = 3 V | – | ±1 | tbf | LSB |
| DNL | differential non-linearity | ramp input; $f_{CLK}$ = 100 MHz; $V_{CCA}$ = $V_{CCD}$ = 3 V | – | ±0.75 | tbf | LSB |
| S/N | signal-to-noise ratio (full scale) | without harmonics; $f_i$ = 50 MHz; $f_{CLK}$ = 100 MHz | – | 44.5 | – | dB |
| $B_{A(-3dB)}$ | –3 dB analog bandwidth | | – | 150 | – | MHz |
| THD | total harmonics distortion | $f_i$ = 50 MHz; single mode | – | –55 | – | dB |
| | | $f_i$ = 50 MHz; differential mode | – | –55 | – | dB |
| $H_{fund(FS)}$ | full scale fundamental harmonics | $f_i$ = 50 MHz; $f_{CLK}$ = 100 MHz | – | – | 0 | dB |
| $H_{D2(FS)}$ | full scale second harmonic distortion all components | $f_i$ = 50 MHz; $f_{CLK}$ = 100 MHz | – | tbf | – | dB |
| $H_{D3(FS)}$ | full scale third harmonic distortion all components | $f_i$ = 50 MHz; $f_{CLK}$ = 100 MHz; single mode | – | tbf | – | dB |
| | | $f_i$ = 50 MHz; $f_{CLK}$ = 100 MHz; differential mode | – | tbf | – | dB |
| EB | effective bits | $f_{CLK}$ = 100 MHz; note 4 | – | – | – | |
| | | $f_i$ = 20 MHz; note 4 | – | 7.2 | – | bits |
| | | $f_i$ = 50 MHz; note 4 | – | 7.0 | – | bits |
| **Data timing; $f_{CLK}$ = 100 MHz; $C_L$ = 10 pF;** (see Fig.7) | | | | | | |
| $t_{ds}$ | sampling delay | | – | – | 1.5 | ns |
| $t_h$ | output hold time | | 3 | – | – | ns |
| $t_d$ | output delay time | | – | 5 | tbf | ns |

**Notes**

1. It is possible to use the reference output voltage (pin SDN) to drive other analog circuits under the limits indicated in Chapter “Characteristics”.
2. In addition to a good layout of the digital and analog grounds, it is recommended that the rise and fall times of the clock must be not less than 0.75 ns.
3. It is possible with an external reference connected to REFIN pin to adjust the ADC input range. The input range variation will be fixed.
4. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8 k acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio: S/N = 6.02 × EB + 1.76 dB.

**Table 1** Standby selection

| STDBY | S0 TO D7 | $I_{CCA} + I_{CCD}$ |
|---|---|---|
| 0 | inactive | 56 mA |
| 1 | active; output logic state LOW | 1.5 mA |

**Table 2** Track-and-hold selection

| $\overline{TEN}$ | TRACK-AND-HOLD |
|---|---|
| 0 | active |
| 1 | inactive; tracking mode |

**Table 3** Output coding and input voltage (typical values; referenced to AGND); $V_{REFIN}$ = 1.25 V

| STEP | $V_{INP}$ (V) | $V_{INN}$ (V) | BINARY OUTPUT BITS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Underflow | <1.6 | >2.1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1.6 | 2.1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | ... | ... | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| 127 | 1.85 | 1.85 | ... | ... | ... | ... | ... | ... | ... | ... |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| 254 | ... | ... | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 255 | 2.1 | 1.6 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Overflow | >2.1 | <1.6 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

## APPLICATION INFORMATION

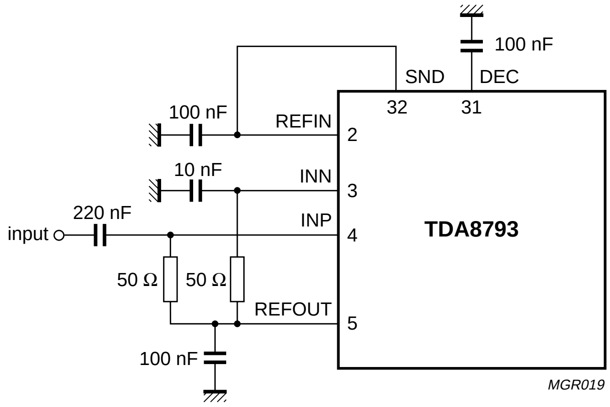



Fig.3 Application diagram for single input mode with internal reference.

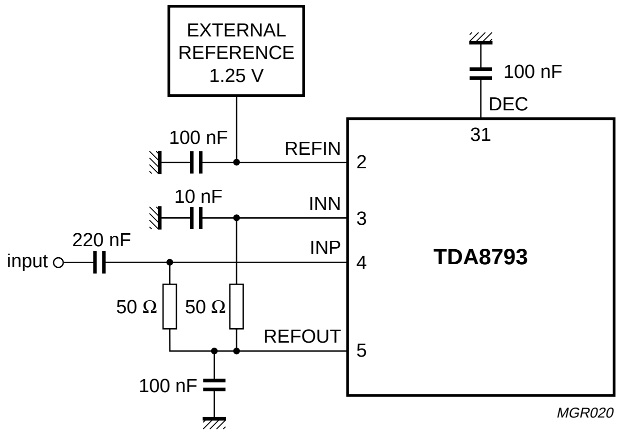



Fig.4 Application diagram for single input mode with external reference.

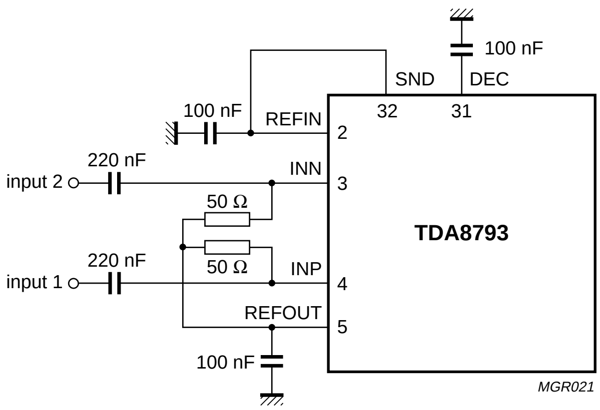



Fig.5 Application diagram for differential input mode with internal reference.

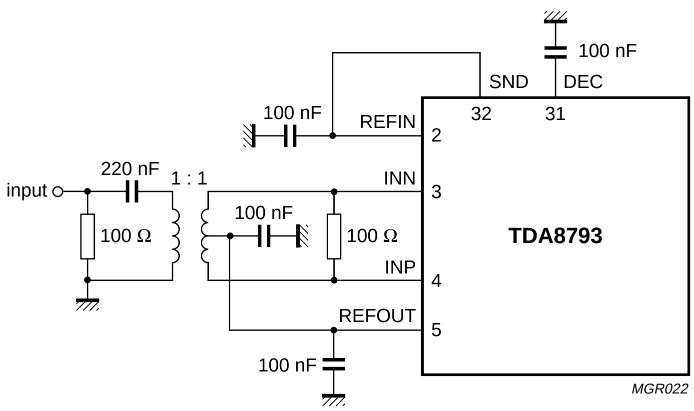



Fig.6 Application diagram for differential input mode using transformer.

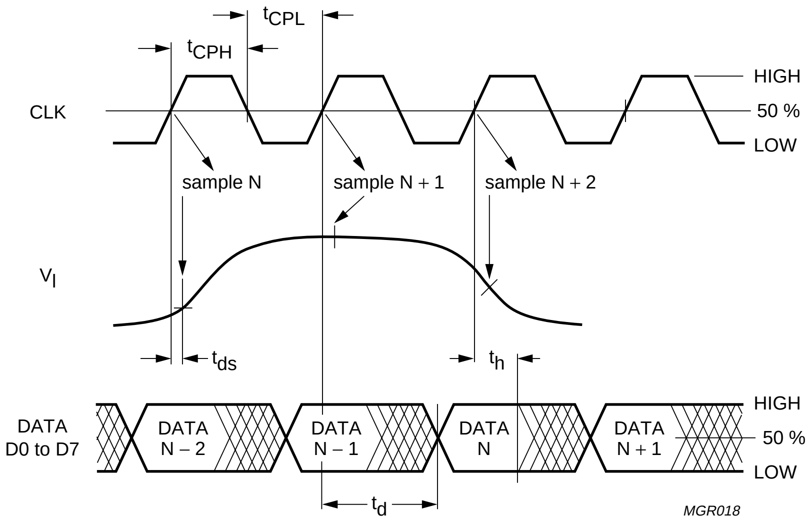
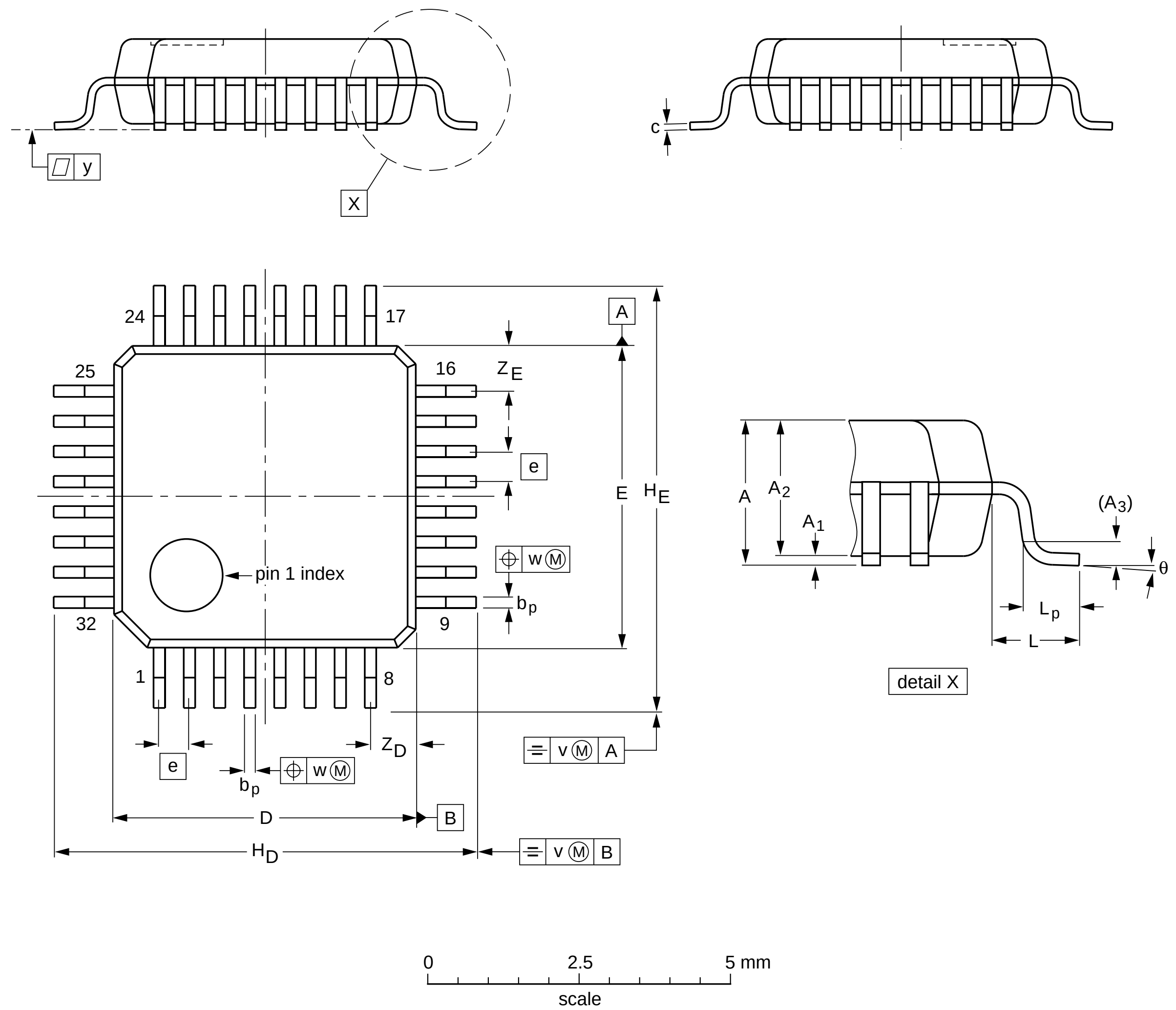



Fig.7 Timing diagram.

## PACKAGE OUTLINE

**LQFP32: plastic low profile quad flat package; 32 leads; body 5 x 5 x 1.4 mm** **SOT401-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D[(1)] | E[(1)] | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D$[(1)] | $Z_E$[(1)] | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.60 | 0.15<br>0.05 | 1.5<br>1.3 | 0.25 | 0.27<br>0.17 | 0.18<br>0.12 | 5.1<br>4.9 | 5.1<br>4.9 | 0.5 | 7.15<br>6.85 | 7.15<br>6.85 | 1.0 | 0.75<br>0.45 | 0.2 | 0.12 | 0.1 | 0.95<br>0.55 | 0.95<br>0.55 | 7°<br>0° |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT401-1 | | | | | | ~~95-12-19~~<br>97-08-04 |

## SOLDERING

### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

### Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

### Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

| CAUTION |
|---|
| **Wave soldering is NOT applicable for all LQFP packages with a pitch (e) equal or less than 0.5 mm.** |

**If wave soldering cannot be avoided, for LQFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:**

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## DEFINITIONS

| Data sheet status | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

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