DATA SHEET

TDA8561TH
2 × 24 W BTL or 4 × 12 W single-ended car radio power amplifier

Preliminary specification
Supersedes data of 1997 Nov 05
File under Integrated Circuits, IC01

2000 Feb 18

Philips Semiconductors

PHILIPS

FEATURES

- Requires very few external components
- High output power
- Flexibility in use; quad single-ended or stereo BTL
- Low output offset voltage
- Fixed gain
- Diagnostic facility (distortion, short-circuit and temperature detection)
- Good ripple rejection
- Mode select switch (operating, mute and standby)
- Load dump protection
- AC and DC short-circuit safe to ground and to V_P
- Low power dissipation in any short-circuit condition
- Thermally protected
- Reverse polarity safe
- Electrostatic discharge protection
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance
- Identical inputs (inverting and non-inverting).

GENERAL DESCRIPTION

The TDA8561TH is an integrated class-B output amplifier in a 20-lead heatsink small outline plastic power package. It contains 4 × 12 W Single-Ended (SE) or 2 × 24 W Bridge-Tied Load (BTL) amplifiers.

The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive operating supply voltage		6	14.4	18	V
I_{ORM}	repetitive peak output current		–	–	4	A
I_P	total quiescent current		–	80	–	mA
I_{sb}	standby current		–	0.1	100	μA
Stereo BTL application						
P_o	output power	R_L = 4 Ω; THD = 10%	–	24	–	W
SVRR	supply voltage ripple rejection		48	–	–	dB
V_{no}	noise output voltage	R_s = 0 Ω	–	70	–	μV
$\|Z_I\|$	input impedance		25	–	–	kΩ
$\|\Delta V_O\|$	DC output offset voltage		–	–	150	mV
Quad single-ended application						
P_o	output power	THD = 10%				
		R_L = 4 Ω	–	7	–	W
		R_L = 2 Ω	–	12	–	W
SVRR	supply voltage ripple rejection		48	–	–	dB
V_{no}	noise output voltage	R_s = 0 Ω	–	50	–	μV
$\|Z_I\|$	input impedance		50	–	–	kΩ

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8561TH	HSOP20	plastic, heatsink small outline package; 20 leads; low stand-off height	SOT418-2

BLOCK DIAGRAM

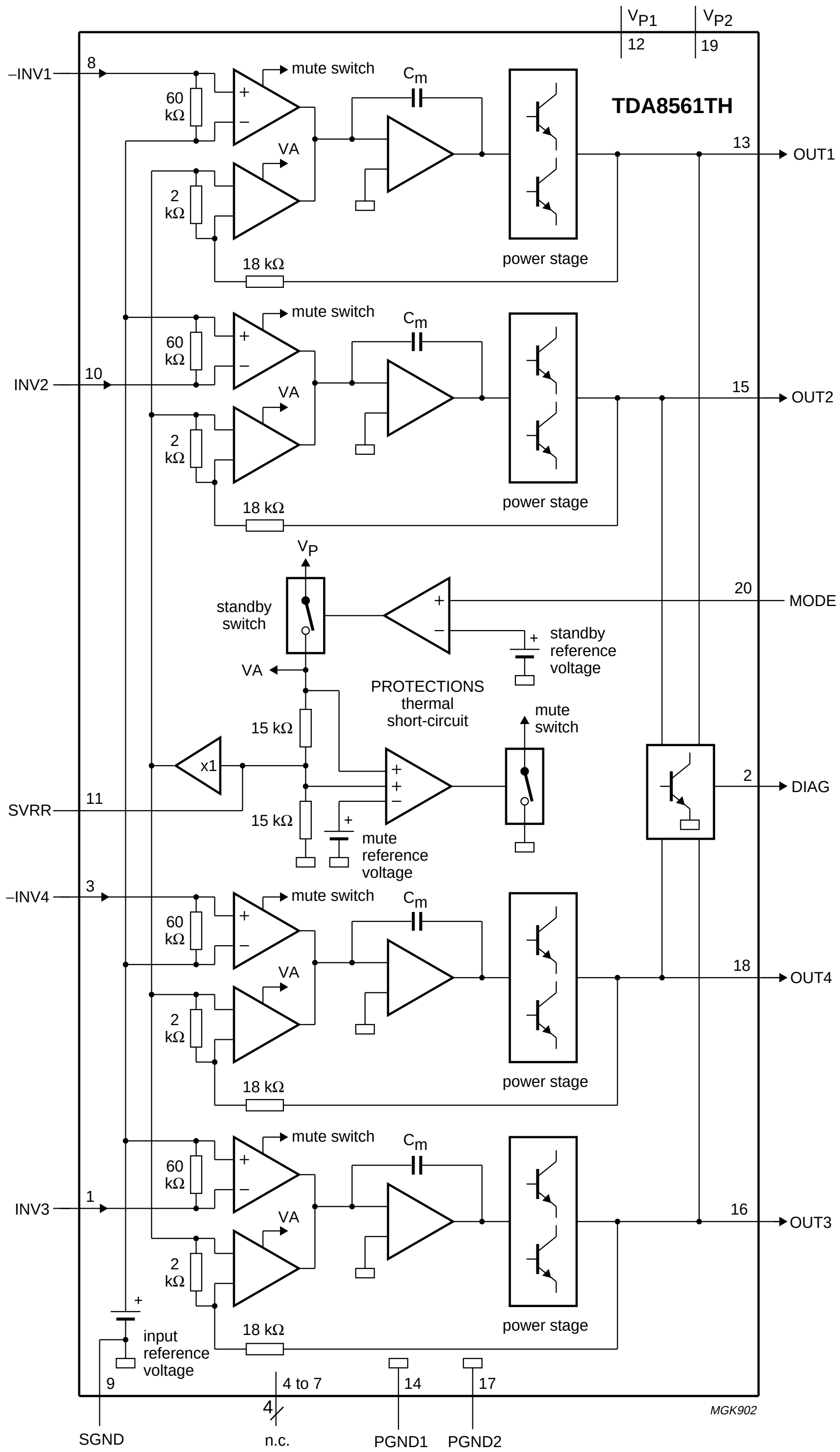


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
INV3	1	inverting input 3
DIAG	2	diagnostic output
–INV4	3	non-inverting input 4
n.c.	4	not connected
n.c.	5	not connected
n.c.	6	not connected
n.c.	7	not connected
–INV1	8	non-inverting input 1
SGND	9	signal ground
INV2	10	inverting input 2
SVRR	11	supply voltage ripple rejection
V_{P1}	12	supply voltage 1
OUT1	13	output 1
PGND1	14	power ground 1
OUT2	15	output 2
OUT3	16	output 3
PGND2	17	power ground 2
OUT4	18	output 4
V_{P2}	19	supply voltage 2
MODE	20	mode select switch (standby/mute/operating)

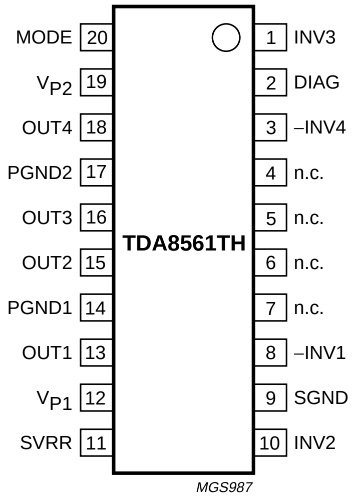


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8561TH contains four identical amplifiers and can be used for Single-Ended (SE) or Bridge-Tied Load (BTL) applications. The gain of each amplifier is fixed at 20 dB (26 dB in BTL). Special features of the device are:

Mode select switch (pin 20)

- Low standby current (<100 μA)
- Low switching current (low cost supply switch)
- Mute facility.

To avoid switch-on plops, it is advised to keep the amplifier in the mute mode during ≥100 ms (charging of the input capacitors at pins 1, 3, 8 and 10). This can be achieved by:

- Microcontroller control
- External timing circuit (see Fig.11).

Diagnostic output (pin 2)

DYNAMIC DISTORTION DETECTOR

At the onset of clipping of one or more output stages, the dynamic distortion detector becomes active and pin 2 goes LOW. This information can be used to drive a sound processor or DC volume control to attenuate the input signal and thus limit the distortion. The output level of pin 2 is independent of the number of channels that are clipping (see Figs 3 and 4).

SHORT-CIRCUIT PROTECTION

When a short-circuit occurs at one or more outputs to ground or to the supply voltage, the output stages are switched off until the short-circuit is removed and the device is switched on again, with a delay of approximately 20 ms, after removal of the short-circuit. During this short-circuit condition, pin 2 is continuously LOW.

When a short-circuit across the load of one or both channels occurs the output stages are switched off for approximately 20 ms. After that time it is checked during approximately 50 µs to see whether the short-circuit is still present. Due to this duty cycle of 50 µs/20 ms the average current consumption during this short-circuit condition is very low (approximately 40 mA).

During this short-circuit condition, pin 2 is LOW for 20 ms and HIGH for 50 µs (see Fig.5).

The power dissipation in any short-circuit condition is very low.

TEMPERATURE DETECTION

When the virtual junction temperature T_{vj} reaches 150 °C, pin 2 will be active LOW.

OPEN-COLLECTOR OUTPUT

Pin 2 is an open-collector output, which allows pin 2 of more devices being tied together.

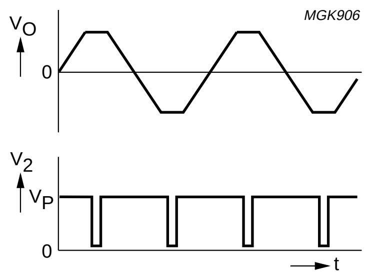


Fig.3 Distortion detector waveform; bridge-tied load application.

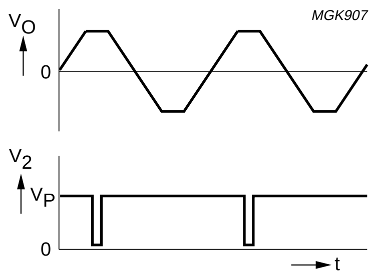


Fig.4 Distortion detector waveform; single-ended application.

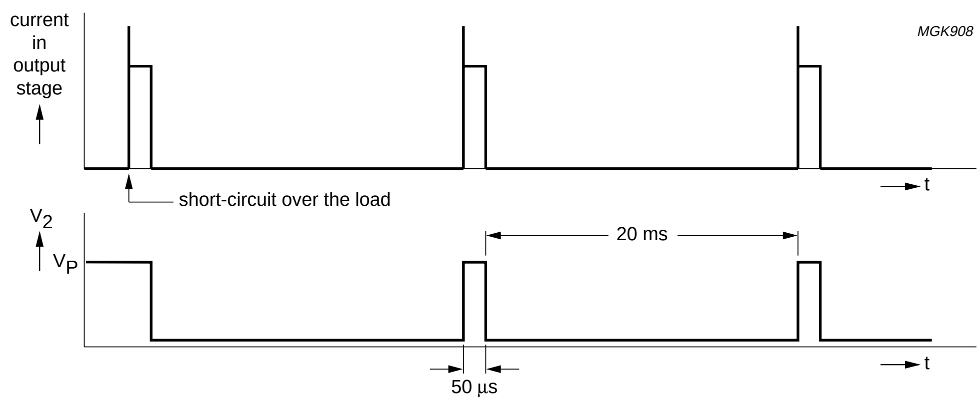


Fig.5 Short-circuit waveform.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage				
	operating		–	18	V
	non-operating		–	30	V
	load dump protection	during 50 ms; $t_r \geq 2.5$ ms	–	45	V
I_{OSM}	non-repetitive peak output current		–	6	A
I_{ORM}	repetitive peak output current		–	4	A
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
T_{vj}	virtual junction temperature		–	150	°C
V_{psc}	AC and DC short-circuit safe voltage		–	18	V
V_{pr}	reverse polarity		–	6	V
P_{tot}	total power dissipation		–	60	W

THERMAL CHARACTERISTICS

In accordance with IEC 60747-1.

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	see Figs 6 and 7	1.3	K/W

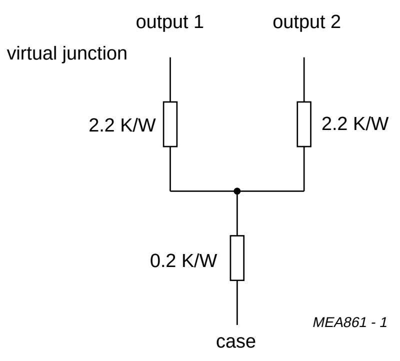


Fig.6 Equivalent thermal resistance network; BTL application.

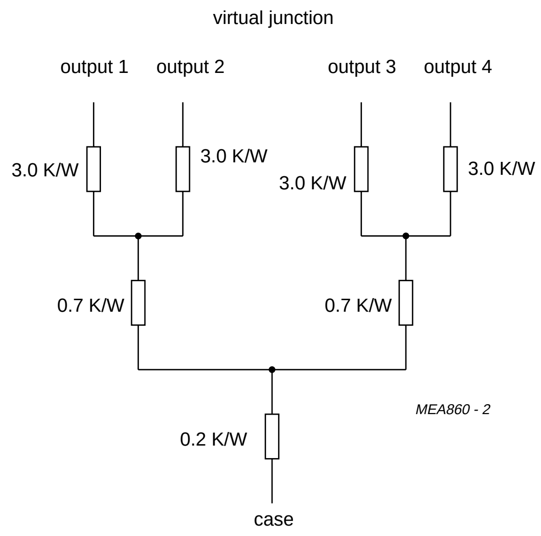


Fig.7 Equivalent thermal resistance network; single-ended application.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measured in Fig.8; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage	note 1	6	14.4	18	V
I_P	total quiescent current		–	80	160	mA
V_O	DC output voltage	note 2	–	6.9	–	V
$\|\Delta V_O\|$	DC output offset voltage		–	–	150	mV
Mode select switch (pin 20)						
OPERATING CONDITION						
V_{on}	switch-on voltage level		8.5	–	–	V
MUTE CONDITION						
V_{mute}	mute voltage		3.3	–	6.4	V
V_O	output voltage in mute position	V_{Imax} = 1 V; f = 1 kHz	–	–	2	mV
$\|\Delta V_O\|$	DC output offset voltage (between pins 13 to 15 and 16 to 18)		–	–	150	mV
STANDBY CONDITION						
V_{sb}	standby voltage		0	–	2	V
I_{sb}	standby current		–	–	100	μA
I_{sw}	switch-on current		–	12	40	μA
Diagnostic output (pin 2)						
V_{DIAG}	diagnostic output voltage	any short-circuit or clipping	–	–	0.6	V

Notes

1. The circuit is DC adjusted at V_P = 6 to 18 V and AC operating at V_P = 8.5 to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage is ≤0.5V_P.

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Stereo BTL application (measured in Fig.8)						
P_o	output power	note 1				
		THD = 0.5%	15	19	–	W
		THD = 10%	20	24	–	W
THD	total harmonic distortion	P_o = 1 W	–	0.1	–	%
P_o	output power	V_P = 13.2 V				
		THD = 0.5%	–	16	–	W
		THD = 10%	–	20	–	W
B	power bandwidth	THD = 0.5%; P_o = –1 dB; with respect to 15 W	–	20 to 15000	–	Hz
f_l	low frequency roll-off	at –1 dB; note 2	–	45	–	Hz
f_h	high frequency roll-off	at –1 dB	20	–	–	kHz
G_v	closed loop voltage gain		25	26	27	dB
SVRR	supply voltage ripple rejection	note 3				
	on		48	–	–	dB
	mute		48	–	–	dB
	standby		80	–	–	dB
$\|Z_I\|$	input impedance		25	30	38	kΩ
V_{no}	noise output voltage					
	on	R_S = 0 Ω; note 4	–	70	–	μV
	on	R_S = 10 kΩ; note 4	–	100	200	μV
	mute	notes 4 and 5	–	60	–	μV
α_{cs}	channel separation	R_S = 10 kΩ	40	–	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB
DYNAMIC DISTORTION DETECTOR						
THD	total harmonic distortion	$V_2 \leq$ 0.6 V; no short-circuit	–	10	–	%
Quad single-ended application (measured in Fig.9)						
P_o	output power	note 1				
		THD = 0.5%	4	5	–	W
		THD = 10%	5.5	7	–	W
THD	total harmonic distortion	P_o = 1 W	–	0.1	–	%
P_o	output power	R_L = 2 Ω; note 1				
		THD = 0.5%	7.5	10	–	W
		THD = 10%	10	12	–	W
f_l	low frequency roll-off	at –1 dB; note 2	–	25	–	Hz
f_h	high frequency roll-off	at –1 dB	20	–	–	kHz
G_v	closed loop voltage gain		19	20	21	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SVRR	supply voltage ripple rejection	note 3				
	on		48	–	–	dB
	mute		48	–	–	dB
	standby		80	–	–	dB
$\|Z_I\|$	input impedance		50	60	75	kΩ
V_{no}	noise output voltage					
	on	R_s = 0 Ω; note 4	–	50	–	μV
	on	R_s = 10 kΩ; note 4	–	70	100	μV
	mute	notes 4 and 5	–	50	–	μV
α_{cs}	channel separation	R_s = 10 kΩ	40	–	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB
DYNAMIC DISTORTION DETECTOR						
THD	total harmonic distortion	$V_2 \leq 0.6$ V; no short-circuit	–	10	–	%

Notes

1. Output power is measured directly at the output pins of the IC.
2. Frequency response externally fixed.
3. Ripple rejection measured at the output with a source impedance of 0 Ω, maximum ripple amplitude of 2 V (p-p) and at a frequency between 100 Hz and 10 kHz.
4. Noise measured in a bandwidth of 20 Hz to 20 kHz.
5. Noise output voltage independent of R_s (V_i = 0 V).

TEST AND APPLICATION INFORMATION

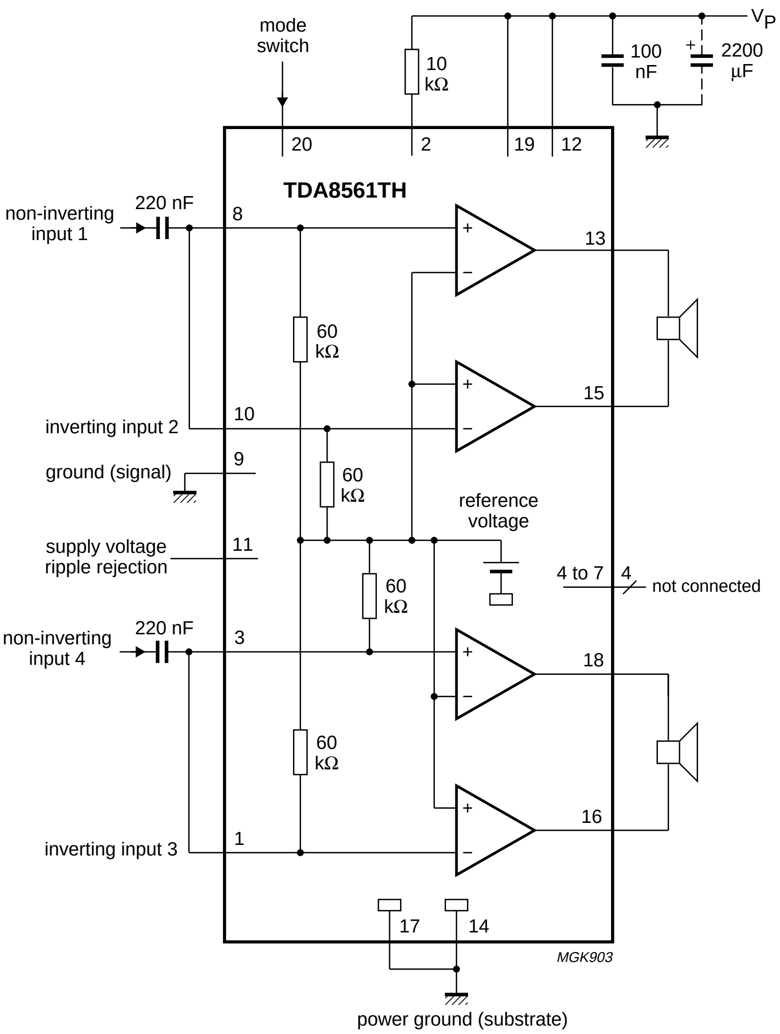


Fig.8 Stereo BTL application diagram.

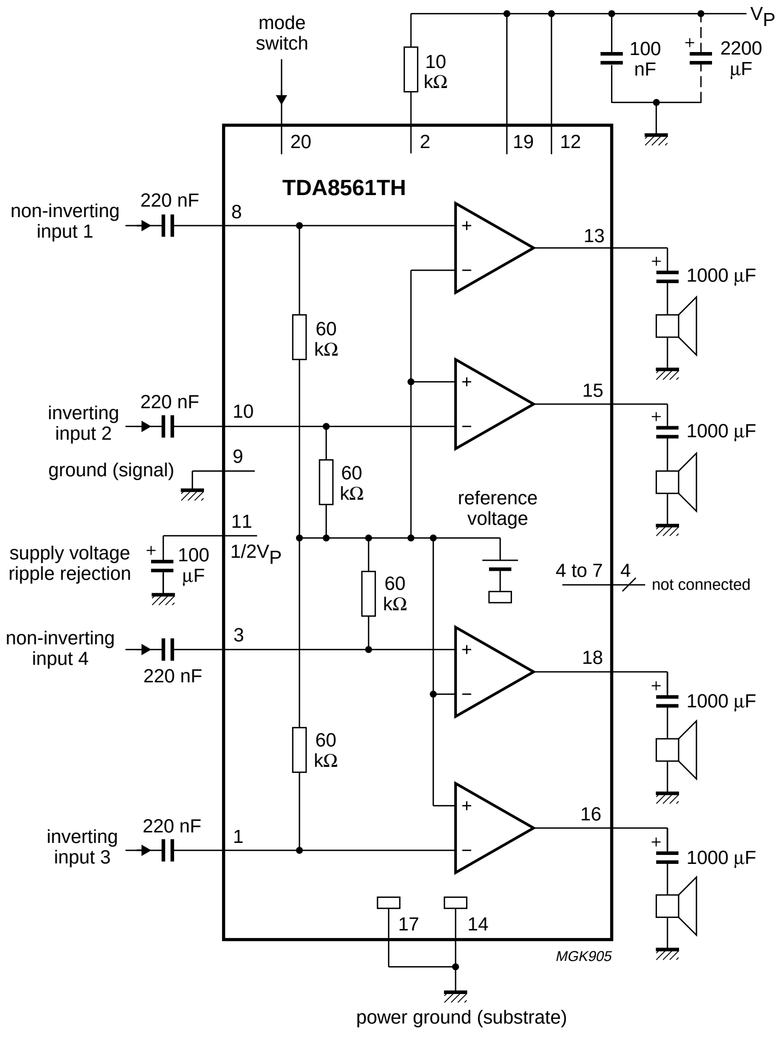
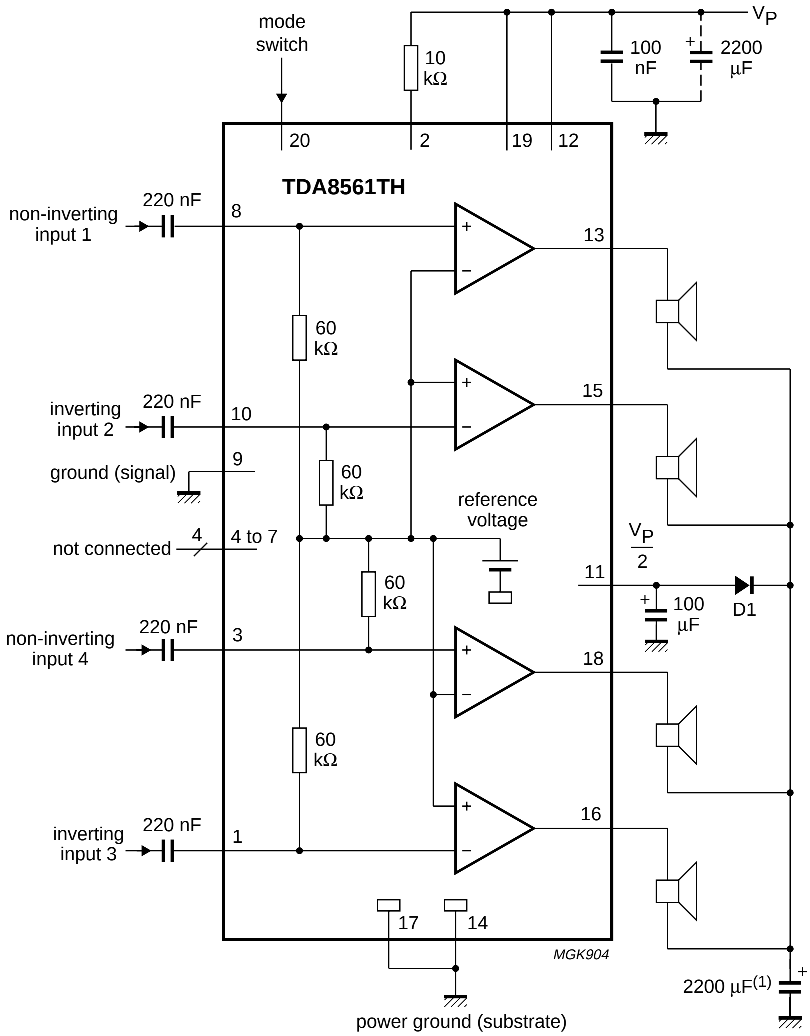


Fig.9 Quad single-ended application diagram 1.



(1) When short-circuiting the single-ended capacitor, the dissipation will be reduced due to diode D1.

Fig.10 Quad single-ended application diagram 2.

Mode select switch

To avoid switch-on plops, it is advised to keep the amplifier in the mute mode during >100 ms (charging of the input capacitors at pins 1, 3, 8 and 10).

The circuit in Fig.11 slowly ramps up the voltage at the mode select switch pin when switching on and results in fast muting when switching off.

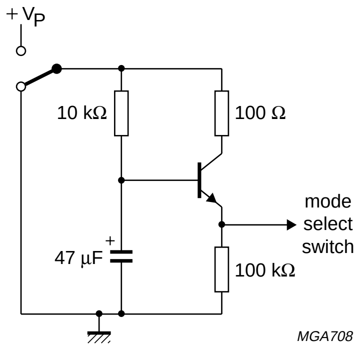
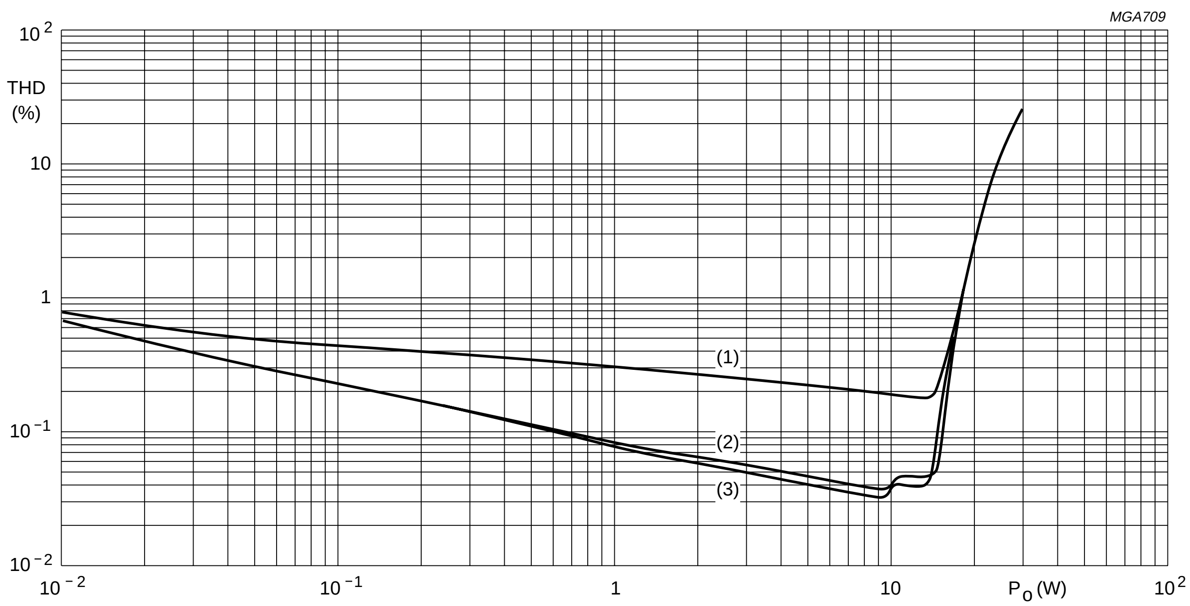
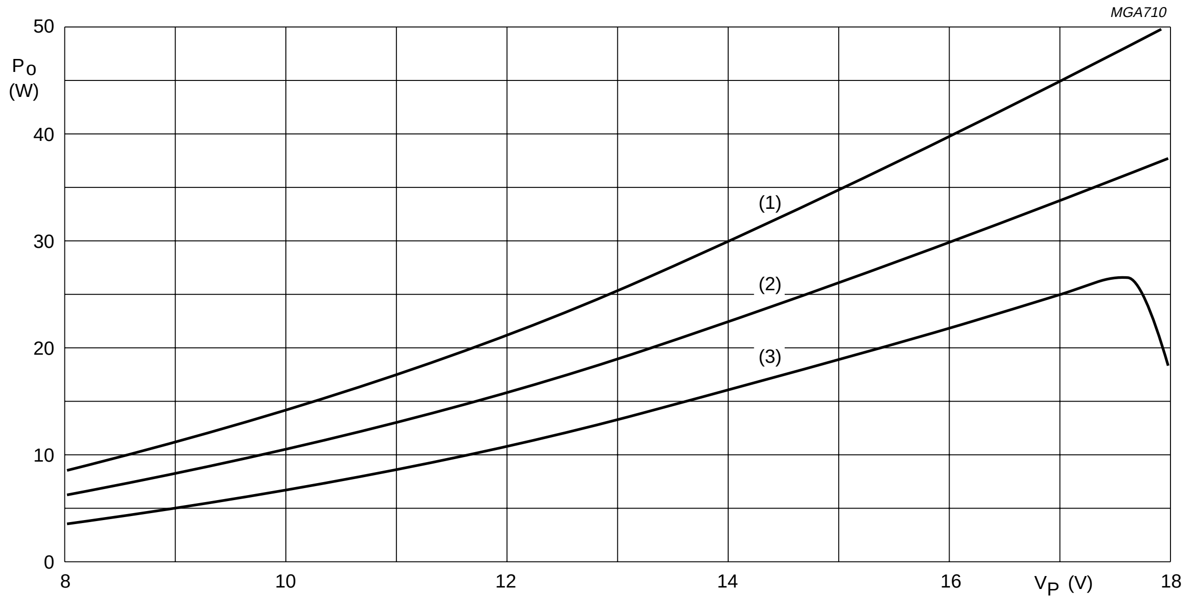


Fig.11 Mode select switch circuitry.



(1) f = 10 kHz.
(2) f = 1 kHz.
(3) f = 100 Hz.

Fig.12 Total harmonic distortion as a function of output power; V_P = 14.4 V, R_L = 4 Ω.



(1) THD = 30%.
(2) THD = 10%.
(3) THD = 0.5%.

Fig.13 Output power as a function of supply voltage.

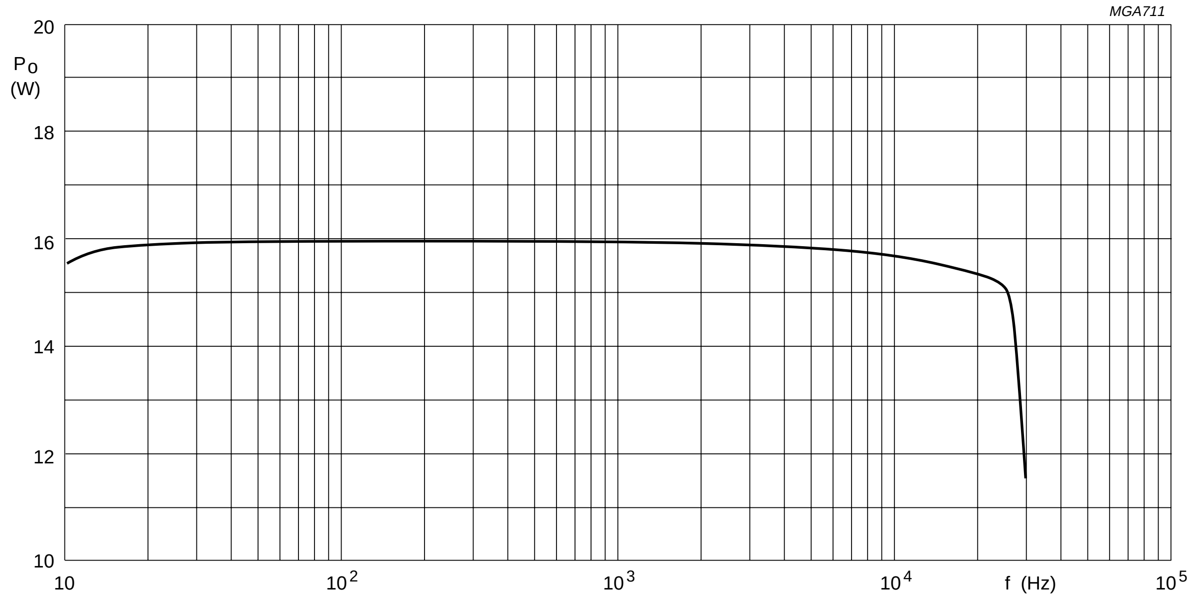
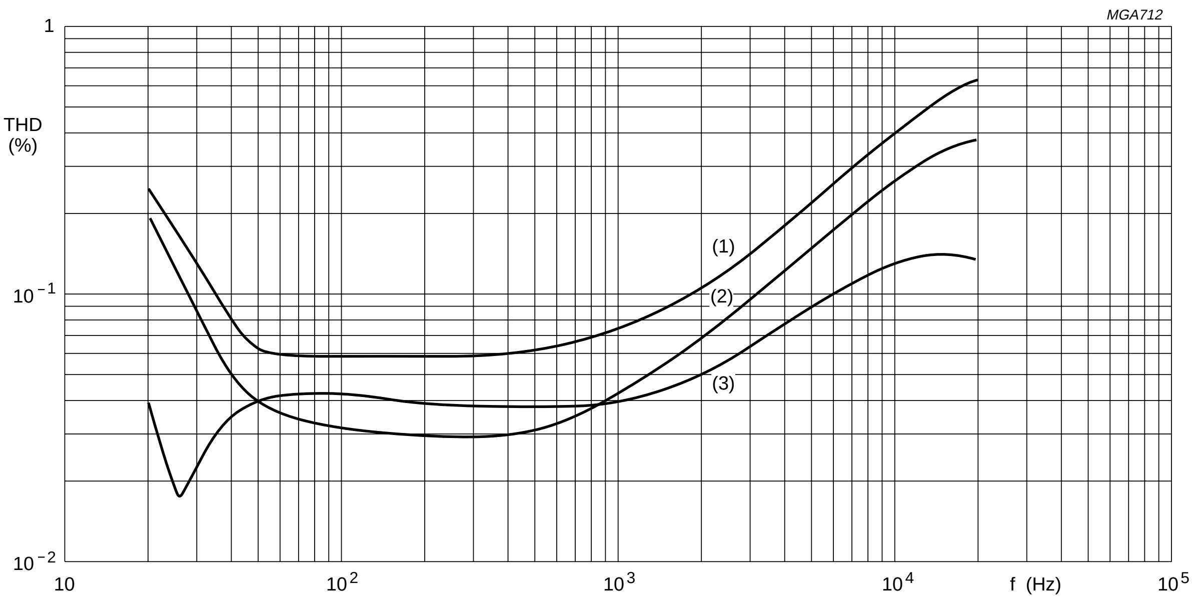
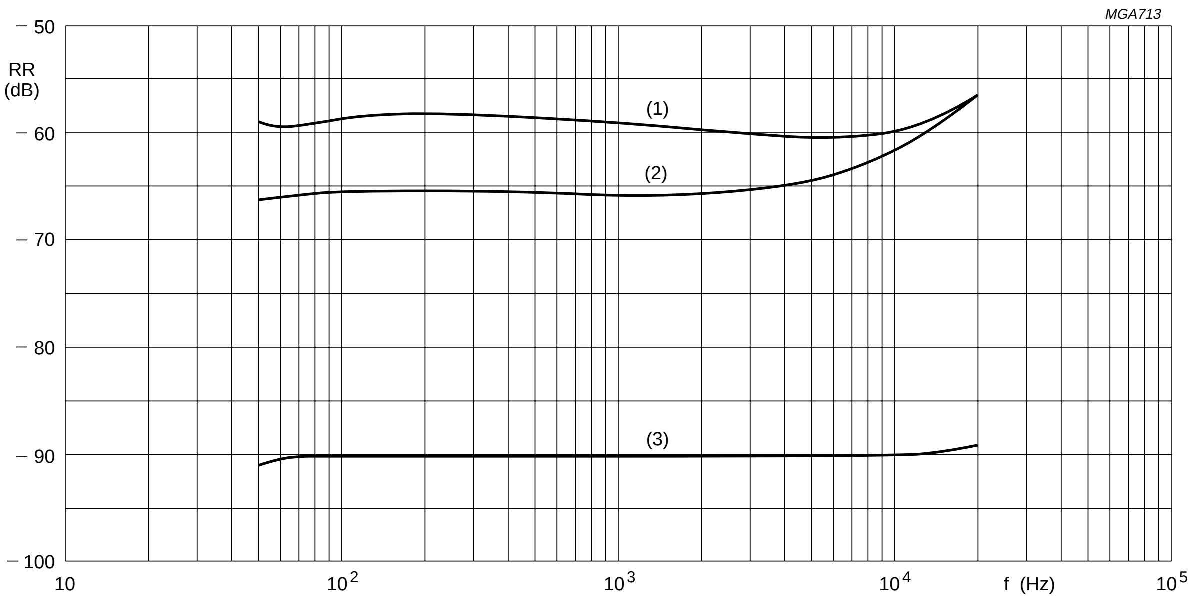


Fig.14 Power bandwidth as a function of frequency; THD = 0.5%, V_P = 14.4 V, R_L = 4 Ω.



(1) P_o = 0.1 W.
(2) P_o = 1 W.
(3) P_o = 10 W.

Fig.15 Total harmonic distortion as a function of frequency; V_P = 14.4 V, R_L = 4 Ω.



(1) On condition.
(2) Mute condition.
(3) Standby condition.

Fig.16 Ripple rejection as a function of frequency.

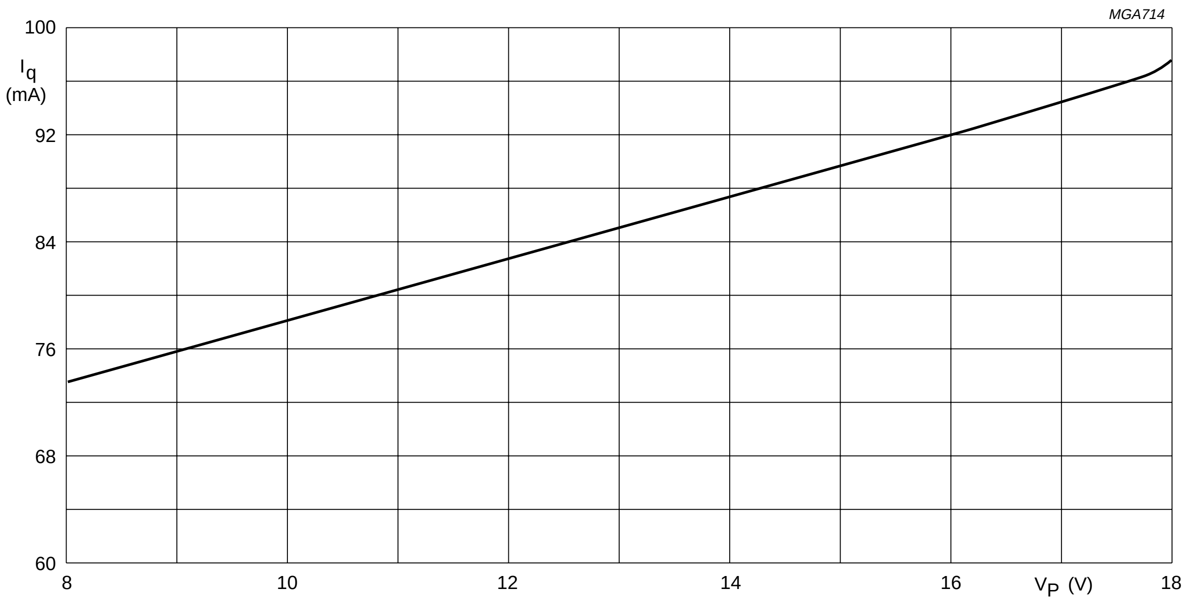
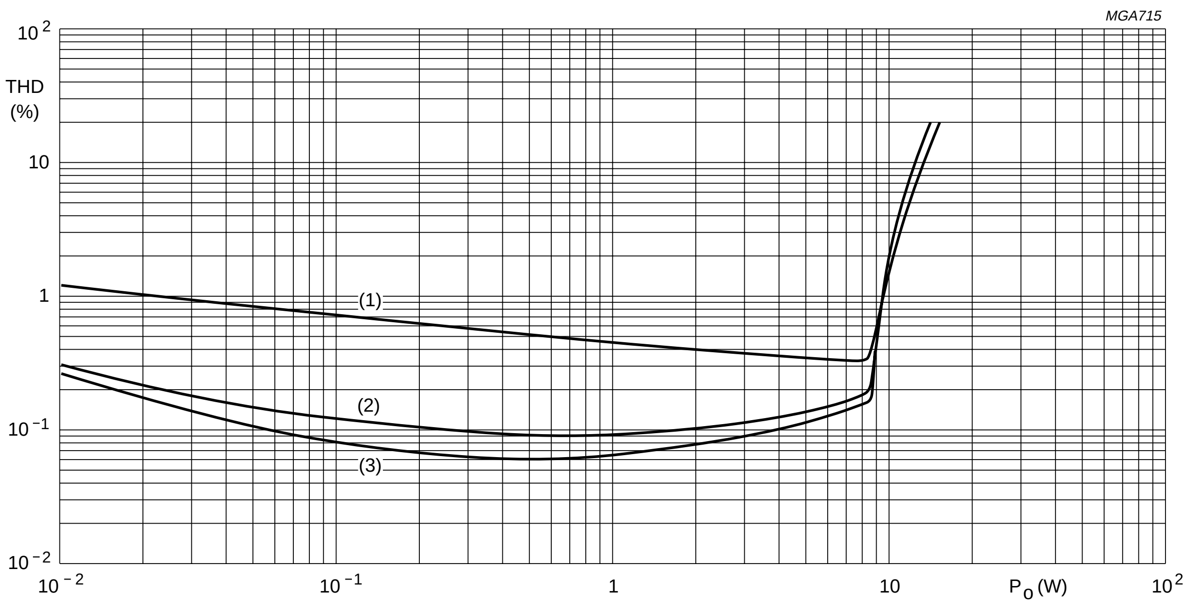


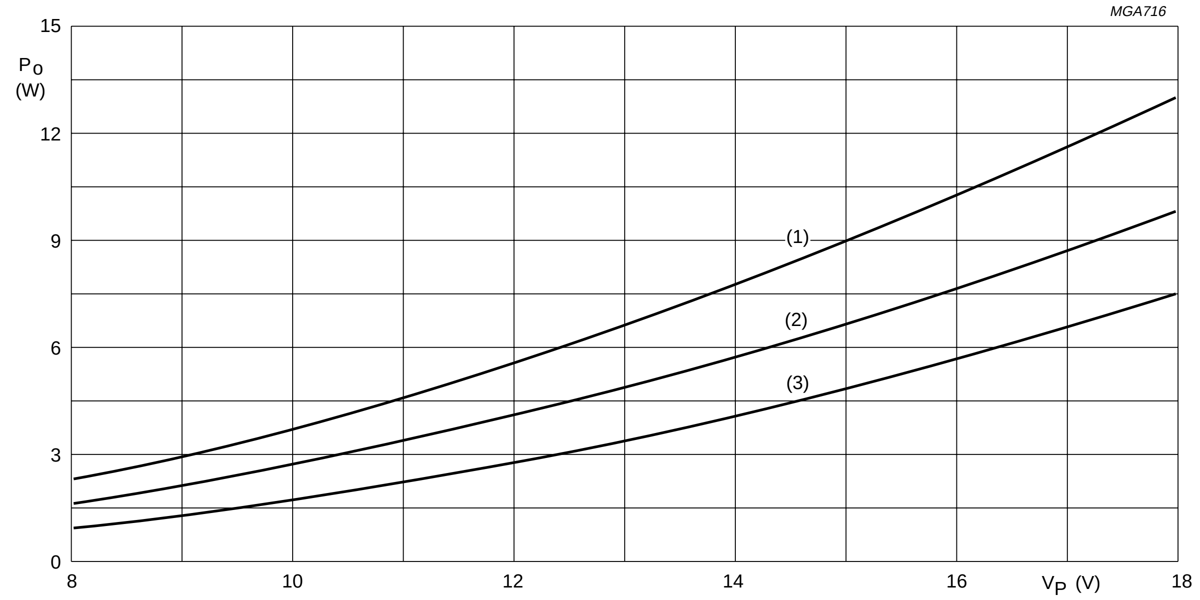
Fig.17 Quiescent current as a function of supply voltage; $R_L = \infty$.

Single-ended application



(1) f = 10 kHz (2) f = 1 kHz (3) f = 100 kHz

Fig.18 Total harmonic distortion as a function of output power; V_P = 14.4 V, R_L = 2 Ω.



(1) THD = 30%.
(2) THD = 10%.
(3) THD = 0.5%.

Fig.19 Output power as a function of supply voltage.

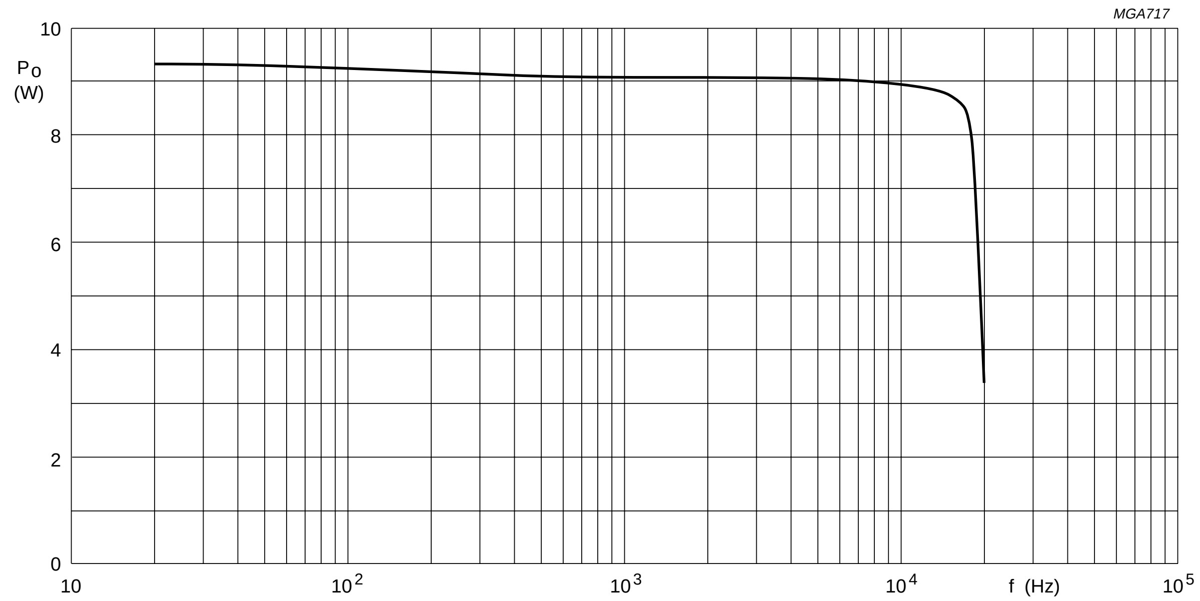
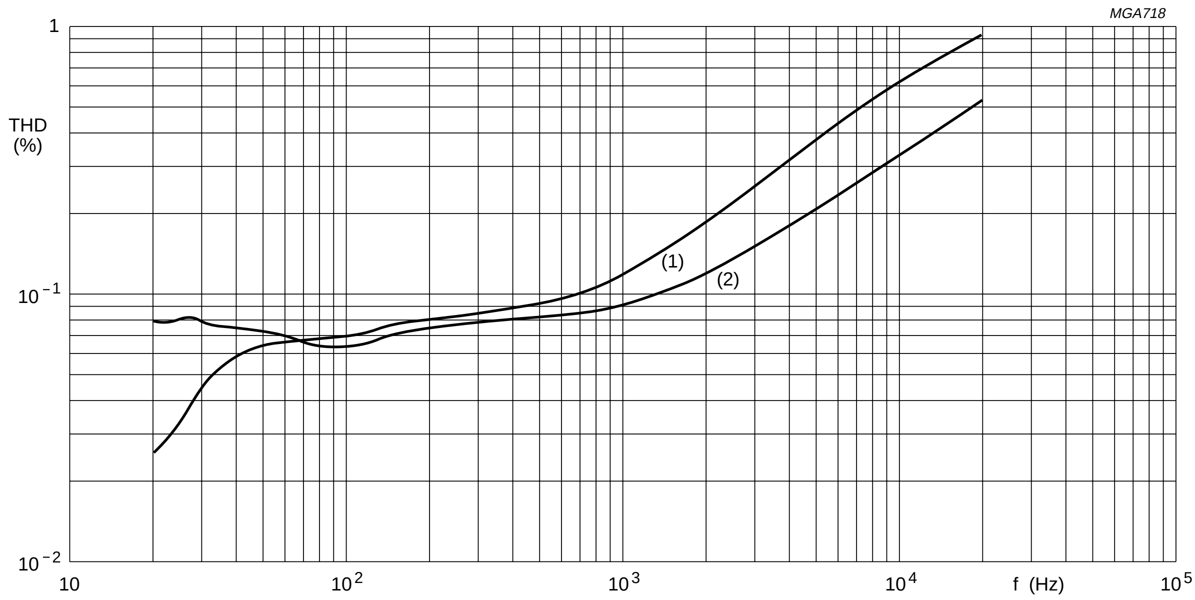


Fig.20 Power bandwidth as a function of frequency; THD = 0.5%, V_P = 14.4 V, R_L = 2 Ω.



(1) P_o = 0.1 W.
(2) P_o = 1 W.

Fig.21 Total harmonic distortion as a function of frequency; V_P = 14.4 V, R_L = 2 Ω.

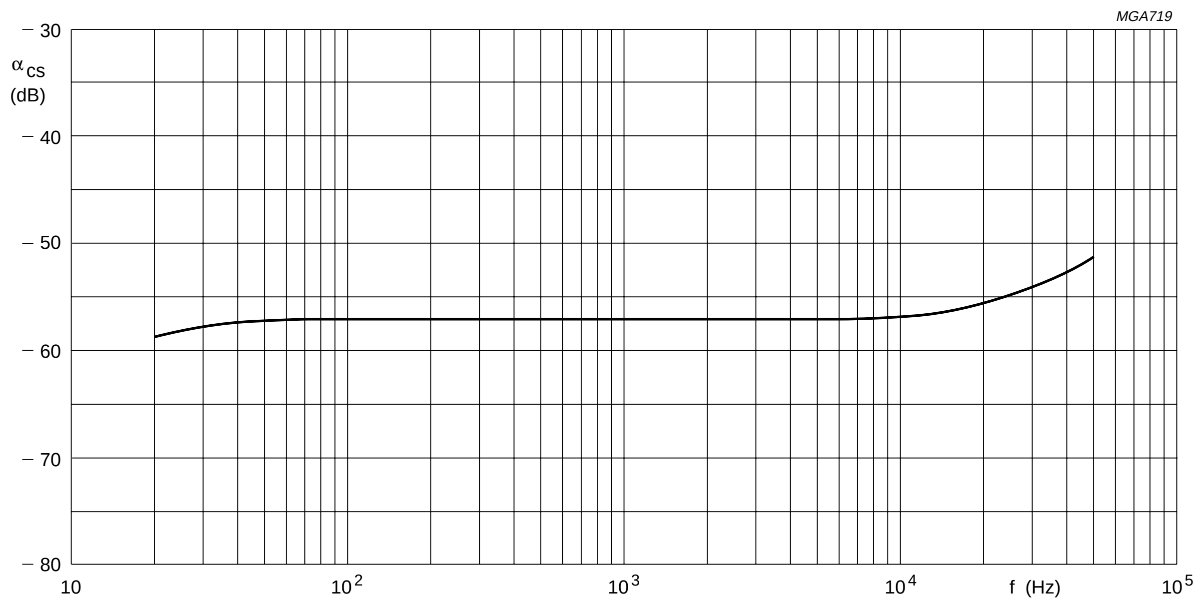


Fig.22 Channel separation as a function of frequency.

BTL Application

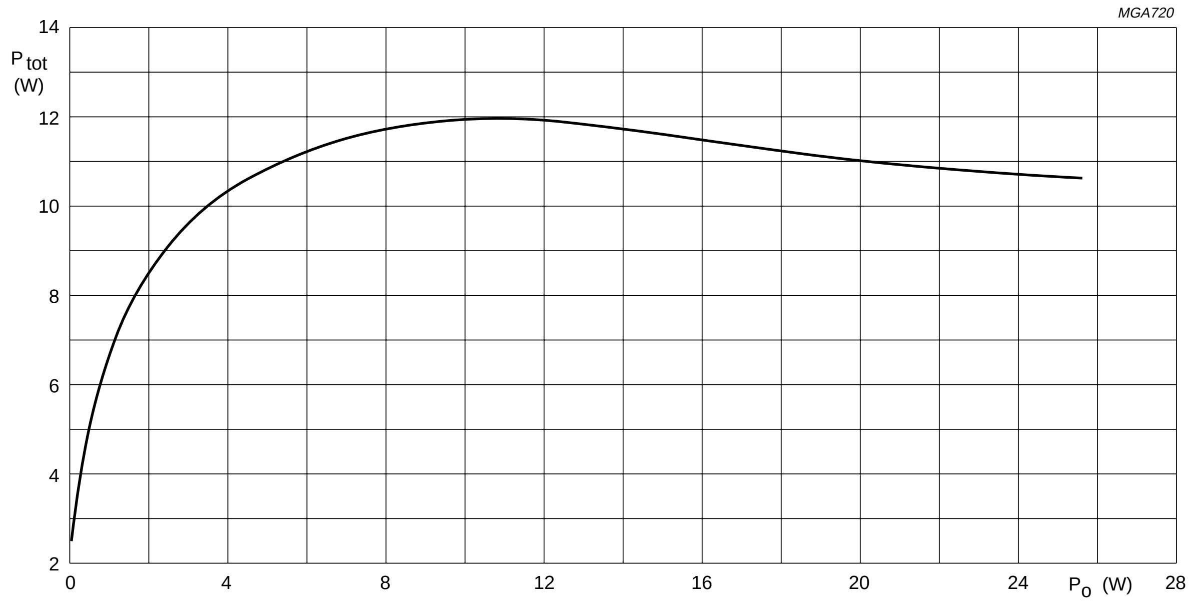
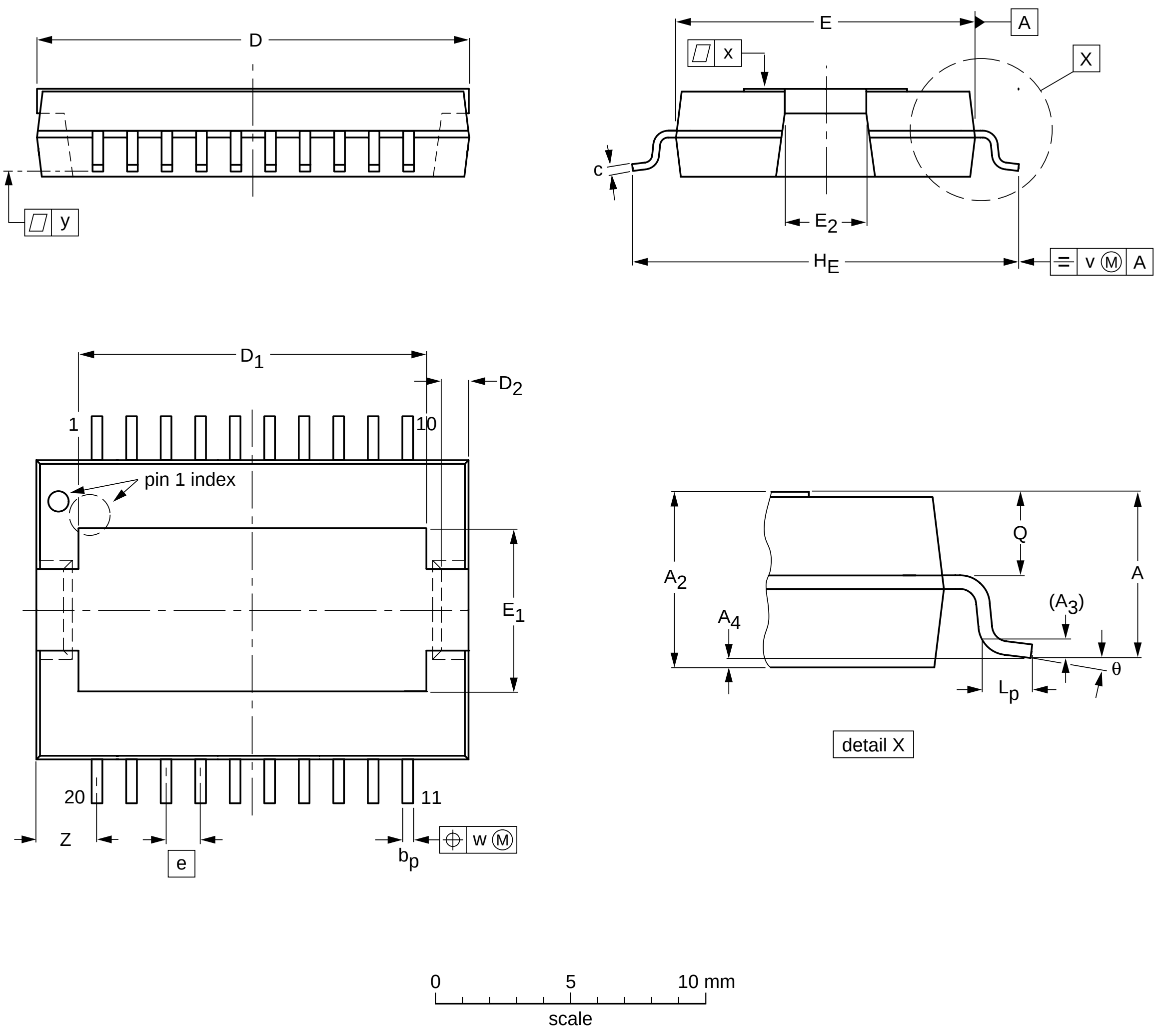


Fig.23 Total power dissipation as a function of output power; V_P = 14.4 V, R_L = 4 Ω (1 channel driven BTL or 4 channels in single-ended mode).

PACKAGE OUTLINE

HSOP20: plastic, heatsink small outline package; 20 leads; low stand-off height **SOT418-2**

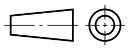


DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2	A_3	A_4(1)	b_p	c	D(2)	D_1	D_2	E(2)	E_1	E_2	e	H_E	L_p	Q	v	w	x	y	Z	θ
mm	3.5	3.5 3.2	0.35	+0.12 −0.02	0.53 0.40	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	1.27	14.5 13.9	1.1 0.8	1.7 1.5	0.25	0.25	0.03	0.07	2.5 2.0	8° 0°

Notes

1. Limits per individual lead.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT418-2						~~98-02-25~~ 99-11-12

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 3 Figtree Drive, HOMEBUSH, NSW 2140,
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),
Tel. +39 039 203 6838, Fax +39 039 203 6800

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Al.Jerozolimskie 195 B, 02-222 WARSAW,
Tel. +48 22 5710 000, Fax. +48 22 5710 001

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,
Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 3341 299, Fax.+381 11 3342 553

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

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