Signetics

TDA8440
Video and Audio Switch IC

Product Specification

Linear Products

DESCRIPTION

The TDA8440 is a versatile video/audio switch, intended to be used in applications equipped with video/audio inputs.

It provides two 3-State switches for audio channels and one 3-State switch for the video channel and a video amplifier with selectable gain (times 1 or times 2).

The integrated circuit can be controlled via a bidirectional I^2C bus or it can be controlled directly by DC switching signals. Sufficient sub-addressing is provided for the I^2C bus mode.

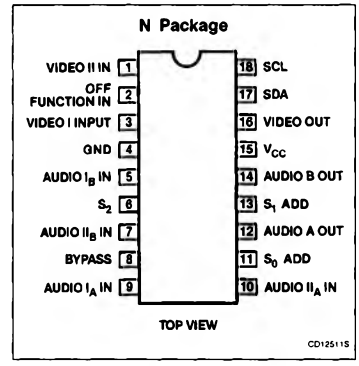
FEATURES

- **Combined analog and digital circuitry gives maximum flexibility in channel switching**
- **3-State switches for all channels**
- **Selectable gain for the video channels**
- **Sub-addressing facility**
- **I^2C bus or non-I^2C bus mode (controlled by DC voltages)**
- **Slave receiver in the I^2C bus mode**
- **External OFF command**
- **System expansion possible up to 7 devices (14 sources)**
- **Static short-circuit proof outputs**

APPLICATIONS

- **TVRO**
- **Video and audio switching**
- **Television**
- **CATV**

PIN CONFIGURATION



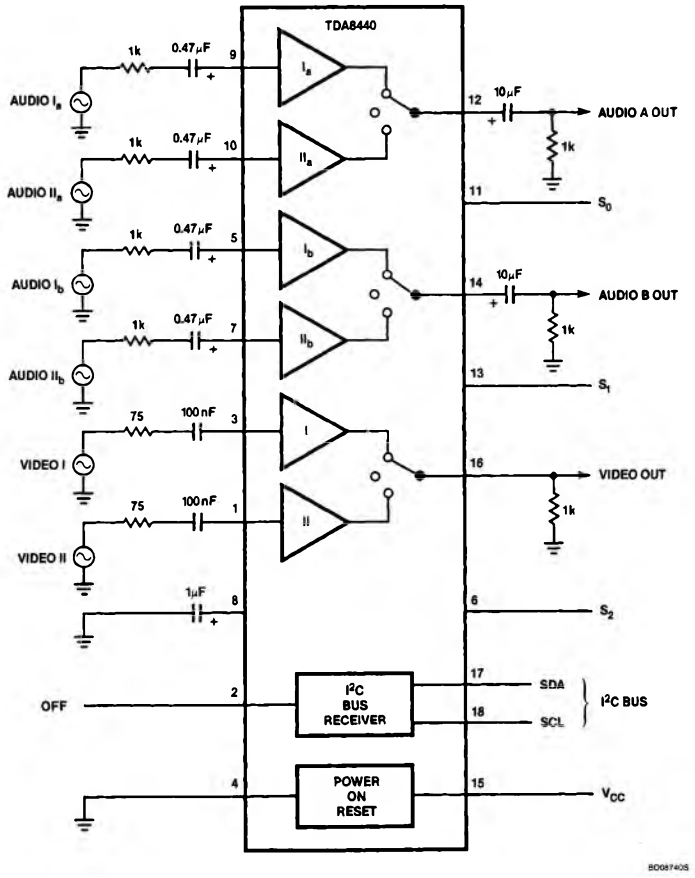
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102)	0 to 70°C	TDA8440N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage Pin 15	14	V
	Input voltage		
V_{SDA}	Pin 17	−0.3 to V_{CC} +0.3	V
V_{SCL}	Pin 18	−0.3 to V_{CC} +0.3	V
V_{OFF}	Pin 2	−0.3 to V_{CC} +0.3	V
V_{S0}	Pin 11	−0.3 to V_{CC} +0.3	V
V_{S1}	Pin 13	−0.3 to V_{CC} +0.3	V
V_{S2}	Pin 6	−0.3 to V_{CC} +0.3	V
$-I_{16}$	Video output current Pin 16	50	mA
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	0 to +70	°C
T_J	Junction temperature	+150	°C
θ_{JA}	Thermal resistance from junction to ambient in free-air	50	°C/W

BLOCK DIAGRAM AND TEST CIRCUIT



NOTE:
S0, S1, S2, and OFF (Pins 11, 13, 6, and 2) connected to V_{CC} or GND. If more than 1 device is used, the outputs and Pin 8 (bias decoupling of the audio inputs) may be connected in parallel.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = 12V$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
V_{15-4}	Supply voltage	10		13.2	V
I_{15}	Supply current (without load)		37	50	mA
Video switch					
C_1C_3	Input coupling capacitor	100			nF
A_{3-16} A_{3-16}	Voltage gain (times 1; SCL = L) (times 2; SCL = H)	−1 +5	0 +6	+1 +7	dB dB
A_{1-16} A_{1-16}	Voltage gain (times 1; SCL = L) (times 2; SCL = H)	−1 +5	0 +6	+1 +7	dB dB
V_{3-4}	Input video signal amplitude (gain times 1)			4.5	V
V_{1-4}	Input video signal amplitude (gain times 1)			4.5	V
Z_{16-4}	Output impedance		7		Ω
Z_{16-4}	Output impedance in 'OFF' state	100			kΩ
	Isolation (off-state) (f_O = 5MHz)	60			dB
S/S + N	Signal-to-noise ratio[2]	60			dB
V_{16-4}	Output top-sync level	2.4	2.8	3.2	V
G	Differential gain			3	%
V_{16-4}	Minimum crosstalk attenuation[1]	60			dB
RR	Supply voltage rejection[3]	36			dB
BW	Bandwidth (1dB)	10			MHz
α	Crosstalk attenuation for interference caused by bus signals (source impedance 75Ω)	60			db
Audio switch "A" and "B"					
V_{9-4} (RMS) V_{10-4} (RMS) V_{5-4} (RMS) V_{7-4} (RMS)	Input signal level			2 2 2 2	V V V V
Z_{9-4} Z_{10-4} Z_{5-4} Z_{7-4}	Input impedance	50 50 50 50	100 100 100 100		kΩ kΩ kΩ kΩ
Z_{12-4} Z_{14-4}	Output impedance			10 10	Ω Ω
Z_{14-4}	Output impedance (off-state)	100			kΩ
V_{9-12} V_{10-12} V_{5-14} V_{7-14}	Voltage gain	−1 −1 −1 −1	0 0 0 0	+1 +1 +1 +1	dB dB dB dB
	Isolation (off-state) (f = 20kHz)	90			dB
S/S + N	Signal-to-noise ratio[4]	90			dB
THD	Total harmonic distortion[6]			0.1	%

DC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$; $V_{CC} = 12V$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	Crosstalk attenuation for interferences caused by video signals[5]				
α	Weighted	80			dB
α	Unweighted	80			dB
α	Crosstalk attenuation for interferences caused by sinusoidal sound signals[5]	80			dB
	Crosstalk attenuation for interferences caused by the bus signal (weighted) (source impedance = 1kΩ)	80			dB
RR	Supply voltage rejection	50			dB
BW	Bandwidth (−1dB)	50			kHz
I²C bus inputs/outputs SDA (Pin 17) and SCL (Pin 18)					
V_{IH}	Input voltage HIGH	3		V_{CC}	V
V_{IL}	Input voltage LOW	−0.3		+1.5	V
I_{IH}	Input current HIGH[7]			10	μA
I_{IL}	Input current LOW[7]			10	μA
V_{OL}	Output voltage LOW at I_{OL} = 3mA			0.4	V
I_{OL}	Maximum output sink current		5		mA
C_I	Capacitance of SDA and SCL inputs, Pins 17 and 18			10	pF
Sub-address inputs S_0 (Pin 11), S_1 (Pin 13), S_2 (Pin 6)					
V_{IH}	Input voltage HIGH	3		V_{CC}	V
V_{IL}	Input voltage LOW	−0.3		+0.4	V
I_{IH}	Input current HIGH			10	μA
I_{IL}	Input current LOW	−50		0	μA
OFF input (Pin 2)					
V_{IH}	Input voltage HIGH	+3		V_{CC}	V
V_{IL}	Input voltage LOW	−0.3		+0.4	V
I_{IH}	Input current HIGH			20	μA
I_{IL}	Input current LOW	−10		2	μA

NOTES:

1. Caused by drive on any other input at maximum level, measured in B = 5MHz, source impedance for the used input 75Ω,
   crosstalk = $20\log \frac{V_{OUT}}{V_{IN}\ max}$.
2. S/N = $20\log \frac{V_O\ \text{video noise}_{(P-P)}\ (2V)}{V_O\ \text{noise}_{RMS}\ B = 5MHz}$.
3. Supply voltage ripple rejection = $20\log \frac{V_R\ \text{supply}}{V_R\ \text{on output}}$ at f = max. 100kHz.
4. S/N = $20\log \frac{V_O\ \text{nominal (0.5V)}}{V_O\ \text{noise}\ B = 20kHz}$.
5. Caused by drive of any other input at maximum level, measured in B = 20kHz, source impedance of the used input = 1kΩ,
   crosstalk = $20\log \frac{V_{OUT}}{V_{IN}\ max}$ according to DIN 45405 (CCIR 468).
6. f = 20Hz to 20kHz.
7. Also if the supply is switched off.

AC ELECTRICAL CHARACTERISTICS I^2C bus load conditions are as follows: 4kΩ pull-up resistor to +5V; 200pF to GND. All values are referred to V_{IH} = 3V and V_{IL} = 1.5V.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
t_{BUF}	Bus free before start	4			μs
$t_{S\ (STA)}$	Start condition setup time	4			μs
$t_{H\ (STA)}$	Start condition hold time	4			μs
t_{LOW}	SCL, SDA LOW period	4			μs
t_{HIGH}	SCL, HIGH period	4			μs
t_R	SCL, SDA rise time			1	μs
t_F	SCL, SDA fall time			0.3	μs
$t_{S\ (DAT)}$	Data setup time (write)	1			μs
$t_{H\ (DAT)}$	Data hold time (write)	1			μs
$t_{S\ (CAC)}$	Acknowledge (from TDA8440) setup time			2	μs
$t_{H\ (CAC)}$	Acknowledge (from TDA8440) hold time	0			μs
$t_{S\ (STO)}$	Stop condition setup time	4			μs

Table 1. Sub-Addressing

S_2	S_1	S_0	SUB-ADDRESS		
			A_2	A_1	A_0
L	L	L	0	0	0
L	L	H	0	0	1
L	H	L	0	1	0
L	H	H	0	1	1
H	L	L	1	0	0
H	L	H	1	0	1
H	H	L	1	1	0
H	H	H	non I^2C addressable		

FUNCTIONAL DESCRIPTION

The TDA8440 is a monolithic system of switches and can be used in CTV receivers equipped with an auxiliary video/audio plug. The IC incorporates 3-State switches which comprise:

a) An electronic video switch with selectable gain (times 1 or times 2) for switching between an internal video signal (from the IF amplifier) with an auxiliary input signal.

b) Two electronic audio switches, for two sound channels (stereo or dual language), for switching between internal audio sources and signals from the auxiliary video/audio plug.

A selection can be made between two input signals and an OFF-state. The OFF-state is necessary if more than one TDA8440 device is used.

The SDA and SCL pins can be connected to the I^2C bus or to DC switching voltages. Inputs S_0 (Pin 11), S_1 (Pin 13), and S_2 (Pin 6) are used for selection of sub-addresses or switching to the non-I^2C mode. Inputs S_0, S_1, and S_2 can be connected to the supply voltage (H) or to ground (L). In this way, no peripheral components are required for selection.

NON-I^2C BUS CONTROL

If the TDA8440 switching device has to be operated via the auxiliary video/audio plug, inputs S_2, S_1, and S_0 must be connected to the supply line (12V).

The sources (internal and external) and the gain of the video amplifier can be selected via the SDA and SCL pins with the switching voltage from the auxiliary video/audio plug:

- Sources I are selected if SDA = 12V (external source)
- Sources II are selected if SDA = 0V (TV mode)
- Video amplifier gain is 2 × if SCL = 12V (external source)
- Video amplifier gain is 1 × if SCL = 0V (TV mode)

If more than one TDA8440 device is used in the non-I^2C bus system, the OFF pin can be used to switch off the desired devices. This can be done via the 12V switching voltage on the plug.

- All switches are in the OFF position if OFF = H (12V)
- All switches are in the selected position via SDA and SCL pins if OFF = L (0V)

I^2C BUS CONTROL

Detailed information on the I^2C bus is available on request.

Table 2. TDA8440 I²C Bus Protocol

STA	A_6	A_5	A_4	A_3	A_2	A_1	A_0	R/W	AC	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	AC	STO

STA = start condition
A_6 = 1
A_5 = 0
A_4 = 0
A_3 = 1
Fixed address bits
A_2 = sub-address bit, fixed via S_2 input
A_1 = sub-address bit, fixed via S_1 input
A_0 = sub-address bit, fixed via S_0 input
R/W = read/write bit (has to be 0, only write mode allowed)
AC = acknowledge bit (= 0) generated by the TDA8440
D_7 = 1 audio I_a is selected to audio output a
D_7 = 0 audio I_a is not selected
D_6 = 1 audio II_a is selected to audio output a
D_6 = 0 audio II_a is not selected
D_5 = 1 audio I_b is selected to audio output b
D_5 = 0 audio I_b output is not selected
D_4 = 1 audio II_b is selected to audio output b
D_4 = 0 audio II_b is not selected
D_3 = 1 video I is selected to video output
D_3 = 0 video I is not selected
D_2 = 1 video II is selected to video output
D_2 = 0 video II is not selected
D_1 = 1 video amplifier gain is times 2
D_1 = 0 video amplifier gain is times 1
D_0 = 1 OFF-input inactive
D_0 = 0 OFF-input active
STO = stop condition

D_0/OFF Gating

D_0	OFF Input	Outputs
0 (off input active)	H	OFF
0	L	In accordance with last defined $D_7 - D_1$ (may be entered while OFF = HIGH)
1 (off input inactive)	H	In accordance with $D_7 - D_1$
1	L	In accordance with $D_7 - D_1$

OFF FUNCTION

With the OFF input all outputs can be switched off (high ohmic mode), depending on the value of D_0.

Power-on Reset

The circuit is provided with a power-on reset function.

When the power supply is switched on, an internal pulse will be generated that will reset the internal memory S_0. In the initial state all the switches will be in the off position and the OFF input is active ($D_7 - D_0 = 0$), (I^2C mode). In the non-I^2C mode, positions are defined via SDA and SCL input voltages.

When the power supply decreases below 5V, a pulse will be generated and the internal memory will be reset. The behavior of the switches will be the same as described above.

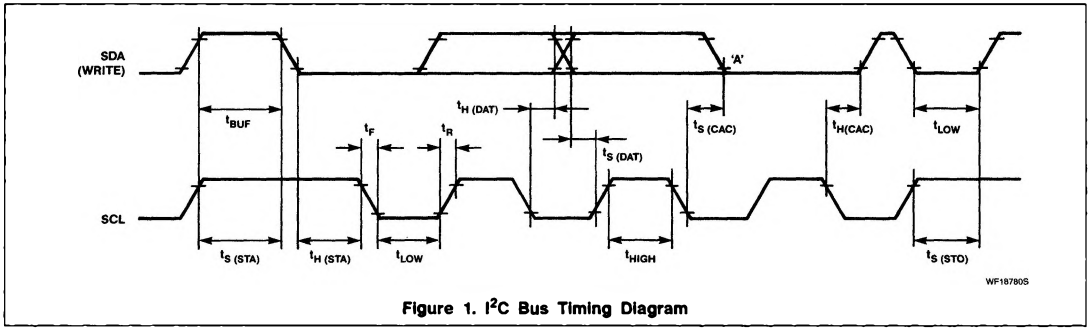


Figure 1. I²C Bus Timing Diagram