Signetics

TDA8400

FLL Tuning Circuit With Prescaler

Product Specification

Linear Products

DESCRIPTION

The TDA8400 provides closed-loop digital tuning of TV receivers, with or without AFC, as required. It comprises a 1.1GHz prescaler, with the divide-by-64 ratio, which drives a tuning interface providing a tuning voltage of 33V (maximum) via an external output transistor. The TDA8400 can also drive external PNP transistors to provide 4 high-current outputs for tuner band selection.

The IC can be used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bi-directional I^2C bus.

FEATURES

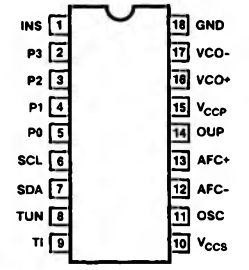
- **Combined analog and digital circuitry minimizes the number of additional interfacing components required**
- **Frequency measurement with resolution of 50kHz**
- **On-chip prescaler**
- **Tuning voltage amplifier**
- **4 high-current outputs for direct band selection**
- **Tuning with control of speed**
- **Tuning with or without AFC**
- **Single-pin, 4MHz, on-chip oscillator**
- **I^2C bus slave transceiver**

APPLICATIONS

- **TV receivers**
- **Satellite receivers**
- **CATV converters**

PIN CONFIGURATION

N Package



TOP VIEW

CD11980S

PIN NO.	SYMBOL	DESCRIPTION
1	INS	Input synthesizer (test)[1]
2	P3	High-current band-selection output ports
3	P2	
4	P1	
5	P0	
6	SCL	Serial clock line (I^2C bus)
7	SDA	Serial data line (I^2C bus)
8	TUN	Tuning voltage amplifier output
9	TI	Tuning voltage amplifier inverting input
10	V_{CCS}	+5V supply voltage (synthesizer)
11	OSC	Crystal oscillator input
12	AFC–	AFC amplifier inputs
13	AFC+	
14	OUP	Output from prescaler (test)
15	V_{CCP}	+5V supply voltage (prescaler)[2]
16	VCO+	Inputs to prescaler
17	VCO–	
18	GND	Ground

NOTES:
1. Connected to ground for application.
2. Left open-circuit for application.

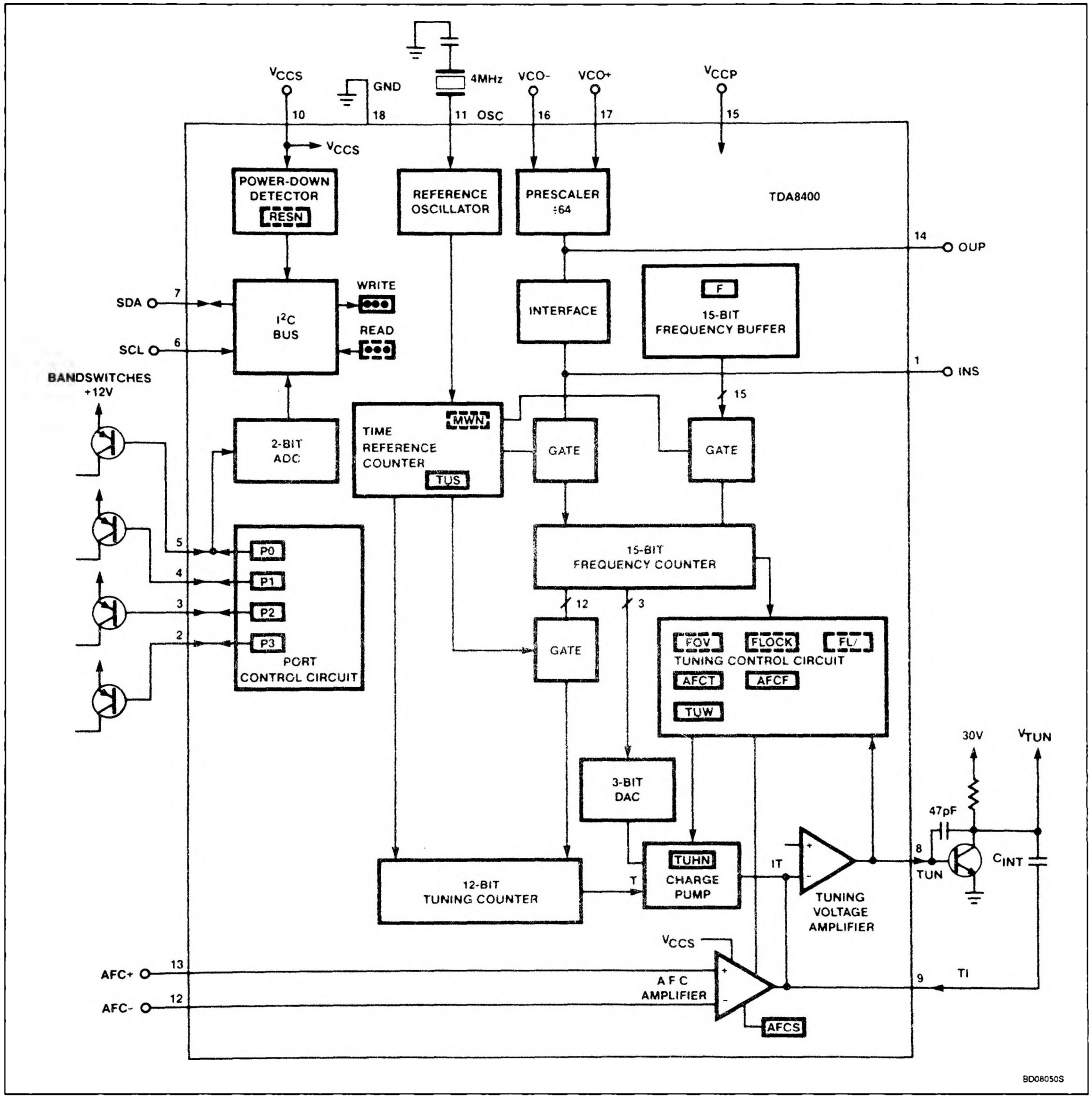
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin DIP (SOT – 102 HE, KE)	0 to 70°C	TDA8400N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Supply voltage:		
V_{CCS}	(Pin 10)	6	V
V_{CCP}	(Pin 15)	6	V
V_N	Input/output voltage (each pin)	6	V
P_{TOT}	Total power dissipation	350	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−10 to +80	°C

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; V_{CCS}, V_{CCP} at typical voltages, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	Supply voltage				
V_{CCS}	Synthesizer (Pin 10)	4.5	5	5.5	V
V_{CCP}	Prescaler (Pin 15)	4.5	5	5.5	V
	Supply current				
I_{CCS}	Synthesizer (Pin 10)		12		mA
I_{CCP}	Prescaler (Pin 15)		43		mA
P_{TOT}	Total power dissipation		275		mW
T_A	Operating ambient temperature range	0		+70	°C
T_{STG}	Operating storage temperature range	−10		+85	°C
I^2C bus inputs/outputs Inputs: SDA (Pin 7); SCL (Pin 6)					
V_{IH}	Input voltage HIGH	3.1		5.5	V
V_{IL}	Input voltage LOW	−0.3		1.6	V
I_{IH}	Input current HIGH			10	μA
I_{IL}	Input current LOW			10	μA
	SDA output (Pin 7, open-collector)				
V_{OL}	Output voltage LOW at I_{OL} = 3mA			0.4	V
I_{OL}	Output sink current			5	mA
Tuning voltage amplifier Input TI, output TUN (Pins 9, 8)					
I_{TI}	Input bias current	−5		+5	nA
$-I_{TUNL}$	Output current LOW at V_{TUN} = 0.4V	20			μA
	Minimum charge IT to tuning amplifier				
CH_0	TUHN = 0		5		μA·μs
CH_1	TUHN = 1		125		μA·μs
	Maximum current I into tuning amplifier				
I_{T0}	TUHN = 0		18		μA
I_{T1}	TUHN = 1		440		μA
AFC amplifier (Inputs AFC+, AFC− Pins 13, 12)					
V_{DIF}	Differential input voltage			1	V
g_1	Transconductance at AFCS = 1	5	10	15	μA/V
g_0	Transconductance at AFCS = 0	30	50	70	μA/V
V_{CM}	Common mode input voltage	2.5		$V_{CC1} - 1$	V
CMRR	Common mode rejection ratio		50		dB
PSRR	Power supply (V_{CC1}) rejection ratio		50		dB
I_I	Input current			1	μA
Main band-selection output ports P0, P1, P2, P3 (Pins 5 to 2, open-collector)					
	Output sink current				
I_{BSL1}	LOW impedance	0.8	1	1.2	mA
I_{BSH1}	HIGH impedance			10	μA

DC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$; V_{CCS}, V_{CCP} at typical voltages, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Prescaler inputs (VCO+ Pin 16; VCO– Pin 17)					
	Input differential voltage (RMS value)				
$V_{I(RMS)}$	at f = 70MHz	17.5		200	mV
$V_{I(RMS)}$	at f = 150MHz	10		200	mV
$V_{I(RMS)}$	at f = 300MHz	10		200	mV
$V_{I(RMS)}$	at f = 500MHz	10		200	mV
$V_{I(RMS)}$	at f = 900MHz	10		200	mV
$V_{I(RMS)}$	at f = 1.1GHz	25		200	mV
f_I	Input frequency	0.07		1.1	GHz
OSC Input (Pin 11)					
R_{XTAL}	Crystal resistance at resonance (4MHz)			150	Ω
Power-down reset					
V_{PD}	Maximum supply voltage V_{CC1} at which power-down reset is active	3		4	V
Voltage level for valid module address					
	Voltage level P0 (Pin 5) for valid module address as a function of MA1, MA0				
	MA1 MA0				
	0 0	pin used as an output			
V_{VA01}	0 1	−0.3		0.8	V
V_{VA10}	1 0	2.4		$V_{CCS} - 1.6$	V
V_{VA11}	1 1	$V_{CCS} - 0.3$		V_{CCS}	V

FUNCTIONAL DESCRIPTION

Prescaler

The integrated prescaler has a divide-by-64 ratio with a maximum input frequency of 1.1GHz. It will oscillate in the absence of an input signal within the frequency range of 800MHz to 1.1GHz.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in the 15-bit frequency buffer. The actual tuner frequency (1.1GHz maximum) is applied to the circuit on the two complementary inputs VCO+ and VCO– which drive the integrated prescaler. The resulting frequency (FDIV) is measured over a period controlled by a time reference counter and fed via a gate to a 15-bit frequency counter where it is compared to the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50kHz within a programmable tuning window (TUW).

The system cycles over a period of 2.56ms, controlled by the time reference counter which is clocked by an on-chip 4MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier (external capacitance $C_{INT} = 0.5\mu F$) is controlled by the tuning counter, 3-bit DAC, and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (control bit TUHN = logic 1; see Table 2) the minimum charge IT at Δf = 50kHz equals $125\mu A \cdot \mu s$ (typ.).

By programming the tuning sensitivity bits (TUS; see Table 3) the charge IT can be doubled up to 6 times. From this, the maximum charge IT at Δf = 50kHz equals $2^6 \times 125\mu A \cdot \mu s$ (typ.). The maximum tuning current I is 440μA, while T is limited to the duration of the tuning cycle (2.56ms).

In the tuning-hold mode (TUHN = logic 0) the tuning current I is reduced, and, as a consequence, the charge into the tuning amplifier is also reduced. An in-lock situation can be detected by reading FLOCK. The TDA8400 can be programmed to tune in the digital mode or the AFC mode by setting AFCF. In the digital mode (AFCF = logic 0), the tuning window is programmable through the TUW flag. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1.

In the AFC mode, FLOCK will remain at logic 1 provided the tuner frequency is within a ± 800kHz hold range. Switching from digital mode to AFC mode is determined by the microcontroller (AFCF flag). Switching from AFC mode to digital mode can be determined by the microcontroller, but if the frequency of the tuning oscillator does not remain within the hold range, the system automatically reverts to digital tuning. Switching back to the AFC mode will then have to be effected externally again. The tuning mode can be checked by reading the AFCT flag.

The occurence of positive and negative transitions in the FLOCK signal can be read by FL/1N and FL/0N. The AFC amplifier has programmable transconductance to 2 predefined values.

Control

For tuner band selection there are four output ports, P0 to P3, which are capable of driving external PNP transistors (open collector) as current sources. Output port P0 can also be used as valid address input with an active level determined by module address bits MA0 and MA1.

Reset

The TDA8400 goes into the power-down reset mode when V_{CC1} is below 3V (typ.). In this mode all registers are set to a defined state.

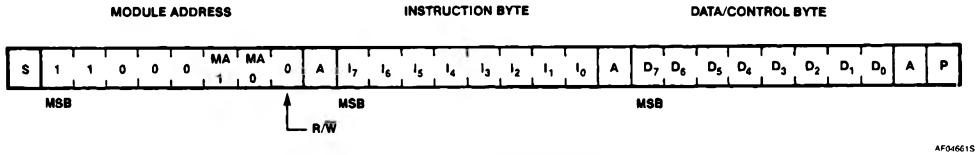


Figure 1. I²C Bus Write Format

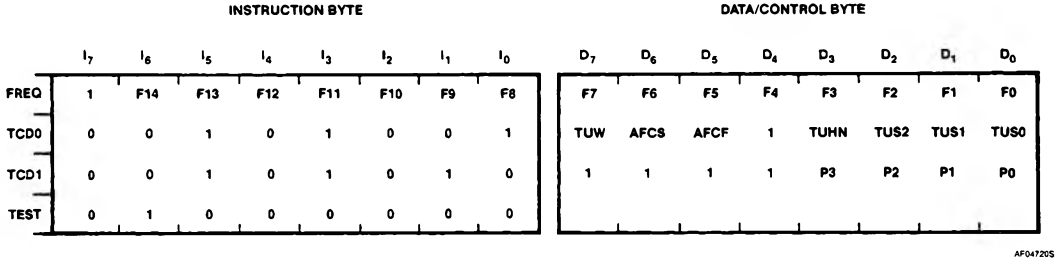


Figure 2. Tuning Control Format

OPERATION

Write

The TDA8400 is controlled via a bidirectional two-wire I²C bus; additional information on the I²C bus is available on request.

For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte, and a data/control byte are written into the device in the format shown in Figure 1.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port input P0 as shown in Table 1.

Table 1. Valid Module Addresses

P0	MA1	MA0
Don't care	0	0
GND	0	1
½ V_{CCS}	1	0
V_{CCS}	1	1

Acknowledge (A) is generated by the TDA8400 only when a valid address is received and the device is not in the power-down reset mode.

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Figure 2.

Frequency

Frequency is set when Bit I_7 of the instruction byte is set to logic 1; the remaining bits of this byte are processed as being data. Instruction bytes are fully decoded. All frequency bits are set to logic 1 and control bits to logic 0 at reset. The test instruction byte cannot be used for any other purpose.

Table 2. Tuning Current Control

TUHN	TYP. I_{MAX} (μA)	TYP. IT_{MIN} (μA/μs)
0	18[1]	5[1]
1	440	125

NOTE:
1. Values after reset.

Tuning Hold

The TUHN bit is used to decrease the maximum tuning current (I) and, as a consequence, the minimum charge IT (at Δf = 50kHz) into the tuning amplifier.

Tuning Sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at Δf = 50kHz; TUHN = logic 1.

Table 3. Minimum Charge IT as a Function of TUS

TUS2	TUS1	TUS0	TYP. IT_{MIN} (mA·μs)
0	0	0	0.125
0	0	1	0.25
0	1	0	0.5
0	1	1	1
1	0	0	2
1	0	1	4
1	1	0	8

NOTE:
The minimum tuning pulse is 2μs.

Tuning Mode

AFCF determines whether the TDA8400 has to tune in the digital mode or the AFC mode as shown in Table 4.

Table 4. Selection of Tuning Mode as a Function of AFCF

AFCF	TUNING MODE
0	Digital
1	AFC

If the tuner oscillator frequency comes out of the hold range when in the AFC mode, the device will automatically switch to digital tuning and AFCF is reset to logic 0.

Tuning Window

In the digital tuning mode TUW determines the tuning window (see Table 5) and the device is said to be in the "in-lock" situation.

Table 5. Tuning Window Programming

TUW	TUNING WINDOW (kHz)
0	0
1	± 200

Transconductance

The transconductance (g) of the AFC amplifier is programmed via the AFC sensitivity bit AFCS as shown in Table 6.

Table 6. Transconductance Programming

AFCS	TYP. TRANSCONDUCTANCE (μA/V)
1	10
0	50

Band Selection Control Ports (PX)

For band selection control, there are four output ports, P0 to P3, which are capable of driving external PNP transistors (open collector) as current sources. If a logic 1 is programmed on any of the PX bits P0 to P3, the PNP transistor will conduct and the relevant output goes LOW. All outputs are HIGH after reset.

Read

Information is read from the TDA8400 when the R/$\overline{W}$ bit is set to logic 1. Only one information byte is sent from the device. No acknowledge is required from the master after transmitting. The format of the information byte is shown in Figure 3.

Tuning/Reset Information Bits

FLOCK — Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window (TUW) in the digital tuning mode, or within the ± 800kHz AFC hold range in the AFC mode.

FL/1N — Set to logic 0 (Active-LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.

FL/0N — Same as for FL/1N but it is set to logic 0 when FLOCK changes from 1 to 0.

FOV — Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and, when too low, FOV is at logic 0.

RESN — Set to logic 0 (active Low) by a power-down reset. It is reset to logic 1 automatically after tuning/reset information has been read.

MWN — MWN (frequency measuring window, Active-LOW) is at logic 1 for a period of 1.28ms, during which time the results of frequency measurement are processed. During the remaining time, MWN is at logic 0 and the received frequency is measured.

AFCT — AFCT (tuning mode flag) is set to logic 1 when the TDA8400 is in AFC mode and reset to logic 0 when in the digital mode.

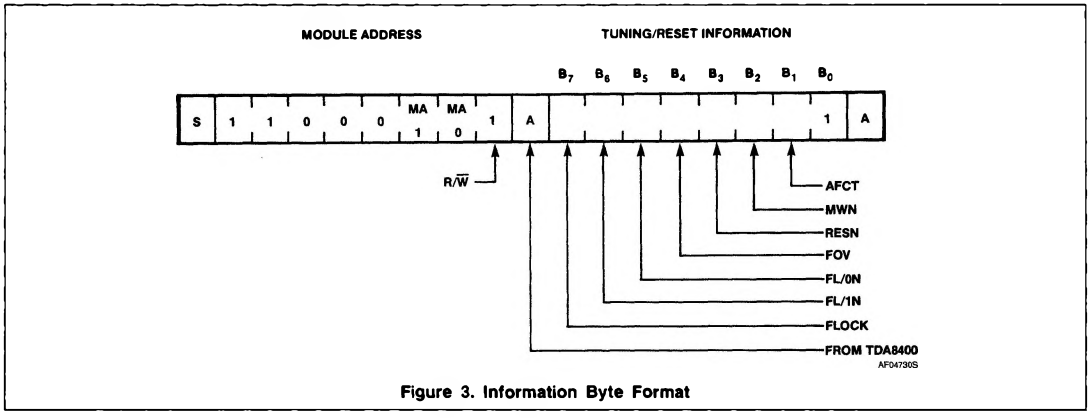


Figure 3. Information Byte Format