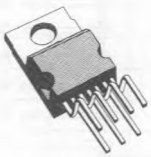
SGS-THOMSON MICROELECTRONICS

TDA8138

DEDICATED VIDEO PRODUCTS
5.1V + 12V REGULATOR WITH DISABLE AND RESET

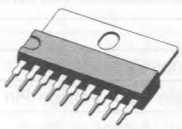
ADVANCE DATA

- OUTPUT CURRENTS UP TO 1A
- FIXED PRECISION OUTPUT 1 VOLTAGE 5.1V ± 2%
- FIXED PRECISION OUTPUT 2 VOLTAGE 12V ± 2%
- OUTPUT 1 WITH RESET FACILITY
- OUTPUT 2 WITH DISABLE BY TTL INPUT
- SHORT-CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROPOUT VOLTAGE
- AVAILABLE ALSO IN HEPTAWATT PACKAGE (but without reset facility)



HEPTAWATT

ORDER CODE : TDA8138



SIP-9

ORDER CODE : TDA8138S

DESCRIPTION

The TDA8138 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages of 5.1V and 12V at currents up to 1A.

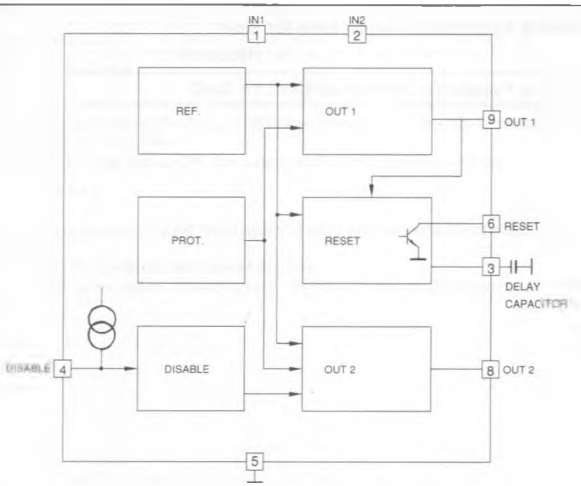
An internal reset circuit generates a delayed reset pulse when the output 1 falls below the regulated voltage value.

Output 2 can be disabled by TTL input.

Short-circuit and thermal protections are included.

BLOCK DIAGRAM

SIP-9 Package



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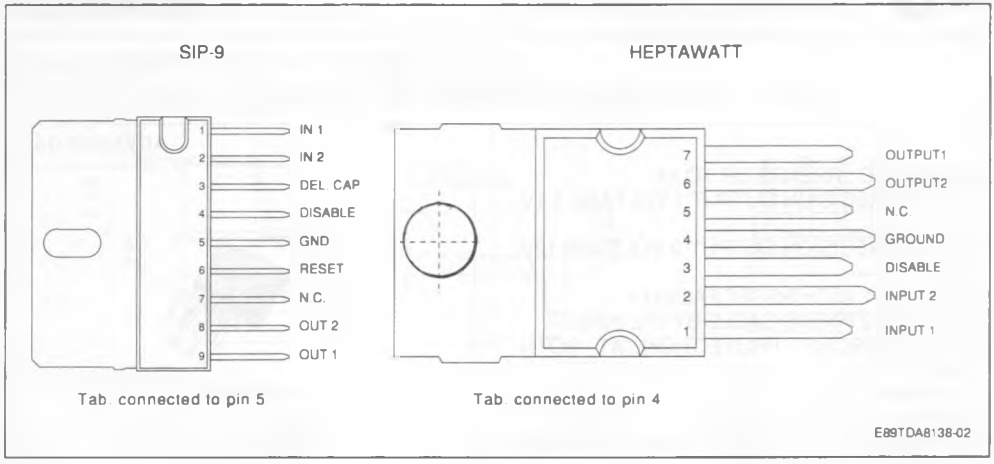
PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	DC Input Voltage Pin 1	20	V
V_{DIS}	Disable Input Voltage Pin 3 (HEPTAWATT) or Pin 4 (SIP-9)	20	V
V_{RST}	Output Voltage at Pin 6	20	V
$I_{O1,2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{STG}	Storage Temperature	– 65 to + 150	°C
T_j	Junction Temperature	0 to + 150	°C

THERMAL DATA

$R_{th(j-c)}$	Maximum Thermal Resistance Junction-case for Sip-9	8	°C/W
	for Heptawatt	3	°C/W
$R_{th(j-a)}$	Maximum Thermal Resistance Junction-ambient for Sip-9	60	°C/W

ELECTRICAL CHARACTERISTICS (V_{IN1} = 7V ; V_{IN2} = 14V ; T_j = 25°C ; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{O1}	Output Voltage	I_{O1} = 10mA	5	5.1	5.2	V
V_{O2}	Output Voltage	I_{O2} = 10mA	11.76	12	12.24	
V_{O1}	Output Voltage	7V < V_{IN1} < 14V	4.9		5.3	V
V_{O2}	Output Voltage	14 < V_{IN2} < 18 5mA < $I_{O1,2}$ < 750mA	11.5		12.5	V
$V_{IO1,2}$	Dropout Voltage	$I_{O1,2}$ = 750mA			1.4	V
		$I_{O1,2}$ = 1A			2	V
$V_{O1,2LI}$	Line Regulation	7V < V_{IN1} < 14V			50	mV
		14V < V_{IN2} < 18V			120	mV
		$I_{O1,2}$ = 200mA				
$V_{O1,2LO}$	Load Regulation	5mA < I_{O1} < 0.6A 5mA < I_{O2} < 0.6A			100 250	mV mV
I_Q	Quiescent Current	I_{O1} = 10mA Output 2 Disabled			2	mA
V_{O1RST}	Reset Threshold Voltage	(K = V_{O1})	K – 0.4	K – .25	K – 0.1	V
V_{RTH}	Reset Threshold Hysteresis	(see note 1)	20	50	75	mV
t_{RD}	Reset Pulse Delay at Pin 6	C_e = 100nF (see note 1)		25		ms
V_{RL}	Saturation Volt. at Pin 6 in Reset Condition	I_5 = 5mA			0.4	V
I_{RH}	Leakage Current at Pin 6 in Normal Condition	V_5 = 10V			10	µA
$V_{O1,2}/T$	Output Volt. Thermal Drift			100		ppm/°C
$I_{O1,2SC}$	Short Circ. Output Current	V_{IN1} = 7V V_{IN2} = 14V			1.6	A
		$V_{IN1,2}$ = 18V (see note 2)			0.7	A
V_{DISH}	Disable Volt. High (out 2 active)		2			V
V_{DISL}	Disable Volt. Low (out 2 disabled)				0.8	V
I_{DIS}	Disable Bias Current	0V < V_{DIS} < 7V	– 100		2	µA
T_{jsd}	Junction Temp. for Thermal Shut Down			145		°C

Notes : 1. If the output voltage OUT 1 goes below 4.85V (V_{OUT} - 0.25V) the comparator "a" (see fig. 1) discharges rapidly the capacitor Ce and the Reset output (pin 6) goes at once LOW.
When the voltage at the OUT 1 rises above 4.9V, the voltage at pin 3 increases with this law :

$$t_0 = \frac{Ce \cdot 2.5V}{10\mu A}$$ (see fig. 2)

as V_2 reach 2.5V the Reset output (pin 6) goes HIGH again To avoid glitches in the Reset output the second comparator "b" has a large hysteresis (1.9V).

2. The output short circuit currents are tested one channel at a time.
During a short circuit a large consumption of power occurs, anyway the thermal protection circuit guarantees the temperature not overcomes high value.

Figure 1.

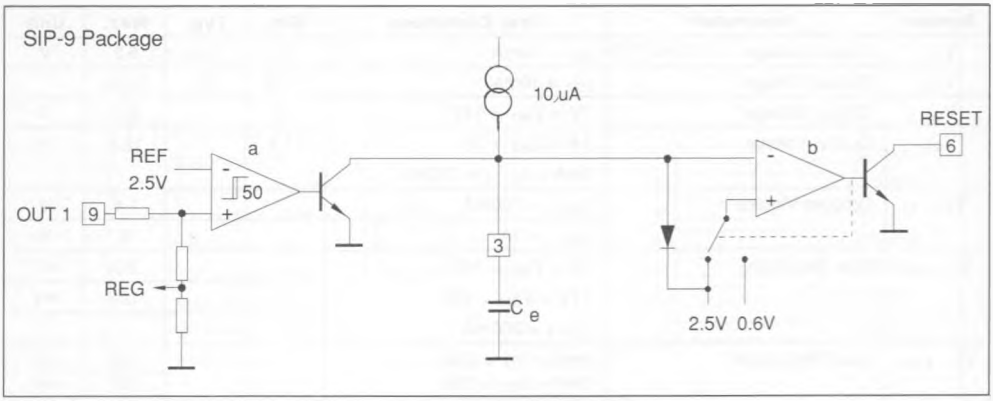
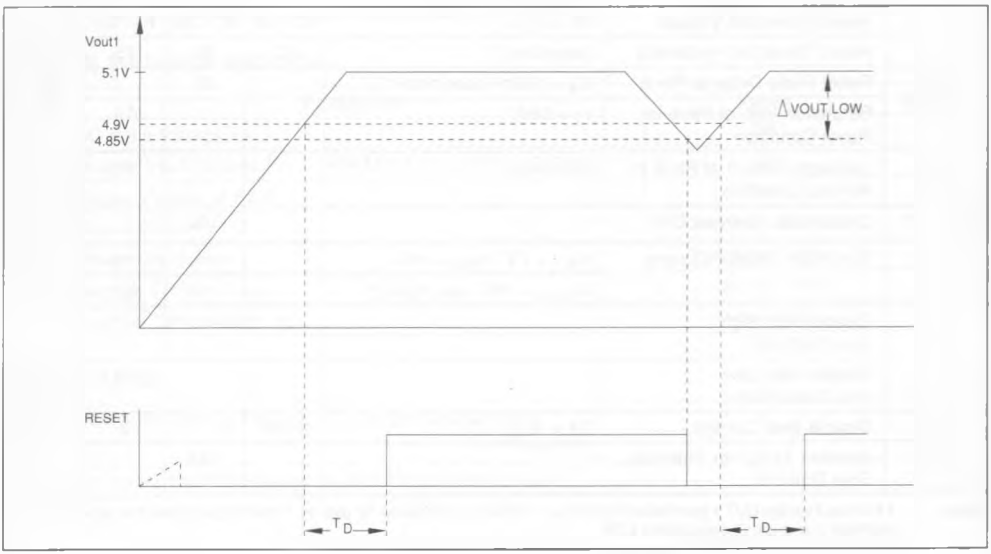


Figure 2.



CIRCUIT DESCRIPTION

The TDA8138 is a dual voltage regulator with Reset and Diasable.

The two regulation parts are supplied from one voltage reference circuit trimmed by zener zap during EWS test.

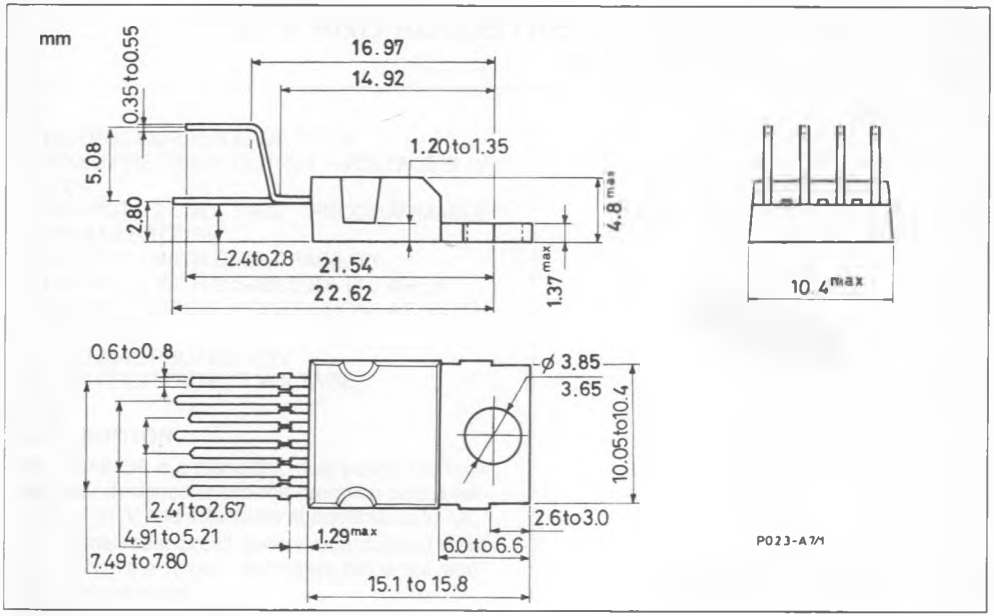
The output stages have been realized in darlington configuration with a drop typical 1.2V.

The disable circuit, switch-off the output 2 if a voltage lower than 0.8V is applied at pin 3 (HEPTAWATT) or pin 4 (SIP-9).

The Reset circuit controls the voltage at the output 1, if this one decrease below 4.85V provides to generate a reset pulse at pin 6 (open collector) with a certain delay depending by an external capacitor connected at pin 3.

PACKAGE MECHANICAL DATA

HEPTAWATT – PLASTIC PACKAGE



9 PINS – PLASTIC SIP