5.1V + 8.5V REGULATOR WITH DISABLE AND RESET

- OUTPUT CURRENTS UP TO 1A
- FIXED PRECISION OUTPUT 1 VOLTAGE 5.1V ± 2%
- FIXED PRECISION OUTPUT 2 VOLTAGE 8.5V ± 2%
- OUTPUT 1 WITH RESET FACILITY
- OUTPUT 2 WITH DISABLE BY TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUTPUT VOLTAGE

DESCRIPTION

The TDA8133 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages of 5.1V and 8.5V at currents up to 1A.

An internal reset circuit generates a delayed reset pulse when the output 1 decreases below the regulated voltage value.
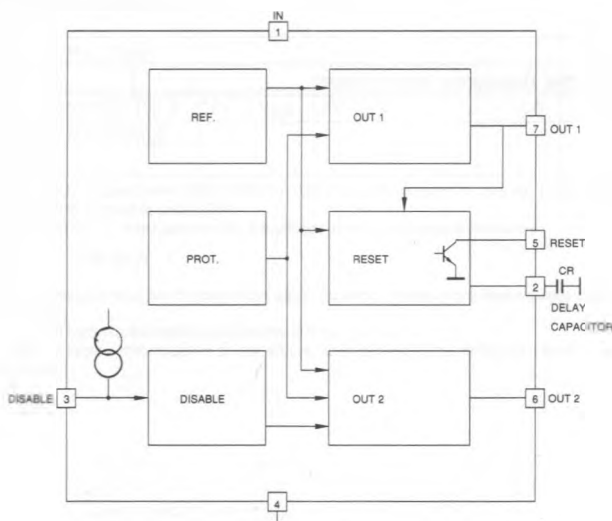
Output 2 can be disabled by TTL input.

Short circuit and thermal protections are included.
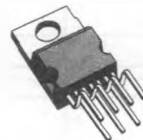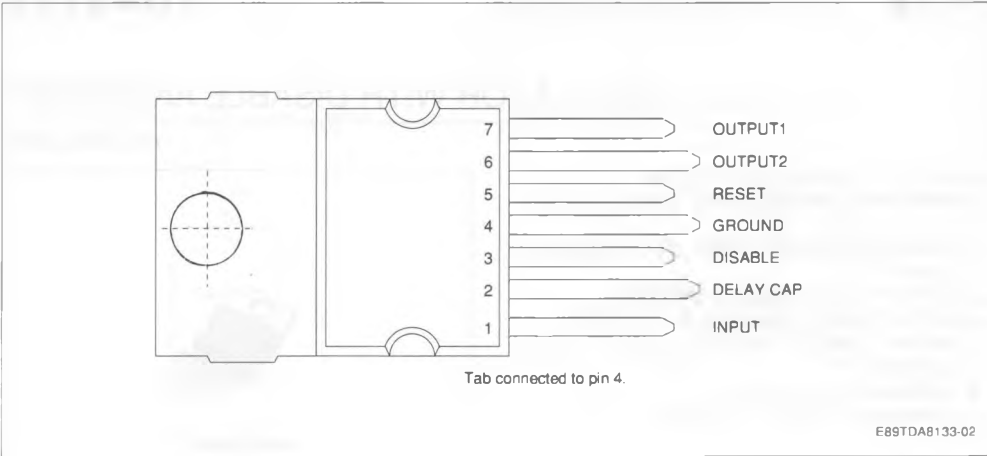
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ORDER CODE : TDA8133

BLOCK DIAGRAM

E89TDA8133-01

PIN CONNECTION (top view)

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                                    7 ──────────  OUTPUT1
                                    6 ──────────  OUTPUT2
                                    5 ──────────  RESET
                                    4 ──────────  GROUND
                                    3 ──────────  DISABLE
                                    2 ──────────  DELAY CAP
                                    1 ──────────  INPUT

                    Tab connected to pin 4.

                                                    E89TDA8133-02
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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	DC Input Voltage Pin 1	20	V
V_{DIS}	Disable Input Voltage Pin 3	20	V
V_{RST}	Output Voltage at pin 5	20	V
$I_{O1,2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{STG}	Storage Temperature	-65 to $+150$	°C
T_J	Junction Temperature	0 to $+150$	°C

THERMAL DATA

$R_{TH(j-c)}$	Maximum Thermal Resistance Junction-case	3	°C/W

ELECTRICAL CHARACTERISTICS (V_{IN} = 7V ; T_j = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{01}	Output Voltage	I_{01} = 10mA	5	5.1	5.2	V
V_{02}	Output Voltage	I_{02} = 10mA	8.33	8.5	8.67	V
V_{01}	Output Voltage	$7V < V_{IN1} < 14V$	4.9		5.3	V
V_{02}	Output Voltage	$10.5V < V_{IN2} < 18V$ $5mA < I_{01, 2} < 750mA$	8.15		8.85	V
$V_{I01, 2}$	Dropout Voltage	$I_{01, 2}$ = 750mA			1.4	V
		$I_{01, 2}$ = 1A			2	V
V_{01LI}	Line Regulation	$7V < V_{IN1} < 14V$			50	mV
V_{02LI}	Line Regulation	$10.5V < V_{IN2} < 18V$ $I_{01, 2}$ = 200mA			85	mV
V_{01LO}	Load Regulation	$5mA < I_{01, 2} < 0.6A$			100	mV
V_{01LO}	Load Regulation				170	mV
I_Q	Quiescent Current	I_{01} = 10mA Output 2 Disabled			2	mA
V_{01RST}	Reset Threshold Voltage	$(K = V_{01})$	K − 0.4	K − .25	K − 0.1	V
V_{RTH}	Reset Threshold Hysteresis	(see note 1)	20	50	75	mV
t_{RD}	Reset Pulse Delay at pin 5	C_e = 100nF (see note 1)		25		ms
V_{RL}	Saturation Volt. at pin 5 in Reset Condition	I_5 = 5mA			0.4	V
I_{RH}	Leakage Current at pin 5 in Normal Condition	V_5 = 10V			10	µA
$V_{01, 2}/T$	Output Voltage Thermal Drift			100		ppm/°C
$I_{01, 2SC}$	Short Circ. Output Current	V_{IN1} = 7V ; V_{IN2} = 10.5V			1.6	A
		$V_{IN1, 2}$ = 18V (see note 2)			0.7	A
V_{DISH}	Disable Volt. at Pin 3 High (out 2 active)		2			V
V_{DISL}	Disable Volt. at Pin 3 Low (out 2 disabled)				0.8	V
I_{DIS}	Disable bias Current at Pin 3	$0V < V_{DIS} < 7V$	− 100		2	µA
T_{jsd}	Junction Temp. for Thermal Shut Down			145		°C

Notes : 1. If the output voltage OUT 1 goes below 4.85V (VOUT − 0.25V) the comparator "a" (see fig. 1) discharges rapidly the capacitor Ce and the Reset output (pin 5) goes at once LOW.
When the voltage at the OUT 1 rises above 4.9V, the voltage at pin 2 increases with this law :

$$t_d = \frac{C_e \cdot 2.5V}{10\mu A} \quad \text{(see fig. 2)}$$

as V2 reach 2.5V the Reset output (pin 5) goes HIGH again. To avoid glitches in the Reset output the second comparator "b" has a large hysteresis (1.9V).
2. The output short circuit currents are tested one channel at time.
During a short circuit a large consumption of power occurs, anyway the thermal protection circuit guarantees the temperature not overcomes high value.
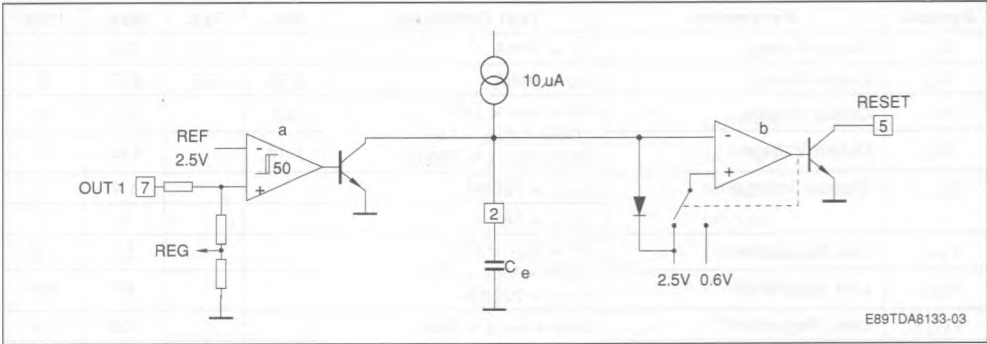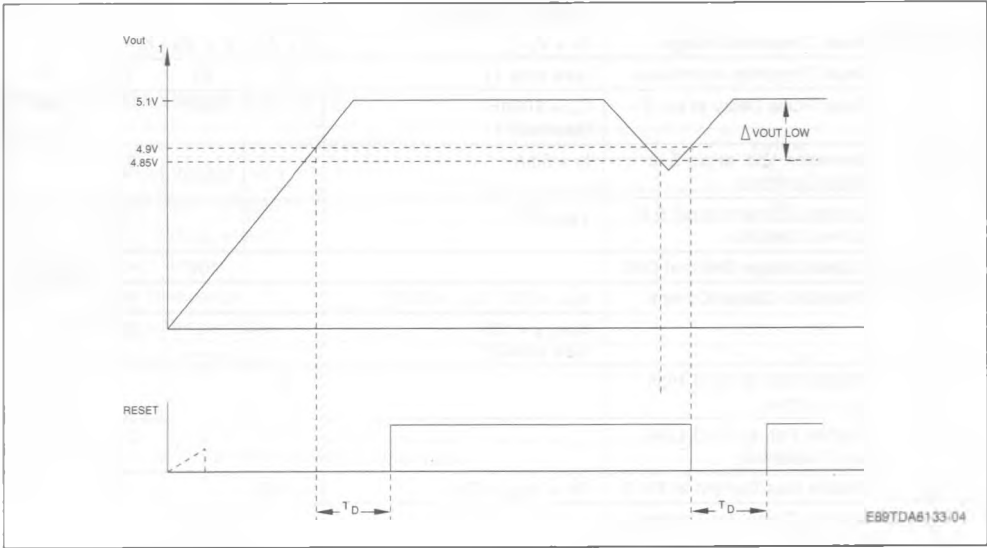
Figure 1.

Figure 2.

CIRCUIT DESCRIPTION

The TDA8133 is a dual voltage regulator with Reset and Disable.

The two regulation parts are supplied from one voltage reference circuit trimmed by zener zap during EWS test.

The outputs stage have been realized in darlington configuration with a drop typical 1.2V.

The disable circuit, switch-off the output 2 if a voltage lower than 0.8V is applied at pin 3.

The Reset circuit controls the voltage at the output 1, if this one decrease below 4.85V provides to generate a reset pulse at pin 5 (open collector) with a certain delay depending by an external capacitor connected at pin 2.

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PACKAGE MACHANICAL DATA

HEPTAWATT – PLASTIC PACKAGE

P023-A7/1