# SIEMENS

## Control IC for Switched-Mode Power Supplies using MOS-Transistor

**TDA 4605-3**

**Bipolar IC**

### Features

- Fold-back characteristics provides overload protection for external components
- Burst operation under secondary short-circuit condition implemented
- Protection against open or a short of the control loop
- Switch-off if line voltage is too low (undervoltage switch-off)
- Line voltage depending compensation of fold-back point
- Soft-start for quiet start-up without noise generated by the transformer
- Chip-over temperature protection implemented (thermal shutdown)
- On-chip ringing suppression circuit against parasitic oscillations of the transformer
- AGC-voltage reduction at low load
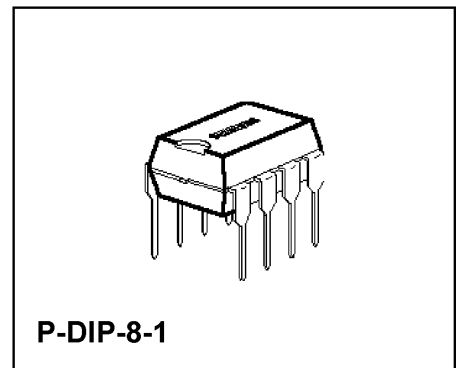
**P-DIP-8-1**

| Type | Ordering Code | Package |
|------|---------------|---------|
| TDA 4605-3 | Q67000-A5066 | P-DIP-8-1 |

The IC TDA 4605-3 controls the MOS-power transistor and performs all necessary control and protection functions in free running flyback converters. Because of the fact that a wide load range is achieved, this IC is applicable for consumer as well as industrial power supplies.

The serial circuit and primary winding of the flyback transformer are connected in series to the input voltage. During the switch-on period of the transistor, energy is stored in the transformer. During the switch-off period the energy is fed to the load via the secondary winding. By varying switch-on time of the power transistor, the IC controls each portion of energy transferred to the secondary side such that the output voltage remains nearly independent of load variations. The required control information is taken from the input voltage during the switch-on period and from a regulation winding during the switch-off period. A new cycle will start if the transformer has transferred the stored energy completely into the load.

In the different load ranges the switched-mode power supply (SMPS) behaves as follows:

### No load operation

The power supply is operating in the burst mode at typical 20 to 40 kHz. The output voltage can be a little bit higher or lower than the nominal value depending of the design of the transformer and the resistors of the control voltage divider.

### Nominal operation

The switching frequency is reduced with increasing load and decreasing AC-voltage.
The output voltage is only dependent on the load.

### Overload point

Maximal output power is available at this point of the output characteristic.

### Overload

The energy transferred per operation cycle is limited at the top. Therefore the output voltages declines by secondary overloading.

## Pin Definitions and Functions

| Pin No. | Function |
|---------|----------|
| 1 | **Information Input Concerning Secondary Voltage.** By comparing the regulating voltage - obtained trom the regulating winding of the transformer - with the internal reference voltage, the output impulse width on pin 5 is adjusted to the load of the secondary side (normal, overload, short-circuit, no load). |
| 2 | **Information Input Regarding the Primary Current.** The primary current rise in the primary winding is simulated at pin 2 as a voltage rise by means of external RC-element. When a voltage level is reached thats derived from the regulating voltage at pin 1, the output impulse at pin 5 is terminated. The RC-element serves to set the maximum power at the overload point set. |
| 3 | **Input for Primary Voltage Monitoring:** In the normal operation $V_3$ is moving between the thresholds $V_{3H}$ and $V_{3L}$ $(V_{3H} > V_3 > V_{3L})$. $V_3 < V_{3L}$: SMPS is switched OFF (line voltage too low). $V_3 > V_{3H}$ : Compensation of the overload point regulation (controlled by pin 2) starts at $V_{3H}$ : $V_{3L}$ = 1.7. |
| 4 | **Ground** |
| 5 | **Output:** Push-pull output provides $\pm$ 1 A for rapid charge and discharge of the gate capacitance of the power MOS-transistor. |
| 6 | **Supply Voltage Input:** A stable internal reference voltage $V_{REF}$ is derived from the supply voltage also the switching thresholds $V_{6A}$ , $V_{6E}$ , $V_{6\,max}$ and $V_{6\,min}$ for the supply voltage detector. If $V_6 > V_{6E}$ then $V_{REF}$ is switched on and swiched off when $V_6 < V_{6A}$ . In addition the logic is only enable for $V_{6\,min} < V_6 < V_{6\,max}$. |
| 7 | **Input for Soft-Start.** Start-up will begin with short pulses by connecting a capacitor from pin 7 to ground. |
| 8 | **Input for the Oscillation Feedback.** After starting oscillation, every zero transition of the feedback voltage (falling edge) through zero (falling edge) triggers an output pulse at pin 5. The trigger threshold is at + 50 mV typical. |
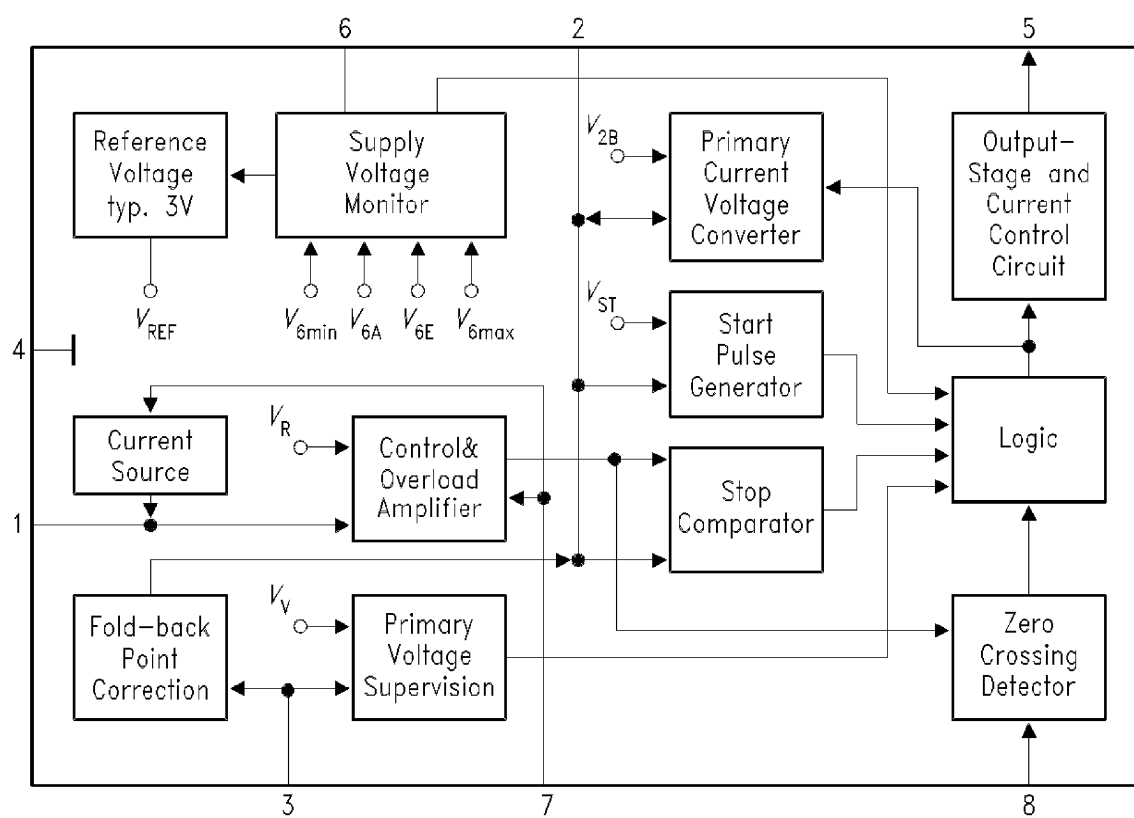
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**Block Diagram**

## Circuit Description

### Application Circuit

The application circuit shows a flyback converter for video recorders with an output power rating of 70 W. The circuit is designed as a wide-range power supply for AC-line voltages of 180 to 264 V. The AC-input voltage is rectified by the bridge rectifier GR1 and smoothed by $C_1$. The NTC limits the rush-in current.

In the period before the switch-on threshold is reached the IC is suppled via resistor $R_1$; during the start-up phase it uses the energy stored in $C_2$, under steady state conditions the IC receives its supply voltage from transformer winding $n_1$ via diode D1. The switching transistor T1 is a BUZ 90. The parallel connected capacitor $C_3$ and the inductance of primary winding $n_2$ determine the system resonance frequency. The $R_2$-$C_4$-D2 circuitry limits overshoot peaks, and $R_3$ protects the gate of T1 against static charges.

During the conductive phase of the power transistor T1 the current rise in the primary winding depends on the winding inductance and the mains voltage. The network consisting of $R_4$-$C_5$ is used to create a model of the sawtooth shaped rise of the collector current. The resulting control voltage is fed into pin 2 of the IC. The RC-time constant given by $R_4$-$C_5$ must be designed that way that driving the transistor core into saturation is avoided.

The ratio of the voltage divider $R_{10}/R_{11}$ is fixing a voltage level threshold. Below this threshold the switching power supply shall stop operation because of the low mains voltage. The control voltage present at pin 3 also determines the correction current for the fold-back point. This current added to the current flowing through $R_4$ and represents an additional charge to $C_5$ in order to reduce the turn-on phase of T1. This is done to stabilize the fold-back point even under higher mains voltages.

Regulation of the switched-mode power supplies via pin 1. The control voltage of winding $n_1$ during the off period of T1 is rectified by D3, smoothed by $C_6$ and stepped down at an adjustable ratio by $R_5$, $R_6$ and $R_7$. The $R_8$-$C_7$ network suppresses parasitic overshoots (transformer oscillation). The peak voltage at pin 2, and thus the primary peak current, is adjusted by the IC so that the voltage applied across the control winding, and hence the output voltages, are at the desired level.

When the transformer has supplied its energy to the load, the control voltage passes through zero. The IC detects the zero crossing via series resistors $R_9$ connected to pin 8. But zero crossings are also produced by transformer oscillation after T1 has turned off if output is short-circuited. Therefore the IC ignores zero crossings occurring within a specified period of time after T1 turn-off.

The capacitor $C_8$ connected to pin 7 causes the power supply to be started with shorter pulses to keep the operating frequency outside the audible range during start-up.

On the secondary side, five output voltages are produced across winding $n_3$ to $n_7$ rectified by D4 to D8 and smoothed by $C_9$ to $C_{13}$. Resistors $R_{12}$, $R_{14}$ and $R_{19}$ to $R_{21}$ are used as bleeder resistors. Fusable resistors $R_{15}$ to $R_{18}$ protect the rectifiers against short circuits in the output circuits, which are designed to supply only small loads.

**Block Diagram**

**Pin 1**

The regulating voltage forwarded to this pin is compared with a stable internal reference voltage $V_R$ in the **regulating and overload amplifier**. The output of this stage is fed to the stop comparator. If the control voltage is rather small at pin 1 an additional current is added by means of current source which is controlled according the level at pin 7. This additional current is virtually reducing the control voltage present at pin 1.

**Pin 2**

A voltage proportional to the drain current of the switching transistor is generated there by the external RC-combination in conjunction with the **primary current transducer**. The output of this transducer is controlled by the logic and referenced to the internal stable voltage $V_{2B}$. If the voltage $V_2$ exceeds the output voltage of the regulations amplifier, the logic is reset by the stop comparator and consequently the output of pin 5 is switched to low potential. Further inputs for the logic stage are the output for the **start impulse generator** with the stable reference potential $V_{ST}$ and the **supply voltage motor**.

**Pin 3**

The down divided primary voltage applied there stabilizes the overload point. In addition the logic is disabled in the event of low voltage by comparison with the internal stable voltage $V_V$ in the **primary voltage monitor** block.

**Pin 4**

Ground

**Pin 5**

In the output stage the output signals produced by the logic are shifted to a level suitable for MOS-power transistors.

**Pin 6**

From the supply voltage $V_6$ are derived a stable internal references $V_{REF}$ and the switching threshold $V_{6A}$, $V_{6E}$, $V_{6\,max}$ and $V_{6\,min}$ for the **supply voltage monitor**. All references values ($V_R$, $V_{2B}$, $V_{ST}$) are derived from $V_{REF}$. If $V_6 > V_{VE}$, the $V_{REF}$ is switched on and switched off when $V_6 < V_{6A}$. In addition, the logic is released only for $V_{6\,min} < V_6 < V_{6\,max}$.

**Pin 7**

The output of the overload amplifier is connected to pin 7. A load on this output causes a reduction in maximal impulse duration. This function can be used to implement a soft start, when pin 7 is connected to ground by a capacitor.

**Pin 8**

The zero detector controlling the logic block recognizes the transformer being discharged by positive to negative zero crossing of pin 8 voltage and enables the logic for a new pulse. Parasitic oscillations occurring at the end of a pulse cannot lead to a new pulse (double pulsing), because an internal circuit inhibits the zero detector for a finite time $t_{UL}$ after the end of each pulse.

**Start-Up Behaviour**

The start-up behaviour of the application circuit per sheet 88 is represented an sheet 90 for a line voltage barely above the lower acceptable limit time $t_0$ the following voltages built up:

- $V_6$ corresponding to the half-wave charge current over $R_1$
- $V_2$ to $V_{2\,max}$ (typically 6.6 V)
- $V_3$ to the value determined by the divider $R_{10}/R_{11}$ .

The current drawn by the IC in this case is less than 1.6 mA.

If $V_6$ reaches the threshold $V_{6E}$ (time point $t_1$), the IC switches on the internal reference voltage. The current draw max. rises to 12 mA. The primary current- voltage reproducer regulates $V_2$ down to $V_{2B}$ and the starting impulse generator generates the starting impulses from time point $t_5$ to $t_6$ . The feedback to pin 8 starts the next impulse and so on. All impulses including the starting impulse are controlled in width by regulating voltage of pin 1. When switching on this corresponds to a short-circuit event, i.e. $V_1 = 0$. Hence the IC starts up with "short-circuit impulses" to assume a width depending on the regulating voltage feedback (the IC operates in the overload range). The IC operates at the overload point. Thereafter the peak values of $V_2$ decrease rapidly, as the starting attempt is aborted (pin 5 is switched to low). As the IC remains switched on, $V_6$ further decreases to $V_6$ . The IC switches off; $V_6$ can rise again (time point $t_4$) and a new start-up attempt begins at time point $t_1$ . If the rectified alternating line voltage (primary voltage) collapses during load, $V_3$ can fall below $V_{3A}$ , as is happening at time point $t_3$ (switch-on attempt when voltage is too low). The primary voltage monitor then clamps $V_3$ to $V_{3S}$ until the IC switches off ($V_6 < V_{6A}$). Then a new start-up attempt begins at time point $t_1$ .

## Regulation, Overload and No-Load Behaviour

When the IC has started up, it is operating in the regulation range. The potential at pin 1 typically is 400 mV. If the output is loaded, the regulation amplifier allows broader impulses ($V_5$ = H). The peak voltage value at pin 2 increases up to $V_{2S\,max}$. If the secondary load is further increased, the overload amplifier begins to regulate the pulse width downward. This point is referred to as the overload point of the power supply. As the IC-supply voltage $V_6$ is directly proportional to the secondary voltage, it goes down in accordance with the overload regulation behaviour. If $V_6$ falls below the value $V_{6\,min}$, the IC goes into burst operation. As the time constant of the half-wave charge-up is relatively large, the short-circuit power remains small. The overload amplifier cuts back to the pulse width $t_{pk}$. This pulse width must remain possible, in order to permit the IC to start-up without problems from the virtual short-circuit, which every switching on with $V_1$ = 0 represents. If the secondary side is unloaded, the loading impulses ($V_5$ = H) become shorter. The frequency increases up to the resonance frequency of the system. If the load is further reduced, the secondary voltages and $V_6$ increase. When $V_6 = V_{6\,max}$ the logic is blocked. The IC converts to burst operation.This renders the circuit absolutely safe under no-load conditions.

## Behaviour when Temperature Exceeds Limit

An integrated temperature protection disables the logic when the chip temperature becomes too high. The IC automatically interrogates the temperature and starts as soon as the temperature decreases to permissible values.

## Absolute Maximum Ratings

$T_A = -20$ to $85\ ^{\circ}C$

| Parameter | | Symbol | Limit Values | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | min. | max. | | |
| Voltages | pin 1 | $V_1$ | – 0.3 | 3 | V | |
| | pin 2 | $V_2$ | – 0.3 | | V | |
| | pin 3 | $V_3$ | – 0.3 | | V | |
| | pin 5 | $V_5$ | – 0.3 | $V_6$ | V | |
| | pin 6 | $V_6$ | – 0.3 | 20 | V | Supply voltage |
| | pin 7 | $V_7$ | – 0.3 | | V | |
| Currents | pin 1 | $I_1$ | | 3 | mA | |
| | pin 2 | $I_2$ | | 3 | mA | |
| | pin 3 | $I_3$ | | 3 | mA | |
| | pin 4 | $I_4$ | – 1.5 | | A | $t_p \leq 50\ \mu s$; $v \leq 0.1$*) |
| | pin 5 | $I_5$ | – 0.5 | 1.5 | A | $t_p \leq 50\ \mu s$; $v \leq 0.1$ |
| | pin 6 | $I_6$ | | 0.5 | A | $t_p \leq 50\ \mu s$; $v \leq 0.1$ |
| | pin 7 | $I_7$ | | 3 | mA | |
| | pin 8 | $I_8$ | – 5 | 3 | mA | |
| Junction temperature | | $T_j$ | | 125 | $^{\circ}C$ | |
| Storage temperature | | $T_{stg}$ | – 40 | 125 | $^{\circ}C$ | |

## Operating Range

| | | | | | | |
|---|---|---|---|---|---|---|
| Supply voltage | | $V_6$ | 7.5 | 15.5 | V | IC "on" |
| Ambient temperature | | $T_A$ | – 20 | 85 | $^{\circ}C$ | |
| Heat resistance | | | | | | |
| Junction to environment | | $R_{th\ JE}$ | | 100 | K/W | |
| Junction case | | $R_{th\ JC}$ | | 70 | K/W | measured at pin 4 |

*) $t_p$ = pulse width
   v = duty circle

## Characteristics

$T_A$ = 25 °C; $V_S$ = 10 V

| Parameter | Symbol | Limit Values | | | Unit | Test Condition | Test Circuit |
|---|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | | |

**Start-Up Hysteresis**

| Parameter | Symbol | min. | typ. | max. | Unit | Test Condition | Test Circuit |
|---|---|---|---|---|---|---|---|
| Start-up current drain | $I_{6E0}$ | | 0.6 | 0.8 | mA | $V_6 = V_{6E}$ | 1 |
| Switch-on voltage | $V_{6E}$ | 11 | 12 | 13 | V | | 1 |
| Switch-off voltage | $V_{6A}$ | 4.5 | 5 | 5.5 | V | | 1 |
| Switch-on current | $I_{6E1}$ | 7 | 11 | 14 | mA | $V_6 = V_{6E}$ | 1 |
| Switch-off current | $I_{6A1}$ | 5 | 10 | 13 | mA | $V_6 = V_{6A}$ | 1 |

**Voltage Clamp ($V_6$ = 10 V, IC switched off)**

| Parameter | Symbol | min. | typ. | max. | Unit | Test Condition | Test Circuit |
|---|---|---|---|---|---|---|---|
| At pin 2 ($V_6 \le V_{6E}$) | $V_{2\,max}$ | 5.6 | 6.6 | 8 | V | $I_2$ = 1 mA | 1 |
| At pin 3 ($V_6 \le V_{6E}$) | $V_{3\,max}$ | 5.6 | 6.6 | 8 | V | $I_3$ = 1 mA | 1 |

**Control Range**

| Parameter | Symbol | min. | typ. | max. | Unit | Test Condition | Test Circuit |
|---|---|---|---|---|---|---|---|
| Control input voltage | $V_{1R}$ | 390 | 400 | 410 | mV | | 2 |
| Voltage gain of the control circuit in the control range | $-V_R$ | 30 | 43 | 60 | dB | $V_R$ = d $(V_{2S} - V_{2B})$ / $-$ d$V_1$ $f$ = 1 kHz | 2 |

**Primary Current Simulation Voltage**

| Parameter | Symbol | min. | typ. | max. | Unit | Test Condition | Test Circuit |
|---|---|---|---|---|---|---|---|
| Basic value | $V_{2B}$ | 0.97 | 1.00 | 1.03 | V | | 2 |

**Overload Range and Short-Circuit Operation**

| Parameter | Symbol | min. | typ. | max. | Unit | Test Condition | Test Circuit |
|---|---|---|---|---|---|---|---|
| Peak value in the range of secondary overload | $V_{2B}$ | 2.9 | 3.0 | 3.1 | V | $V_1 = V_{1R} - 10$ mV | 2 |
| Peak value in the range of secondary short-circuit operation | $V_{2K}$ | 2.2 | 2.4 | 2.6 | V | $V_1$ = 0 V | 2 |

**Fold-Back Point Correction**

| Parameter | Symbol | min. | typ. | max. | Unit | Test Condition | Test Circuit |
|---|---|---|---|---|---|---|---|
| Fold-back point correction current | $-I_2$ | 300 | 500 | 650 | μA | $V_3$ = 3.7 V | 1 |

## Characteristics (cont'd)

$T_A = 25\ °C;\ V_S = 10\ V$

| Parameter | Symbol | Limit Values | | | Unit | Test Condition | Test Circuit |
|---|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | | |

### Generally Valid Data ($V_6 = 10\ V$)

**Voltage of the Zero Transition Detector**

| Parameter | Symbol | min. | typ. | max. | Unit | Test Condition | Test Circuit |
|---|---|---|---|---|---|---|---|
| Positive clamping voltage | $V_{8P}$ | 0.7 | 0.75 | 0.82 | V | $I_8 = 1\ mA$ | 2 |
| Negative clamping voltage | $V_{8N}$ | − 0.25 | − 0.2 | − 0.15 | V | $I_8 = -1\ mA$ | 2 |
| Threshold value | $V_{8S}$ | 40 | 50 | 76 | mV | | 2 |
| Suppression of transformer ringing | $t_{UL}$ | 3.0 | 3.5 | 3.8 | µs | | 2 |
| Input current | $-I_8$ | 0 | | 4 | µA | $V_8 = 0$ | 2 |

**Push-Pull Output Stage**

| Parameter | Symbol | min. | typ. | max. | Unit | Test Condition | Test Circuit |
|---|---|---|---|---|---|---|---|
| Saturation voltages | | | | | | | |
| Pin 5 sourcing | $V_{Sat0}$ | | 1.5 | 2.0 | V | $I_5 = -0.1\ A$ | 1 |
| Pin 5 sinking | $V_{SatV}$ | | 1.0 | 1.2 | V | $I_5 = +0.1\ A$ | 1 |
| Pin 5 sinking | $V_{SatV}$ | | 1.4 | 1.8 | V | $I_5 = +0.5\ A$ | 1 |

**Output Slew Rate**

| Parameter | Symbol | min. | typ. | max. | Unit | Test Condition | Test Circuit |
|---|---|---|---|---|---|---|---|
| Rising edge | $+\,dV_5/dt$ | | 70 | | V/µs | | 2 |
| Falling edge | $+\,dV_5/dt$ | | 100 | | V/µs | | 2 |

**Reduction of Control Voltage**

| Parameter | Symbol | min. | typ. | max. | Unit | Test Condition | Test Circuit |
|---|---|---|---|---|---|---|---|
| Current to reduce the control voltage | $-I_1$ | | 50 | 130 | µA | $V_7 = 1.1\ V,\ V_1 = 0.4\ V$ | |

## Characteristics (cont'd)

$T_A = 25\ °C;\ V_S = 10\ V$

| Parameter | Symbol | Limit Values | | | Unit | Test Condition | Test Circuit |
|---|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | | |

### Protection Circuit

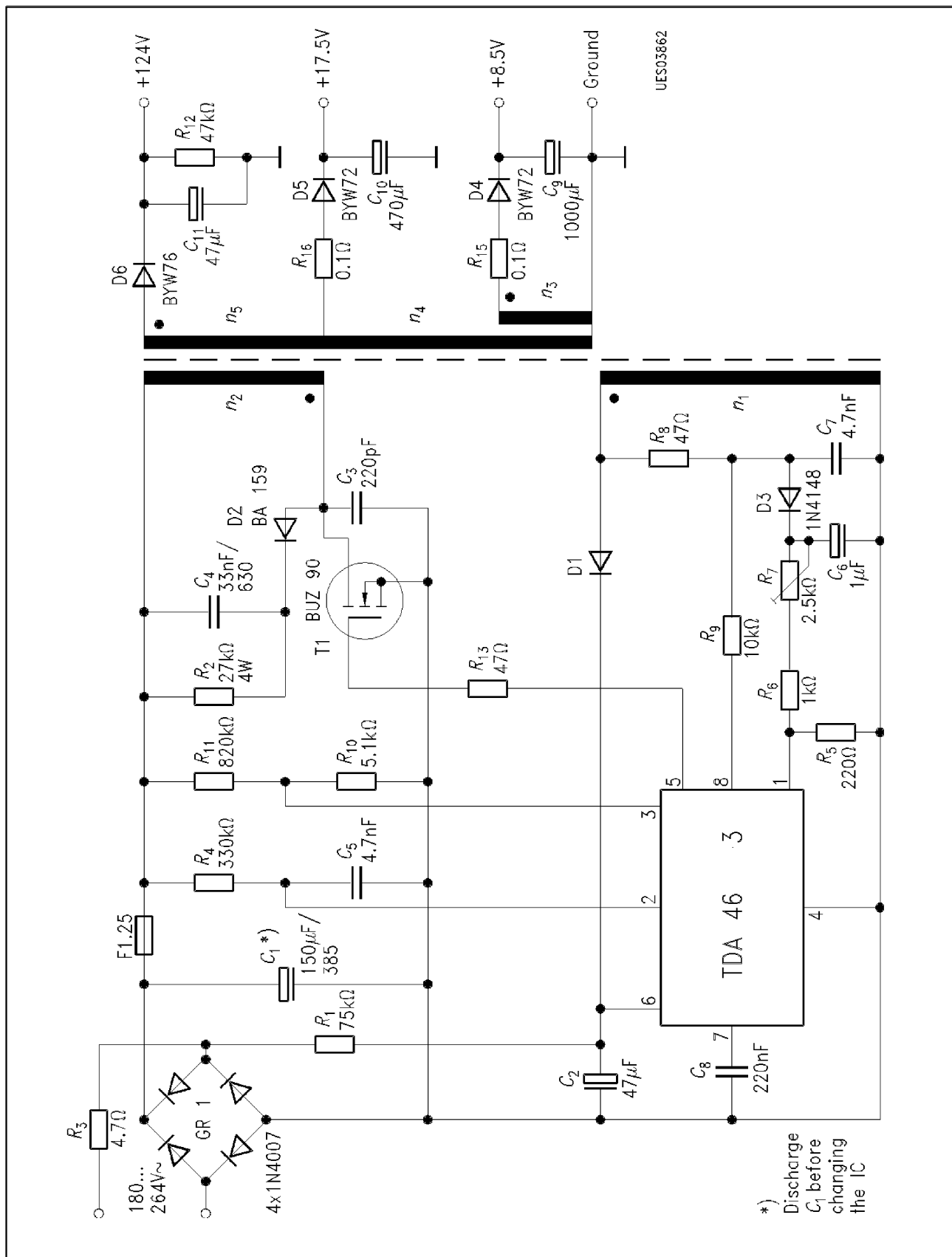| Parameter | Symbol | min. | typ. | max. | Unit | Test Condition | Test Circuit |
|---|---|---|---|---|---|---|---|
| Undervoltage protection for $V_6$ : voltage at pin 5 = $V_{5\ min}$ if $V_6 < V_{5\ min}$ | $V_{6\ min}$ | 7.0 | 7.25 | 7.5 | V | | 2 |
| Undervoltage protection for $V_6$ : voltage at pin 5 = $V_{5\ min}$ if $V_6 > V_{6\ max}$ | $V_{6\ max}$ | 15.5 | 16 | 16.5 | V | | 2 |
| Undervoltage protection for $V_{AC}$ : voltage at pin 4 = $V_{5\ min}$ if $V_3 < V_{3A}$ | $V_{3A}$ | 985 | 1000 | 1015 | mV | $V_2 = 0\ V$ | 1 |
| Over temperature at the given chip temperature the IC will switch $V_5$ to $V_{5\ min}$ | $T_j$ | | 150 | | °C | | 2 |
| Voltage at pin 3 if one of the protection function was triggered; ($V_3$ will be clamped until $V_6 < V_{6A}$) | $V_{3Sat}$ | | 0.4 | 0.8 | V | $I_3 = 750\ \mu A$ | 1 |
| Current drain during burst operation | $I_6$ | | 8 | | mA | $V_3 = V_2 = 0\ V$ | 1 |

$$V_{Sat\,0} = V_6 - V_5$$
$$V_{Sat\,V} = V_5$$
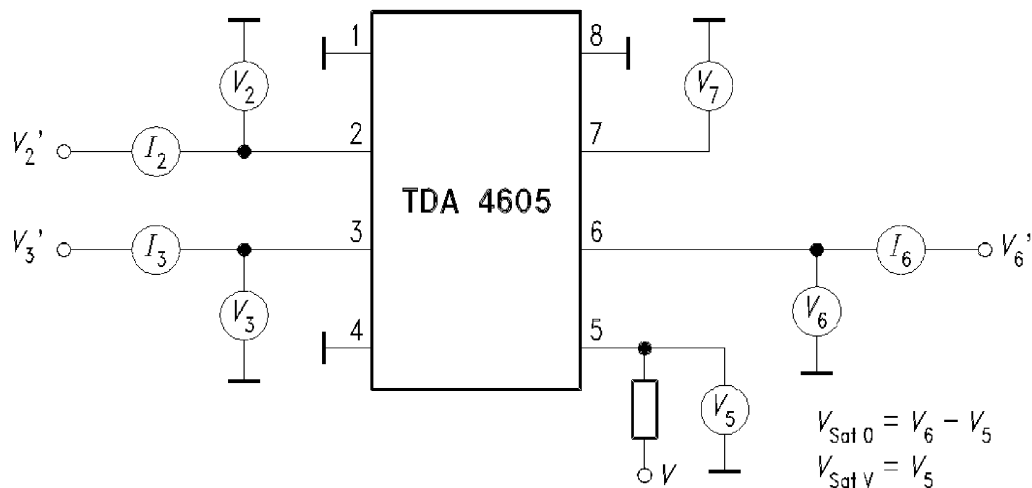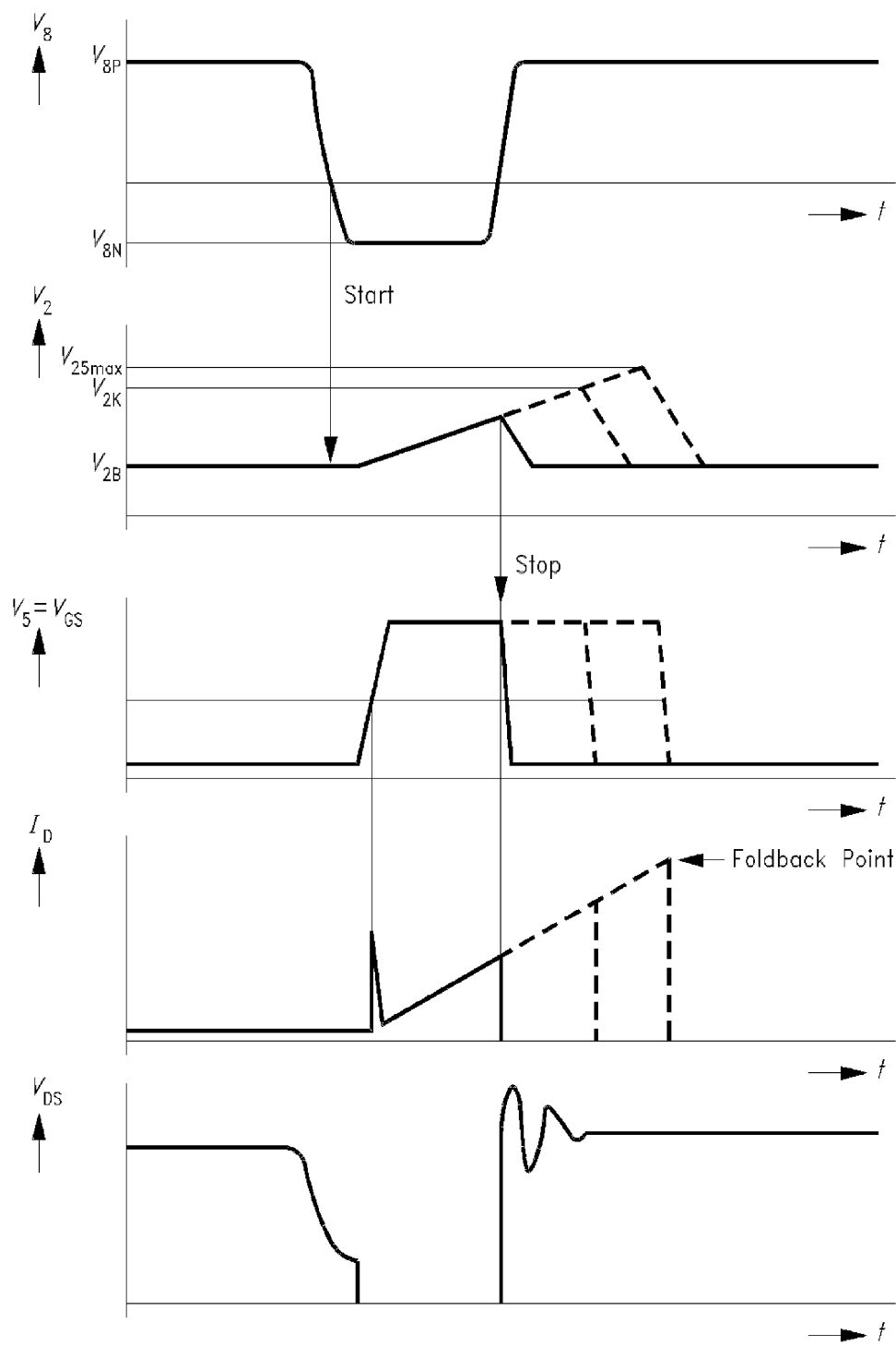
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**Test Circuit 1**
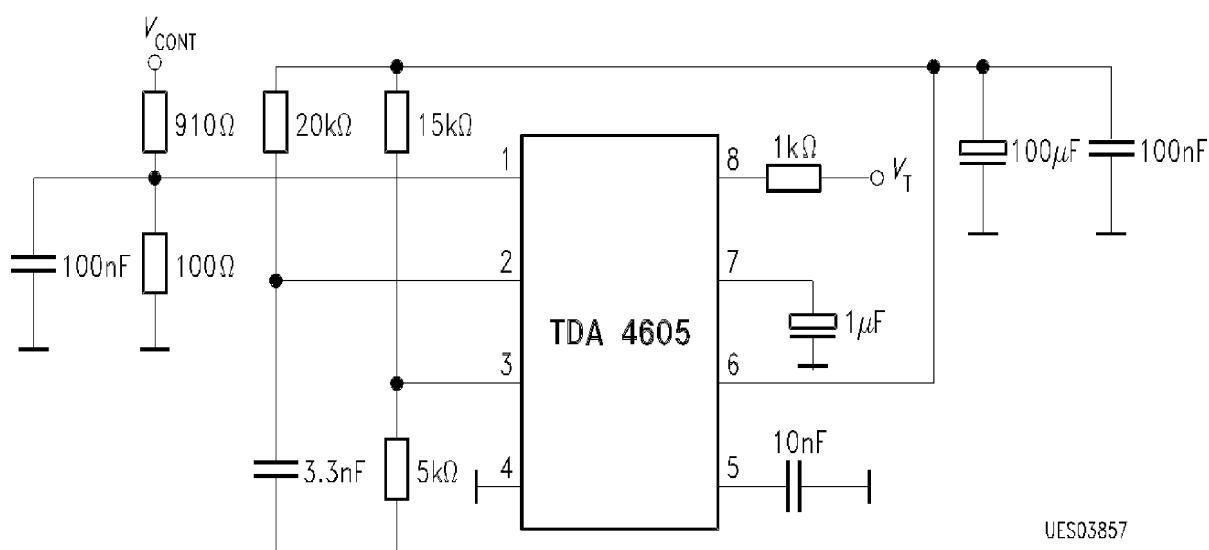


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**Test Circuit 2**

**Application Circuit**
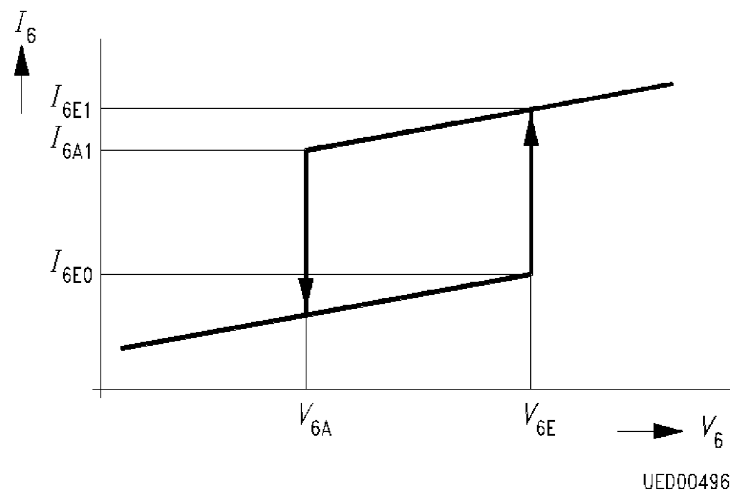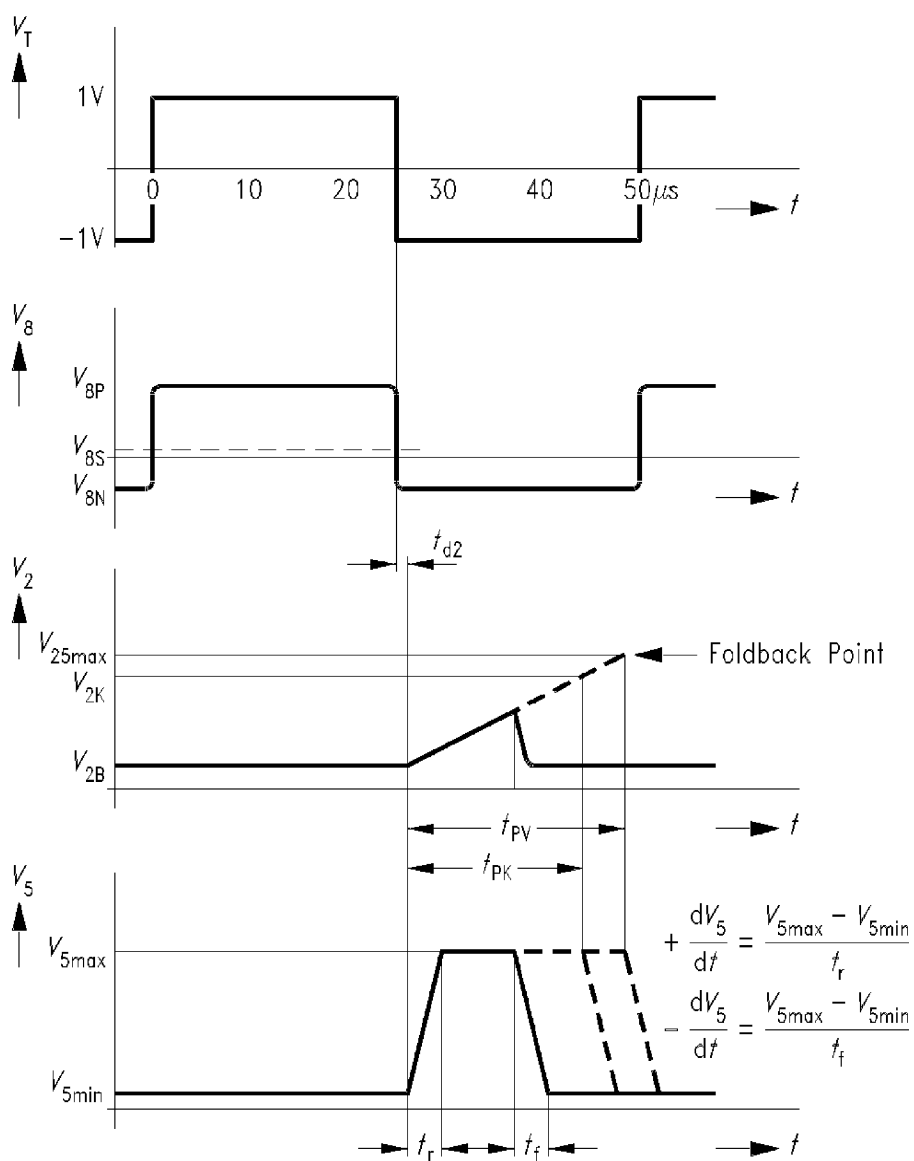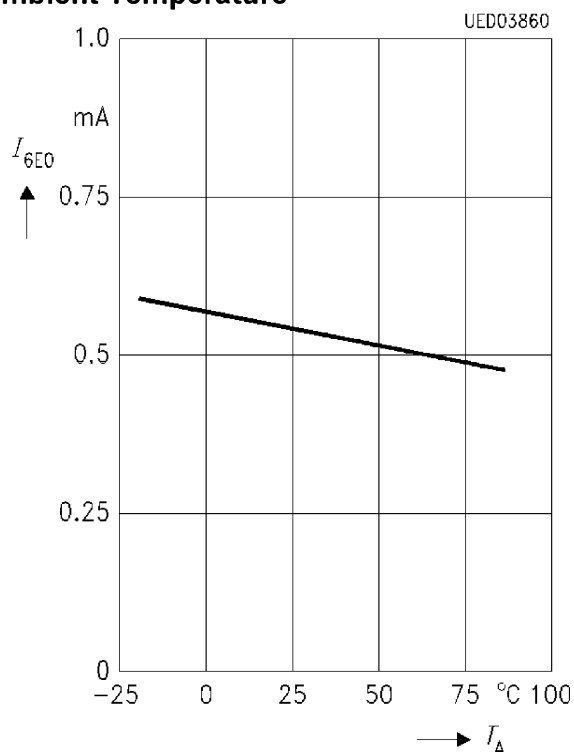
**Diagrams**



UFD00494

UED00495

**Start-Up Hysteresis**

$V_T$

1V

0    10    20    30    40    50 $\mu$s    $t$

−1V

$V_8$

$V_{8P}$

$V_{8S}$

$V_{8N}$

$t$

$t_{d2}$

$V_2$

$V_{25max}$
$V_{2K}$

$V_{2B}$

Foldback Point

$t_{PV}$

$t_{PK}$

$t$

$V_5$

$V_{5max}$

$V_{5min}$

$$+\frac{dV_5}{dt} = \frac{V_{5max} - V_{5min}}{t_r}$$

$$-\frac{dV_5}{dt} = \frac{V_{5max} - V_{5min}}{t_f}$$

$t_r$    $t_f$    $t$
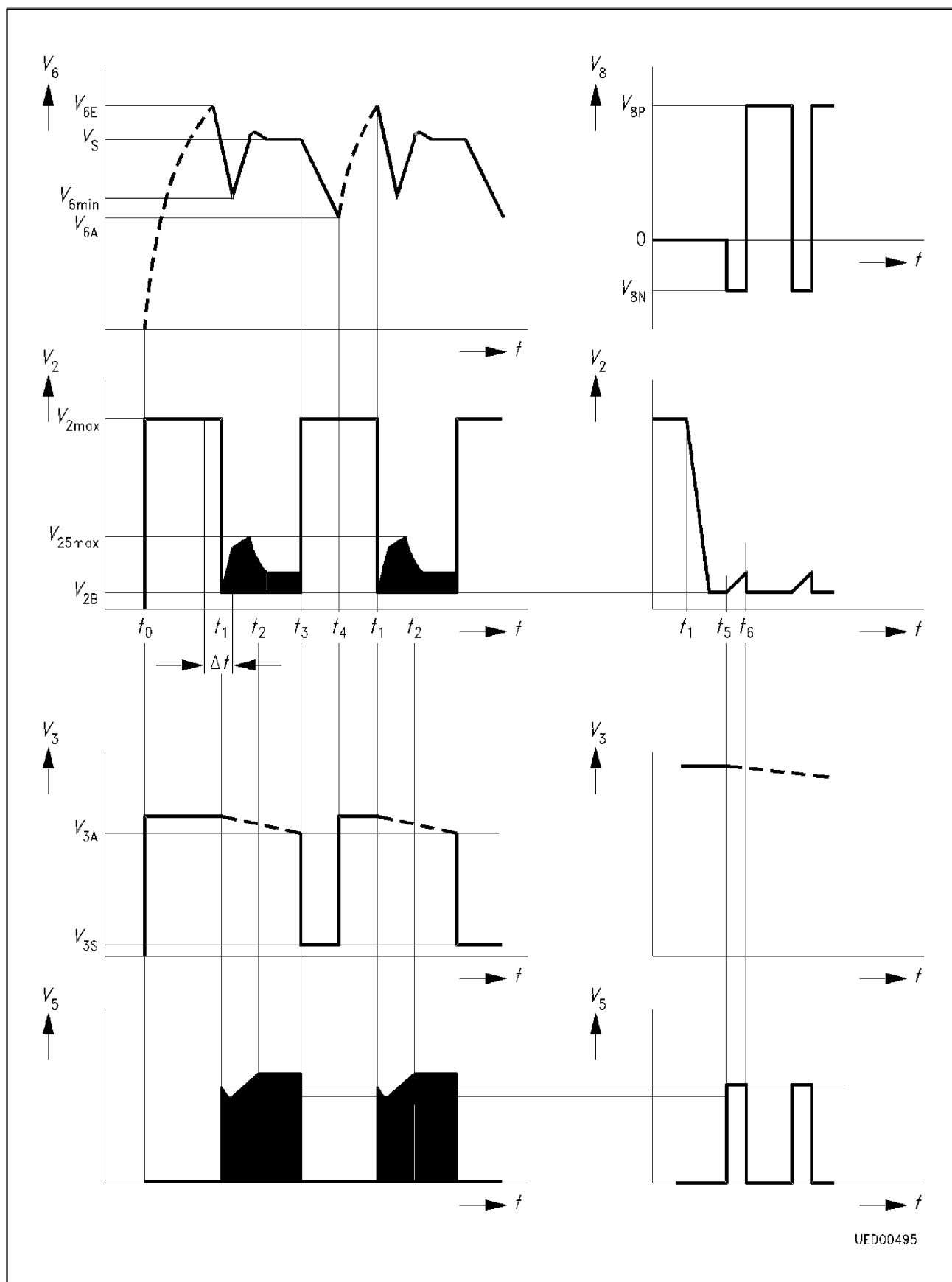
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**Operation in Test Circuit 2**

**Start-Up Current as a Function of the Ambient Temperature**

UED03860



$I_{6E0}$

mA

1.0

0.75

0.5

0.25

0

−25    0    25    50    75 °C 100

$I_A$

**Overload Point Correction as a Function of the Voltage at Pin 3**

UED03861



$I_2$

μA

750

562.3

375

187.5

0

0    2    4    6    V    8

$V_3$
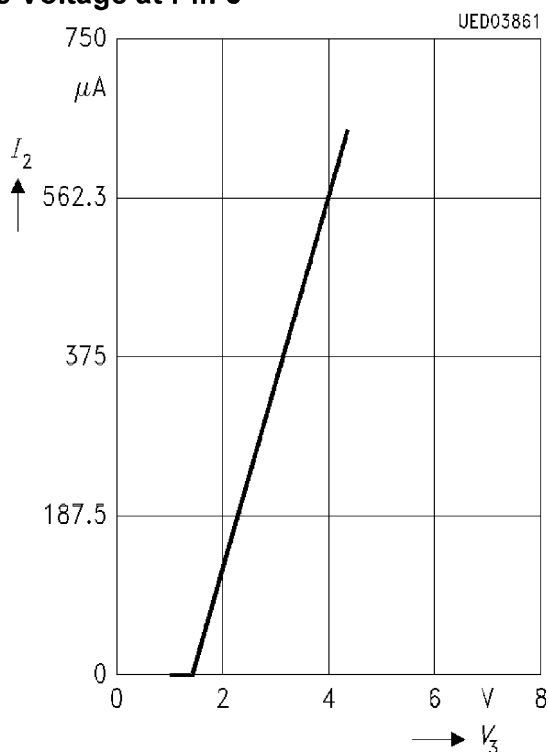
**Recommended Heat Sink by 60 °C Ambient Temperature**

**Narrow Range 180 V ... 120 V ~**



**Narrow Range 90 V ... 270 V ~**