TDA2594
Horizontal Combination

Product Specification

Linear Products

DESCRIPTION

The TDA2594 is a monolithic integrated circuit intended for use in color television receivers.

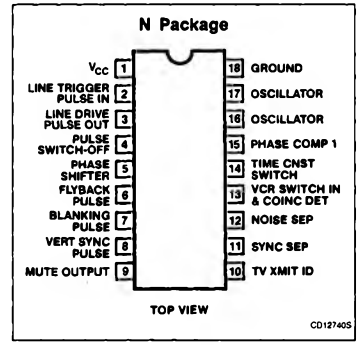
FEATURES

- Horizontal oscillator based on the threshold switching principle
- Phase comparison between sync pulse and oscillator voltage (φ_1)
- Internal key pulse for phase detector (φ1) (additional noise limiting)
- Phase comparison between line flyback pulse and oscillator voltage (φ_2)
- Larger catching range obtained by coincidence detector (φ_3 between sync and key pulse)
- Switch for changing the filter characteristic and the gate circuit (VCR operation)
- Sync separator
- Noise separator
- Vertical sync separator and output stage
- Color burst keying and line flyback blanking pulse generator and clamp circuit for vertical blanking
- Phase shifter for the output pulse
- Output pulse duration for transistor reflection systems
- External switching off of the line trigger pulse
- Output stage with separate supply voltage
- Low supply voltage protection
- Transmitter identification and muting circuit, and vertical sync switch-off

APPLICATIONS

- Video processing
- Television receivers
- Video monitors
- Sync separator

PIN CONFIGURATION

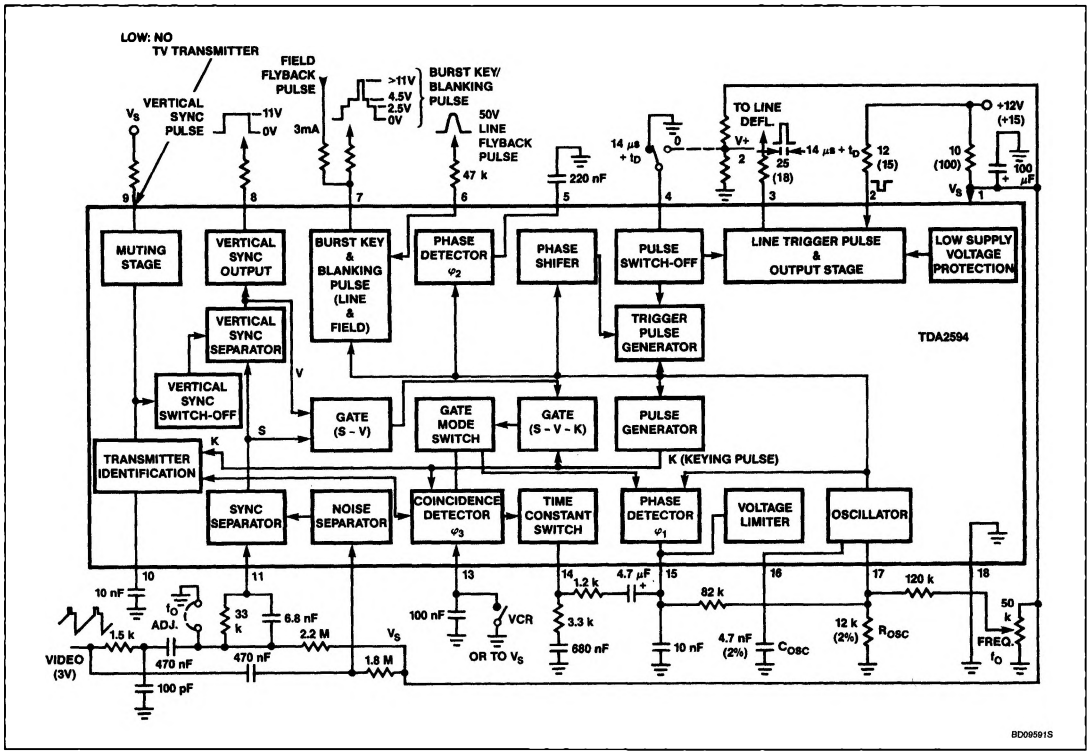


ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102DS)	−20°C to +70°C	TDA2594N

Horizontal Combination | TDA2594

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Supply voltage		
$V_{1-18} = V_S$	at Pin 1 (voltage source)	13.2	V
V_{2-18}	at Pin 2	18	V
	Voltages		
V_{4-18}	Pin 4	13.2	V
V_{9-18}	Pin 9	18	V
$-V_{9-18}$		0.5	V
$\pm V_{11-18}$	Pin 11	6	V
$\pm V_{12-18}$	Pin 12	6	V
V_{13-18}	Pin 13	13.2	V
	Currents		
I_{2M}, $-I_{3M}$	Pins 2 and 3 (transistor driving) (peak value)	400	mA
I_4	Pin 4	1	mA
$\pm I_6$	Pin 6	10	mA
$-I_7$	Pin 7	5	mA
I_9	Pin 9	10	mA
I_{13}	Pin 13	2	mA
P_{TOT}	Total power dissipation	800	mW
T_{STG}	Storage temperature range	−25 to +125	°C
T_A	Operating ambient temperature range	−20 to +70	°C

DC AND AC ELECTRICAL CHARACTERISTICS at $V_{1-18} = 12V$; $T_A = 25°C$; measured in Block Diagram.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Sync separator (Pin 11)					
V_{11-18}	Input switching voltage		0.8		V
I_{11}	Input keying current	5		100	μA
I_{11}	Input leakage current at $V_{11-18} = -5V$			1	μA
I_{11}	Input switching current			5	μA
I_{11}	Switch off current	100	150		μA
$V_{11-18(P-P)}$	Input signal (peak-to-peak value)	3		4	V[1]
Noise separator (Pin 12)					
V_{12-18}	Input switching voltage		1.4		V
I_{12}	Input keying current	5		100	μA
I_{12}	Input switching current	100	150		μA
I_{12}	Input leakage current at $V_{12-18} = -5V$			1	μA
$V_{12-18(P-P)}$	Input signal (peak-to-peak value)	3		4	V[1]
$V_{12-18(P-P)}$	Permissible superimposed noise signal (peak-to-peak value)			7	V
Line flyback pulse (Pin 6)					
I_6	Input current	0.02	1		mA
V_{6-18}	Input switching voltage		1.4		V
V_{6-18}	Input limiting voltage	−0.7		+1.4	V
Switching on VCR (Pin 13)					
V_{13-18}	Input voltage	0		2.5 9 to V_S	V V
$-I_{13}$ or: I_{13}	Input current			200 2	μA mA
Pulse switching off (Pin 4) For t = 0; input Pin 4 open or $V_{3-18} = 0$					
V_{4-18}	Input voltage	5.4		6.6	V
I_4	Input current		0		μA
Vertical sync pulse (Pin 8) (positive-going)					
$V_{8-18(P-P)}$	Output voltage (peak-to-peak value)	10	11		V
R_8	Output resistance		2		kΩ
t_{ON}	Delay between leading edge of input and output signal		15		μs
t_{OFF}	Delay between trailing edge of input and output signal	t_{ON}			μs
V_{10-18}	Switching off the vertical sync pulse			3	V
Burst key pulse (Pin 7) (positive-going)					
V_{7-18}	Output voltage	10	11		V
R_7	Output resistance		70		Ω
t_P	Pulse duration; $V_{7-18} = 7V$	3.7	4	4.3	μs
t	Phase relation between middle of sync pulse at the input and the leading edge of the burst key pulse; $V_{7-18} = 7V$	2.15	2.65	3.15	μs
I_7	Output trailing edge current		2	2	mA
V_{7-18}	Saturation voltage during line scan			1	V

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) at $V_{1-18} = 12V$; $T_A = 25°C$; measured in Block Diagram.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Line flyback-blanking pulse (Pin 7) (positive-going)					
V_{7-18}	Output voltage	4.1		4.9	V
R_7	Output resistance		70		Ω
I_7	Output trailing edge current		2		mA
Field flyback/blanking pulse (Pin 7)					
V_{7-18}	Output voltage with externally forced in current $I_7 = 2.4$ to 3.6mA	2		3	V
R_7	Output resistance at $I_7 = 3mA$		70		Ω
TV transmitter identification output (Pin 9) (open-collector)					
V_{9-18}	Output voltage at $I_9 = 3mA$; no TV transmitter			0.5	V
R_9	Output resistance at $I_9 = 3mA$; no TV transmitter			100	Ω
I_9	Output current at $V_{10-18} \geqslant 3V$; TV transmitter identified			5	μA
TV transmitter identification (Pin 10)					
	When receiving a TV signal, the voltage V_{10-18} will change from $\leqslant 1V$ to $\geqslant 7V$				
Line drive pulse (positive-going)					
$V_{3-18(P-P)}$	Output voltage (peak-to-peak value)		10		V
R_3	Output resistance for leading edge of line pulse for trailing edge of line pulse		 2.5 20		 Ω Ω
t_P	Pulse duration (transistor driving) $V_{4-18} = 0$ to 3.5V; $-I_4 \geqslant 200\mu A$; $t_{FP} = 12\mu s$			$14 + t_D$	μs[2]
V_{1-18}	Supply voltage for switching off the output pulse		4		V
Overall phase relation					
Δt	Phase relation between middle of sync pulse and the middle of the flyback pulse		2.6		μs[3]
	The adjustment of the overall phase relation and consequently the leading edge of the line drive pulse occurs automatically by phase control φ_2.				
$\Delta I/\Delta t$	If additional adjustment is applied, it can be arranged by current supply at Pin 5, such that: supplying current		 30		 μA/μs

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) at $V_{1-18} = 12V$; $T_A = 25°C$; measured in Block Diagram.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Oscillator (Pins 16 and 17)					
V_{16-18}	Threshold voltage low level		4.4		V
V_{16-18}	Threshold voltage high level		7.6		V
$\pm I_{16}$	Charging current		0.47		mA
f_O	Frequency; free running ($C_{OSC} = 4.7nF$; $R_{OSC} = 12k\Omega$)		15.625		kHz
Δf_O	Spread of frequency			± 5	%[6]
$\Delta f_O/\Delta_{17}$	Frequency control sensitivity		31		Hz/μA
Δf_O	Adjustment range of network in circuit (Block Diagram)		± 10		%
$\frac{\Delta f_O/f_O}{\Delta V/V_{NOM}}$	Influence of supply voltage on frequency; reference at $V_S = 12V$			± 0.05	%[6]
Δf_O	Change of frequency when V_S drops to 5V; reference at $V_S = 12V$			± 10	%[6]
TC	Temperature coefficient of oscillator frequency			$\pm 10^{-4}$	K^{-1} [6]
Phase comparison φ_1 (Pin 15)					
V_{15-18}	Control voltage range	4.1		7.9	V
$\pm I_{15M}$	Control current (peak value)	1.8		2.2	mA
I_{15}	Output leakage current at $V_{15-18} = 4.3$ to 7.7V			1	μA
R_{13} R_{13}	Output resistance at $V_{15-18} = 4.3$ to 7.7V[4] at $V_{15-18} \leq 4.1V$ or $\geq 7.9V$[5]		high ohmic low ohmic		
	Control sensitivity		2		kHz/μs
Δf	Catching and holding range (82kΩ between Pins 15 and 17)		± 680		Hz
$\Delta(\Delta f)$	Spread of catching and holding range		± 12		%[6]
Phase comparison φ_2 and phase shifter (Pin 5)					
V_{5-18}	Control voltage range	5.4		7.6	V
$\pm I_{5M}$	Control current (peak value)		1		mA
R_5	Output resistance at $V_{5-18} = 5.4$ to 7.6V[4]		high ohmic		
I_5	Input leakage current at $V_{5-18} = 5.4$ to 7.6V			5	μA
t_D	Permissible delay between leading edge of output pulse and leading edge of flyback pulse ($t_{FP} = 12\mu s$)			15.5	μs
$\Delta t/\Delta t_D$	Static control error			0.2	%
Coincidence detector φ_3 (Pin 13)					
V_{13-18}	Output voltage	0.5		6	V
I_{13M} $-I_{13M}$	Output current (peak value) without coincidence with coincidence		0.1 0.5		mA mA

NOTES:
1. Permissible range 1 to 7V.
2. t_D = switch-off delay of line output stage.
3. Line flyback pulse duration $t_{FP} = 12\mu s$.
4. Current source.
5. Emitter-follower.
6. Excluding external component tolerances.