

TDA2593 Horizontal Combination

Product Specification

Linear Products

DESCRIPTION

The TDA2593 is a monolithic integrated circuit intended for use in color television receivers in combination with TDA2510, TDA2520, TDA2560 as well as with TDA3505, TDA3510, and TDA3520.

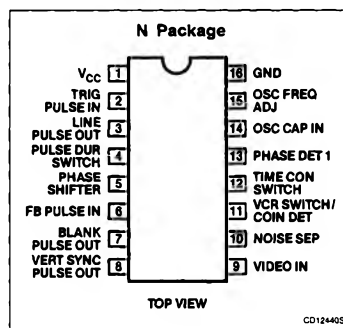
FEATURES

- Horizontal oscillator based on the threshold switching principle
- Phase comparison between sync pulse and oscillator voltage (φ_1)
- Internal key pulse for phase detector (φ_1) (additional noise limiting)
- Phase comparison between line flyback pulse and oscillator voltage (φ_2)
- Larger catching range obtained by coincidence detector (φ_3 ; between sync and key pulse)
- Switch for changing the filter characteristic and the gate circuit (VCR operation)
- Sync separator
- Noise separator
- Vertical sync separator and output stage
- Color burst keying and line flyback blanking pulse generator
- Phase shifter for the output pulse
- Output pulse duration switching
- Output stage with separate supply voltage for direct drive of thyristor deflection circuits
- Low supply voltage protection

APPLICATIONS

- Video monitors
- TV receivers

PIN CONFIGURATION



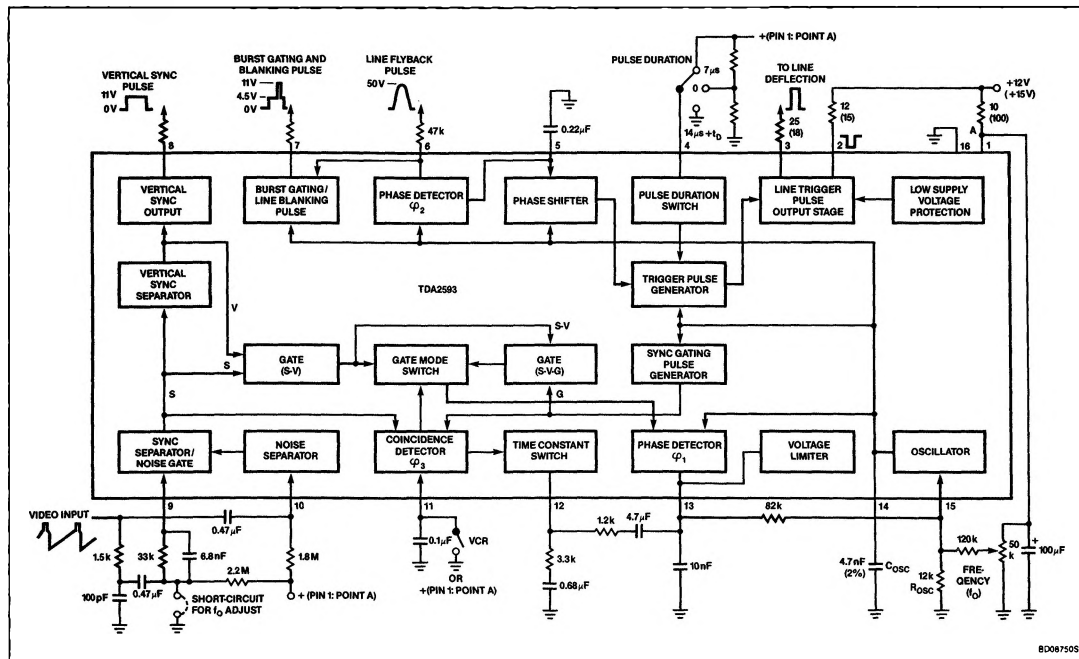
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	-20°C to +70°C	TDA2593N

Horizontal Combination

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{1-16}	Supply voltage at Pin 1 (voltage source) at Pin 2	13.2	V
V_{2-16}		18	V
V_{4-16}	Voltages Pin 4 Pin 9 Pin 10 Pin 11	13.2	V
$\pm V_{9-16}$		6	V
$\pm V_{10-16}$		6	V
V_{11-16}		13.2	V
$I_{2M} - I_{3M}$	Currents Pins 2 and 3 (thyristor driving) (peak value) Pins 2 and 3 (transistor driving) (peak value) Pin 4 Pin 6 Pin 7 Pin 11	650	mA
$I_{2M} - I_{3M}$		400	mA
I_4		1	mA
$\pm I_6$		10	mA
$-I_7$		10	mA
I_{11}		2	mA
P_{TOT}	Total power dissipation	800	mW
T_{STG}	Storage temperature range	-25 to +125	°C
T_A	Operating ambient temperature range	-20 to +70	°C

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DC AND AC ELECTRICAL CHARACTERISTICS at $V_{CC} = 12V$; $T_A = 25^\circ C$; measured in Block Diagram.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Sync separator					
V_{9-16}	Input switching voltage		0.8		V
I_9	Input keying current	5		100	μA
I_9	Input leakage current at $V_{9-16} = -5V$			1	μA
I_9	Input switching current			5	μA
I_9	Switch off current	100	150		μA
$V_{9-16(P-P)}$	Input signal (peak-to-peak value)	3		4	V^1
Noise separator					
V_{10-16}	Input switching voltage		1.4		V
I_{10}	Input keying current	5		100	μA
I_{10}	Input switching current	100	150		μA
I_{10}	Input leakage current at $V_{10-16} = -5V$			1	μA
$V_{10-16(P-P)}$	Input signal (peak-to-peak value)	3		4	V^1
$V_{10-16(P-P)}$	Permissible superimposed noise signal (peak-to-peak value)			7	V
Line flyback pulse					
I_6	Input current	0.02	1	2	mA
V_{6-16}	Input switching voltage		1.4		V
V_{6-16}	Input limiting voltage	-0.7		+1.4	V
Switching on VCR					
V_{11-16} V_{11-16}	Input voltage	0 to 2.5 9 to V_{1-16}			V V
$-I_{11}$ I_{11}	Input current			200 2	μA mA
Pulse duration switch for $t = 7\mu s$ (thyristor driving)					
V_{4-16}	Input voltage		9.4 to V_{1-16}		V
I_4	Input current	200			μA
Pulse duration switch for $t = 14\mu s + t_D$ (transistor driving)					
V_{4-16}	Input voltage	0		3.5	V
$-I_4$	Input current	200			μA
Pulse duration switch for $t = 0$; $V_{3-16} = 0$ or input Pin 4 open					
V_{4-16}	Input voltage	5.4		6.6	V
I_4	Input current		0	0	μA
Vertical sync pulse (positive-going)					
$V_{8-16(P-P)}$	Output voltage (peak-to-peak value)	10	11		V
R_8	Output resistance		2		$k\Omega$
t_{ON}	Delay between leading edge of input and output signal		15		μs
t_{OFF}	Delay between trailing edge of input and output signal		t_{on}		μs

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued) at $V_{CC} = 12V$; $T_A = 25^\circ C$; measured in Block Diagram.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Burst gating pulse (positive-going)					
V _{7-16(P-P)}	Output voltage (peak-to-peak value)	10	11		V
R ₇	Output resistance		70		Ω
t _p	Pulse duration; V ₇₋₁₆ = 7V	3.7	4 4.3		μs μs
t	Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse; V ₇₋₁₆ = 7V	2.15	2.65	3.15	μs
I ₇	Output trailing edge current		2		mA
Line flyback-blanking pulse (positive-going)					
V _{7-16(P-P)}	Output voltage (peak-to-peak value)	4	5		V
R ₇	Output resistance		70		Ω
I ₇	Output trailing edge current		2		mA
Line drive pulse (positive-going)					
V _{3-16(P-P)}	Output voltage (peak-to-peak value)		10.5		V
R ₃ R ₃	Output resistance for leading edge of line pulse for trailing edge of line pulse		2.5 20		Ω Ω
t _p	Pulse duration (thyristor driving) V ₄₋₁₆ = 9.4 to V ₁₋₁₆ V	5.5	7	8.5	μs
t _p	Pulse duration (transistor driving) V ₄₋₁₆ = 0 to 4V; t _{FP} = 12μs		14 + t _D		μs ²
V ₁₋₁₆	Supply voltage for switching off the output pulse		4		V
Overall phase relation					
t	Phase relation between middle of sync pulse and the middle of the flyback pulse		2.6		μs ³
Δt	Tolerance of phase relation			0.7	μs
ΔI ₅ /Δt	The adjustment of the overall phase relation and consequently the leading edge of the line drive occurs automatically by phase control φ ₂ . If additional adjustment is applied it can be arranged by current supply at Pin 5		30		μA/μs
Oscillator					
V ₁₄₋₁₆	Threshold voltage low level		4.4		V
V ₁₄₋₁₆	Threshold voltage high level		7.6		V
± I ₁₄	Discharge current		0.47		mA
f _O	Frequency; free running (C _{Osc} = 4.7nF; R _{Osc} = 12kΩ)		15.625		kHz
Δf _O /f _O	Spread of frequency		< ± 5		% ⁴
Δf _O /ΔI ₁₅	Frequency control sensitivity		31		Hz/μA
Δf _O /f _O	Adjustment range of network in circuit (see Block Diagram)		± 10		%
$\frac{\Delta f_O/f_O}{\Delta V/V_{NOM}}$	Influence of supply voltage on frequency		< ± 0.05		% ⁴
Δf _O	Change of frequency when V ₁₋₁₆ drops to 5V		< ± 10		% ⁴
	Temperature coefficient of oscillator frequency		< ± 10 ⁻⁴		Hz/°C ⁴

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued) at $V_{CC} = 12V$; $T_A = 25^\circ C$; measured in Block Diagram.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Phase comparison φ_1					
V_{13-16}	Control voltage range	3.8	8.2		V
$\pm I_{13M}$	Control current (peak value)	1.9	2.3		mA
I_{13}	Output leakage current at $V_{13-16} = 4$ to 8V			1	μA
R_{13} R_{13}	Output resistance at $V_{13-16} = 4$ to 8V ⁵ at $V_{13-16} < 3.8V$ or $> 8.2V^6$	high ohmic low ohmic			
	Control sensitivity		2		kHz/ μs
Δf	Catching and holding range (82k Ω between Pins 13 and 15)		± 780		Hz
$\Delta(\Delta f)$	Spread of catching and holding range		± 10		% ⁴
Phase comparison φ_2 and phase shifter					
V_{5-16}	Control voltage range	5.4		7.6	V
$\pm I_{5M}$	Control current (peak value)		1		mA
R_5	Output resistance at $V_{5-16} = 5.4$ to 7.6V ⁷ at $V_{5-16} < 5.4$ or $> 7.6V$		high ohmic 8		k Ω
I_5	Input leakage current $V_{5-16} = 5.4$ to 7.6V			5	μA
t_D	Permissible delay between leading edge of output pulse and leading edge of flyback pulse ($t_{FP} = 12\mu s$)			15	μs
$\Delta t/\Delta t_D$	Static control error			0.2	%
Coincidence detector φ_3					
V_{11-16}	Output voltage	0.5		6	V
I_{11M} $-I_{11M}$	Output current (peak value) without coincidence with coincidence		0.1 0.5		mA mA
Time constant switch					
V_{12-16}	Output voltage		6		V
$\pm I_{12}$	Output current (limited)			1	mA
R_{12} R_{12}	Output resistance at $V_{11-16} = 2.5$ to 7V at $V_{11-16} < 1.5V$ or $> 9V$		0.1 60		k Ω k Ω
Internal gating pulse					
t_p	Pulse duration		7.5		μs

NOTES:

1. Permissible range 1 to 7V.
2. t_D = switch-off delay of line output stage.
3. Line flyback pulse duration $t_{FP} = 12\mu s$.
4. Excluding external component tolerances.
5. Current source.
6. Emitter-follower.
7. Current source.