TDA 2008

LINEAR INTEGRATED CIRCUIT

12W AUDIO AMPLIFIER (V_s = 22V, R_L = 4Ω)

The TDA 2008 is a monolithic class B audio power amplifier in Pentawatt® package designed for driving low impedance loads (down to 3.2Ω). The device provides a high output current capability (up to 3A), very low harmonic and crossover distortion.
In addition, the device offers the following features:

- very low number of external components
- assembly ease, due to Pentawatt® power package with no electrical insulation requirement
- space and cost saving
- high reliability
- flexibility in use
- thermal protection

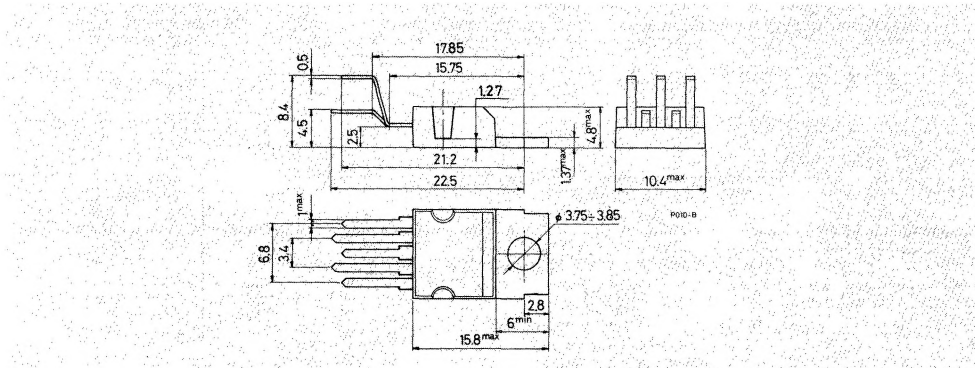
ABSOLUTE MAXIMUM RATINGS

V_s	DC supply voltage	28	V
I_o	Output peak current (repetitive)	3	A
I_o	Output peak current (non repetitive)	4	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

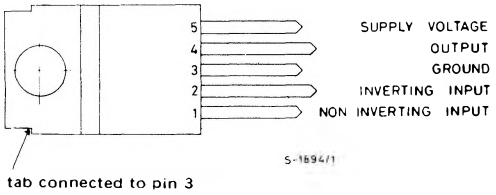
ORDERING NUMBERS: TDA 2008V

MECHANICAL DATA

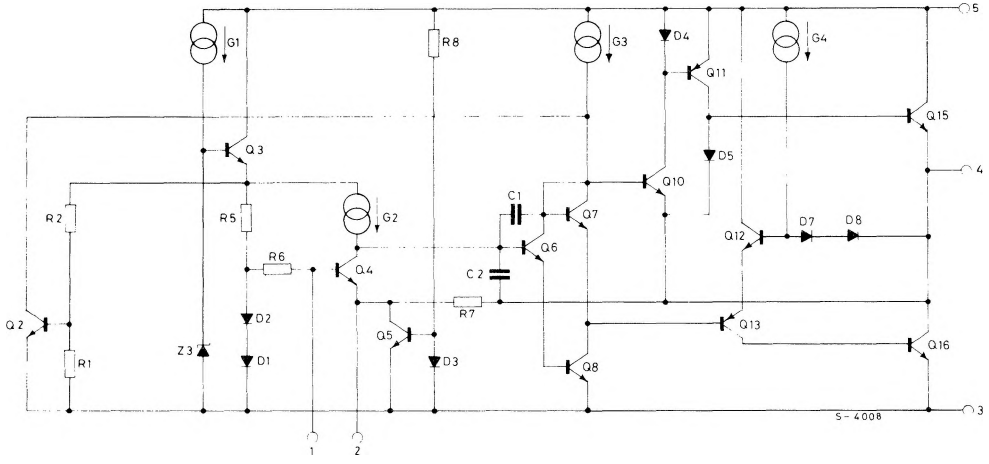
Dimensions in mm



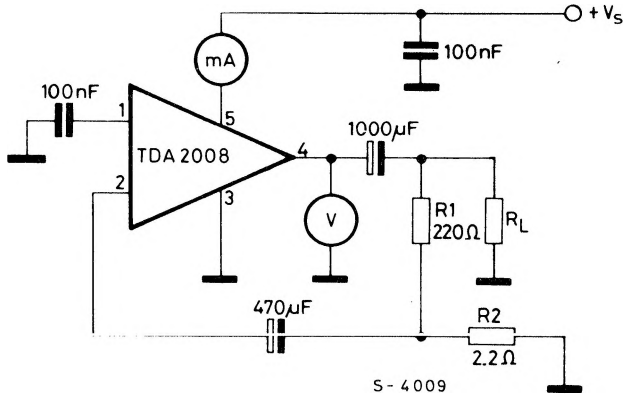
CONNECTION DIAGRAM (top view)



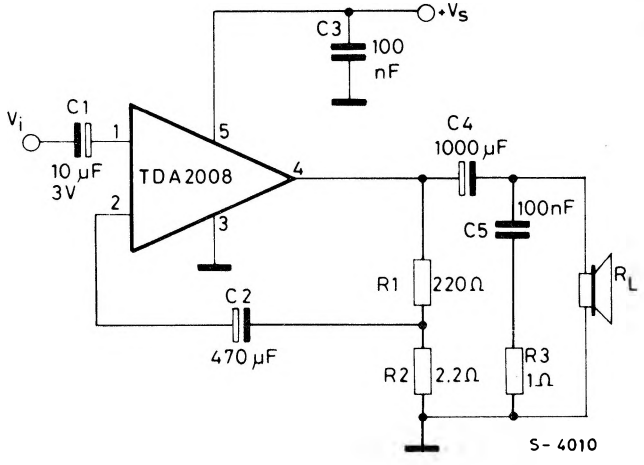
SCHEMATIC DIAGRAM



DC TEST CIRCUIT



AC TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, V_s = 22V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			10		28	V
V_o	Quiescent output voltage (pin 4)				10.5		V
I_d	Quiescent drain current (pin 5)				65	115	mA
P_o	Output power	d = 10%	R_L = 8Ω		8		W
		f = 1 KHz	R_L = 4Ω	10	12		W
V_i (RMS)	Input saturation voltage			300			mV
V_i	Input sensitivity	f = 1 KHz P_o = 0.5W P_o = 8W P_o = 0.5W P_o = 12W	 R_L = 8Ω R_L = 8Ω R_L = 4Ω R_L = 4Ω		 20 80 14 70		 mV mV mV mV
B	Frequency response (-3 dB)	P_o = 1W R_L = 4Ω		40 to 15 000			Hz
d	Distortion	f = 1 KHz P_o = 0.05 to 4W P_o = 0.05 to 6W	 R_L = 8Ω R_L = 4Ω		 0.15 0.15		 % %
R_i	Input resistance (pin 1)	f = 1 KHz		70	150		KΩ
G_v	Voltage gain (open loop)	f = 1 KHz	R_L = 8Ω		80		dB
G_v	Voltage gain (closed loop)			39.5	40	40.5	dB
e_N	Input noise voltage	BW= 22Hz to 22 KHz			1	5	μV
i_N	Input noise current				60	200	pA
SVR	Supply voltage rejection	V_{ripple} = 0.5V R_g = 10KΩ R_L = 4Ω	f = 100 Hz	30	36		dB
			f = 15 KHz		36		dB

APPLICATION INFORMATION

Fig. 1 - Typical application circuit

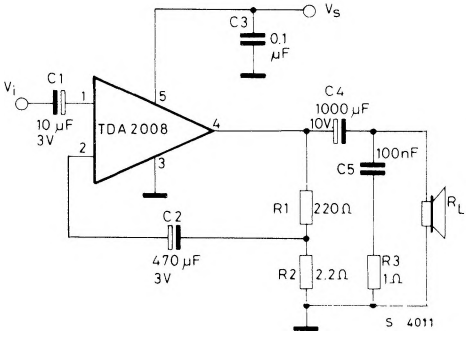


Fig. 2 - P.C. board and component layout for the circuit of fig. 1 (1:1 scale)

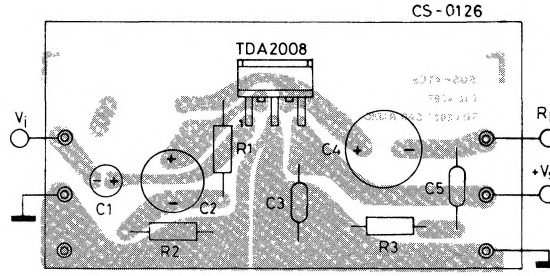


Fig. 3 - 25W bridge configuration application circuit (°)

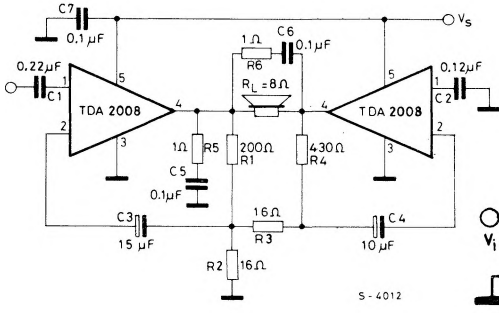
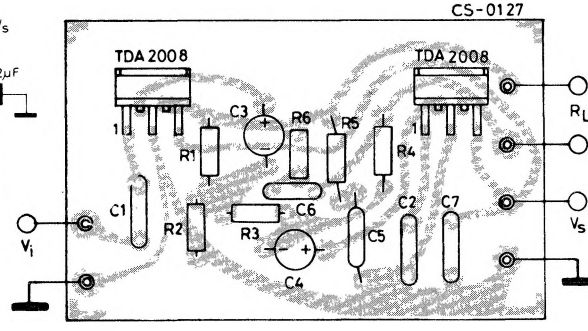


Fig. 4 - P.C. board and component layout for the circuit of fig. 3 (1:1 scale)



(°) The value of the capacitors C3 and C4 are different to optimize the SVR (Typ. = 40 dB)

Fig. 5 - Vertical deflection for count-down circuits