Signetics

TDA1541A
Dual 16-Bit Digital-to-Analog Converter

Product Specification

Linear Products

DESCRIPTION

The TDA1541A is a monolithic integrated dual 16-bit digital-to-analog converter (DAC) designed for use in hi-fi digital audio equipment such as compact disc players, digital tape, or cassette recorders.

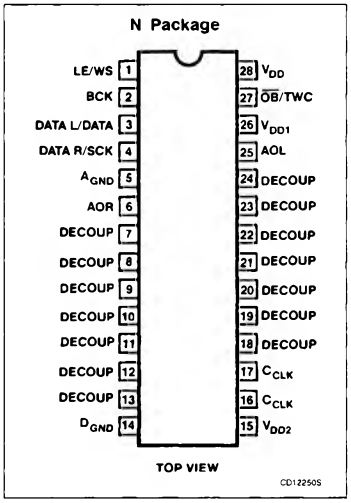
FEATURES

- **Selectable input format: offset binary or two's complement**
- **Internal timing and control circuit**
- **TTL-compatible digital inputs**
- **High maximum input bit rate and fast settling time**
- **6Mbits/s data rate**
- **Low linearity error (½ LSB typ.)**
- **Fast settling (1μs typ.)**

APPLICATIONS

- **Compact disc players**
- **Digital audio tape, and cassette recorders and players**
- **Waveform generation**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP	−20°C to +70°C	TDA1541AN

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Supply voltage ranges		
V_{DD}	Pin 28	+7	V
V_{DD1}	Pin 26	−7	V
V_{DD2}	Pin 15	−17	V
T_J	Junction temperature range	−55 to +150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−40 to +85	°C
V_{ES}	Electrostatic handling[1]	−1000 to +1000	V

NOTE:
1. Discharging a 250pF capacitor through a 1kΩ series resistor.

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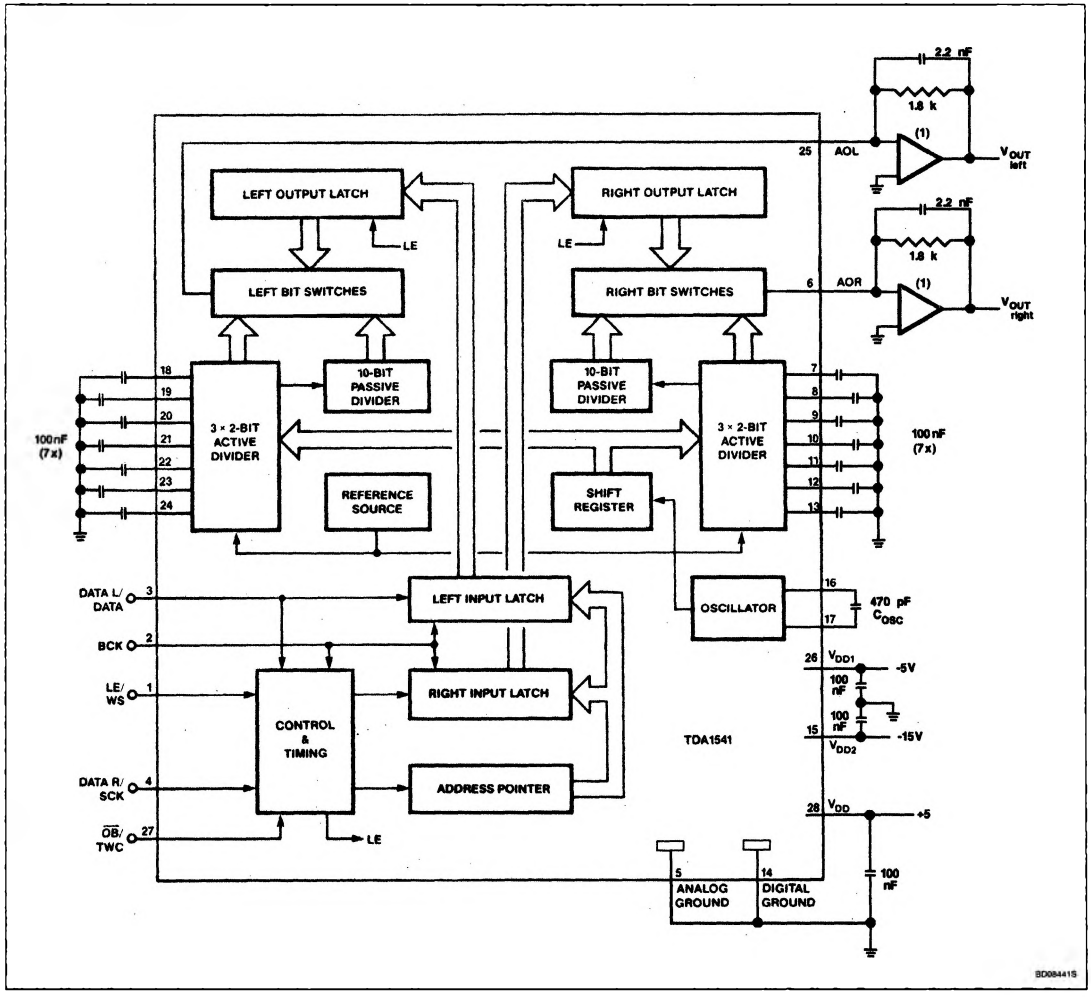
BLOCK DIAGRAM



DC AND AC ELECTRICAL CHARACTERISTICS $V_{DD} = +5V$; $V_{DD1} = -5V$; $V_{DD2} = -15V$; $T_A = +25°C$; measured in Figure 1, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
	Supply voltage ranges				
V_{DD}	Pin 28	4.5	5.0	5.5	V
$-V_{DD1}$	Pin 26	4.5	5.0	5.5	V
$-V_{DD2}$	Pin 15	14	15	16	V
	Supply currents				
I_{DD}	Pin 28		27	40	mA
$-I_{DD1}$	Pin 26		37	50	mA
$-I_{DD2}$	Pin 15		25	35	mA
	Resolution		16		bits
	Voltage difference between analog and digital ground	−0.3		+0.3	V
Inputs					
	Input current (Pins 1, 2, 3 and 4)				
I_{IL}	digital inputs LOW (< 0.8V)			0.4	mA
I_{IH}	digital inputs HIGH (> 2.0V)			20	μA
	Digital input current (Pin 27)				
$\|\ \overline{OB}/TWC\|$	+5V			1	μA
$\|\ \overline{OB}/TWC\|$	0V			20	μA
$\|\ \overline{OB}/TWC\|$	−5V			40	μA
	Input frequency				
f_{BCK}	at clock input (Pin 2)			0.4	MHz
f_{DAT}	at data inputs (Pin 3 and Pin 4)			0.4	MHz
f_{WS}	at word select input (Pin 1)			200	kHz
f_{LE}	at latch enable Pin 1			200	kHz
C_I	Input capacitance of digital inputs		12		pF
Oscillator					
f_{OSC}	Oscillator frequency $C_{OSC} = 470pF$	150	200	275	kHz
Analog outputs (AOL; AOR)					
V_{OC}	Output voltage compliance				mV
I_{FS}	Full-scale current	3.4	4.0	4.6	mA
$\pm I_{ZS}$	Zero-scale current	–	25	50	mA
TC_{FS}	Full-scale temperature coefficient $T_A = -20$ to $+85°C$		$\pm 200 \times 10^{-6}$		ppm/°C
	Linearity error integral				
E_L	at $T_A = 25°C$		0.5	1.0	LSB
E_L	at $T_A = -20$ to $+85°C$			1.0	LSB
	Linearity error differential				
E_{DL}	at $T_A = 25°C$		0.5	1.0	LSB
E_{DL}	at $T_A = -20$ to $+85°C$			1.0	LSB
THD	Total harmonic distortion		−100		dB
S/N	Signal-to-noise ratio + THD[2]	90	95		dB
t_{CS}	Settling time to ±1 LSB		0.5		μs

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{DD} = +5V$; $V_{DD1} = -5V$; $V_{DD2} = -15V$; $T_A = +25°C$; measured in Figure 1, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
α	Channel separation	80	98		dB
ΔI_{FS}	Unbalance between outputs		0.1	0.3	dB
t_D	Time delay between outputs			0.2	μs
	Supply voltage ripple rejection[3]				
SVRR	$V_{DD} = +5V$		-76		dB
SVRR	$V_{DD1} = -5V$		-84		dB
SVRR	$V_{DD2} = -15V$		-58		dB
	Signal-to-noise ratio				
S/N	at bipolar zero		110		dB
	at full scale	98	104		dB
Timing (see Figures 2, 3, and 4)					
t_R	Rise time			32	ns
t_F	Fall time			32	ns
t_{CY}	Bit clock cycle time	156			ns
t_{HB}	Bit clock High time	46			ns
t_{LB}	Bit clock Low time	46			ns
t_{FBRL}	Bit clock fall time to latch rise time	0			ns
t_{RBFL}	Bit clock rise time to latch fall time	0			ns
t_{SDB}	Data setup time to bit clock	32			ns
t_{HDB}	Data hold time to bit clock	0			ns
t_{SDS}	Data setup time to system clock	32			ns
t_{HWS}	Word select hold time to system clock	0			ns
t_{SWS}	Word select setup time to system clock	32			ns

NOTES:
1. To ensure no performance losses, permitted output voltage compliance is ±25mV maximum.
2. Signal-to-noise ratio + THD with 1kHz full-scale sine wave generated at a sampling rate of 176.4kHz.
3. $V_{RIPPLE} = 100mV$ and $f_{RIPPLE} = 100Hz$.

FUNCTIONAL DESCRIPTION

The TDA1541A accepts input sample formats in time multiplexed mode or simultaneous mode with any bit length. The most significant bit (MSB) must always be first. This flexible input data format allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits, pulse code modulation adaptors and audio signal processors (ASP).

The high maximum input bit rate and fast settling time facilitates application in 4 × oversampling systems (44.1kHz to 176.4kHz or 48kHz to 192kHz) with the associated simple analog filtering function (low-order, linear phase filter).

Input Data Selection

(See also Table 1)

With input $\overline{OB}$/TWC connected to ground, data input (offset binary format) must be in time multiplexed mode. It is accompanied with a word select (WS) and a bit clock input (BCK) signal. A separate system clock input (SCK) is provided for accurate, jitter-free timing of the analog outputs AOL and AOR.

With $\overline{OB}$/TWC connected to V_{DD}, the mode is the same, but data format must be in two's complement.

When input $\overline{OB}$/TWC is connected to (V_{DD1}) the two channels of data (L/R) are input simultaneously via (DATA L) and (DATA R), accompanied by BCK and a latch-enable input (LE). With this mode selected, the data must be in offset binary.

The format of data input signals is shown in Figures 2, 3, and 4.

True 16-bit performance is achieved by each channel using three 2-bit active dividers, operating on the dynamic element matching principle, in combination with a 10-bit passive current-divider, based on emitter scaling. All digital inputs are TTL-compatible.

Table 1. Input Data Selection

$\overline{OB}$/TWC	MODE	PIN 1	PIN 2	PIN 3	PIN 4
−5V	Simultaneous	LE	BCK	DATA L	DATA R
0V	Time MUX OB	WS	BCK	DATA OB	NOT USED
+5V	Time MUX TWC	WS	BCK	DATA TWC	NOT USED

Where:
LE = Latch enable
WS = Word select
BCK = Bit clock
DATA L = Data left
DATA R = Data right
DATA OB = Data offset binary
DATA TWC = Data two's complement
MUX OB = Multiplexed offset binary
MUX TWC = Multiplexed two's complement

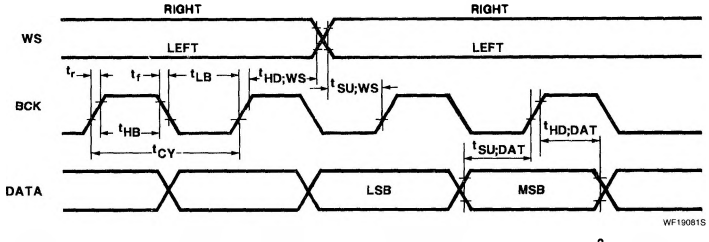


Figure 1. Format of Input Signals; Time Multiplexed at $f_{SCK} = f_{CK}$ (I^2S Format)

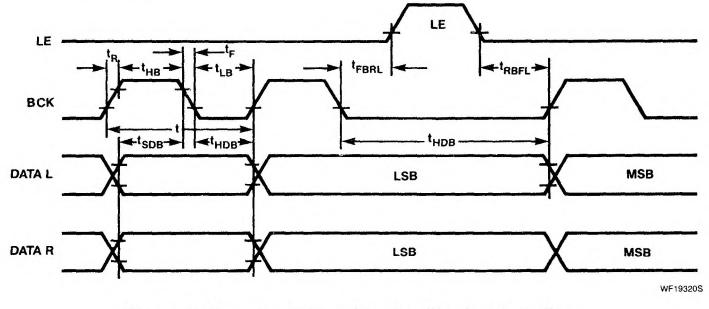


Figure 2. Format of Input Signals; Simultaneous Data