

LOW-NOISE TV VERTICAL DEFLECTION SYSTEM

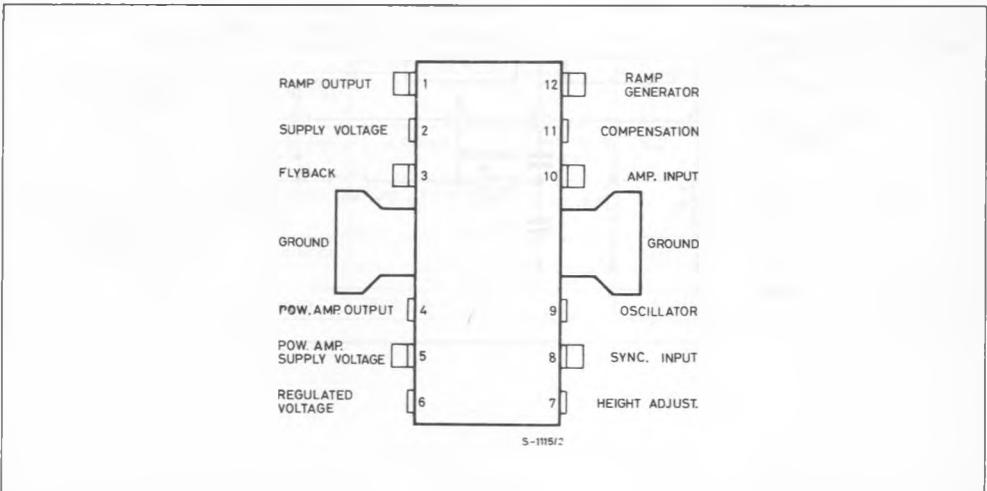
- COMPLETE VERTICAL DEFLECTION SYSTEM
- LOW NOISE
- SUITABLE FOR HIGH DEFINITION MONITORS

DESCRIPTION

The TDA 1170N is a monolithic integrated circuit in a 12-lead quad in-line plastic package. It is intended for use in black and white and colour TV receivers. Low-noise makes this device particularly suitable for use in monitors. The functions incorporated are : synchronization circuit, oscillator and ramp generator, high power gain amplifier, flyback generator, voltage regulator.



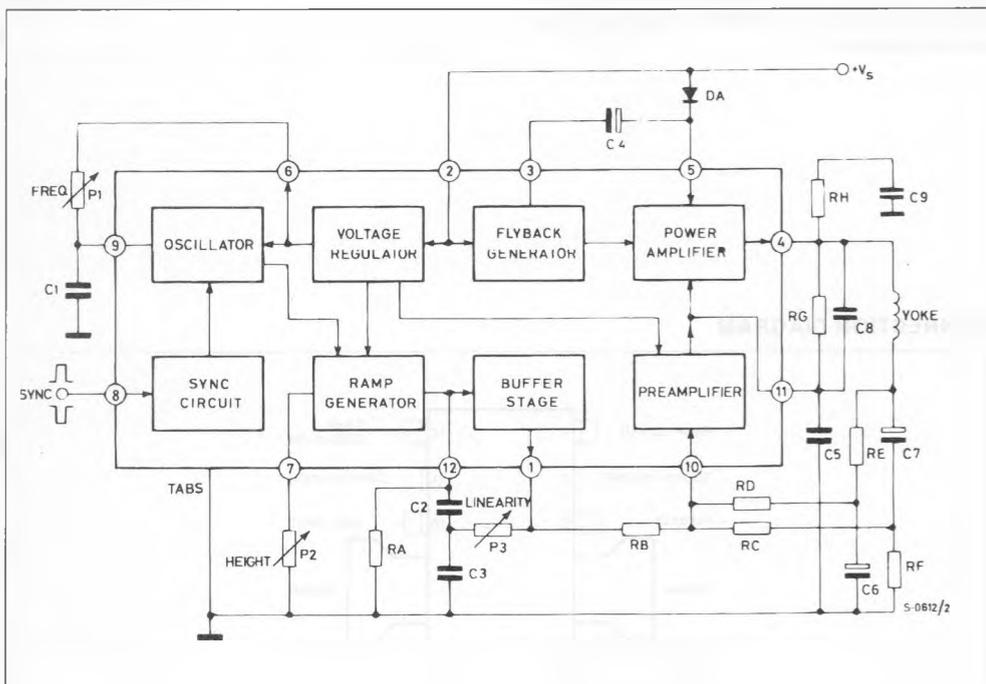
CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage at Pin 2	35	V
V_4, V_5	Flyback Peak Voltage	60	V
V_{10}	Power Amplifier Input Voltage	{ + 10 - 0.5	V
I_o	Output Peak Current (non repetitive) at $t = 2$ msec	2	A
I_o	output Peak Current at $f = 50$ Hz $t \leq 10$ μ sec	2.5	A
I_o	Output Peak Current at $f = 50$ Hz $t > 10$ μ sec	1.5	A
I_3	pin 3 DC Current at $V_4 < V_2$	100	mA
I_3	Pin 3 Peak to Peak Flyback Current for $f = 50$ Hz, $t_{fly} \leq 1.5$ msec	1.8	A
I_8	Pin 8 Current	± 20	mA
P_{Tot}	Power Dissipation : at $T_{ab} = 90$ °C	5	W
	at $T_{amb} = 80$ °C (free air)	1	W
T_{stg}, T_j	Storage and Junction Temperature	- 40 to 150	°C

BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j-tab}$	Thermal Resistance Junction-tab	Max	12	$^{\circ}\text{C}/\text{W}$
$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	Max	70	$^{\circ}\text{C}/\text{W}(^{\circ})$

(*) Obtained with tabs soldered to printed circuit with minimized copper area.

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, $V_S = 35\text{ V}$, $T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_2	Pin 2 Quiescent Current	$I_3 = 0$		7	14	mA	1b
I_5	Pin 5 Quiescent Current	$I_4 = 0$		8	17	mA	1b
$-I_9$	Oscillator Bias Current	$V_9 = 1\text{ V}$		0.1	1	μA	1a
$-I_{10}$	Amplifier Input Bias Current	$V_{10} = 1\text{ V}$		1	10	μA	1b
$-I_{12}$	Ramp Generator Bias Current	$V_{12} = 0$		0.02	0.3	μA	1a
$-I_{12}$	Ramp Generator Current	$I_7 = 20\text{ }\mu\text{A}$ $V_{12} = 0$	18.5	20	21.5	μA	1b
$\frac{\Delta I_{12}}{I_{12}}$	Ramp Generator Non-linearity	$\Delta V_{12} = 0\text{ to }12\text{ V}$ $I_7 = 20\text{ }\mu\text{A}$		0.2	1	%	1b
V_S	Supply Voltage Range		10		35	V	
V1	Pin 1 Saturation Voltage to Ground	$I_1 = 1\text{ mA}$		1	1.4	V	
V3	Pin 3 Saturation Voltage to Ground	$I_3 = 10\text{ mA}$		300	450	mV	1a
V4	Quiescent output Voltage	$V_S = 10\text{ V}$ $R_2 = 1\text{ k}\Omega$	4.1	4.4	4.75	V	1a
		$V_S = 35\text{ V}$ $R_2 = 1\text{ k}\Omega$	8.3	8.8	9.45	V	1a
V4L	Output Saturation Voltage to Ground	$-I_4 = 0.1\text{ A}$		0.9	1.2	V	1c
		$-I_4 = 0.8\text{ A}$		1.9	2.3	V	1c
V4H	Output Saturation Voltage to Supply	$I_4 = 0.1\text{ A}$		1.4	2.1	V	1d
		$I_4 = 0.8\text{ A}$		2.8	3.2	V	1d
V6	Regulated Voltage at Pin 6		6.1	6.5	6.9	V	1b
V7	Regulated Voltage at Pin 7	$I_7 = 20\text{ }\mu\text{A}$	6.2	6.6	7	V	1b
$\frac{\Delta V_6}{\Delta V_S}, \frac{\Delta V_7}{\Delta V_S}$	Regulated Voltage Drift with Supply Voltage	$\Delta V_S = 10\text{ to }35\text{ V}$		1		mV/V	1b
V10	Amplifier Input Reference Voltage		2.07	2.2	2.3	V	
R8	pin 8 Input Resistance	$V_8 \leq 0.4\text{ V}$	1			$\text{M}\Omega$	1a

Figure 1 : DC Test Circuits.

Figure 1a.

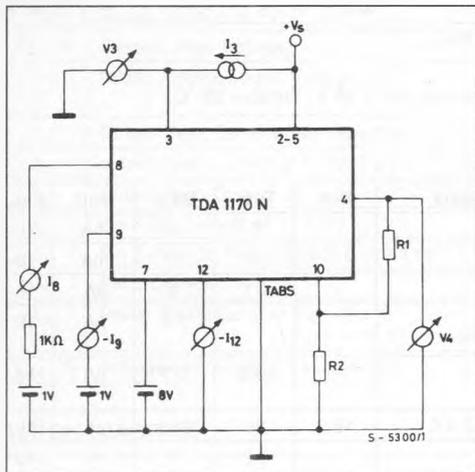


Figure 1b.

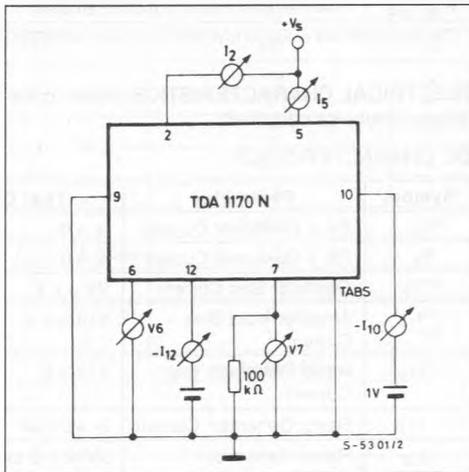


Figure 1c.

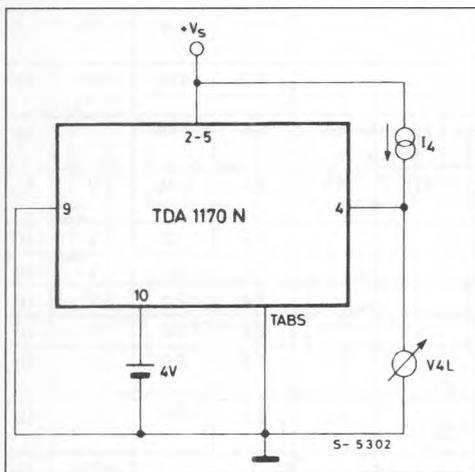


Figure 1d.

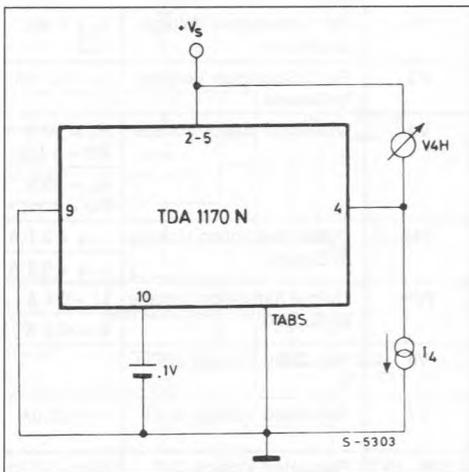


Figure 3 : Typical Application Circuit for Small Screen 90" TVC Set ($R_Y = 15 \Omega$, $L_Y = 30 \text{ mH}$, $I_Y = 0.82 \text{ App}$).

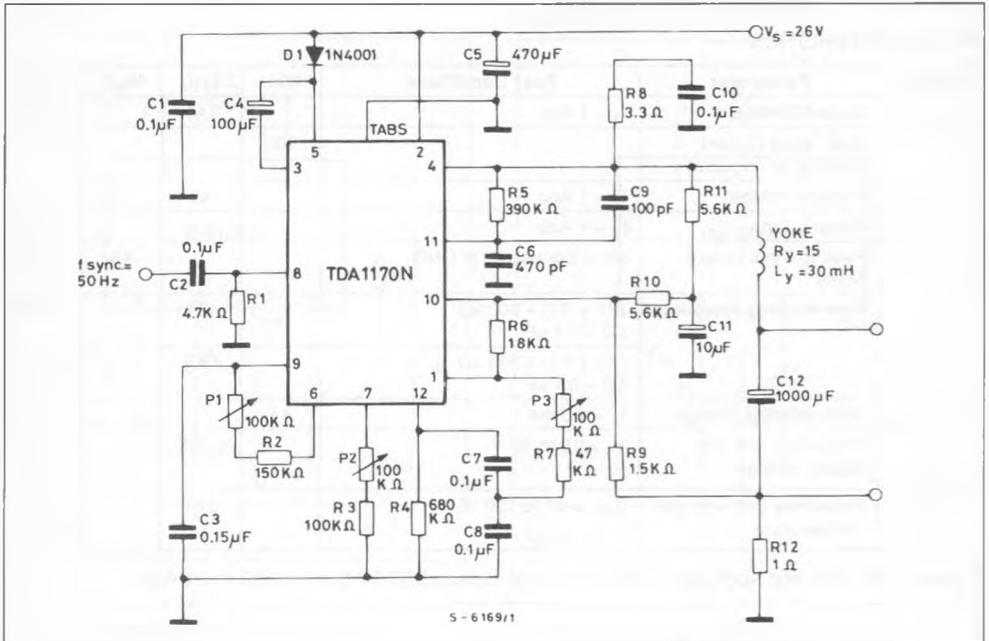
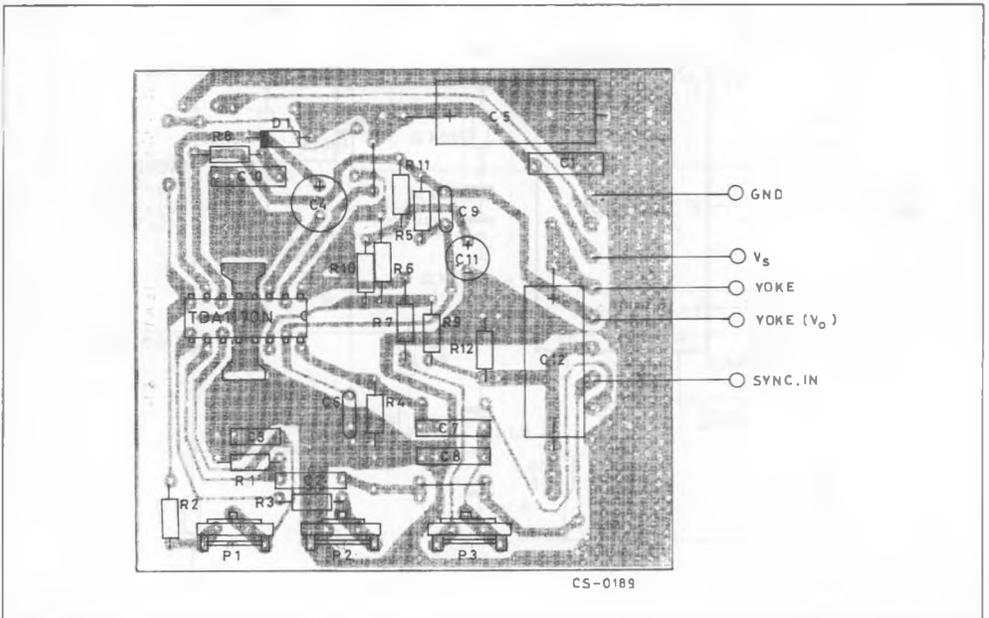


Figure 4 : P.C. Board and Components Layout of the Circuit of fig. 3 (1:1 scale).



MOUNTING INSTRUCTION

During soldering the tab temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

The junction to ambient thermal resistance can be reduced by soldering the tabs to a suitable copper

Figure 5 : Exmple of P.C. Board Copper Area Used as Heatsink.

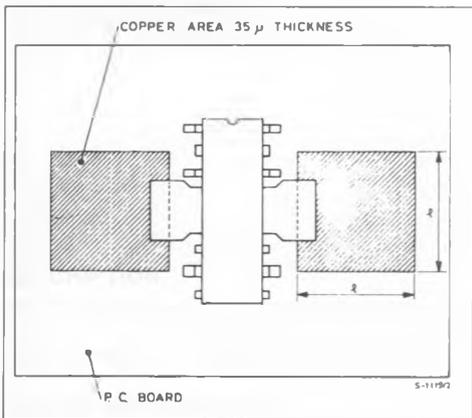
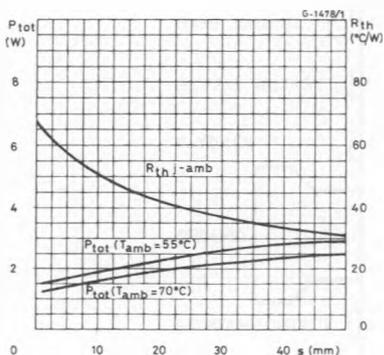


Figure 7 : Maximum Power Dissipation and Junctional Ambient Thermal Resistance vs. "e".



area of the printed circuit board (fig. 5) or to an external heatsink (fig. 6).

The diagram of fig. 7 shows the maximum dissippable power P_{tot} and the $R_{th\ j-amb}$ as a function of the side "e" of two equal square copper areas having a thickness of 35 μ (1.4 mil).

Figure 6 : Example of External heatsink.

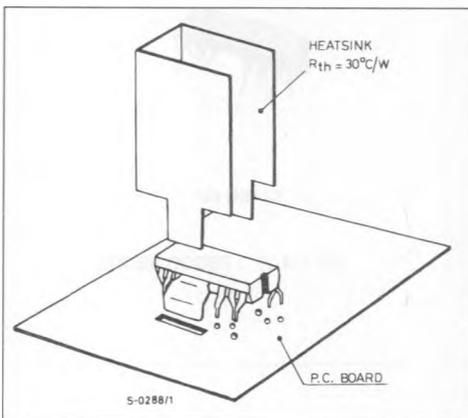


Figure 8 : Maximum Allowable Power Dissipation Versus Ambient Temperature.

