TCI6634K2K

Multicore DSP KeyStone II System-on-Chip (SoC)

Data Manual

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1 TCI6634K2K Features and Description

1.1 Features

- Eight TMS320C66x™ DSP Core Subsystems (C66x CorePacs), Each With
  - 1.0 GHz or 1.2 GHz C66x Fixed/Floating-Point DSP Core
    - 38.4 GMacs/Core for Fixed Point @ 1.2 GHz
    - 19.2 GFlops/Core for Floating Point @ 1.2 GHz
  - Memory
    - 32K Byte L1P Per CorePac
    - 32K Byte L1D Per CorePac
    - 1024K Byte Local L2 Per CorePac
- Multicore Shared Memory Controller (MSMC)
  - 6 MB MSM SRAM Memory Shared by Eight DSP CorePacs
  - Memory Protection Unit for Both MSM SRAM and DDR3_EMIF
- Hardware Coprocessors
  - Four Turbo Decoders
    - Supports WCDMA/HSPA/HSPA+/TD-SCDMA, LTE, LTE-A and WiMAX
    - Supports Up To 282 Mbps for LTE at Block Size 6144, 8 Iterations and Up To 206 Mbps for WCDMA at Block Size 5114, 8 Iterations
    - Low DSP Overhead – HW Interleaver Table Generation and CRC Check
  - Eight Viterbi Decoders
    - Supports Up To 50 Mbps (Length 9, Rate 1/3, Block Size 2500)
  - Four WCDMA Receive Acceleration Coprocessors
    - Supports Up To 8192 Correlators
  - WCDMA Transmit Acceleration Coprocessor
    - Supports Up To 2304 Spreaders
  - Six Fast Fourier Transform Coprocessors
    - Support Up To 2400 Mscps at FFT Size 1024
  - Bit Rate Coprocessor
    - WCDMA/HSPA+, TD-SCDMA, LTE, LTE-A and WiMAX Uplink and Downlink Bit Processing
    - Includes Encoding, Rate Matching/Dematching, Segmentation, Multiplexing, and More
    - Supports Up To DL 1525 Mbps and UL 1030 Mbsp for LTE and DL 784 Mbps and UL 216 Mbsp for WCDMA/TD-SCDMA
- Multicore Navigator
  - 16k Multi-Purpose Hardware Queues with Queue Manager
  - Packet-Based DMA for Zero-Overhead Transfers
- Network Coprocessor
  - Packet Accelerator Enables Support for
    - Transport Plane IPsec, GTP-U, SCTP, PDCP
    - L2 User Plane PDCP (RoHC, Air Ciphering)
    - 1 Gbps Wire Speed Throughput at 1.5 MPackets Per Second
  - Security Accelerator Engine Enables Support for
    - IPSec, SRTP, 3GPP and WiMAX Air Interface, and SSL/TLS Security
    - ECB, CBC, CTR, F8, A5/3, CCM, GCM, HMAC, CMAC, GMAC, AES, DES, 3DES, Kasumi, SNOW 3G, SHA-1, SHA-2 (256-bit Hash), MD5
    - Up To 6.4 Gbps IPSec and 3 Gbps Air Ciphering
  - Ethernet Subsystem
    - Five SGMII Port Switch
- Sixteen Rake/Search Accelerators (RSA) for
  - Chip Rate Processing for WCDMA Rel'99, HSDPA, and HSDPA+
  - Reed-Muller Decoding
- Peripherals
  - Six-Lane SerDes-Based Antenna Interface (AIF2)
    - Operating at Up To 6.144 Gbps
    - Compliant with OBSAI RP3 and CPRI Standards for 3G / 4G (WCDMA, LTE TDD, LTE FDD, TD-SCDMA, and WiMAX)
  - Four Lanes of SRIO 2.1
    - 5 Gbps Operation Per Lane
    - Supports Direct I/O, Message Passing
  - Two Lanes PCIe Gen2
    - Supports Up To 5 GBaud
  - Two HyperLinks
    - Supports Connections to Other KeyStone Architecture Devices Providing Resource Scalability
    - Supports Up To 50 GBaud
  - 10-Gigabit Ethernet (10-GbE) Switch Subsystem
    - Two XGMII Ports
    - IEEE1588 Support
  - Five Enhanced Direct Memory Access (EDMA) Modules
  - Two 72-Bit DDR3 Interfaces with Speeds Up To 1600 MHz
  - EMIF16 Interface
  - USB 3.0
  - USIM Interface
  - Two UART Interfaces
  - Three I^2C Interfaces
  - 32 GPIO Pins
  - Three SPI Interfaces
  - Semaphore Module
  - Twenty 64-Bit Timers
  - Four On-Chip PLLs
- Commercial Case Temperature:
  - 0°C to 100°C

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- **Extended Case Temperature:**
  - **- 40°C to 100°C**

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1.2 KeyStone Architecture

TI's KeyStone Multicore Architecture provides a high performance structure for integrating RISC and DSP cores with application-specific coprocessors and I/O. KeyStone is the first of its kind in that it provides adequate internal bandwidth for nonblocking access to all processing cores, peripherals, coprocessors, and I/O. This is achieved with four main hardware elements: Multicore Navigator, TeraNet, Multicore Shared Memory Controller, and HyperLink.

Multicore Navigator is an innovative packet-based manager that controls 16k queues. When tasks are allocated to the queues, Multicore Navigator provides hardware-accelerated dispatch that directs tasks to the appropriate available hardware. The packet-based system on a chip (SoC) uses the 2-Tbps capacity of the TeraNet switched central resource to move packets. The Multicore Shared Memory Controller enables processing cores to access shared memory directly without drawing from the TeraNet's capacity, so packet movement cannot be blocked by memory access.

HyperLink provides a 50-GBaud chip-level interconnect that allows SoCs to work in tandem. Its low-protocol overhead and high throughput make HyperLink an ideal interface for chip-to-chip interconnections. Working with Multicore Navigator, HyperLink dispatches tasks to tandem devices transparently and executes tasks as if they are running on local resources.

1.3 Device Description

The TCI6634K2K Communications Infrastructure KeyStone SoC is a member of the C66x family based on TI's new KeyStone II Multicore SoC Architecture designed specifically for high performance wireless infrastructure applications. The TCI6634K2K provides a very high performance macro basestation platform for developing all wireless standards including WCDMA/HSPA/HSPA+, TD-SCDMA, GSM, TDD-LTE, FDD-LTE, and WiMAX.

TI's KeyStone II Architecture provides a programmable platform integrating various subsystems (C66x CorePacs, IP network, radio layers 1, 2, and 3, and transport processing) and uses a queue-based communication system that allows the SoC resources to operate efficiently and seamlessly. This unique SoC architecture also includes a TeraNet switch that enables the wide mix of system elements, from programmable cores to dedicated coprocessors and high-speed IO, to each operate at maximum efficiency with no blocking or stalling.

TI's new C66x core launches a new era of DSP technology by combining fixed-point and floating-point computational capability in the processor without sacrificing speed, size, or power consumption. The raw computational performance is an industry-leading 38.4 GMACS/core and 19.2 Gflops/core (@ 1.2 GHz operating frequency). The C66x is also 100% backward compatible with software for C64x+ devices. The C66x CorePac incorporates 90 new instructions targeted for floating point (FPi) and vector math oriented (VPi) processing. These enhancements yield tremendous performance improvements in multi-antenna 4.8G signal processing for algorithms like MIMO and beamforming.

The TCI6634K2K contains many wireless basestation coprocessors to offload the bulk of the processing demands of layer 1 and layer 2 basestation processing. This keeps the cores free for receiver algorithms and other differentiating functions. The SoC contains multiple copies of key coprocessors such as the FFTC and TCP3d. A key coprocessor for enabling high data rates is the Bit Rate Coprocessor (BCP), which handles the entire downlink bit-processing chain and much of the receive bit processing. The architectural elements of the SoC (Multicore Navigator) ensure that all the bits are processed without any CPU intervention or overhead, allowing the system to make optimal use of its resources.

TI's scalable multicore SoC architecture solutions provide developers with a range of software-compatible and hardware-compatible devices to minimize development time and maximize reuse across all basestation platforms from Femto to Macro.

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The TCI6634K2K device has a complete set of development tools that includes: a C compiler, an assembly optimizer to simplify programming and scheduling, and a Windows debugger interface for visibility into source code execution.

1.4 Enhancements in KeyStone II

The KeyStone II architecture provides many major enhancements over the previous KeyStone I generation of devices. The number of DSP cores and FFTC accelerators has been doubled for 2× improvement in Layer 1 processing. The external memory bandwidth has been doubled with the integration of dual DDR3 1600 EMIFs. MSMC internal memory bandwidth is quadrupled with MSMC V2 architecture improvements. Multicore Navigator supports 2× the number of queues, descriptors and packet DMA, 4× the number of micro RISC engines and a significant increase in the number of push/pops per second, compared to the previous generation. The new peripherals that have been added include the USB 2.0/3.0 controllerand Asynchronous EMIF controller for NAND/NOR memory access. The 2-port Gigabit Ethernet switch in KeyStone I has been replaced with a 4-port Gigabit Ethernet switch in KeyStone II. Time synchronization support has been enhanced to reduce software workload and support additional standards like IEEE1588 Annex D/E and SyncE. The number of GPIOs and serial interface peripherals like I2C and SPI have been increased to enable more board level control functionality.

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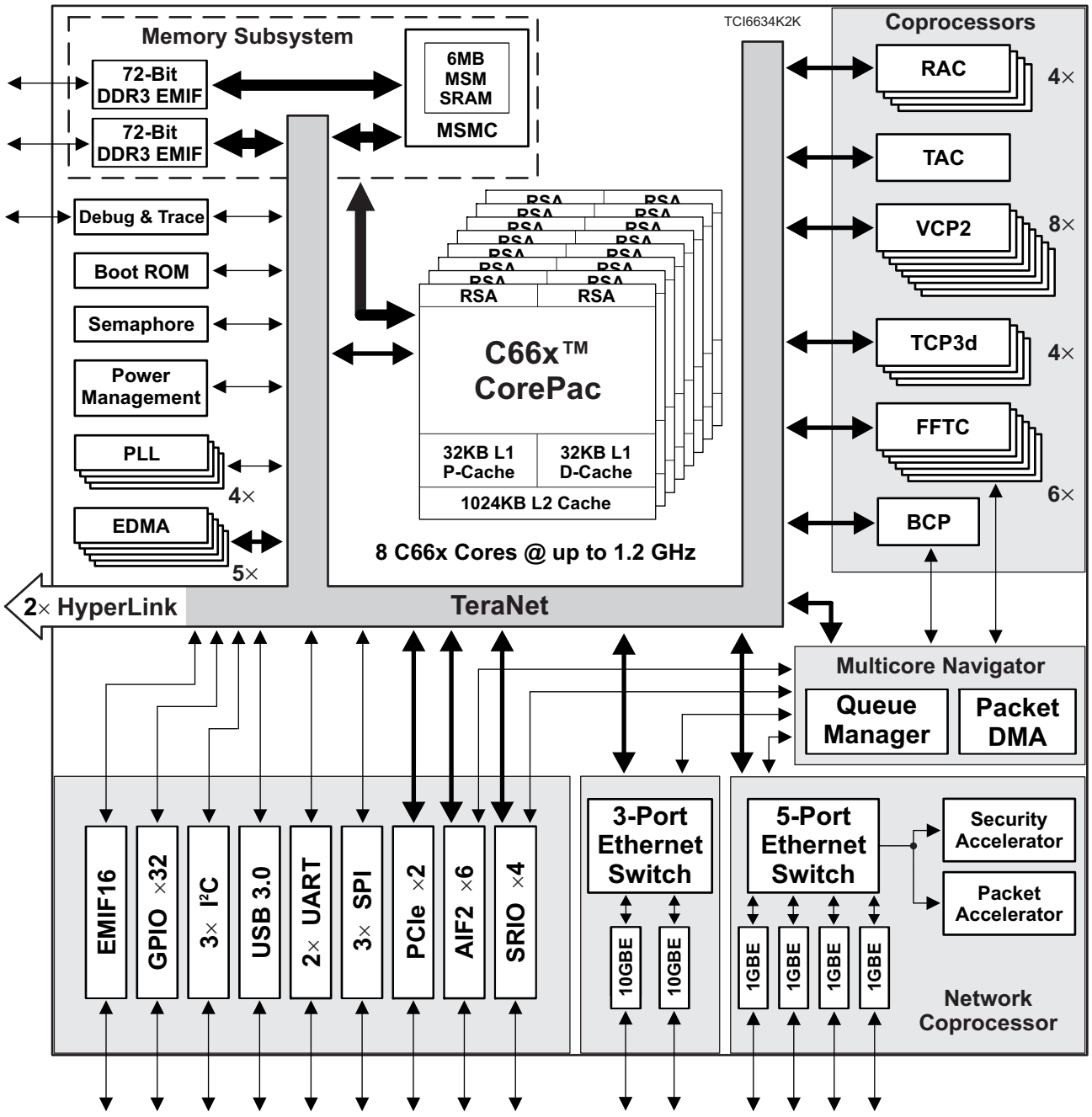
1.5 Functional Block Diagram

Figure 1-1 shows the functional block diagram of the device.

Figure 1-1 Functional Block Diagram



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1.6 Device Characteristics

The following table provides an overview of the TCI6634K2K SoC. The table shows the significant features of the device, including the capacity of on-chip RAM, the peripherals, the CPU frequency, and the package type with pin count.

Table 1-1 Characteristics of the TCI6634K2K Processor (Part 1 of 2)

HARDWARE FEATURES		TCI6634K2K
Peripherals	DDR3 memory controller (72-bit bus width) [1.5-V I/O] (clock source = DDRREFCLKN|P)	2
	16-bit ASYNC EMIF	1
	EDMA3 (64 independent channels) [CPU/3 clock rate]	5
	High-speed 1×/2×/4× Serial RapidIO port (4 lanes)	1
	HyperLink	2
	Second generation Antenna Interface (AIF2)	1
	I^2C	3
	SPI	3
	PCIe (2 lanes)	1
	USB 3.0	1
	USIM (1)	1
	UART	2
	10/100/1000/10000 Ethernet	2 (external ports)
	10/100/1000 Ethernet	4 (external ports)
	Management Data Input/Output (MDIO)	1
	64-bit timers (configurable) (internal clock source = CPU/6 clock frequency)	Twenty 64-bit ***or*** Forty 32-bit
	General-Purpose Input/Output port (GPIO)	32
Encoder/Decoder Coprocessors	VCP2 (clock source = CPU/3 clock frequency)	8
	TCP3d (clock source = CPU/2 clock frequency)	4
	FFTC (clock source = CPU/3 clock frequency)	6
	BCP (clock source = CPU/3 clock frequency)	1
Accelerators	Receive Accelerator (RAC)	4
	Transmit Accelerator (TAC)	1
	Rake/Search Accelerator (RSA)	16
	Packet Accelerator	1
	Security Accelerator (2)	1
On-Chip Memory Organization	L1 program memory controller (C66x)	256KB
	L1 data memory controller (C66x)	256KB
	Shared L2 Cache (C66x)	8192KB
	L3 ROM (C66x)	128KB
	MSMC	6MB
C66x CorePac Revision ID	CorePac Revision ID Register (address location: 0x01812000)	TBD
JTAG BSDL_ID	JTAGID Register (address location: 0x02620018)	TBD
Frequency	MHz	1200 (1.2 GHz) 1000 (1.0 GHz)
Voltage	Core (V)	SmartReflex variable supply
	I/O (V)	.85 V, 1.0 V, 1.35 V, 1.5 V, 1.8 V and 3.3 V
BGA Package	40 mm × 40 mm	1517-Pin Flip-Chip Plastic BGA (AAW)

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Table 1-1 Characteristics of the TCI6634K2K Processor (Part 2 of 2)

HARDWARE FEATURES		TCI6634K2K
Process Technology	µm	0.028 µm
Product Status (3)	Product Preview (PP), Advance Information (AI), or Production Data (PD)	PP
End of Table 1-1		

1 The USIM is implemented for support of secure devices only. Contact your local technical sales representative for further details.

2 The Security Accelerator function is subject to export control and will be enabled *only* for approved device shipments.

3 PRODUCT PREVIEW information applies to products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

1.7 C66x DSP CorePac

The C66x DSP CorePac extends the performance of the C64x+ and C674x CPUs through enhancements and new features. Many of the new features target increased performance for vector processing. The C64x+ and C674x DSPs support 2-way SIMD operations for 16-bit data and 4-way SIMD operations for 8-bit data. On the C66x DSP, the vector processing capability is improved by extending the width of the SIMD instructions. C66x DSPs can execute instructions that operate on 128-bit vectors. The C66x CPU also supports SIMD for floating-point operations. Improved vector processing capability (each instruction can process multiple data in parallel) combined with the natural instruction level parallelism of C6000 architecture (e.g., execution of up to 8 instructions per cycle) results in a very high level of parallelism that can be exploited by DSP programmers through the use of TI's optimized C/C++ compiler.

Each C66x DSP CorePac has two Rake and Search Accelerators (RSA) integrated on-chip. The tightly coupled accelerator RSA can be used for:

- Chip rate spreading of WCDMA Rel'99, CDMA2000, HSDPA, and HSDPA+
- Chip rate despreading and correlation of WCDMA Rel'99, HSDPA, and HSDPA+ (e.g., Rake receiver, preamble detection)
- Reed-Muller decoding

For more details on the C66x CPU and its enhancements over the C64x+ and C674x architectures, see the following documents (1.9 "Related Documentation from Texas Instruments" on page 22):

- *C66x CPU and Instruction Set Reference Guide*
- *C66x DSP Cache User Guide*
- *C66x CorePac User Guide*

1.8 Development Tools

1.8.1 Development Support

In case the customer would like to develop their own features and software on the TCI6634 device, TI offers an extensive line of development tools for the TMS320C6000™ DSP platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

The following products support development of KeyStone devices:

- **Software Development Tools:**
  - Code Composer Studio™ Integrated Development Environment (IDE), including Editor C/C++/Assembly Code Generation, and Debug plus additional development tools
  - Scalable, Real-Time Foundation Software (DSP/BIOS™), which provides the basic run-time target software needed to support any DSP application

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- **Hardware Development Tools:**
  - Extended Development System (XDS™) Emulator (supports multiprocessor system debug)
  - EVM (Evaluation Module)

1.8.2 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all devices and support tools. Each family member has one of two prefixes: X or [blank]. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices/tools.

Device development evolutionary flow:

- **X:** Experimental device that is not necessarily representative of the final device's electrical specifications
- **[Blank]:** Fully qualified production device

Support tool development evolutionary flow:

- **X:** Development-support product that has not yet completed Texas Instruments internal qualification testing.
- **[Blank]:** Fully qualified development-support product

Experimental (X) and fully qualified [Blank] devices and development-support tools are shipped with the following disclaimer:

Developmental product is intended for internal evaluation purposes.

Fully qualified and production devices and development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that experimental devices (X) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, AAW), the temperature range (for example, blank is the default case temperature range), and the device speed range, in Megahertz (for example, blank is 1000 MHz [1 GHz]).

For device part numbers and further ordering information for TCI6634in the AAW package type, see the TI website www.ti.com or contact your TI sales representative.

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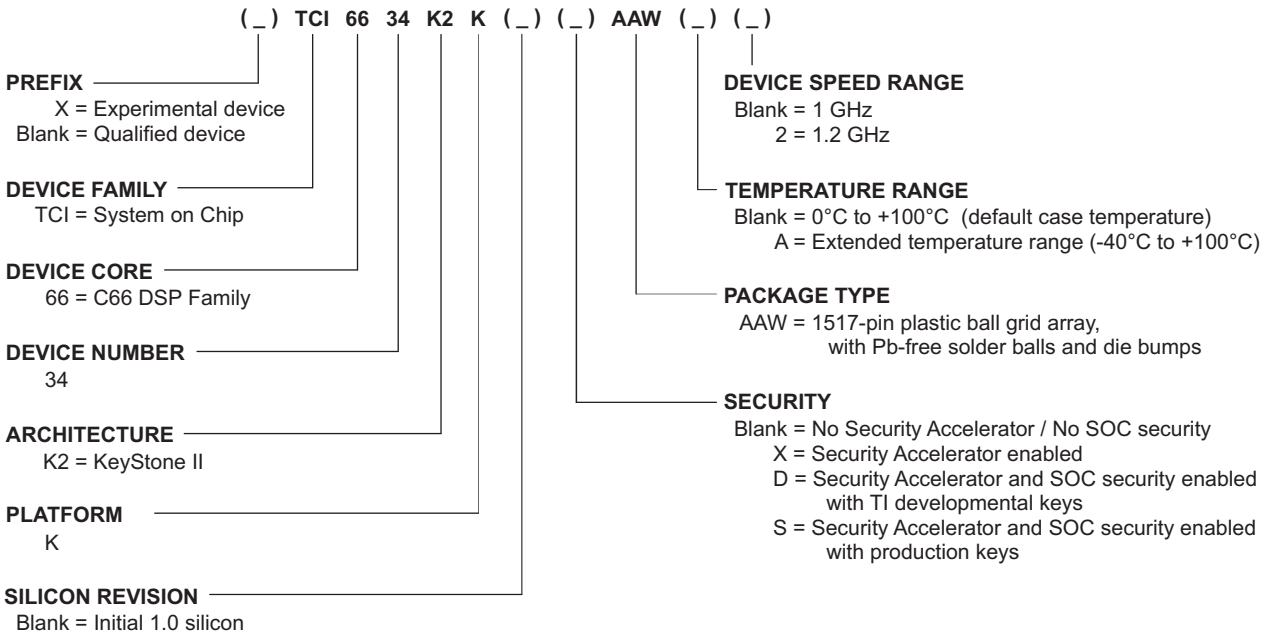
1.8.3 Device Nomenclature

Figure 1-2 provides a legend for reading the complete device name for any C66x+™ DSP generation member.

Figure 1-2 C66x™ DSP Device Nomenclature (including the TCI6634K2K DSP)



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1.9 Related Documentation from Texas Instruments

These documents describe the TCI6634K2K Multicore DSP KeyStone II System-on-Chip (SoC). Copies of these documents are available on the Internet at www.ti.com.

64-bit Timer (Timer 64) for KeyStone Devices User Guide	SPRUGV5
Antenna Interface 2 (AIF2) for KeyStone Devices User Guide	SPRUGV7
AIF1-to-AIF2 Antenna Interface Migration Guide for KeyStone Devices	SPRABH8
Bit Coprocessor (BCP) for KeyStone Devices User Guide	SPRUGZ1
BCP-TCP3d for KeyStone Devices	SPRABH6
Bootloader for the C66x DSP User Guide	SPRUGY5
C66x CorePac User Guide	SPRUGW0
C66x CPU and Instruction Set Reference Guide	SPRUGH7
C66x DSP Cache User Guide	SPRUGY8
Chip Interrupt Controller (CIC) for KeyStone Devices User Guide	SPRUGW4
Connecting AIF2 with FFTC	SPRABF3
Debug and Trace for KeyStone Devices User Guide	SPRUGZ2
DDR3 Memory Controller for KeyStone Devices User Guide	SPRUGV8
DSP Power Consumption Summary for KeyStone Devices	SPRABL4
External Memory Interface (EMIF16) for KeyStone Devices User Guide	SPRUGZ3
Emulation and Trace Headers Technical Reference	SPRU655
Enhanced Direct Memory Access 3 (EDMA3) for KeyStone Devices User Guide	SPRUGS5
Fast Fourier Transform Coprocessor (FFTC) for KeyStone Devices User Guide	SPRUGS2
General Purpose AIF2 Traffic for KeyStone Devices	SPRABH3
General Purpose Input/Output (GPIO) for KeyStone Devices User Guide	SPRUGV1
Gigabit Ethernet (GbE) Switch Subsystem (1 GB) for KeyStone Devices User Guide	SPRUGV9
Gigabit Ethernet (GbE) Switch Subsystem (10 GB) for KeyStone II Devices User Guide	SPRUHJ5
HyperLink for KeyStone Devices User Guide	SPRUGW8
Inter Integrated Circuit (I^2C) for KeyStone Devices User Guide	SPRUGV3
Interrupt Controller (INTC) for KeyStone Devices User Guide	SPRUGW4
Memory Protection Unit (MPU) for KeyStone Devices User Guide	SPRUGW5
Multicore Navigator for KeyStone Devices User Guide	SPRUGR9
Multicore Shared Memory Controller (MSMC) for KeyStone II Devices User Guide	SPRUHJ6
Multicore Programming Guide	SPRAB27
Network Coprocessor (NETCP) for KeyStone Devices User Guide	SPRUGZ6
Optimizing Application Software on KeyStone Devices	SPRABG8
Optimizing Loops on the C66x DSP	SPRABG7
Packet Accelerator (PA) for KeyStone Devices User Guide	SPRUGS4
Peripheral Component Interconnect Express (PCIe) for KeyStone Devices User Guide	SPRUGS6
Phase Locked Loop (PLL) Controller for KeyStone Devices User Guide	SPRUGV2
Power Sleep Controller (PSC) for KeyStone Devices User Guide	SPRUGV4
Rake Search Accelerator (RSA) for KeyStone Devices User Guide	SPRUGY7
Receive Accelerator Coprocessor (RAC) for KeyStone Devices User Guide	SPRUGY9
Security Accelerator (SA) for KeyStone Devices User Guide	SPRUGY6
Semaphore2 Hardware Module for KeyStone Devices User Guide	SPRUGS3
Serial Peripheral Interface (SPI) for KeyStone Devices User Guide	SPRUGP2
Serial RapidIO (SRIO) for KeyStone Devices User Guide	SPRUGW1

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Transmit Accelerator Coprocessor (TAC) for KeyStone Devices User Guide	SPRUGZ4
Turbo Decoder Coprocessor 3 (TCP3d) for KeyStone Devices User Guide	SPRUGS0
Turbo Encoder Coprocessor 3 (TCP3e) for KeyStone Devices User Guide	SPRUGS1
Universal Serial Bus 3 (USB3) for KeyStone II Devices User Guide	SPRUHJ7
Universal Asynchronous Receiver/Transmitter (UART) for KeyStone Devices User Guide	SPRUGP1
Viterbi Coprocessor (VCP2) for KeyStone Devices User Guide	SPRUGV6

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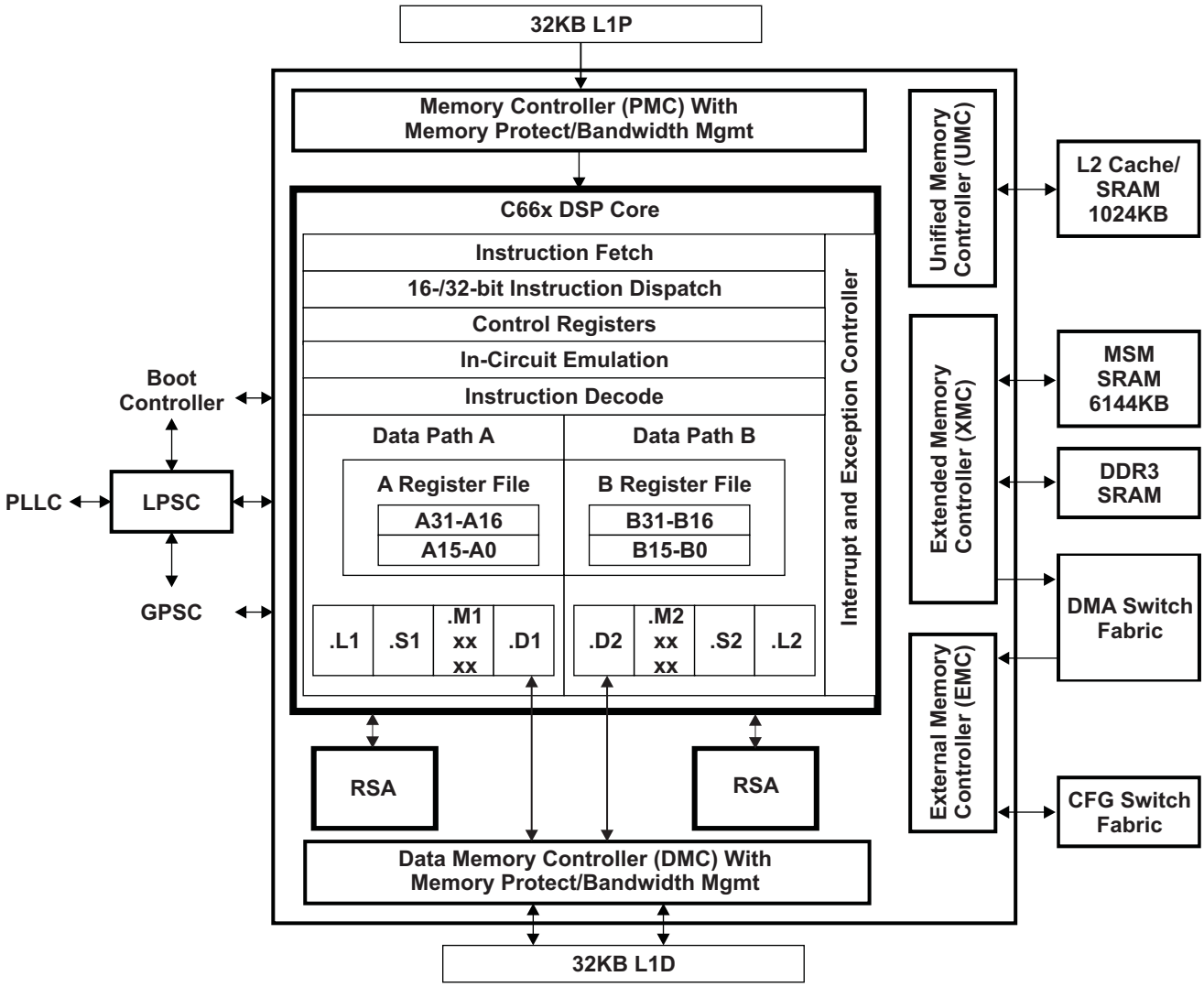
2 C66x CorePac

The C66x CorePac consists of several components:

- Level-one and level-two memories (L1P, L1D, L2)
- Data Trace Formatter (DTF)
- Embedded Trace Buffer (ETB)
- Interrupt controller
- Power-down controller
- External memory controller
- Extended memory controller
- A dedicated local power/sleep controller (LPSC)

The C66x CorePac also provides support for big and little endianness, memory protection, and bandwidth management (for resources local to the CorePac). Figure 2-1 shows a block diagram of the C66x CorePac.

Figure 2-1 C66x CorePac Block Diagram



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For more detailed information on the C66x CorePac in the TCI6634K2K device, see the *C66x CorePac User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

2.1 Memory Architecture

Each C66x CorePac of the TCI6634K2K device contains a 1024KB level-2 memory (L2), a 32KB level-1 program memory (L1P), and a 32KB level-1 data memory (L1D). The device also contain a 6144KB multicore shared memory (MSM). All memory on the TCI6634 has a unique location in the memory map (see the Memory, Interrupts, and EDMA chapter).

After device reset, L1P and L1D cache are configured as all cache, by default. The L1P and L1D cache can be reconfigured via software through the L1PMODE field of the L1P Configuration Register (L1PMODE) and the L1DMODE field of the L1D Configuration Register (L1DCFG) of the C66x CorePac. L1D is a two-way set-associative cache, while L1P is a direct-mapped cache.

The on-chip bootloader changes the reset configuration for L1P and L1D. For more information, see the *Bootloader for the C66x DSP User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

For more information on the operation L1 and L2 caches, see the *C66x DSP Cache User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

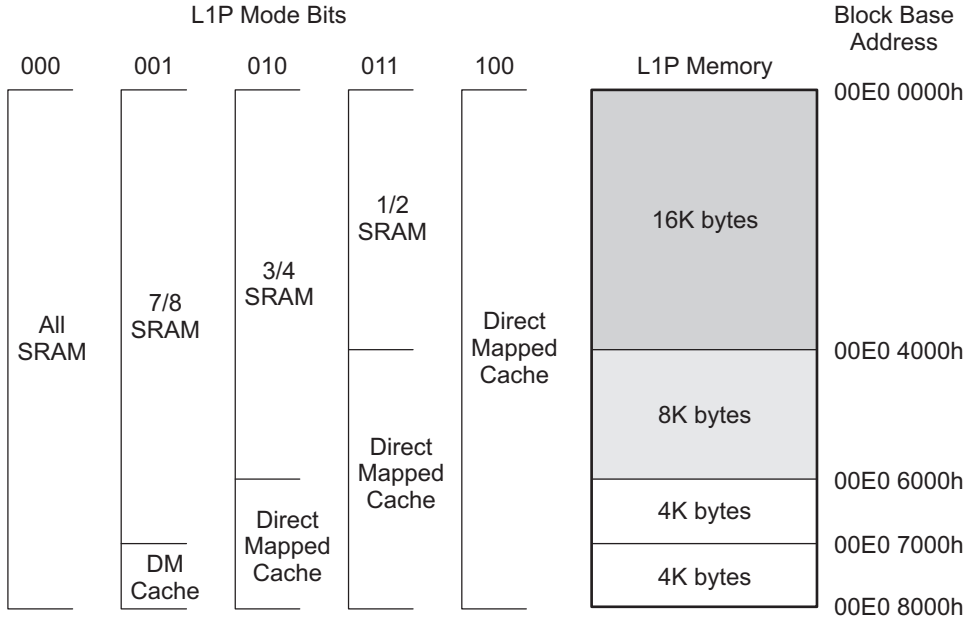
2.1.1 L1P Memory

The L1P memory configuration for the TCI6634K2K device is as follows:

- Region 0 size is 0K bytes (disabled)
- Region 1 size is 32K bytes with no wait states

Figure 2-2 shows the available SRAM/cache configurations for L1P.

Figure 2-2 L1P Memory Configurations



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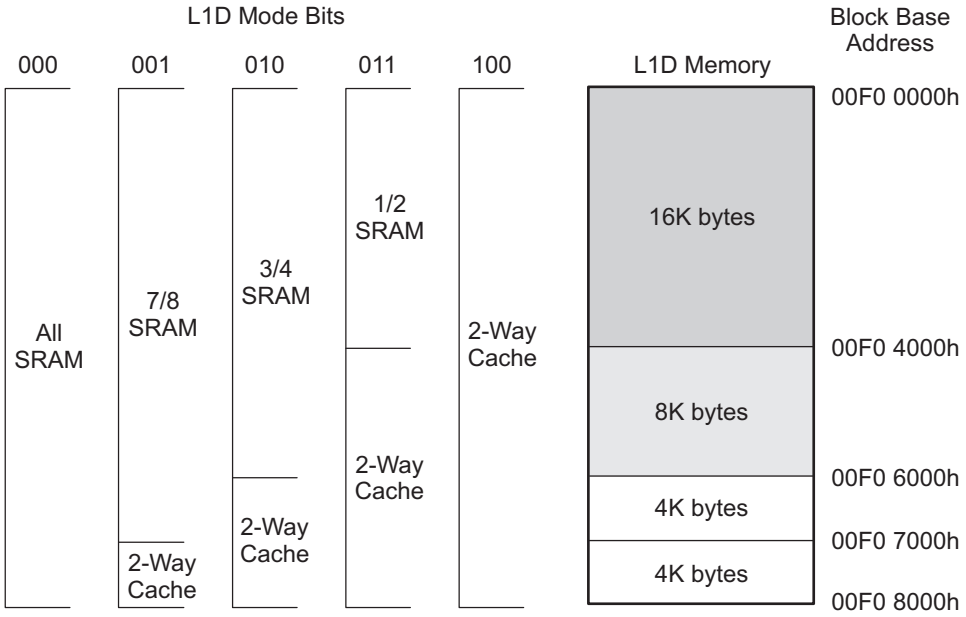
2.1.2 L1D Memory

The L1D memory configuration for the TCI6634K2K device is as follows:

- Region 0 size is 0K bytes (disabled)
- Region 1 size is 32K bytes with no wait states

Figure 2-3 shows the available SRAM/cache configurations for L1D.

Figure 2-3 L1D Memory Configurations



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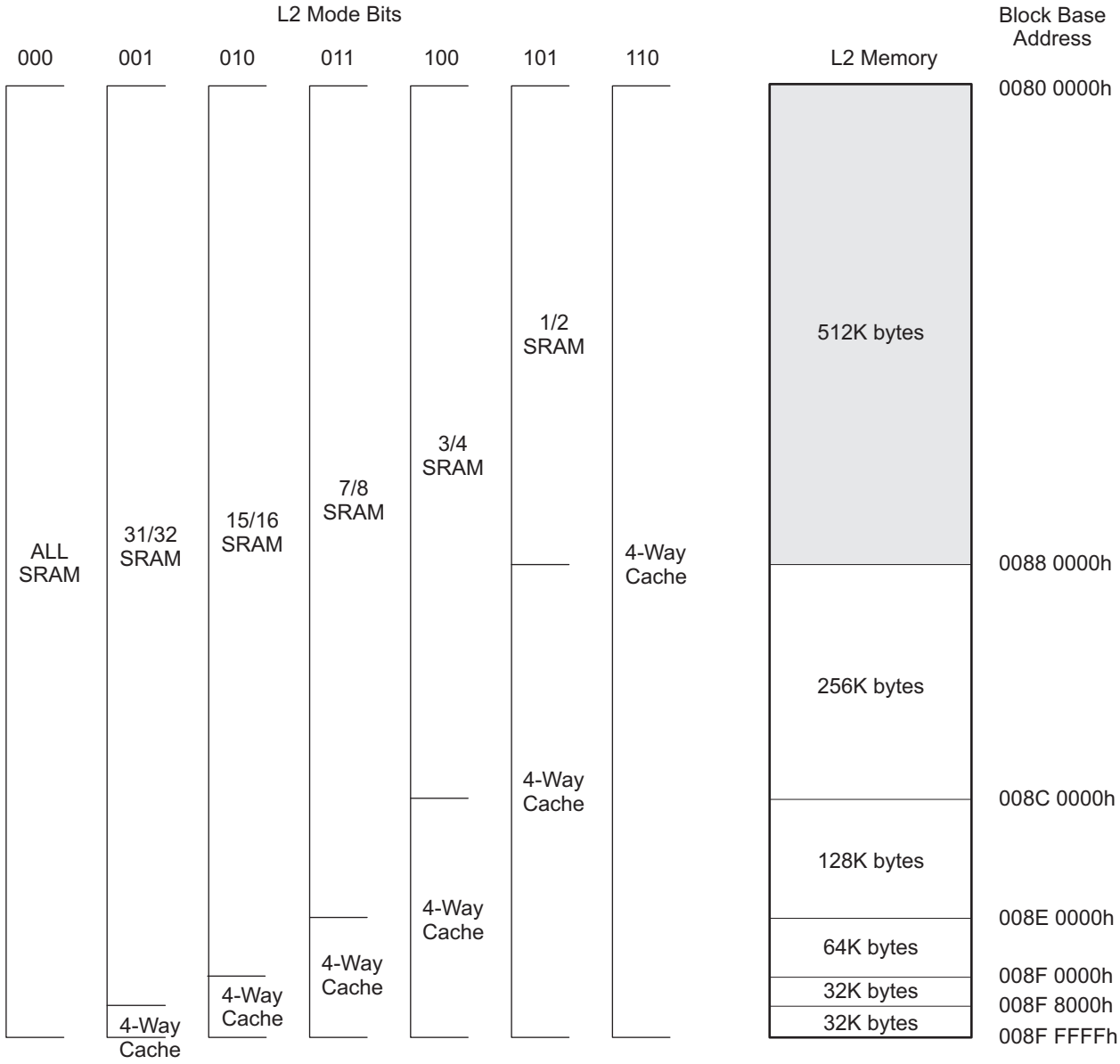
2.1.3 L2 Memory

The L2 memory configuration for the TCI6634K2K device is as follows:

- Total memory size is 8192KB
- Each CorePac contains 1024KB of memory
- Local starting address for each CorePac is 0080 0000h

L2 memory can be configured as all SRAM, all 4-way set-associative cache, or a mix of the two. The amount of L2 memory that is configured as cache is controlled through the L2MODE field of the L2 Configuration Register (L2CFG) of the C66x CorePac. Figure 2-4 shows the available SRAM/cache configurations for L2. By default, L2 is configured as all SRAM after device reset.

Figure 2-4 L2 Memory Configurations



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Global addresses that are accessible to all masters in the system are in all memory local to the processors. In addition, local memory can be accessed directly by the associated processor through aliased addresses, where the eight MSBs are masked to 0. The aliasing is handled within the CorePac and allows for common code to be run unmodified on multiple cores. For example, address location 0x10800000 is the global base address for CorePac0's L2 memory. CorePac0 can access this location by either using 0x10800000 or 0x00800000. Any other master on the device must use 0x10800000 only. Conversely, 0x00800000 can by used by any of the C66x CorePacs as their own L2 base addresses. For CorePac0, as mentioned, this is equivalent to 0x10800000, for CorePac1 this is equivalent to 0x11800000, and for CorePac2 this is equivalent to 0x12800000. Local addresses should be used only for shared code or data, allowing a single image to be included in memory. Any code/data targeted to a specific core, or a memory region allocated during run-time by a particular CorePac should always use the global address only.

2.1.4 Multicore Shared Memory SRAM

The MSM SRAM configuration for the TCI6634K2K device is as follows:

- Memory size of 6144KB
- Can be configured as shared L2 or shared L3 memory
- Allows extension of external addresses from 2GB up to 8GB
- Has built-in memory protection features

The MSM SRAM is always configured as all SRAM. When configured as a shared L2, its contents can be cached in L1P and L1D. When configured in shared L3 mode, it's contents can be cached in L2 also. For more details on external memory address extension and memory protection features, see the *Multicore Shared Memory Controller (MSMC) for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

2.1.5 L3 Memory

The L3 ROM on the device is 128KB. The ROM contains software used to boot the device. There is no requirement to block accesses from this portion to the ROM.

2.2 Memory Protection

Memory protection allows an operating system to define who or what is authorized to access L1D, L1P, and L2 memory. To accomplish this, the L1D, L1P, and L2 memories are divided into pages. There are 16 pages of L1P (2KB each), 16 pages of L1D (2KB each), and 32 pages of L2 (32KB each). The L1D, L1P, and L2 memory controllers in the C66x CorePac are equipped with a set of registers that specify the permissions for each memory page.

Each page may be assigned with fully orthogonal user and supervisor read, write, and execute permissions. In addition, a page may be marked as either (or both) locally accessible or globally accessible. A local access is a direct DSP access to L1D, L1P, and L2, while a global access is initiated by a DMA (either IDMA or the EDMA3) or by other system masters. Note that EDMA or IDMA transfers programmed by the DSP count as global accesses. On a secure device, pages can be restricted to secure access only (default) or opened up for public, non-secure access.

The DSP and each of the system masters on the device are all assigned a privilege ID. It is possible to specify only whether memory pages are locally or globally accessible.

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The AIDx and LOCAL bits of the memory protection page attribute registers specify the memory page protection scheme, see Table 2-1.

Table 2-1 Available Memory Page Protection Schemes

AIDx [1] Bit	Local Bit	Description
0	0	No access to memory page is permitted.
0	1	Only direct access by DSP is permitted.
1	0	Only accesses by system masters and IDMA are permitted (includes EDMA and IDMA accesses initiated by the DSP).
1	1	All accesses permitted.
End of Table 2-1		

1 x = 0, 1, 2, 3, 4, 5

Faults are handled by software in an interrupt (or an exception, programmable within the CorePac interrupt controller) service routine. A DSP or DMA access to a page without the proper permissions will:

- Block the access — reads return 0, writes are ignored
- Capture the initiator in a status register — ID, address, and access type are stored
- Signal the event to the DSP interrupt controller

The software is responsible for taking corrective action to respond to the event and resetting the error status in the memory controller. For more information on memory protection for L1D, L1P, and L2, see the *C66x CorePac User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

2.3 Bandwidth Management

When multiple requestors contend for a single C66x CorePac resource, the conflict is resolved by granting access to the highest priority requestor. The following four resources are managed by the bandwidth management control hardware:

- Level 1 Program (L1P) SRAM/Cache
- Level 1 Data (L1D) SRAM/Cache
- Level 2 (L2) SRAM/Cache
- Memory-mapped registers configuration bus

The priority level for operations initiated within the C66x CorePac are declared through registers in the CorePac. These operations are:

- DSP-initiated transfers
- User-programmed cache coherency operations
- IDMA-initiated transfers

The priority level for operations initiated outside the CorePac by system peripherals is declared through the Priority Allocation Register (PRI_ALLOC). System peripherals with no fields in PRI_ALLOC have their own registers to program their priorities.

More information on the bandwidth management features of the CorePac can be found in the *C66x CorePac Reference Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

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2.4 Power-Down Control

The C66x CorePac supports the ability to power-down various parts of the CorePac. The power-down controller (PDC) of the CorePac can be used to power down L1P, the cache control hardware, the DSP, and the entire CorePac. These power-down features can be used to design systems for lower overall system power requirements.

Note—The TCI6634K2K does not support power-down modes for the L2 memory at this time.

More information on the power-down features of the C66x CorePac can be found in the *C66x CorePac Reference Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22

2.5 C66x CorePac Revision

The version and revision of the C66x CorePac can be read from the CorePac Revision ID Register (MM_REVID) located at address 0181 2000h. The MM_REVID register is shown in Table 2-2 and described in Table 2-2. The C66x CorePac revision is dependent on the silicon revision being used.

Figure 2-5 CorePac Revision ID Register (MM_REVID)

31	16	15	0
VERSION		REVISION	
R-n		R-n	

Legend: R = Read only; R/W = Read/Write; -*n* = value after reset

Table 2-2 CorePac Revision ID Register (MM_REVID) Field Descriptions

Bit	Name	Value	Description
31-16	VERSION	xxxxh	Version of the C66x CorePac implemented on the device will depend on the silicon being used.
15-0	REVISION	0000h	Revision of the C66x CorePac version implemented on this device.
End of Table 2-2			

2.6 C66x CorePac Register Descriptions

See the *C66x CorePac User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22 for register offsets and definitions.

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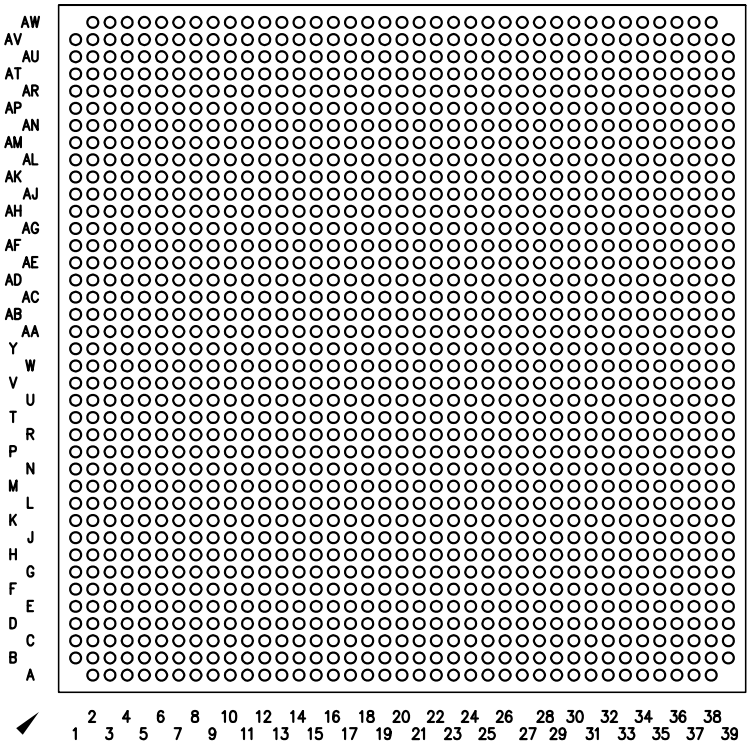
3 Terminals

3.1 Package Terminals

Figure 3-1 shows the AAW ball grid array package (bottom view).

Figure 3-1 AAW 1517-PIN BGA Package (Bottom View)



3.2 Pin Map

The following figures show the TCI6634 pin assignments in four quadrants (A, B, C, and D).

Figure 3-2 Pin Map Panels (Bottom View)

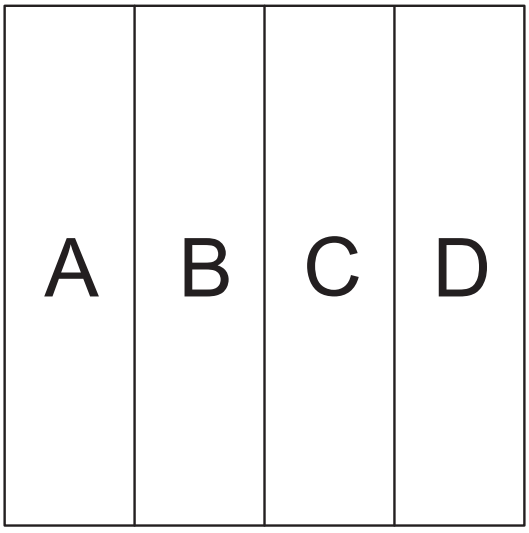


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Figure 3-3 TCI6634K2K Pin Map Left Side Panel (A) — Bottom View

	1	2	3	4	5	6	7	8	9	10
AW	(nopin)	VSS	VSS	HYP1CLKP	HYP1CLKN	VSS	HYP0RXN3	HYP0RXP3	VSS	HYP0RXN0
AV	VSS	VSS	HYP1RXN3	HYP1RXP3	VSS	HYP1RXN1	HYP1RXP1	VSS	HYP0RXN2	HYP0RXP2
AU	VSS	VSS	VSS	HYP1RXN2	HYP1RXP2	VSS	HYP1RXN0	HYP1RXP0	VSS	HYP0RXN1
AT	RP1FBN	VSS	HYP1TXN3	HYP1TXP3	VSS	HYP1TXN0	HYP1TXP0	VSS	HYP0CLKP	HYP0CLKN
AR	RP1FBP	RP1CLKP	VSS	HYP1TXN2	HYP1TXP2	VSS	HYP0TXN3	HYP0TXP3	VSS	HYP0TXN1
AP	TSRXCLKOUT0N	RP1CLKN	TSRXCLKOUT1N	VSS	HYP1TXN1	HYP1TXP1	VSS	HYP0TXN2	HYP0TXP2	VSS
AN	TSRXCLKOUT0P	VSS	TSRXCLKOUT1P	RSV002	VSS	VSS	VSS	VSS	VSS	RSV019
AM	TSREFCLKP	ALTCORECLKP	VSS	RSV003	CVDD	HYP1REFRES	RSV020	VSS	HYP0REFRES	VSS
AL	TSREFCLKN	ALTCORECLKN	SYSCLKP	CORECLKSEL	VSS	CVDD	VSS	CVDD	VSS	VDDAHV
AK	SYSCLKOUT	VSS	SYSCLKN	$\overline{\text{POR}}$	RSV012	VSS	CVDD	VSS	CVDD	VSS
AJ	HYP0TXPMDAT	HYP0RXPMCLK	HYP0TXFLCLK	HYP0RXFLDAT	HYP0RXFLCLK	VSS	VSS	CVDD	VSS	CVDD
AH	HYP1TXPMCLK	HYP1TXFLDAT	HYP1TXFLCLK	HYP1RXFLCLK	HYP0TXPMCLK	VSS	VSS	VSS	CVDD	VSS
AG	TDI	HYP1RXFLDAT	HYP0RXPMDAT	VSS	HYP0TXFLDAT	DVDD18	VSS	CVDD	VSS	CVDD
AF	TDO	HYP1TXPMDAT	HYP1RXPMCLK	HYP1RXPMDAT	BOOTCOMPLETE	VSS	DVDD18	VSS	CVDD	VSS
AE	TCK	TMS	VSS	$\overline{\text{LRESET}}$	HOUT	DVDD18	VSS	CVDD	VSS	CVDD
AD	$\overline{\text{TRST}}$	$\overline{\text{RESET}}$	$\overline{\text{RESETFULL}}$	$\overline{\text{LRESETNMIEN}}$	$\overline{\text{NMI}}$	VSS	DVDD18	VSS	CVDD	VSS
AC	TSPUSHEVT1	TSPUSHEVT0	TSSYNCEVT	EXTFRAMEEVENT	$\overline{\text{RESETSTAT}}$	DVDD18	VSS	CVDD	VSS	CVDD
AB	TSCOMPOUT	EMU01	EMU14	EMU10	DVDD18	VSS	DVDD18	VSS	CVDD	VSS
AA	USBRESREF	EMU00	EMU11	EMU18	VSS	DVDD18	VSS	CVDD	VSS	CVDD
Y	USBRX0M	VSS	EMU02	EMU03	DVDD18	VSS	DVDD18	VSS	CVDD	VSS
W	USBRX0P	USBCLKP	EMU04	EMU05	VSS	DVDD18	VSS	CVDD	VSS	CVDD
V	USBTX0M	USBCLKM	VSS	EMU06	DVDD18	VSS	DVDD18	VSS	CVDD	VSS
U	USBTX0P	USBDP	EMU08	EMU07	EMU12	DVDD18	VSS	CVDD	VSS	CVDD
T	USBVBUS	USBDM	EMU09	EMU13	EMU16	VSS	DVDD18	VSS	CVDD	VSS
R	USBID0	VSS	EMU15	EMU17	VSS	DVDD18	VSS	CVDD	VSS	CVDD
P	RSV001	RSV000	SDA0	SCL2	VSS	VSS	CVDD	VSS	CVDD	VSS
N	SCL0	SDA1	SDA2	SCL1	VSS	CVDD	VSS	CVDD	VSS	CVDD
M	TIMI1	TIMI0	TIMO0	TIMO1	UART1RTS	VSS	CVDD	VSS	CVDD	VSS
L	UART0CTS	UART1RXD	USBDRVVBUS	UART0RTS	VSS	CVDD	VSS	DVDD15	VSS	DVDD15
K	UART1CTS	UART0TXD	UART1TXD	UART0RXD	VSS	VSS	DVDD15	VSS	DVDD15	VSS
J	VSS	VSS	VSS	VSS	VSS	DVDD15	VSS	DVDD15	VSS	DVDD15
H	DDR3AD04	DDR3AD01	DDR3AD13	VSS	DDR3AD17	VSS	DVDD15	VSS	DVDD15	$\overline{\text{DDR3ARQ1}}$
G	DDR3AD00	DDR3AD03	DDR3AD10	DDR3AD16	DDR3AD20	DDR3AD29	DDR3AD30	DDR3AA02	DDR3AA01	DDR3AA03
F	DDR3AD02	DDR3AD06	DDR3ADQM1	DDR3AD09	DDR3AD19	DDR3AD26	DDR3AD25	DDR3AA05	DDR3AA04	DDR3AA10
E	DDR3ADQS0P	DDR3AD05	VSS	DDR3AD08	VSS	DDR3ADQM3	VSS	DDR3AA00	VSS	DDR3AA12
D	DDR3ADQS0N	DDR3AD07	DDR3AD14	DDR3AD15	DDR3AD18	DDR3AD21	DDR3AD31	DDR3AA09	DDR3AA07	DDR3AA15
C	VSS	DDR3ADQM0	DDR3ADQS1N	VSS	DDR3AD22	VSS	DDR3AD24	VSS	DDR3AA06	VSS
B	VSS	VSS	DDR3ADQS1P	DDR3AD12	DDR3ADQS2N	DDR3AD23	DDR3ADQS3P	DDR3AD28	DDR3AA08	DDR3AA14
A	(nopin)	VSS	VSS	DDR3AD11	DDR3ADQS2P	DDR3ADQM2	DDR3ADQS3N	DDR3AD27	DDR3AA11	DDR3AA13
	1	2	3	4	5	6	7	8	9	10

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Figure 3-4 TCI6634K2K Pin Map Left Center Panel (B) — Bottom View

	11	12	13	14	15	16	17	18	19	20
AW	HYP0RXP0	VSS	AIFRXN3	AIFRXP3	VSS	AIFRXN0	AIFRXP0	VSS	XFIRXP1	XFIRXN1
AV	VSS	AIFRXN5	AIFRXP5	VSS	AIFRXN2	AIFRXP2	VSS	XFIRXP0	XFIRXN0	VSS
AU	HYP0RXP1	VSS	AIFRXN4	AIFRXP4	VSS	AIFRXN1	AIFRXP1	VSS	XFICLKP	XFICLKN
AT	VSS	AIFTXN5	AIFTXP5	VSS	AIFTXN2	AIFTXP2	VSS	XFITXP0	XFITXN0	VSS
AR	HYP0TXP1	VSS	AIFTXN4	AIFTXP4	VSS	AIFTXN1	AIFTXP1	VSS	XFITXP1	XFITXN1
AP	HYP0TXN0	HYP0TXP0	VSS	AIFTXN3	AIFTXP3	VSS	AIFTXN0	AIFTXP0	VSS	VSS
AN	VSS	VSS	VSS	VSS	VSS	XFIREFRES0	VSS	VSS	RSV026	VSS
AM	AIFREFRES1	VSS	VSS	RSV025	AIFREFRES0	RSV024	VSS	VSS	XFIREFRES1	VSS
AL	VSS	VDDAHV	VSS	VDDAHV	VSS	VDDAHV	VSS	VDDAHV	VSS	VDDAHV
AK	VDDAHV	VSS	VDDAHV	VSS	VDDAHV	VSS	VDDAHV	VSS	VDDAHV	VSS
AJ	VSS	VDDALV	VSS	VDDALV	VSS	VDDALV	VSS	VDDALV	VSS	VDDALV
AH	VDDALV	VSS	VDDALV	VSS	VDDALV	VSS	VDDALV	VSS	VDDALV	VSS
AG	VSS	VDDALV	VSS	VDDALV	VSS	VDDALV	VSS	VDDALV	VSS	VDDALV
AF	AVDDA1	VSS	VDDALV	VSS	VDDALV	VSS	VDDALV	VSS	VDDALV	VSS
AE	VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS	CVDD
AD	VNWA2	VSS	CVDD	VSS	CVDD	VSS	CVDD1	VSS	CVDD1	VSS
AC	VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS	CVDD1	VSS	CVDD
AB	CVDD	VSS	VDDUSB	VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS
AA	VSS	VP	VSS	DVDD33	VSS	CVDD	VSS	CVDD	VSS	CVDD
Y	VPTX	VSS	VPH	VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS
W	VSS	CVDD	VSS	CVDD	VSS	CVDD1	VSS	CVDD	VSS	CVDD
V	VNWA4	VSS	CVDD1	VSS	CVDD	VSS	CVDD1	VSS	CVDD	VSS
U	VSS	CVDD	VSS	CVDD1	VSS	CVDD1	VSS	CVDD	VSS	CVDD1
T	CVDD	VSS	CVDD1	VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS
R	VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS	CVDD
P	AVDDA6	VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS
N	VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS	AVDDA2
M	DVDD15	VSS	AVDDA7	VSS	AVDDA8	VSS	DVDD15	AVDDA9	DVDD15	AVDDA10
L	VSS	DVDD15	VSS	DVDD15	VSS	DVDD15	VSS	DVDD15	VSS	DVDD15
K	DVDD15	VSS	DVDD15	VSS	DVDD15	VSS	DVDD15	VSS	DVDD15	VSS
J	VSS	DVDD15	VSS	DVDD15	VSS	DVDD15	VSS	DVDD15	VSS	DVDD15
H	DVDD15	VSS	DVDD15	VSS	DVDD15	DDR3ARQ0	DVDD15	VSS	DVDD15	VSS
G	DDR3ABA2	DDR3ACKE0	DDR3AODT1	DDR3AVREFSSTL	DDR3ACB07	DDR3AD33	DDR3AD35	DDR3AD42	DDR3AD44	DDR3AD51
F	DDR3ACE1	DDR3AWE	RSV029	DDR3ACB05	DDR3ACB03	DDR3AD34	DDR3AD38	DDR3AD47	DDR3AD43	DDR3AD54
E	VSS	DDR3AODT0	VSS	DDR3ADQM8	VSS	DDR3AD32	VSS	DDR3AD39	VSS	DDR3AD53
D	DDR3ACE0	RSV027	RSV028	DDR3ACB06	DDR3ACB04	DDR3AD36	DDR3AD37	DDR3AD46	DDR3AD41	DDR3AD50
C	DDR3ABA1	VSS	DDR3ACAS	VSS	DDR3ACB01	VSS	DDR3ADQM4	VSS	DDR3AD40	VSS
B	DDR3ABA0	DDR3ACLKOUTN0	DDR3ACLKOUTN1	DDR3ARESET	DDR3ADQS8P	DDR3ACB02	DDR3ADQS4N	DDR3AD45	DDR3ADQS5P	DDR3AD49
A	DDR3ACKE1	DDR3ACLKOUTP0	DDR3ACLKOUTP1	DDR3ARAS	DDR3ADQS8N	DDR3ACB00	DDR3ADQS4P	DDR3ADQM5	DDR3ADQS5N	DDR3AD48
	11	12	13	14	15	16	17	18	19	20

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Figure 3-5 TCI6634K2K Pin Map Right Center Panel (C) — Bottom View

21	22	23	24	25	26	27	28	29	30	
VSS	RIORXN2	RIORXP2	VSS	SGMII3RXN	SGMII3RXP	VSS	SGMII0RXN	SGMII0RXP	VSS	AW
RIORXN3	RIORXP3	VSS	RIORXN0	RIORXP0	VSS	SGMII1RXN	SGMII1RXP	VSS	PCIERXN1	AV
VSS	RIORXN1	RIORXP1	VSS	SGMII2RXN	SGMII2RXP	VSS	SGMII0TXN	SGMII0TXP	VSS	AU
RIOTXN3	RIOTXP3	VSS	RIOTXN0	RIOTXP0	VSS	SGMII1TXN	SGMII1TXP	VSS	PCIETXN0	AT
VSS	VSS	RIOTXN1	RIOTXP1	VSS	SGMII2TXN	SGMII2TXP	VSS	PCIETXN1	PCIETXP1	AR
VSS	RIOTXN2	RIOTXP2	VSS	SGMII3TXN	SGMII3TXP	VSS	VSS	VSS	VSS	AP
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	PACLKSEL	AN
RIOREFRES	VSS	RSV021	SGMIIREFRES	RSV023	PCIEREFRES	DVDD18	RSV022	DVDD18	RADSYNC	AM
VSS	VDDAHV	VSS	VDDAHV	VSS	DVDD18	VSS	DVDD18	VSS	CVDD	AL
VDDAHV	VSS	VDDAHV	VSS	VDDAHV	VSS	DVDD18	VSS	CVDD	VSS	AK
VSS	VDDALV	VSS	VDDALV	VSS	DVDD18	VSS	CVDD	VSS	DVDD15	AJ
VDDALV	VSS	VDDALV	VSS	VDDALV	VSS	CVDD	VSS	AVDDA4	VSS	AH
VSS	VDDALV	VSS	VNWA1	VSS	AVDDA5	VSS	CVDD	VSS	DVDD15	AG
VDDALV	VSS	VDDALV	VSS	CVDD	VSS	CVDD	VSS	DVDD15	VSS	AF
VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS	AVDDA15	VSS	DVDD15	AE
CVDD	VSS	CVDD	VSS	CVDD	VSS	CVDD	AVDDA14	DVDD15	VSS	AD
VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS	AVDDA13	VSS	DVDD15	AC
CVDD	VSS	CVDD	VSS	CVDD	VSS	CVDD	AVDDA12	DVDD15	VSS	AB
VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS	DVDD15	VSS	DVDD15	AA
CVDD	VSS	CVDD	VSS	CVDD	VSS	CVDD	AVDDA11	DVDD15	VSS	Y
VSS	RSV082	VSS	RSV078	VSS	RSV079	VSS	DVDD15	VSS	DVDD15	W
CVDD1	VSS	RSV076	VSS	RSV077	VSS	CVDD	VSS	DVDD15	VSS	V
VSS	RSV081	VSS	RSV074	VSS	RSV075	VSS	DVDD15	VSS	DVDD15	U
CVDD1	VSS	RSV058	VSS	RSV059	VSS	CVDD	VSS	DVDD15	VSS	T
VSS	RSV080	VSS	RSV056	VSS	RSV057	VSS	DVDD15	VSS	DVDD15	R
CVDD	VSS	RSV054	VSS	RSV055	VSS	CVDD	VSS	DVDD15	VSS	P
VSS	CVDD	VSS	RSV052	VSS	RSV053	VSS	RSV046	VSS	DVDD18	N
VPP	VSS	VNWA3	VSS	CVDD	VSS	RSV051	VSS	DVDD18	VSS	M
VSS	VPP	VSS	DVDD18	VSS	DVDD18	VSS	RSV050	VSS	DVDD18	L
DVDD15	VSS	DVDD15	VSS	DVDD18	VSS	DVDD18	VSS	RSV049	VSS	K
VSS	DVDD15	VSS	VSS	VSS	DVDD18	VSS	DVDD18	VSS	RSV048	J
DVDD15	$\overline{\text{DDR3ARQ2}}$	DVDD15	VSS	DVDD18	VSS	DVDD18	VSS	VSS	VSS	H
DDR3AD55	DDR3AD57	VSS	CORESEL3	VSS	RSV018	VSS	SPI2DOUT	VSS	GPIO09	G
DDR3AD62	DDR3AD59	RSV013	CORESEL0	SPI0SCS0	RSV017	SPI1DIN	SPI2DIN	GPIO00	GPIO12	F
VSS	DDR3AD60	RSV014	CORESEL1	SPI2SCS3	SPI0SCS2	SPI1SCS3	VSS	GPIO05	GPIO11	E
DDR3ADQM6	DDR3AD63	DDR3AD58	CORESEL2	SPI2CLK	SPI0SCS3	SPI1SCS2	SPI2SCS1	GPIO02	GPIO06	D
DDR3AD52	VSS	DDR3AD56	VSS	SPI0SCS1	VSS	SPI1SCS1	SPI1CLK	VSS	GPIO07	C
DDR3ADQS6N	DDR3AD61	DDR3ADQS7N	RSV004	DDR3ACLKP	SPI0CLK	SPI1SCS0	SPI2SCS0	GPIO04	GPIO01	B
DDR3ADQS6P	DDR3ADQM7	DDR3ADQS7P	RSV005	DDR3ACLKN	SPI0DIN	SPI0DOUT	SPI1DOUT	SPI2SCS2	GPIO08	A
21	22	23	24	25	26	27	28	29	30	

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Figure 3-6 TCI6634K2K Pin Map Right Side Panel (D) — Bottom View

31	32	33	34	35	36	37	38	39	
PCIECLKP	PCIECLKN	VSS	SRIOSGMIICLKP	SRIOSGMIICLKN	RSV044	VSS	VSS	(NOPIN)	AW
PCIERXP1	VSS	PASSCLKP	PASSCLKN	VSS	RSV042	RSV040	VSS	VSS	AV
PCIERXN0	PCIERXP0	VSS	RSV008	RSV043	RSV039	RSV041	VCNTL4	VSS	AU
PCIETXP0	VSS	XFIMDIO	RSV009	RSV045	VSS	RSV038	VCNTL3	VCNTL0	AT
VSS	MDIO	VSS	XFIMDCLK	VCNTL5	VCNTL2	VCNTL1	DDR3BCLKP	DDR3BCLKN	AR
MDCLK	RSV034	RSV035	PHYSYNC	VD	VCL	VSS	RSV006	RSV007	AP
VSS	RSV033	DDR3BD58	DDR3BD56	VSS	DDR3BD57	DDR3BD63	DDR3BDQS7P	DDR3BDQS7N	AN
CVDD	VSS	VSS	DDR3BD59	DDR3BD60	DDR3BD62	VSS	DDR3BD61	DDR3BDQM7	AM
VSS	DVDD15	DDR3BD55	DDR3BD52	VSS	DDR3BD53	DDR3BD54	DDR3BDQS6N	DDR3BDQS6P	AL
DVDD15	DDR3BRQ2	VSS	DDR3BDQM6	DDR3BD51	DDR3BD50	VSS	DDR3BD49	DDR3BD48	AK
VSS	VSS	DDR3BD41	DDR3BD43	VSS	DDR3BD44	DDR3BD47	DDR3BDQS5N	DDR3BDQS5P	AJ
DVDD15	DDR3BD40	VSS	DDR3BD37	DDR3BD38	DDR3BD42	VSS	DDR3BD46	DDR3BD45	AH
VSS	DDR3BD39	DDR3BDQM4	DDR3BD35	VSS	DDR3BD36	DDR3BD32	DDR3BD34	DDR3BDQM5	AG
DVDD15	DDR3BCB00	VSS	DDR3BCB01	DDR3BCB03	DDR3BD33	VSS	DDR3BDQS4P	DDR3BDQS4N	AF
VSS	DDR3BCB02	DDR3BCB04	DDR3BCB07	VSS	DDR3BCB05	DDR3BDQM8	DDR3BDQS8N	DDR3BDQS8P	AE
DVDD15	DDR3BRAS	VSS	DDR3BODT1	RSV030	DDR3BCB06	VSS	DDR3BCLKOUTP0	DDR3BCLKOUTN0	AD
DDR3BVREFSSTL	DDR3BRESET	DDR3BODT0	RSV031	VSS	DDR3BCAS	DDR3BWE	DDR3BCLKOUTN1	DDR3BCLKOUTP1	AC
DVDD15	RSV032	VSS	DDR3BCE0	DDR3BBA2	VSS	VSS	DDR3BCKE1	DDR3BCKE0	AB
DDR3BRQ0	DDR3BA00	DDR3BA08	DDR3BBA1	VSS	DDR3BCE1	DDR3BBA0	DDR3BA14	DDR3BA11	AA
DVDD15	DDR3BA09	VSS	DDR3BA03	DDR3BA12	DDR3BA15	VSS	DDR3BA10	DDR3BA13	Y
VSS	DDR3BA02	DDR3BA01	DDR3BA04	VSS	DDR3BA06	DDR3BA07	DDR3BD27	DDR3BD28	W
DVDD15	DDR3BD30	VSS	DDR3BA05	DDR3BD24	DDR3BD31	VSS	DDR3BDQS3N	DDR3BDQS3P	V
VSS	DDR3BDQM3	DDR3BD29	DDR3BD26	VSS	DDR3BD25	DDR3BD21	DDR3BD23	DDR3BDQM2	U
DVDD15	DDR3BD08	VSS	DDR3BD16	DDR3BD18	DDR3BD22	VSS	DDR3BDQS2N	DDR3BDQS2P	T
VSS	DDR3BD09	DDR3BD14	DDR3BD17	VSS	DDR3BD20	DDR3BD19	DDR3BD12	DDR3BD11	R
DVDD15	DDR3BRQ1	VSS	DDR3BDQM1	DDR3BD10	DDR3BD15	VSS	DDR3BDQS1N	DDR3BDQS1P	P
VSS	DDR3BD13	DDR3BD04	DDR3BD01	VSS	DDR3BD06	DDR3BD05	DDR3BD07	DDR3BDQM0	N
DVDD15	EMIFD00	VSS	EMIFD13	EMIFD15	EMIFD14	DDR3BD02	DDR3BDQS0P	DDR3BDQS0N	M
VSS	DVDD15	EMIFD02	EMIFD03	EMIFD12	EMIFD11	VSS	DDR3BD00	DDR3BD03	L
DVDD18	VSS	EMIFA07	EMIFA16	VSS	EMIFD10	EMIFD06	EMIFD09	EMIFD08	K
VSS	DVDD18	VSS	EMIFA05	EMIFA18	EMIFA21	EMIFD01	EMIFD05	EMIFD07	J
RSV047	VSS	EMIFBE1	EMIFBE0	EMIFA06	EMIFA12	VSS	EMIFA22	EMIFD04	H
VSS	EMIFCE1	EMIFCE0	EMIFCE2	VSS	EMIFA02	EMIFA09	EMIFA14	EMIFA19	G
GPIO10	RSV016	EMIFRNW	EMIFA00	EMIFA17	EMIFWE	EMIFA01	EMIFA10	EMIFA15	F
GPIO25	GPIO14	RSV015	EMIFA04	EMIFA13	EMIFCE3	EMIFOE	EMIFWAIT0	EMIFA03	E
GPIO22	GPIO27	GPIO21	VSS	EMIFA11	EMIFA23	VSS	RSV011	EMIFWAIT1	D
GPIO18	VSS	GPIO28	GPIO29	EMIFA08	EMIFA20	RSV037	RSV010	VSS	C
GPIO15	GPIO19	GPIO24	GPIO31	GPIO23	GPIO30	RSV036	VSS	VSS	B
GPIO13	GPIO17	GPIO20	GPIO26	GPIO03	GPIO16	VSS	VSS	(NOPIN)	A
31	32	33	34	35	36	37	38	39	

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3.3 Terminal Functions

The terminal functions table (Table 3-2) identifies the external signal names, the associated pin (ball) numbers, the pin type (I, O/Z, or I/O/Z), whether the pin has any internal pullup/pulldown resistors, and gives functional pin descriptions. This table is arranged by function. The power terminal functions table (Table 3-3) lists the various power supply pins and ground pins and gives functional pin descriptions. Table 3-4 shows all pins arranged by signal name. Table 3-5 shows all pins arranged by ball number.

There are 17 pins that have a secondary function as well as a primary function. The secondary function is indicated with a dagger (†).

For more detailed information on device configuration, peripheral selection, multiplexed/shared pins, and pullup/pulldown resistors, see section 6.2 "Device Configuration" on page 185.

Use the symbol definitions in Table 3-1 when reading Table 3-2.

Table 3-1 I/O Functional Symbol Definitions

Functional Symbol	Definition	Table 3-2 Column Heading
IPD or IPU	Internal 100-µA pulldown or pullup is provided for this terminal. In most systems, a 1-kΩ resistor can be used to oppose the IPD/IPU. For more detailed information on pulldown/pullup resistors and situations in which external pulldown/pullup resistors are required, see the *Hardware Design Guide for KeyStone Devices* in 1.9 "Related Documentation from Texas Instruments" on page 22.	IPD/IPU
A	Analog signal	Type
GND	Ground	Type
I	Input terminal	Type
O	Output terminal	Type
S	Supply voltage	Type
Z	Three-state terminal or high impedance	Type
End of Table 3-1		

Table 3-2 Terminal Functions — Signals and Control by Function (Part 1 of 20)

Signal Name	Ball No.	Type	IPD/IPU	Description
AIF				
AIFRXN0	AW16	I		Antenna Interface receive data (6 links)
AIFRXP0	AW17	I		
AIFRXN1	AU16	I		
AIFRXP1	AU17	I		
AIFRXN2	AV15	I		
AIFRXP2	AV16	I		
AIFRXN3	AW13	I		
AIFRXP3	AW14	I		
AIFRXN4	AU13	I		
AIFRXP4	AU14	I		
AIFRXN5	AV12	I		
AIFRXP5	AV13	I		

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Table 3-2 Terminal Functions — Signals and Control by Function (Part 2 of 20)

Signal Name	Ball No.	Type	IPD/IPU	Description
AIFTXN0	AP17	O		Antenna Interface transmit data (6 links)
AIFTXP0	AP18	O		
AIFTXN1	AR16	O		
AIFTXP1	AR17	O		
AIFTXN2	AT15	O		
AIFTXP2	AT16	O		
AIFTXN3	AP14	O		
AIFTXP3	AP15	O		
AIFTXN4	AR13	O		
AIFTXP4	AR14	O		
AIFTXN5	AT12	O		
AIFTXP5	AT13	O		
AIFREFRES0	AM15	A		Antenna SERDES0 reference resistor input (3 kΩ +/- 1%)
AIFREFRES1	AM11	A		Antenna SERDES1 reference resistor input (3 kΩ +/- 1%)
Antenna Timer				
EXTFRAMEEVENT	AC4	OZ	Down	Frame sync clock output
PHYSYNC	AP34	I	Down	Alternate frame sync clock input (vs. FSYNCCLK(N|P)
RADSYNC	AM30	I	Down	Alternate frame sync input (vs. FRAMBURST (N|P)
RP1CLKN	AP2	I		Frame sync interface clock used to drive the frame synchronization interface (OBSAI RP1 clock)
RP1CLKP	AR2	I		
RP1FBN	AT1	I		Frame burst to drive frame indicators to the frame synchronization module (OBSAI RP1)
RP1FBP	AR1	I		
Boot Configuration Pins				
AVSIFSEL0†	M2	I	Down	Default value (Boot Strapped) for SR PINMUX register (SR_PINCTL). Pins shared with TIMI0 and TIMI1.
AVSIFSEL1†	M1	I	Down	
BOOTMODE00†	B30	I	Down	User defined Boot Mode pins See 6.1.2 "Boot Modes Supported" on page 174 for more details. († Pins are secondary functions and are shared with GPIO[01:13])
BOOTMODE01†	D29	I	Down	
BOOTMODE02†	A35	I	Down	
BOOTMODE03†	B29	I	Down	
BOOTMODE04†	E29	I	Down	
BOOTMODE05†	D30	I	Down	
BOOTMODE06†	C30	I	Down	
BOOTMODE07†	A30	I	Down	
BOOTMODE08†	G30	I	Down	
BOOTMODE09†	F31	I	Down	
BOOTMODE10†	E30	I	Down	
BOOTMODE11†	F30	I	Down	
BOOTMODE12†	A31	I	Down	
BOOTMODE13†	F24	I		User defined Boot Mode pins See 6.1.2 "Boot Modes Supported" on page 174 for more details. († Pins are secondary functions and are shared with CORESEL[0:2])
BOOTMODE14†	E24	I		
BOOTMODE15†	D24	I		
BOOTCOMPLETE	AF5	OZ	Down	Boot progress indication output
LENDIAN†	F29	I	Up	Little endian configuration pin. Pin shared with GPIO00

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Table 3-2 Terminal Functions — Signals and Control by Function (Part 3 of 20)

Signal Name	Ball No.	Type	IPD/IPU	Description
MAINPLLODSEL†	E32	I	Down	Main PLL Output divider select. Pin shared with GPIO14.
Clock / Reset				
ALTCORECLKN	AL2	I		Alternate clock input to Main PLL
ALTCORECLKP	AM2	I		
CORECLKSEL	AL4	I	Down	Core clock select to select between SYSCLK(N|P) and ALTCORECCLK to the main PLL
CORESEL0	F24	I	Down	Select for the target core for LRESET and NMI
CORESEL1	E24	I	Down	
CORESEL2	D24	I	Down	
CORESEL3	G24	I	Down	
DDR3ACLKN	A25	I		DDR3A reference clock input to DDR PLL
DDR3ACLKP	B25	I		
DDR3BCLKN	AR39	I		DDR3B reference clock input to DDR PLL
DDR3BCLKP	AR38	I		
HOUT	AE5	OZ	Up	Interrupt output pulse created by IPCGRH
HYP0CLKN	AT10	I		HyperLink reference clock to drive HyperLink0 SerDes
HYP0CLKP	AT9	I		
HYP1CLKN	AW5	I		HyperLink reference clock to drive HyperLink1 SerDes
HYP1CLKP	AW4	I		
$\overline{\text{LRESET}}$	AE4	I	Up	Warm reset
$\overline{\text{LRESETNMIEN}}$	AD4	I	Up	Enable for core selects
$\overline{\text{NMI}}$	AD5	I	Up	Non-maskable interrupt
PACLKSEL	AN30	I	Down	PA clock select to choose between core clock and PASSCLK pins
PASSCLKN	AV34	I		Packet Accelerator subsystem reference clock
PASSCLKP	AV33	I		
PCIECLKN	AW32	I		PCIe clock input to drive PCIe SerDes
PCIECLKP	AW31	I		
$\overline{\text{POR}}$	AK4	I		Power-on reset
$\overline{\text{RESETFULL}}$	AD3	I	Up	Full reset
$\overline{\text{RESET}}$	AD2	I	Up	Warm reset of non isolated portion of the device
$\overline{\text{RESETSTAT}}$	AC5	O	Up	Reset status output
SRIOSGMIICLKN	AW35	I		RapidIO/SGMII reference clock to drive the RapidIO and SGMII SerDes
SRIOSGMIICLKP	AW34	I		
SYSCLKN	AK3	I		System clock input to antenna interface and Main PLL (Main PLL optional vs. ALTCORECLK)
SYSCLKP	AL3	I		
SYSCLKOUT	AK1	OZ	Down	System clock output to be used as a general purpose output clock for debug purposes
TSREFCLKN	AL1	I		External precision clock source for SyncE
TSREFCLKP	AM1	I		
TSRXCLKOUT0N	AP1	O		SerDes recovered clock output for SyncE.
TSRXCLKOUT0P	AN1	O		
TSRXCLKOUT1N	AP3	O		SerDes recovered clock output for SyncE.
TSRXCLKOUT1P	AN3	O		

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Table 3-2 Terminal Functions — Signals and Control by Function (Part 4 of 20)

Signal Name	Ball No.	Type	IPD/IPU	Description
DDR3A				
DDR3ADQM0	C2	OZ		DDR3A EMIF data masks
DDR3ADQM1	F3	OZ		
DDR3ADQM2	A6	OZ		
DDR3ADQM3	E6	OZ		
DDR3ADQM4	C17	OZ		
DDR3ADQM5	A18	OZ		
DDR3ADQM6	D21	OZ		
DDR3ADQM7	A22	OZ		
DDR3ADQM8	E14	OZ		
DDR3ADQS0P	E1	IOZ		DDR3A EMIF data strobe
DDR3ADQS0N	D1	IOZ		
DDR3ADQS1P	B3	IOZ		
DDR3ADQS1N	C3	IOZ		
DDR3ADQS2P	A5	IOZ		
DDR3ADQS2N	B5	IOZ		
DDR3ADQS3P	B7	IOZ		
DDR3ADQS3N	A7	IOZ		
DDR3ADQS4P	A17	IOZ		
DDR3ADQS4N	B17	IOZ		
DDR3ADQS5P	B19	IOZ		
DDR3ADQS5N	A19	IOZ		
DDR3ADQS6P	A21	IOZ		
DDR3ADQS6N	B21	IOZ		
DDR3ADQS7P	A23	IOZ		
DDR3ADQS7N	B23	IOZ		
DDR3ADQS8P	B15	IOZ		
DDR3ADQS8N	A15	IOZ		
DDR3ACB00	A16	IOZ		DDR3A EMIF check bits
DDR3ACB01	C15	IOZ		
DDR3ACB02	B16	IOZ		
DDR3ACB03	F15	IOZ		
DDR3ACB04	D15	IOZ		
DDR3ACB05	F14	IOZ		
DDR3ACB06	D14	IOZ		
DDR3ACB07	G15	IOZ		

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Table 3-2 Terminal Functions — Signals and Control by Function (Part 5 of 20)

Signal Name	Ball No.	Type	IPD/IPU	Description
DDR3AD00	G1	IOZ		DDR3A EMIF data bus
DDR3AD01	H2	IOZ		
DDR3AD02	F1	IOZ		
DDR3AD03	G2	IOZ		
DDR3AD04	H1	IOZ		
DDR3AD05	E2	IOZ		
DDR3AD06	F2	IOZ		
DDR3AD07	D2	IOZ		
DDR3AD08	E4	IOZ		
DDR3AD09	F4	IOZ		
DDR3AD10	G3	IOZ		
DDR3AD11	A4	IOZ		
DDR3AD12	B4	IOZ		
DDR3AD13	H3	IOZ		
DDR3AD14	D3	IOZ		
DDR3AD15	D4	IOZ		
DDR3AD16	G4	IOZ		DDR3A EMIF data bus
DDR3AD17	H5	IOZ		
DDR3AD18	D5	IOZ		
DDR3AD19	F5	IOZ		
DDR3AD20	G5	IOZ		
DDR3AD21	D6	IOZ		
DDR3AD22	C5	IOZ		
DDR3AD23	B6	IOZ		
DDR3AD24	C7	IOZ		
DDR3AD25	F7	IOZ		
DDR3AD26	F6	IOZ		
DDR3AD27	A8	IOZ		
DDR3AD28	B8	IOZ		
DDR3AD29	G6	IOZ		
DDR3AD30	G7	IOZ		
DDR3AD31	D7	IOZ		

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Table 3-2 Terminal Functions — Signals and Control by Function (Part 6 of 20)

Signal Name	Ball No.	Type	IPD/IPU	Description
DDR3AD32	E16	IOZ		DDR3A EMIF data bus
DDR3AD33	G16	IOZ		
DDR3AD34	F16	IOZ		
DDR3AD35	G17	IOZ		
DDR3AD36	D16	IOZ		
DDR3AD37	D17	IOZ		
DDR3AD38	F17	IOZ		
DDR3AD39	E18	IOZ		
DDR3AD40	C19	IOZ		
DDR3AD41	D19	IOZ		
DDR3AD42	G18	IOZ		
DDR3AD43	F19	IOZ		
DDR3AD44	G19	IOZ		
DDR3AD45	B18	IOZ		
DDR3AD46	D18	IOZ		
DDR3AD47	F18	IOZ		
DDR3AD48	A20	IOZ		
DDR3AD49	B20	IOZ		DDR3A EMIF data bus
DDR3AD50	D20	IOZ		
DDR3AD51	G20	IOZ		
DDR3AD52	C21	IOZ		
DDR3AD53	E20	IOZ		
DDR3AD54	F20	IOZ		
DDR3AD55	G21	IOZ		
DDR3AD56	C23	IOZ		
DDR3AD57	G22	IOZ		
DDR3AD58	D23	IOZ		
DDR3AD59	F22	IOZ		
DDR3AD60	E22	IOZ		
DDR3AD61	B22	IOZ		
DDR3AD62	F21	IOZ		
DDR3AD63	D22	IOZ		
$\overline{\text{DDR3ACE0}}$	D11	OZ		DDR3A EMIF chip enable
$\overline{\text{DDR3ACE1}}$	F11	OZ		DDR3A EMIF chip enable
DDR3ABA0	B11	OZ		DDR3A EMIF bank address
DDR3ABA1	C11	OZ		
DDR3ABA2	G11	OZ		

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Table 3-2 Terminal Functions — Signals and Control by Function (Part 7 of 20)

Signal Name	Ball No.	Type	IPD/IPU	Description
DDR3AA00	E8	OZ		DDR3A EMIF address bus
DDR3AA01	G9	OZ		
DDR3AA02	G8	OZ		
DDR3AA03	G10	OZ		
DDR3AA04	F9	OZ		
DDR3AA05	F8	OZ		
DDR3AA06	C9	OZ		
DDR3AA07	D9	OZ		
DDR3AA08	B9	OZ		
DDR3AA09	D8	OZ		
DDR3AA10	F10	OZ		
DDR3AA11	A9	OZ		
DDR3AA12	E10	OZ		
DDR3AA13	A10	OZ		
DDR3AA14	B10	OZ		
DDR3AA15	D10	OZ		
$\overline{\text{DDR3ACAS}}$	C13	OZ		DDR3A EMIF column address strobe
$\overline{\text{DDR3ARAS}}$	A14	OZ		DDR3A EMIF row address strobe
$\overline{\text{DDR3AWE}}$	F12	OZ		DDR3A EMIF write enable
DDR3ACKE0	G12	OZ		DDR3A EMIF clock enable0
DDR3ACKE1	A11	OZ		DDR3A EMIF clock enable1
DDR3ACLKOUTP0	A12	OZ		DDR3A EMIF output clocks to drive SDRAMs (one clock pair per SDRAM) for Rank0
DDR3ACLKOUTN0	B12	OZ		
DDR3ACLKOUTP1	A13	OZ		DDR3A EMIF output clocks to drive SDRAMs (one clock pair per SDRAM) for Rank1
DDR3ACLKOUTN1	B13	OZ		
DDR3AODT0	E12	OZ		DDR3A EMIF on die termination outputs used to set termination on the SDRAMs for Rank0
DDR3AODT1	G13	OZ		DDR3A EMIF on die termination outputs used to set termination on the SDRAMs for Rank1
$\overline{\text{DDR3ARESET}}$	B14	OZ		DDR3A reset signal
DDR3ARZQ0	H16	A		PTV compensation pin for DDR3A
DDR3ARZQ1	H10	A		PTV compensation pin for DDR3A
DDR3ARZQ2	H22	A		PTV compensation pin for DDR3A
DDR3B				
DDR3BDQM0	N39	OZ		DDR3B EMIF data masks
DDR3BDQM1	P34	OZ		
DDR3BDQM2	U39	OZ		
DDR3BDQM3	U32	OZ		
DDR3BDQM4	AG33	OZ		
DDR3BDQM5	AG39	OZ		
DDR3BDQM6	AK34	OZ		
DDR3BDQM7	AM39	OZ		
DDR3BDQM8	AE37	OZ		

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Table 3-2 Terminal Functions — Signals and Control by Function (Part 8 of 20)

Signal Name	Ball No.	Type	IPD/IPU	Description
DDR3BDQS0P	M38	IOZ		DDR3B EMIF data strobe
DDR3BDQS0N	M39	IOZ		
DDR3BDQS1P	P39	IOZ		
DDR3BDQS1N	P38	IOZ		
DDR3BDQS2P	T39	IOZ		
DDR3BDQS2N	T38	IOZ		
DDR3BDQS3P	V39	IOZ		
DDR3BDQS3N	V38	IOZ		
DDR3BDQS4P	AF38	IOZ		
DDR3BDQS4N	AF39	IOZ		
DDR3BDQS5P	AJ39	IOZ		
DDR3BDQS5N	AJ38	IOZ		
DDR3BDQS6P	AL39	IOZ		
DDR3BDQS6N	AL38	IOZ		
DDR3BDQS7P	AN38	IOZ		
DDR3BDQS7N	AN39	IOZ		
DDR3BDQS8P	AE39	IOZ		
DDR3BDQS8N	AE38	IOZ		
DDR3BCB00	AF32	IOZ		DDR3B EMIF check bits
DDR3BCB01	AF34	IOZ		
DDR3BCB02	AE32	IOZ		
DDR3BCB03	AF35	IOZ		
DDR3BCB04	AE33	IOZ		
DDR3BCB05	AE36	IOZ		
DDR3BCB06	AD36	IOZ		
DDR3BCB07	AE34	IOZ		
DDR3BD00	L38	IOZ		DDR3B EMIF data bus
DDR3BD01	N34	IOZ		
DDR3BD02	M37	IOZ		
DDR3BD03	L39	IOZ		
DDR3BD04	N33	IOZ		
DDR3BD05	N37	IOZ		
DDR3BD06	N36	IOZ		
DDR3BD07	N38	IOZ		
DDR3BD08	T32	IOZ		
DDR3BD09	R32	IOZ		
DDR3BD10	P35	IOZ		
DDR3BD11	R39	IOZ		
DDR3BD12	R38	IOZ		
DDR3BD13	N32	IOZ		
DDR3BD14	R33	IOZ		
DDR3BD15	P36	IOZ		

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Table 3-2 Terminal Functions — Signals and Control by Function (Part 9 of 20)

Signal Name	Ball No.	Type	IPD/IPU	Description
DDR3BD16	T34	IOZ		DDR3B EMIF data bus
DDR3BD17	R34	IOZ		
DDR3BD18	T35	IOZ		
DDR3BD19	R37	IOZ		
DDR3BD20	R36	IOZ		
DDR3BD21	U37	IOZ		
DDR3BD22	T36	IOZ		
DDR3BD23	U38	IOZ		
DDR3BD24	V35	IOZ		
DDR3BD25	U36	IOZ		
DDR3BD26	U34	IOZ		
DDR3BD27	W38	IOZ		
DDR3BD28	W39	IOZ		
DDR3BD29	U33	IOZ		
DDR3BD30	V32	IOZ		
DDR3BD31	V36	IOZ		
DDR3BD32	AG37	IOZ		DDR3B EMIF data bus
DDR3BD33	AF36	IOZ		
DDR3BD34	AG38	IOZ		
DDR3BD35	AG34	IOZ		
DDR3BD36	AG36	IOZ		
DDR3BD37	AH34	IOZ		
DDR3BD38	AH35	IOZ		
DDR3BD39	AG32	IOZ		
DDR3BD40	AH32	IOZ		
DDR3BD41	AJ33	IOZ		
DDR3BD42	AH36	IOZ		
DDR3BD43	AJ34	IOZ		
DDR3BD44	AJ36	IOZ		
DDR3BD45	AH39	IOZ		

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Table 3-2 Terminal Functions — Signals and Control by Function (Part 10 of 20)

Signal Name	Ball No.	Type	IPD/IPU	Description
DDR3BD46	AH38	IOZ		DDR3B EMIF data bus
DDR3BD47	AJ37	IOZ		
DDR3BD48	AK39	IOZ		
DDR3BD49	AK38	IOZ		
DDR3BD50	AK36	IOZ		
DDR3BD51	AK35	IOZ		
DDR3BD52	AL34	IOZ		
DDR3BD53	AL36	IOZ		
DDR3BD54	AL37	IOZ		
DDR3BD55	AL33	IOZ		
DDR3BD56	AN34	IOZ		
DDR3BD57	AN36	IOZ		
DDR3BD58	AN33	IOZ		
DDR3BD59	AM34	IOZ		
DDR3BD60	AM35	IOZ		
DDR3BD61	AM38	IOZ		
DDR3BD62	AM36	IOZ		
DDR3BD63	AN37	IOZ		
$\overline{\text{DDR3BCE0}}$	AB34	OZ		DDR3B EMIF chip enable
$\overline{\text{DDR3BCE1}}$	AA36	OZ		DDR3B EMIF chip enable
DDR3BBA0	AA37	OZ		DDR3B EMIF bank address
DDR3BBA1	AA34	OZ		
DDR3BBA2	AB35	OZ		
DDR3BA00	AA32	OZ		DDR3B EMIF address bus
DDR3BA01	W33	OZ		
DDR3BA02	W32	OZ		
DDR3BA03	Y34	OZ		
DDR3BA04	W34	OZ		
DDR3BA05	V34	OZ		
DDR3BA06	W36	OZ		
DDR3BA07	W37	OZ		
DDR3BA08	AA33	OZ		
DDR3BA09	Y32	OZ		
DDR3BA10	Y38	OZ		
DDR3BA11	AA39	OZ		
DDR3BA12	Y35	OZ		
DDR3BA13	Y39	OZ		
DDR3BA14	AA38	OZ		
DDR3BA15	Y36	OZ		
$\overline{\text{DDR3BCAS}}$	AC36	OZ		DDR3B EMIF column address strobe
$\overline{\text{DDR3BRAS}}$	AD32	OZ		DDR3B EMIF row address strobe
$\overline{\text{DDR3BWE}}$	AC37	OZ		DDR3B EMIF write enable
DDR3BCKE0	AB39	OZ		DDR3B EMIF clock enable0
DDR3BCKE1	AB38	OZ		DDR3B EMIF clock enable1

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Table 3-2 Terminal Functions — Signals and Control by Function (Part 11 of 20)

Signal Name	Ball No.	Type	IPD/IPU	Description
DDR3BCLKOUTP0	AD38	OZ		DDR3B EMIF output clocks to drive SDRAM (one clock pair for Rank0)
DDR3BCLKOUTN0	AD39	OZ		
DDR3BCLKOUTP1	AC39	OZ		DDR3B EMIF output clocks to drive SDRAM (one clock pair for Rank1)
DDR3BCLKOUTN1	AC38	OZ		
DDR3BODT0	AC33	OZ		DDR3B EMIF on-die termination outputs used to set termination on the SDRAMs
DDR3BODT1	AD34	OZ		DDR3B EMIF on-die termination outputs used to set termination on the SDRAMs
$\overline{\text{DDR3BRESET}}$	AC32	OZ		DDR3B reset signal
DDR3BRZQ0	AA31	A		PTV compensation pin for DDR3B
DDR3BRZQ1	P32	A		PTV compensation pin for DDR3B
DDR3BRZQ2	AK32	A		PTV compensation pin for DDR3B
EMIF16				
$\overline{\text{EMIFBE0}}$	H34	O	Up	EMIF control signals
$\overline{\text{EMIFBE1}}$	H33	O	Up	
$\overline{\text{EMIFCE0}}$	G33	O	Up	
$\overline{\text{EMIFCE1}}$	G32	O	Up	
$\overline{\text{EMIFCE2}}$	G34	O	Up	
$\overline{\text{EMIFCE3}}$	E36	O	Up	
$\overline{\text{EMIFOE}}$	E37	O	Up	
EMIFR$\overline{\text{W}}$	F33	O	Up	
EMIFWAIT0	E38	I	Down	
EMIFWAIT1	D39	I	Down	
$\overline{\text{EMIFWE}}$	F36	O	Up	
EMIFA00	F34	O	Down	EMIF address
EMIFA01	F37	O	Down	
EMIFA02	G36	O	Down	
EMIFA03	E39	O	Down	
EMIFA04	E34	O	Down	
EMIFA05	J34	O	Down	
EMIFA06	H35	O	Down	
EMIFA07	K33	O	Down	
EMIFA08	C35	O	Down	
EMIFA09	G37	O	Down	
EMIFA10	F38	O	Down	
EMIFA11	D35	O	Down	
EMIFA12	H36	O	Down	
EMIFA13	E35	O	Down	
EMIFA14	G38	O	Down	
EMIFA15	F39	O	Down	

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Table 3-2 Terminal Functions — Signals and Control by Function (Part 12 of 20)

Signal Name	Ball No.	Type	IPD/IPU	Description
EMIFA16	K34	O	Down	EMIF address
EMIFA17	F35	O	Down	
EMIFA18	J35	O	Down	
EMIFA19	G39	O	Down	
EMIFA20	C36	O	Down	
EMIFA21	J36	O	Down	
EMIFA22	H38	O	Down	
EMIFA23	D36	O	Down	
EMIFD00	M32	IOZ	Down	EMIF data
EMIFD01	J37	IOZ	Down	
EMIFD02	L33	IOZ	Down	
EMIFD03	L34	IOZ	Down	
EMIFD04	H39	IOZ	Down	
EMIFD05	J38	IOZ	Down	
EMIFD06	K37	IOZ	Down	
EMIFD07	J39	IOZ	Down	
EMIFD08	K39	IOZ	Down	
EMIFD09	K38	IOZ	Down	
EMIFD10	K36	IOZ	Down	
EMIFD11	L36	IOZ	Down	
EMIFD12	L35	IOZ	Down	
EMIFD13	M34	IOZ	Down	
EMIFD14	M36	IOZ	Down	
EMIFD15	M35	IOZ	Down	
EMU				
EMU00	AA2	IOZ	Up	Emulation and trace port
EMU01	AB2	IOZ	Up	
EMU02	Y3	IOZ	Up	
EMU03	Y4	IOZ	Up	
EMU04	W3	IOZ	Up	
EMU05	W4	IOZ	Up	
EMU06	V4	IOZ	Up	
EMU07	U4	IOZ	Up	
EMU08	U3	IOZ	Up	
EMU09	T3	IOZ	Up	
EMU10	AB4	IOZ	Up	
EMU11	AA3	IOZ	Up	
EMU12	U5	IOZ	Up	
EMU13	T4	IOZ	Up	
EMU14	AB3	IOZ	Up	
EMU15	R3	IOZ	Up	
EMU16	T5	IOZ	Up	
EMU17	R4	IOZ	Up	
EMU18	AA4	IOZ	Up	

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Table 3-2 Terminal Functions — Signals and Control by Function (Part 13 of 20)

Signal Name	Ball No.	Type	IPD/IPU	Description
EMU19†	A32	IOZ	Down	Emulation and trace port († Pins shared with GPIO[17:31])
EMU20†	C31	IOZ	Down	
EMU21†	B32	IOZ	Down	
EMU22†	A33	IOZ	Down	
EMU23†	D33	IOZ	Down	
EMU24†	D31	IOZ	Down	
EMU25†	B35	IOZ	Down	
EMU26†	B33	IOZ	Down	
EMU27†	E31	IOZ	Down	
EMU28†	A34	IOZ	Down	
EMU29†	D32	IOZ	Down	
EMU30†	C33	IOZ	Down	
EMU31†	C34	IOZ	Down	
EMU32†	B36	IOZ	Down	
EMU33†	B34	IOZ	Down	
General Purpose Input/Output (GPIO)				
GPIO00	F29	IOZ	Up	GPIO
GPIO01	B30	IOZ	Down	
GPIO02	D29	IOZ	Down	
GPIO03	A35	IOZ	Down	
GPIO04	B29	IOZ	Down	
GPIO05	E29	IOZ	Down	
GPIO06	D30	IOZ	Down	
GPIO07	C30	IOZ	Down	
GPIO08	A30	IOZ	Down	
GPIO09	G30	IOZ	Down	
GPIO10	F31	IOZ	Down	
GPIO11	E30	IOZ	Down	
GPIO12	F30	IOZ	Down	
GPIO13	A31	IOZ	Down	
GPIO14	E32	IOZ	Down	
GPIO15	B31	IOZ	Down	

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Table 3-2 Terminal Functions — Signals and Control by Function (Part 14 of 20)

Signal Name	Ball No.	Type	IPD/IPU	Description
GPIO16	A36	IOZ	Down	GPIO
GPIO17	A32	IOZ	Down	
GPIO18	C31	IOZ	Down	
GPIO19	B32	IOZ	Down	
GPIO20	A33	IOZ	Down	
GPIO21	D33	IOZ	Down	
GPIO22	D31	IOZ	Down	
GPIO23	B35	IOZ	Down	
GPIO24	B33	IOZ	Down	
GPIO25	E31	IOZ	Down	
GPIO26	A34	IOZ	Down	
GPIO27	D32	IOZ	Down	
GPIO28	C33	IOZ	Down	
GPIO29	C34	IOZ	Down	
GPIO30	B36	IOZ	Down	
GPIO31	B34	IOZ	Down	
HyperLink0				
HYP0RXN0	AW10	I		HyperLink0 receive data
HYP0RXP0	AW11	I		
HYP0RXN1	AU10	I		
HYP0RXP1	AU11	I		
HYP0RXN2	AV9	I		
HYP0RXP2	AV10	I		
HYP0RXN3	AW7	I		
HYP0RXP3	AW8	I		
HYP0TXN0	AP11	O		HyperLink0 transmit data
HYP0TXP0	AP12	O		
HYP0TXN1	AR10	O		
HYP0TXP1	AR11	O		
HYP0TXN2	AP8	O		
HYP0TXP2	AP9	O		
HYP0TXN3	AR7	O		
HYP0TXP3	AR8	O		
HYP0RXFLCLK	AJ5	O	Down	HyperLink0 sideband signals
HYP0RXFLDAT	AJ4	O	Down	
HYP0TXFLCLK	AJ3	I	Down	
HYP0TXFLDAT	AG5	I	Down	
HYP0RXPMCLK	AJ2	I	Down	
HYP0RXPMDAT	AG3	I	Down	
HYP0TXPMCLK	AH5	O	Down	
HYP0TXPMDAT	AJ1	O	Down	
HYP0REFRES	AM9	A		HyperLink0 SerDes reference resistor input (3 kΩ +/- 1%)

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Table 3-2 Terminal Functions — Signals and Control by Function (Part 15 of 20)

Signal Name	Ball No.	Type	IPD/IPU	Description
HyperLink1				
HYP1RXN0	AU7	I		HyperLink1 receive data
HYP1RXP0	AU8	I		
HYP1RXN1	AV6	I		
HYP1RXP1	AV7	I		
HYP1RXN2	AU4	I		
HYP1RXP2	AU5	I		
HYP1RXN3	AV3	I		
HYP1RXP3	AV4	I		
HYP1TXN0	AT6	O		HyperLink1 transmit data
HYP1TXP0	AT7	O		
HYP1TXN1	AP5	O		
HYP1TXP1	AP6	O		
HYP1TXN2	AR4	O		
HYP1TXP2	AR5	O		
HYP1TXN3	AT3	O		
HYP1TXP3	AT4	O		
HYP1RXFLCLK	AH4	O	Down	HyperLink1 sideband signals
HYP1RXFLDAT	AG2	O	Down	
HYP1TXFLCLK	AH3	I	Down	
HYP1TXFLDAT	AH2	I	Down	
HYP1RXPMCLK	AF3	I	Down	
HYP1RXPMDAT	AF4	I	Down	
HYP1TXPMCLK	AH1	O	Down	
HYP1TXPMDAT	AF2	O	Down	
HYP1REFRES	AM6	A		HyperLink1 SerDes reference resistor input (3 kΩ +/- 1%)
I^2C				
SCL0	N1	IOZ		I^2C0 clock
SCL1	N4	IOZ		I^2C1 clock
SCL2	P4	IOZ		I^2C2 clock
SDA0	P3	IOZ		I^2C0 data
SDA1	N2	IOZ		I^2C1 data
SDA2	N3	IOZ		I^2C2 data
JTAG				
TCK	AE1	I	Up	JTAG clock input
TDI	AG1	I	Up	JTAG data input
TDO	AF1	OZ	Up	JTAG data output
TMS	AE2	I	Up	JTAG test mode input
$\overline{TRST}$	AD1	I	Down	JTAG reset
MDIO				
MDCLK	AP31	O	Down	MDIO clock
MDIO	AR32	IOZ	Up	MDIO data

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Table 3-2 Terminal Functions — Signals and Control by Function (Part 16 of 20)

Signal Name	Ball No.	Type	IPD/IPU	Description
PCIe				
PCIERXN0	AU31	I		PCIexpress lane 0 receive data
PCIERXP0	AU32	I		
PCIERXN1	AV30	I		PCIexpress lane 1 receive data
PCIERXP1	AV31	I		
PCIETXN0	AT30	O		PCIexpress lane 0 transmit data
PCIETXP0	AT31	O		
PCIETXN1	AR29	O		PCIexpress lane 1 transmit data
PCIETXP1	AR30	O		
PCIEREFRES	AM26	A		PCIexpress SerDes reference resistor input (3 kΩ +/- 1%)
Serial RapidIO				
RIORXN0	AV24	I		Serial RapidIO lane 0 receive data
RIORXP0	AV25	I		
RIORXN1	AU22	I		Serial RapidIO lane 1 receive data
RIORXP1	AU23	I		
RIORXN2	AW22	I		Serial RapidIO lane 2 receive data
RIORXP2	AW23	I		
RIORXN3	AV21	I		Serial RapidIO lane 3 receive data
RIORXP3	AV22	I		
RIOTXN0	AT24	O		Serial RapidIO lane 0 transmit data
RIOTXP0	AT25	O		
RIOTXN1	AR23	O		Serial RapidIO lane 1 transmit data
RIOTXP1	AR24	O		
RIOTXN2	AP22	O		Serial RapidIO lane 2 transmit data
RIOTXP2	AP23	O		
RIOTXN3	AT21	O		Serial RapidIO lane 3 transmit data
RIOTXP3	AT22	O		
RIOREFRES	AM21	A		Serial RapidIO SerDes reference resistor input (3 kΩ +/- 1%)
SGMII				
SGMII0RXN	AW28	I		Ethernet MAC SGMII port 0 receive data
SGMII0RXP	AW29	I		
SGMII0TXN	AU28	O		Ethernet MAC SGMII port 0 transmit data
SGMII0TXP	AU29	O		
SGMII1RXN	AV27	I		Ethernet MAC SGMII port 1 receive data
SGMII1RXP	AV28	I		
SGMII1TXN	AT27	O		Ethernet MAC SGMII port 1 transmit data
SGMII1TXP	AT28	O		
SGMII2RXN	AU25	I		Ethernet MAC SGMII port 2 receive data
SGMII2RXP	AU26	I		
SGMII2TXN	AR26	O		Ethernet MAC SGMII port 2 transmit data
SGMII2TXP	AR27	O		
SGMII3RXN	AW25	I		Ethernet MAC SGMII port 3 receive data
SGMII3RXP	AW26	I		

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Table 3-2 Terminal Functions — Signals and Control by Function (Part 17 of 20)

Signal Name	Ball No.	Type	IPD/IPU	Description
SGMII3TXN	AP25	O		Ethernet MAC SGMII port 3 transmit data
SGMII3TXP	AP26	O		
SGMIIREFRES	AM24	A		SGMII SerDes reference resistor input (3 kΩ +/- 1%)
SmartReflex				
VCL	AP36	IOZ		Voltage control I^2C clock
VCNTL0	AT39	OZ		Voltage control outputs to variable core power supply
VCNTL1	AR37	OZ		
VCNTL2	AR36	OZ		
VCNTL3	AT38	OZ		
VCNTL4	AU38	OZ		
VCNTL5	AR35	OZ		
VD	AP35	IOZ		Voltage control I^2C data
SPI0				
SPI0CLK	B26	OZ	Down	SPI0 clock
SPI0DIN	A26	I	Down	SPI0 data in
SPI0DOUT	A27	OZ	Down	SPI0 data out
SPI0SCS0	F25	OZ	Up	SPI0 interface enable 0
SPI0SCS1	C25	OZ	Up	SPI0 interface enable 1
SPI0SCS2	E26	OZ	Up	SPI0 interface enable 2
SPI0SCS3	D26	OZ	Up	SPI0 interface enable 3
SPI1				
SPI1CLK	C28	OZ	Down	SPI1 clock
SPI1DIN	F27	I	Down	SPI1 data in
SPI1DOUT	A28	OZ	Down	SPI1 data out
SPI1SCS0	B27	OZ	Up	SPI1 interface enable 0
SPI1SCS1	C27	OZ	Up	SPI1 interface enable 1
SPI1SCS2	D27	OZ	Up	SPI1 interface enable 2
SPI1SCS3	E27	OZ	Up	SPI1 interface enable 3
SPI2				
SPI2CLK	D25	OZ	Down	SPI2 clock
SPI2DIN	F28	I	Down	SPI2 data in
SPI2DOUT	G28	OZ	Down	SPI2 data out
SPI2SCS0	B28	OZ	Up	SPI2 interface enable 0
SPI2SCS1	D28	OZ	Up	SPI2 interface enable 1
SPI2SCS2	A29	OZ	Up	SPI2 interface enable 2
SPI2SCS3	E25	OZ	Up	SPI2 interface enable 3
Sync-Ethernet / IEEE1588				
TSCOMPOUT	AB1	O	Down	IEEE1588 compare output.
TSPUSHEVT0	AC2	IOZ	Down	PPS push event from GPS for IEEE1588
TSPUSHEVT1	AC1	IOZ	Down	Push event from BCN for IEEE1588
TSSYNCEVT	AC3	O	Down	IEEE1588 sync event output.
Timer				
TIMI0	M2	I	Down	Timer inputs
TIMI1	M1	I	Down	

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Table 3-2 Terminal Functions — Signals and Control by Function (Part 18 of 20)

Signal Name	Ball No.	Type	IPD/IPU	Description
TIMO0	M3	OZ	Down	Timer outputs
TIMO1	M4	OZ	Down	
UART0				
UART0CTS	L1	I	Down	UART0
UART0RTS	L4	OZ	Down	
UART0RXD	K4	I	Down	
UART0TXD	K2	OZ	Down	
UART1				
UART1CTS	K1	I	Down	UART1
UART1RTS	M5	OZ	Down	
UART1RXD	L2	I	Down	
UART1TXD	K3	OZ	Down	
USB 3.0				
USBCLKM	V2	I		USB ref clock
USBCLKP	W2	I		
USBDM	T2	IOZ		USB D-
USBDP	U2	IOZ		USB D+
USBDRVVBUS	L3	O	Down	USB DRVVBUS output
USBID0	R1	A		USB ID
USBRX0M	Y1	I		USB receive data
USBRX0P	W1	I		
USBTX0M	V1	O		USB transmit data
USBTX0P	U1	O		
USBVBUS	T1	A		Reserved — leave unconnected
USBRESREF	AA1	P		Reference resistor connection for USB PHY
XGMII				
XFICLKP	AU19	I		XGMII reference clock to drive the XGMII SerDes
XFICLKN	AU20	I		
XFIMDCLK	AR34	O	Down	XGMII MDIO clock
XFIMDIO	AT33	IOZ	Up	XGMII MDIO data
XFIRXN0	AV19	I		Ethernet MAC XGMII port 0 receive data
XFIRXP0	AV18	I		
XFITXN0	AT19	O		Ethernet MAC XGMII port 0 transmit data
XFITXP0	AT18	O		
XFIRXN1	AW20	I		Ethernet MAC XGMII port 1 receive data
XFIRXP1	AW19	I		
XFITXN1	AR20	O		Ethernet MAC XGMII port 1 transmit data
XFITXP1	AR19	O		
XFIREFRES0	AN16	A		XGMII SerDes reference resistor input (3 kΩ +/- 1%)
XFIREFRES1	AM19	A		XGMII SerDes reference resistor input (3 kΩ +/- 1%)
Reserved				
RSV000	P2	OZ	Down	Reserved — leave unconnected
RSV001	P1	OZ	Down	Reserved — leave unconnected

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Table 3-2 Terminal Functions — Signals and Control by Function (Part 19 of 20)

Signal Name	Ball No.	Type	IPD/IPU	Description
RSV002	AN4	O		Reserved — leave unconnected
RSV003	AM4	O		Reserved — leave unconnected
RSV004	B24	O		Reserved — leave unconnected
RSV005	A24	O		Reserved — leave unconnected
RSV006	AP38	O		Reserved — leave unconnected
RSV007	AP39	O		Reserved — leave unconnected
RSV008	AU34	O		Reserved — leave unconnected
RSV009	AT34	O		Reserved — leave unconnected
RSV010	C38	O		Reserved — leave unconnected
RSV011	D38	O		Reserved — leave unconnected
RSV012	AK5	OZ	Down	Reserved — leave unconnected
RSV013	F23	A		Reserved — connect to GND
RSV014	E23	A		Reserved — leave unconnected
RSV015	E33	A		Reserved — leave unconnected
RSV016	F32	A		Reserved — leave unconnected
RSV017	F26	A		Reserved — leave unconnected
RSV018	G26	A		Reserved — leave unconnected
RSV019	AN10	A		Reserved — leave unconnected
RSV020	AM7	A		Reserved — leave unconnected
RSV021	AM23	A		Reserved — leave unconnected
RSV022	AM28	A		Reserved — leave unconnected
RSV023	AM25	A		Reserved — leave unconnected
RSV024	AM16	A		Reserved — leave unconnected
RSV025	AM14	A		Reserved — leave unconnected
RSV026	AN19	A		Reserved — leave unconnected
RSV027	D12	OZ		Reserved — leave unconnected
RSV028	D13	OZ		Reserved — leave unconnected
RSV029	F13	A		Reserved — leave unconnected
RSV030	AD35	OZ		Reserved — leave unconnected
RSV031	AC34	OZ		Reserved — leave unconnected
RSV032	AB32	A		Reserved — leave unconnected
RSV033	AN32	OZ		Reserved — leave unconnected
RSV034	AP32	IOZ		Reserved — leave unconnected
RSV035	AP33	OZ		Reserved — leave unconnected
RSV036	B37	I		Reserved — leave unconnected
RSV037	C37	I		Reserved — leave unconnected
RSV038	AT37	IOZ		Reserved — connect to VCL
RSV039	AU36	OZ		Reserved — connect to VCNTL0
RSV040	AV37	OZ		Reserved — connect to VCNTL1
RSV041	AU37	OZ		Reserved — connect to VCNTL2
RSV042	AV36	OZ		Reserved — connect to VCNTL3
RSV043	AU35	OZ		Reserved — connect to VCNTL4
RSV044	AW36	OZ		Reserved — connect to VCNTL5
RSV045	AT35	IOZ		Reserved — connect to VDT

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Table 3-2 Terminal Functions — Signals and Control by Function (Part 20 of 20)

Signal Name	Ball No.	Type	IPD/IPU	Description
RSV046	N28	P		Reserved — Connect to AVDDA1
RSV047	H31			Reserved — Connect to CVDD
RSV048	J30	P		Reserved — Connect to CVDD
RSV049	K29	P		Reserved — Connect to CVDD
RSV050	L28	P		Reserved — Connect to CVDD
RSV051	M27	P		Reserved — Connect to CVDD
RSV052	N24	P		Reserved — Connect to CVDD
RSV053	N26	P		Reserved — Connect to CVDD
RSV054	P23	P		Reserved — Connect to CVDD
RSV055	P25	P		Reserved — Connect to CVDD
RSV056	R24	P		Reserved — Connect to CVDD
RSV057	R26	P		Reserved — Connect to CVDD
RSV058	T23	P		Reserved — Connect to CVDD
RSV059	T25	P		Reserved — Connect to CVDD
RSV074	U24	P		Reserved — Connect to CVDD
RSV075	U26	P		Reserved — Connect to CVDD
RSV076	V23	P		Reserved — Connect to CVDD
RSV077	V25	P		Reserved — Connect to CVDD
RSV078	W24	P		Reserved — Connect to CVDD
RSV079	W26	P		Reserved — Connect to CVDD
RSV080	R22	P		Reserved — Connect to CVDD1
RSV081	U22	P		Reserved — Connect to CVDD1
RSV082	W22	P		Reserved — Connect to CVDD1
End of Table 3-2				

Table 3-3 Terminal Functions — Power and Ground (Part 1 of 3)

Supply	Ball No.	Volts	Description
AVDDA1	AF11	1.8 V	C66x CorePac PLL supply
AVDDA2	N20	1.8 V	DDR3A PLL supply
AVDDA4	AH29	1.8 V	DDR3B PLL supply
AVDDA5	AG26	1.8 V	Network Coprocessor PLL supply
AVDDA6	P11	1.8 V	DDRA DLL supply
AVDDA7	M13	1.8 V	DDRA DLL supply
AVDDA8	M15	1.8 V	DDRA DLL supply
AVDDA9	M18	1.8 V	DDRA DLL supply
AVDDA10	M20	1.8 V	DDRA DLL supply
AVDDA11	Y28	1.8 V	DDRB DLL supply
AVDDA12	AB28	1.8 V	DDRB DLL supply
AVDDA13	AC28	1.8 V	DDRB DLL supply
AVDDA14	AD28	1.8 V	DDRB DLL supply
AVDDA15	AE28	1.8 V	DDRB DLL supply

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Table 3-3 Terminal Functions — Power and Ground (Part 2 of 3)

Supply	Ball No.	Volts	Description
CVDD	L6, M7, M9, M25, N6, N8, N10, N12, N14, N16, N18, N22, P7, P9, P13, P15, P17, P19, P21, P27, R8, R10, R12, R14, R16, R18, R20, T9, T11, T15, T17, T19, T27, U8, U10, U12, U18, V9, V15, V19, V27, W8, W10, W12, W14, W18, W20, Y9, Y15, Y17, Y19, Y21, Y23, Y25, Y27, AA8, AA10, AA16, AA18, AA20, AA22, AA24, AA26, AB9, AB11, AB15, AB17, AB19, AB21, AB23, AB25, AB27, AC8, AC10, AC12, AC14, AC16, AC20, AC22, AC24, AC26, AD9, AD13, AD15, AD21, AD23, AD25, AD27, AE8, AE10, AE12, AE14, AE16, AE18, AE20, AE22, AE24, AE26, AF9, AF25, AF27, AG8, AG10, AG28, AH9, AH27, AJ8, AJ10, AJ28, AK7, AK9, AK29, AL6, AL8, AL30, AM5, AM31	AVS	SmartReflex DSP core supply voltage
CVDD1	T13, T21, U14, U16, U20, V13, V17, V21, W16, AC18, AD17, AD19	0.95 V	Core supply voltage for memory array
DDR3AVREFSSTL	G14	0.75 V	0.75-V DDR3A reference voltage
DDR3BVREFSSTL	AC31	0.75 V	0.75-V DDR3B reference voltage
DVDD15	H7, H9, H11, H13, H15, H17, H19, H21, H23, J6, J8, J10, J12, J14, J16, J18, J20, J22, K7, K9, K11, K13, K15, K17, K19, K21, K23, L8, L10, L12, L14, L16, L18, L20, L32, M11, M17, M19, M31, P29, P31, R28, R30, T29, T31, U28, U30, V29, V31, W28, W30, Y29, Y31, AA28, AA30, AB29, AB31, AC30, AD29, AD31, AE30, AF29, AF31, AG30, AH31, AJ30, AK31, AL32	1.5 V	1.5-V DDR IO supply
DVDD18	H25, H27, J26, J28, J32, K25, K27, K31, L24, L26, L30, M29, N30, R6, T7, U6, V5, V7, W6, Y5, Y7, AA6, AB5, AB7, AC6, AD7, AE6, AF7, AG6, AJ26, AK27, AL26, AL28, AM27, AM29	1.8 V	1.8-V IO supply
DVDD33	AA14	3.3 V	3.3-V USB supply
VDDAHV	AK11, AK13, AK15, AK17, AK19, AK21, AK23, AK25, AL10, AL12, AL14, AL16, AL18, AL20, AL22, AL24	1.8 V	SerDes IO supply
VDDALV	AF13, AF15, AF17, AF19, AF21, AF23, AG12, AG14, AG16, AG18, AG20, AG22, AH11, AH13, AH15, AH17, AH19, AH21, AH23, AH25, AJ12, AJ14, AJ16, AJ18, AJ20, AJ22, AJ24	0.85 V	SerDes low voltage
VDDUSB	AB13	0.85 V	SerDes digital IO supply
VNWA1	AG24	0.95 V	Fixed Nwell supply
VNWA2	AD11	0.95 V	Fixed Nwell supply
VNWA3	M23	0.95 V	Fixed Nwell supply
VNWA4	V11	0.95 V	Fixed Nwell supply
VP	AA12	0.85 V	Filtered 0.85-V supply
VPH	Y13	3.3 V	Filtered 3.3-V USB supply
VPP	L22, M21		Leave unconnected

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Table 3-3 Terminal Functions — Power and Ground (Part 3 of 3)

Supply	Ball No.	Volts	Description
VPTX	Y11	0.85 V	Filtered 0.85 V
VSS	A2, A3, A37, A38, B1, B2, B38, B39, C1, C4, C6, C8, C10, C12, C14, C16, C18, C20, C22, C24, C26, C29, C32, C39, D34, D37, E3, E5, E7, E9, E11, E13, E15, E17, E19, E21, E28, G23, G25, G27, G29, G31, G35, H4, H6, H8, H12, H14, H18, H20, H24, H26, H28, H29, H30, H32, H37, J1, J2, J3, J4, J5, J7, J9, J11, J13, J15, J17, J19, J21, J23, J24, J25, J27, J29, J31, J33, K5, K6, K8, K10, K12, K14, K16, K18, K20, K22, K24, K26, K28, K30, K32, K35, L5, L7, L9, L11, L13, L15, L17, L19, L21, L23, L25, L27, L29, L31, L37, M6, M8, M10, M12, M14, M16, M22, M24, M26, M28, M30, M33, N5, N7, N9, N11, N13, N15, N17, N19, N21, N23, N25, N27, N29, N31, N35, P5, P6, P8, P10, P12, P14, P16, P18, P20, P22, P24, P26, P28, P30, P33, P37, R2, R5, R7, R9, R11, R13, R15, R17, R19, R21, R23, R25, R27, R29, R31, R35, T6, T8, T10, T12, T14, T16, T18, T20, T22, T24, T26, T28, T30, T33, T37, U7, U9, U11, U13, U15, U17, U19, U21, U23, U25, U27, U29, U31, U35, V3, V6, V8, V10, V12, V14, V16, V18, V20, V22, V24, V26, V28, V30, V33, V37, W5, W7, W9, W11, W13, W15, W17, W19, W21, W23, W25, W27, W29, W31, W35, Y2, Y6, Y8, Y10, Y12, Y14, Y16, Y18, Y20, Y22, Y24, Y26, Y30, Y33, Y37, AA5, AA7, AA9, AA11, AA13, AA15, AA17, AA19, AA21, AA23, AA25, AA27, AA29, AA35, AB6, AB8, AB10, AB12, AB14, AB16, AB18, AB20, AB22, AB24, AB26, AB30, AB33, AB36, AB37, AC7, AC9, AC11, AC13, AC15, AC17, AC19, AC21, AC23, AC25, AC27, AC29, AC35, AD6, AD8, AD10, AD12, AD14, AD16, AD18, AD20, AD22, AD24, AD26, AD30, AD33, AD37, AE3, AE7, AE9, AE11, AE13, AE15, AE17, AE19, AE21, AE23, AE25, AE27, AE29, AE31, AE35, AF6, AF8, AF10, AF12, AF14, AF16, AF18, AF20, AF22, AF24, AF26, AF28, AF30, AF33, AF37, AG4, AG7, AG9, AG11, AG13, AG15, AG17, AG19, AG21, AG23, AG25, AG27, AG29, AG31, AG35, AH6, AH7, AH8, AH10, AH12, AH14, AH16, AH18, AH20, AH22, AH24, AH26, AH28, AH30, AH33, AH37, AJ6, AJ7, AJ9, AJ11, AJ13, AJ15, AJ17, AJ19, AJ21, AJ23, AJ25, AJ27, AJ29, AJ31, AJ32, AJ35, AK2, AK6, AK8, AK10, AK12, AK14, AK16, AK18, AK20, AK22, AK24, AK26, AK28, AK30, AK33, AK37, AL5, AL7, AL9, AL11, AL13, AL15, AL17, AL19, AL21, AL23, AL25, AL27, AL29, AL31, AL35, AM3, AM8, AM10, AM12, AM13, AM17, AM18, AM20, AM22, AM32, AM33, AM37, AN2, AN5, AN6, AN7, AN8, AN9, AN11, AN12, AN13, AN14, AN15, AN17, AN18, AN20, AN21, AN22, AN23, AN24, AN25, AN26, AN27, AN28, AN29, AN31, AN35, AP4, AP7, AP10, AP13, AP16, AP19, AP20, AP21, AP24, AP27, AP28, AP29, AP30, AP37, AR3, AR6, AR9, AR12, AR15, AR18, AR21, AR22, AR25, AR28, AR31, AR33, AT2, AT5, AT8, AT11, AT14, AT17, AT20, AP27, AP28, AP29, AP30, AP37, AR3, AR6, AR9, AR12, AR15, AR18, AR21, AR22, AR25, AR28, AR31, AR33, AT2, AT5, AT8, AT11, AT14, AT17, AT20, AT23, AT26, AT29, AT32, AT36, AU1, AU2, AU3, AU6, AU9, AU12, AU15, AU18, AU21, AU24, AU27, AU30, AU33, AU39, AV1, AV2, AV5, AV8, AV11, AV14, AV17, AV20, AV23, AV26, AV29, AV32, AV35, AV38, AV39, AW2, AW3, AW6, AW9, AW12, AW15, AW18, AW21, AW24, AW27, AW30, AW33, AW37, AW38	GND	Ground
End of Table 3-3			

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Table 3-4 Terminal Functions — By Signal Name (Part 1 of 22)

Signal Name	Ball Number
(nopin)	A1
(nopin)	A39
(nopin)	AW1
(nopin)	AW39
AIFREFRES0	AM15
AIFREFRES1	AM11
AIFRXN0	AW16
AIFRXP0	AW17
AIFRXN1	AU16
AIFRXP1	AU17
AIFRXN2	AV15
AIFRXP2	AV16
AIFRXN3	AW13
AIFRXP3	AW14
AIFRXN4	AU13
AIFRXN5	AV12
AIFRXP4	AU14
AIFRXP5	AV13
AIFTXN0	AP17
AIFTXP0	AP18
AIFTXN1	AR16
AIFTXP1	AR17
AIFTXN2	AT15
AIFTXP2	AT16
AIFTXN3	AP14
AIFTXP3	AP15
AIFTXN4	AR13
AIFTXP4	AR14
AIFTXN5	AT12
AIFTXP5	AT13
ALTCORECLKN	AL2
ALTCORECLKP	AM2
AVDDA1	AF11
AVDDA2	N20
AVDDA4	AH29
AVDDA5	AG26
AVDDA6	P11
AVDDA7	M13
AVDDA8	M15
AVDDA9	M18
AVDDA10	M20
AVDDA11	Y28

Table 3-4 Terminal Functions — By Signal Name (Part 2 of 22)

Signal Name	Ball Number
AVDDA12	AB28
AVDDA13	AC28
AVDDA14	AD28
AVDDA15	AE28
AVSIFSEL0†	M2
AVSIFSEL1†	M1
BOOTMODE00†	B30
BOOTMODE01†	D29
BOOTMODE02†	A35
BOOTMODE03†	B29
BOOTMODE04†	E29
BOOTMODE05†	D30
BOOTMODE06†	C30
BOOTMODE07†	A30
BOOTMODE08†	G30
BOOTMODE09†	F31
BOOTMODE10†	E30
BOOTMODE11†	F30
BOOTMODE12†	A31
BOOTMODE13†	F24
BOOTMODE14†	E24
BOOTMODE15†	D24
BOOTCOMPLETE	AF5
CORECLKSEL	AL4
CORESEL0	F24
CORESEL1	E24
CORESEL2	D24
CORESEL3	G24
CVDD	L6, M7, M9, M25, N6, N8, N10, N12, N14, N16, N18, N22, P7, P9, P13, P15, P17, P19, P21, P27, R8, R10, R12, R14, R16, R18, R20, T9, T11, T15, T17, T19, T27
CVDD	U8, U10, U12, U18, V9, V15, V19, V27, W8, W10, W12, W14, W18, W20, Y9, Y15, Y17, Y19, Y21, Y23, Y25, Y27, AA8, AA10, AA16, AA18, AA20, AA22, AA24

Table 3-4 Terminal Functions — By Signal Name (Part 3 of 22)

Signal Name	Ball Number
CVDD	AA26, AB9, AB11, AB15, AB17, AB19, AB21, AB23, AB25, AB27, AC8, AC10, AC12, AC14, AC16, AC20, AC22, AC24, AC26, AD9, AD13, AD15, AD21, AD23
CVDD	AD25, AD27, AE8, AE10, AE12, AE14, AE16, AE18, AE20, AE22, AE24, AE26, AF9, AF25, AF27, AG8, AG10, AG28, AH9, AH27, AJ8, AJ10, AJ28, AK7
CVDD	AK9, AK29, AL6, AL8, AL30, AM5, AM31
CVDD1	T13, T21, U14, U16, U20, V13, V17, V21, W16, AC18, AD17, AD19
DDR3AA00	E8
DDR3AA01	G9
DDR3AA02	G8
DDR3AA03	G10
DDR3AA04	F9
DDR3AA05	F8
DDR3AA06	C9
DDR3AA07	D9
DDR3AA08	B9
DDR3AA09	D8
DDR3AA10	F10
DDR3AA11	A9
DDR3AA12	E10
DDR3AA13	A10
DDR3AA14	B10
DDR3AA15	D10
DDR3ABA0	B11
DDR3ABA1	C11
DDR3ABA2	G11
$\overline{\text{DDR3ACAS}}$	C13
DDR3ACB00	A16
DDR3ACB01	C15
DDR3ACB02	B16
DDR3ACB03	F15
DDR3ACB04	D15
DDR3ACB05	F14
DDR3ACB06	D14

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Table 3-4 Terminal Functions — By Signal Name (Part 4 of 22)

Signal Name	Ball Number
DDR3ACB07	G15
DDR3ACE0	D11
DDR3ACE1	F11
DDR3ACKE0	G12
DDR3ACKE1	A11
DDR3ACLKN	A25
DDR3ACLKOUTN0	B12
DDR3ACLKOUTN1	B13
DDR3ACLKOUTP0	A12
DDR3ACLKOUTP1	A13
DDR3ACLKP	B25
DDR3AD00	G1
DDR3AD01	H2
DDR3AD02	F1
DDR3AD03	G2
DDR3AD04	H1
DDR3AD05	E2
DDR3AD06	F2
DDR3AD07	D2
DDR3AD08	E4
DDR3AD09	F4
DDR3AD10	G3
DDR3AD11	A4
DDR3AD12	B4
DDR3AD13	H3
DDR3AD14	D3
DDR3AD15	D4
DDR3AD16	G4
DDR3AD17	H5
DDR3AD18	D5
DDR3AD19	F5
DDR3AD20	G5
DDR3AD21	D6
DDR3AD22	C5
DDR3AD23	B6
DDR3AD24	C7
DDR3AD25	F7
DDR3AD26	F6
DDR3AD27	A8
DDR3AD28	B8
DDR3AD29	G6
DDR3AD30	G7

Table 3-4 Terminal Functions — By Signal Name (Part 5 of 22)

Signal Name	Ball Number
DDR3AD31	D7
DDR3AD32	E16
DDR3AD33	G16
DDR3AD34	F16
DDR3AD35	G17
DDR3AD36	D16
DDR3AD37	D17
DDR3AD38	F17
DDR3AD39	E18
DDR3AD40	C19
DDR3AD41	D19
DDR3AD42	G18
DDR3AD43	F19
DDR3AD44	G19
DDR3AD45	B18
DDR3AD46	D18
DDR3AD47	F18
DDR3AD48	A20
DDR3AD49	B20
DDR3AD50	D20
DDR3AD51	G20
DDR3AD52	C21
DDR3AD53	E20
DDR3AD54	F20
DDR3AD55	G21
DDR3AD56	C23
DDR3AD57	G22
DDR3AD58	D23
DDR3AD59	F22
DDR3AD60	E22
DDR3AD61	B22
DDR3AD62	F21
DDR3AD63	D22
DDR3ADQM0	C2
DDR3ADQM1	F3
DDR3ADQM2	A6
DDR3ADQM3	E6
DDR3ADQM4	C17
DDR3ADQM5	A18
DDR3ADQM6	D21
DDR3ADQM7	A22
DDR3ADQM8	E14

Table 3-4 Terminal Functions — By Signal Name (Part 6 of 22)

Signal Name	Ball Number
DDR3ADQS0N	D1
DDR3ADQS0P	E1
DDR3ADQS1N	C3
DDR3ADQS1P	B3
DDR3ADQS2N	B5
DDR3ADQS2P	A5
DDR3ADQS3N	A7
DDR3ADQS3P	B7
DDR3ADQS4N	B17
DDR3ADQS4P	A17
DDR3ADQS5N	A19
DDR3ADQS5P	B19
DDR3ADQS6N	B21
DDR3ADQS6P	A21
DDR3ADQS7N	B23
DDR3ADQS7P	A23
DDR3ADQS8N	A15
DDR3ADQS8P	B15
DDR3AODT0	E12
DDR3AODT1	G13
DDR3ARAS	A14
DDR3ARESET	B14
DDR3ARZQ0	H16
DDR3ARZQ1	H10
DDR3ARZQ2	H22
DDR3AVREFSSTL	G14
DDR3AWE	F12
DDR3BA00	AA32
DDR3BA01	W33
DDR3BA02	W32
DDR3BA03	Y34
DDR3BA04	W34
DDR3BA05	V34
DDR3BA06	W36
DDR3BA07	W37
DDR3BA08	AA33
DDR3BA09	Y32
DDR3BA10	Y38
DDR3BA11	AA39
DDR3BA12	Y35
DDR3BA13	Y39
DDR3BA14	AA38

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Table 3-4 Terminal Functions — By Signal Name (Part 7 of 22)

Signal Name	Ball Number
DDR3BA15	Y36
DDR3BBA0	AA37
DDR3BBA1	AA34
DDR3BBA2	AB35
$\overline{\text{DDR3BCAS}}$	AC36
DDR3BCB00	AF32
DDR3BCB01	AF34
DDR3BCB02	AE32
DDR3BCB03	AF35
DDR3BCB04	AE33
DDR3BCB05	AE36
DDR3BCB06	AD36
DDR3BCB07	AE34
$\overline{\text{DDR3BCE0}}$	AB34
$\overline{\text{DDR3BCE1}}$	AA36
DDR3BCKE0	AB39
DDR3BCKE1	AB38
DDR3BCLKN	AR39
DDR3BCLKOUTN0	AD39
DDR3BCLKOUTN1	AC38
DDR3BCLKOUTP0	AD38
DDR3BCLKOUTP1	AC39
DDR3BCLKP	AR38
DDR3BD00	L38
DDR3BD01	N34
DDR3BD02	M37
DDR3BD03	L39
DDR3BD04	N33
DDR3BD05	N37
DDR3BD06	N36
DDR3BD07	N38
DDR3BD08	T32
DDR3BD09	R32
DDR3BD10	P35
DDR3BD11	R39
DDR3BD12	R38
DDR3BD13	N32
DDR3BD14	R33
DDR3BD15	P36
DDR3BD16	T34
DDR3BD17	R34
DDR3BD18	T35

Table 3-4 Terminal Functions — By Signal Name (Part 8 of 22)

Signal Name	Ball Number
DDR3BD19	R37
DDR3BD20	R36
DDR3BD21	U37
DDR3BD22	T36
DDR3BD23	U38
DDR3BD24	V35
DDR3BD25	U36
DDR3BD26	U34
DDR3BD27	W38
DDR3BD28	W39
DDR3BD29	U33
DDR3BD30	V32
DDR3BD31	V36
DDR3BD32	AG37
DDR3BD33	AF36
DDR3BD34	AG38
DDR3BD35	AG34
DDR3BD36	AG36
DDR3BD37	AH34
DDR3BD38	AH35
DDR3BD39	AG32
DDR3BD40	AH32
DDR3BD41	AJ33
DDR3BD42	AH36
DDR3BD43	AJ34
DDR3BD44	AJ36
DDR3BD45	AH39
DDR3BD46	AH38
DDR3BD47	AJ37
DDR3BD48	AK39
DDR3BD49	AK38
DDR3BD50	AK36
DDR3BD51	AK35
DDR3BD52	AL34
DDR3BD53	AL36
DDR3BD54	AL37
DDR3BD55	AL33
DDR3BD56	AN34
DDR3BD57	AN36
DDR3BD58	AN33
DDR3BD59	AM34
DDR3BD60	AM35

Table 3-4 Terminal Functions — By Signal Name (Part 9 of 22)

Signal Name	Ball Number
DDR3BD61	AM38
DDR3BD62	AM36
DDR3BD63	AN37
DDR3BDQM0	N39
DDR3BDQM1	P34
DDR3BDQM2	U39
DDR3BDQM3	U32
DDR3BDQM4	AG33
DDR3BDQM5	AG39
DDR3BDQM6	AK34
DDR3BDQM7	AM39
DDR3BDQM8	AE37
DDR3BDQS0N	M39
DDR3BDQS0P	M38
DDR3BDQS1N	P38
DDR3BDQS1P	P39
DDR3BDQS2N	T38
DDR3BDQS2P	T39
DDR3BDQS3N	V38
DDR3BDQS3P	V39
DDR3BDQS4N	AF39
DDR3BDQS4P	AF38
DDR3BDQS5N	AJ38
DDR3BDQS5P	AJ39
DDR3BDQS6N	AL38
DDR3BDQS6P	AL39
DDR3BDQS7N	AN39
DDR3BDQS7P	AN38
DDR3BDQS8N	AE38
DDR3BDQS8P	AE39
DDR3BODT0	AC33
DDR3BODT1	AD34
$\overline{\text{DDR3BRAS}}$	AD32
$\overline{\text{DDR3BRESET}}$	AC32
DDR3BRZQ0	AA31
DDR3BRZQ1	P32
DDR3BRZQ2	AK32
DDR3BVREFSSTL	AC31
$\overline{\text{DDR3BWE}}$	AC37

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Table 3-4 Terminal Functions — By Signal Name (Part 10 of 22)

Signal Name	Ball Number
DVDD15	H7, H9, H11, H13, H15, H17, H19, H21, H23, J6, J8, J10, J12, J14, J16, J18, J20, J22, K7, K9, K11, K13, K15, K17, K19, K21, K23, L8, L10, L12, L14, L16, L18, L20
DVDD15	L32, M11, M17, M19, M31, P29, P31, R28, R30, T29, T31, U28, U30, V29, V31, W28, W30, Y29, Y31, AA28, AA30, AB29, AB31, AC30, AD29, AD31, AE30, AF29
DVDD15	AF31, AG30, AH31, AJ30, AK31, AL32
DVDD18	H25, H27, J26, J28, J32, K25, K27, K31, L24, L26, L30, M29, N30, R6, T7, U6, V5, V7, W6, Y5, Y7, AA6, AB5, AB7, AC6, AD7, AE6, AF7, AG6, AJ26, AK27, AL26, AL28, AM27, AM29
DVDD33	AA14
EMIFA00	F34
EMIFA01	F37
EMIFA02	G36
EMIFA03	E39
EMIFA04	E34
EMIFA05	J34
EMIFA06	H35
EMIFA07	K33
EMIFA08	C35
EMIFA09	G37
EMIFA10	F38
EMIFA11	D35
EMIFA12	H36
EMIFA13	E35
EMIFA14	G38
EMIFA15	F39
EMIFA16	K34
EMIFA17	F35
EMIFA18	J35
EMIFA19	G39
EMIFA20	C36
EMIFA21	J36
EMIFA22	H38

Table 3-4 Terminal Functions — By Signal Name (Part 11 of 22)

Signal Name	Ball Number
EMIFA23	D36
$\overline{\text{EMIFBE0}}$	H34
$\overline{\text{EMIFBE1}}$	H33
$\overline{\text{EMIFCE0}}$	G33
$\overline{\text{EMIFCE1}}$	G32
$\overline{\text{EMIFCE2}}$	G34
$\overline{\text{EMIFCE3}}$	E36
EMIFD00	M32
EMIFD01	J37
EMIFD02	L33
EMIFD03	L34
EMIFD04	H39
EMIFD05	J38
EMIFD06	K37
EMIFD07	J39
EMIFD08	K39
EMIFD09	K38
EMIFD10	K36
EMIFD11	L36
EMIFD12	L35
EMIFD13	M34
EMIFD14	M36
EMIFD15	M35
$\overline{\text{EMIFOE}}$	E37
EMIFRNW	F33
EMIFWAIT0	E38
EMIFWAIT1	D39
$\overline{\text{EMIFWE}}$	F36
EMU00	AA2
EMU01	AB2
EMU02	Y3
EMU03	Y4
EMU04	W3
EMU05	W4
EMU06	V4
EMU07	U4
EMU08	U3
EMU09	T3
EMU10	AB4
EMU11	AA3
EMU12	U5
EMU13	T4

Table 3-4 Terminal Functions — By Signal Name (Part 12 of 22)

Signal Name	Ball Number
EMU14	AB3
EMU15	R3
EMU16	T5
EMU17	R4
EMU18	AA4
EXTFRAMEEVENT	AC4
GPIO00	F29
GPIO01	B30
GPIO02	D29
GPIO03	A35
GPIO04	B29
GPIO05	E29
GPIO06	D30
GPIO07	C30
GPIO08	A30
GPIO09	G30
GPIO10	F31
GPIO11	E30
GPIO12	F30
GPIO13	A31
GPIO14	E32
GPIO15	B31
GPIO16	A36
GPIO17	A32
GPIO18	C31
GPIO19	B32
GPIO20	A33
GPIO21	D33
GPIO22	D31
GPIO23	B35
GPIO24	B33
GPIO25	E31
GPIO26	A34
GPIO27	D32
GPIO28	C33
GPIO29	C34
GPIO30	B36
GPIO31	B34
HOUT	AE5
HYP0CLKN	AT10
HYP0CLKP	AT9
HYP0REFRES	AM9

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Table 3-4 Terminal Functions — By Signal Name (Part 13 of 22)

Signal Name	Ball Number
HYP0RXFLCLK	AJ5
HYP0RXFLDAT	AJ4
HYP0RXN0	AW10
HYP0RXN1	AU10
HYP0RXN2	AV9
HYP0RXN3	AW7
HYP0RXP0	AW11
HYP0RXP1	AU11
HYP0RXP2	AV10
HYP0RXP3	AW8
HYP0RXPMCLK	AJ2
HYP0RXPMDAT	AG3
HYP0TXFLCLK	AJ3
HYP0TXFLDAT	AG5
HYP0TXN0	AP11
HYP0TXN1	AR10
HYP0TXN2	AP8
HYP0TXN3	AR7
HYP0TXP0	AP12
HYP0TXP1	AR11
HYP0TXP2	AP9
HYP0TXP3	AR8
HYP0TXPMCLK	AH5
HYP0TXPMDAT	AJ1
HYP1CLKN	AW5
HYP1CLKP	AW4
HYP1REFRES	AM6
HYP1RXFLCLK	AH4
HYP1RXFLDAT	AG2
HYP1RXN0	AU7
HYP1RXN1	AV6
HYP1RXN2	AU4
HYP1RXN3	AV3
HYP1RXP0	AU8
HYP1RXP1	AV7
HYP1RXP2	AU5
HYP1RXP3	AV4
HYP1RXPMCLK	AF3
HYP1RXPMDAT	AF4
HYP1TXFLCLK	AH3
HYP1TXFLDAT	AH2
HYP1TXN0	AT6

Table 3-4 Terminal Functions — By Signal Name (Part 14 of 22)

Signal Name	Ball Number
HYP1TXN1	AP5
HYP1TXN2	AR4
HYP1TXN3	AT3
HYP1TXP0	AT7
HYP1TXP1	AP6
HYP1TXP2	AR5
HYP1TXP3	AT4
HYP1TXPMCLK	AH1
HYP1TXPMDAT	AF2
LENDIAN†	F29
$\overline{\text{LRESETNMIEN}}$	AD4
$\overline{\text{LRESET}}$	AE4
MAINPLLODSEL†	E32
MDCLK	AP31
MDIO	AR32
$\overline{\text{NMI}}$	AD5
PACLKSEL	AN30
PASSCLKN	AV34
PASSCLKP	AV33
PCIECLKN	AW32
PCIECLKP	AW31
PCIEREFRES	AM26
PCIERXN0	AU31
PCIERXN1	AV30
PCIERXP0	AU32
PCIERXP1	AV31
PCIETXN0	AT30
PCIETXN1	AR29
PCIETXP0	AT31
PCIETXP1	AR30
PHYSYNC	AP34
$\overline{\text{POR}}$	AK4
$\overline{\text{RESETFULL}}$	AD3
$\overline{\text{RESETSTAT}}$	AC5
$\overline{\text{RESET}}$	AD2
RADSYNC	AM30
RIOREFRES	AM21
RIORXN0	AV24
RIORXN1	AU22
RIORXN2	AW22
RIORXN3	AV21
RIORXP0	AV25

Table 3-4 Terminal Functions — By Signal Name (Part 15 of 22)

Signal Name	Ball Number
RIORXP1	AU23
RIORXP2	AW23
RIORXP3	AV22
RIOTXN0	AT24
RIOTXN1	AR23
RIOTXN2	AP22
RIOTXN3	AT21
RIOTXP0	AT25
RIOTXP1	AR24
RIOTXP2	AP23
RIOTXP3	AT22
RP1CLKP	AR2
RP1CLKN	AP2
RP1FBP	AR1
RP1FBN	AT1
RSV000	P2
RSV001	P1
RSV002	AN4
RSV003	AM4
RSV004	B24
RSV005	A24
RSV006	AP38
RSV007	AP39
RSV008	AU34
RSV009	AT34
RSV010	C38
RSV011	D38
RSV012	AK5
RSV013	F23
RSV014	E23
RSV015	E33
RSV016	F32
RSV017	F26
RSV018	G26
RSV019	AN10
RSV020	AM7
RSV021	AM23
RSV022	AM28
RSV023	AM25
RSV024	AM16
RSV025	AM14
RSV026	AN19

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Table 3-4 Terminal Functions — By Signal Name (Part 16 of 22)

Signal Name	Ball Number
RSV027	D12
RSV028	D13
RSV029	F13
RSV030	AD35
RSV031	AC34
RSV032	AB32
RSV033	AN32
RSV034	AP32
RSV035	AP33
RSV036	B37
RSV037	C37
RSV038	AT37
RSV039	AU36
RSV040	AV37
RSV041	AU37
RSV042	AV36
RSV043	AU35
RSV044	AW36
RSV045	AT35
RSV046	N28
RSV047	H31
RSV048	J30
RSV049	K29
RSV050	L28
RSV051	M27
RSV052	N24
RSV053	N26
RSV054	P23
RSV055	P25
RSV056	R24
RSV057	R26
RSV058	T23
RSV059	T25
RSV074	U24
RSV075	U26
RSV076	V23
RSV077	V25
RSV078	W24
RSV079	W26
RSV080	R22
RSV081	U22
RSV082	W22

Table 3-4 Terminal Functions — By Signal Name (Part 17 of 22)

Signal Name	Ball Number
SCL0	N1
SCL1	N4
SCL2	P4
SDA0	P3
SDA1	N2
SDA2	N3
SGMII0RXN	AW28
SGMII0RXP	AW29
SGMII0TXN	AU28
SGMII0TXP	AU29
SGMII1RXN	AV27
SGMII1RXP	AV28
SGMII1TXN	AT27
SGMII1TXP	AT28
SGMII2RXN	AU25
SGMII2RXP	AU26
SGMII2TXN	AR26
SGMII2TXP	AR27
SGMII3RXN	AW25
SGMII3RXP	AW26
SGMII3TXN	AP25
SGMII3TXP	AP26
SGMIIREFRES	AM24
SPI0CLK	B26
SPI0DIN	A26
SPI0DOUT	A27
SPI0SCS0	F25
SPI0SCS1	C25
SPI0SCS2	E26
SPI0SCS3	D26
SPI1CLK	C28
SPI1DIN	F27
SPI1DOUT	A28
SPI1SCS0	B27
SPI1SCS1	C27
SPI1SCS2	D27
SPI1SCS3	E27
SPI2CLK	D25
SPI2DIN	F28
SPI2DOUT	G28
SPI2SCS0	B28
SPI2SCS1	D28

Table 3-4 Terminal Functions — By Signal Name (Part 18 of 22)

Signal Name	Ball Number
SPI2SCS2	A29
SPI2SCS3	E25
SRIOSGMIICLKN	AW35
SRIOSGMIICLKP	AW34
SYSCLKN	AK3
SYSCLKOUT	AK1
SYSCLKP	AL3
TCK	AE1
TDI	AG1
TDO	AF1
TIMI0	M2
TIMI1	M1
TIMO0	M3
TIMO1	M4
TMS	AE2
$\overline{\text{TRST}}$	AD1
TSCOMPOUT	AB1
TSPUSHEVT0	AC2
TSPUSHEVT1	AC1
TSREFCLKN	AL1
TSREFCLKP	AM1
TSRXCLKOUT0N	AP1
TSRXCLKOUT0P	AN1
TSRXCLKOUT1N	AP3
TSRXCLKOUT1P	AN3
TSSYNCEVT	AC3
UART0CTS	L1
UART0RTS	L4
UART0RXD	K4
UART0TXD	K2
UART1CTS	K1
UART1RTS	M5
UART1RXD	L2
UART1TXD	K3
USBCLKM	V2
USBCLKP	W2
USBDM	T2
USBDP	U2
USBDRVVBUS	L3
USBID0	R1
USBRESREF	AA1
USBRX0M	Y1

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Table 3-4 Terminal Functions — By Signal Name (Part 19 of 22)

Signal Name	Ball Number
USBRX0P	W1
USBTX0M	V1
USBTX0P	U1
USBVBUS	T1
VCL	AP36
VCNTL0	AT39
VCNTL1	AR37
VCNTL2	AR36
VCNTL3	AT38
VCNTL4	AU38
VCNTL5	AR35
VD	AP35
VDDAHV	AK11, AK13, AK15, AK17, AK19, AK21, AK23, AK25, AL10, AL12, AL14, AL16, AL18, AL20, AL22, AL24
VDDALV	AF13, AF15, AF17, AF19, AF21, AF23, AG12, AG14, AG16, AG18, AG20, AG22, AH11, AH13, AH15, AH17, AH19, AH21, AH23, AH25, AJ12, AJ14, AJ16, AJ18, AJ20, AJ22, AJ24
VDDUSB	AB13
VNWA1	AG24
VNWA2	AD11
VNWA3	M23
VNWA4	V11
VP	AA12
VPH	Y13
VPP	L22, M21
VPTX	Y11
VSS	A2, A3, A37, A38, B1, B2, B38, B39, C1, C4, C6, C8, C10, C12, C14, C16, C18, C20, C22, C24, C26, C29, C32, C39, D34, D37, E3, E5, E7, E9, E11, E13, E15, E17, E19
VSS	E21, E28, G23, G25, G27, G29, G31, G35, H4, H6, H8, H12, H14, H18, H20, H24, H26, H28, H29, H30, H32, H37, J1, J2, J3, J4, J5, J7, J9, J11, J13, J15, J17, J19

Table 3-4 Terminal Functions — By Signal Name (Part 20 of 22)

Signal Name	Ball Number
VSS	J21, J23, J24, J25, J27, J29, J31, J33, K5, K6, K8, K10, K12, K14, K16, K18, K20, K22, K24, K26, K28, K30, K32, K35, L5, L7, L9, L11, L13, L15, L17, L19, L21, L23
VSS	L25, L27, L29, L31, L37, M6, M8, M10, M12, M14, M16, M22, M24, M26, M28, M30, M33, N5, N7, N9, N11, N13, N15, N17, N19, N21, N23, N25, N27, N29
VSS	N31, N35, P5, P6, P8, P10, P12, P14, P16, P18, P20, P22, P24, P26, P28, P30, P33, P37, R2, R5, R7, R9, R11, R13, R15, R17, R19, R21, R23, R25, R27, R29, R31, R35
VSS	T6, T8, T10, T12, T14, T16, T18, T20, T22, T24, T26, T28, T30, T33, T37, U7, U9, U11, U13, U15, U17, U19, U21, U23, U25, U27, U29, U31, U35, V3, V6, V8, V10, V12
VSS	V14, V16, V18, V20, V22, V24, V26, V28, V30, V33, V37, W5, W7, W9, W11, W13, W15, W17, W19, W21, W23, W25, W27, W29, W31, W35, Y2, Y6, Y8, Y10
VSS	Y12, Y14, Y16, Y18, Y20, Y22, Y24, Y26, Y30, Y33, Y37, AA5, AA7, AA9, AA11, AA13, AA15, AA17, AA19, AA21, AA23, AA25, AA27, AA29, AA35, AB6, AB8
VSS	AB10, AB12, AB14, AB16, AB18, AB20, AB22, AB24, AB26, AB30, AB33, AB36, AB37, AC7, AC9, AC11, AC13, AC15, AC17, AC19, AC21, AC23, AC25, AC27

Table 3-4 Terminal Functions — By Signal Name (Part 21 of 22)

Signal Name	Ball Number
VSS	AC29, AC35, AD6, AD8, AD10, AD12, AD14, AD16, AD18, AD20, AD22, AD24, AD26, AD30, AD33, AD37, AE3, AE7, AE9, AE11, AE13, AE15, AE17, AE19
VSS	AE21, AE23, AE25, AE27, AE29, AE31, AE35, AF6, AF8, AF10, AF12, AF14, AF16, AF18, AF20, AF22, AF24, AF26, AF28, AF30, AF33, AF37, AG4, AG7
VSS	AG9, AG11, AG13, AG15, AG17, AG19, AG21, AG23, AG25, AG27, AG29, AG31, AG35, AH6, AH7, AH8, AH10, AH12, AH14, AH16, AH18, AH20, AH22, AH24
VSS	AH26, AH28, AH30, AH33, AH37, AJ6, AJ7, AJ9, AJ11, AJ13, AJ15, AJ17, AJ19, AJ21, AJ23, AJ25, AJ27, AJ29, AJ31, AJ32, AJ35, AK2, AK6, AK8, AK10
VSS	AK12, AK14, AK16, AK18, AK20, AK22, AK24, AK26, AK28, AK30, AK33, AK37, AL5, AL7, AL9, AL11, AL13, AL15, AL17, AL19, AL21, AL23, AL25, AL27, AL29
VSS	AL31, AL35, AM3, AM8, AM10, AM12, AM13, AM17, AM18, AM20, AM22, AM32, AM33, AM37, AN2, AN5, AN6, AN7, AN8, AN9, AN11, AN12, AN13, AN14
VSS	AN15, AN17, AN18, AN20, AN21, AN22, AN23, AN24, AN25, AN26, AN27, AN28, AN29, AN31, AN35, AP4, AP7, AP10, AP13, AP16, AP19, AP20, AP21, AP24

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Table 3-4 Terminal Functions — By Signal Name (Part 22 of 22)

Signal Name	Ball Number
VSS	AP27, AP28, AP29, AP30, AP37, AR3, AR6, AR9, AR12, AR15, AR18, AR21, AR22, AR25, AR28, AR31, AR33, AT2, AT5, AT8, AT11, AT14, AT17, AT20
VSS	AT23, AT26, AT29, AT32, AT36, AU1, AU2, AU3, AU6, AU9, AU12, AU15, AU18, AU21, AU24, AU27, AU30, AU33, AU39, AV1, AV2, AV5, AV8, AV11
VSS	AV14, AV17, AV20, AV23, AV26, AV29, AV32, AV35, AV38, AV39, AW2, AW3, AW6, AW9, AW12, AW15, AW18, AW21, AW24, AW27, AW30, AW33, AW37, AW38
XFICLKN	AU20
XFICLKP	AU19
XFIMDCLK	AR34
XFIMDIO	AT33
XFIREFRES0	AN16
XFIREFRES1	AM19
XFIRXN0	AV19
XFIRXN1	AW20
XFIRXP0	AV18
XFIRXP1	AW19
XFITXN0	AT19
XFITXN1	AR20
XFITXP0	AT18
XFITXP1	AR19
End of Table 3-4	

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Table 3-5 Terminal Functions — By Ball Number (Part 1 of 37)

Ball Number	Signal Name
A1	(nopin)
A2	VSS
A3	VSS
A4	DDR3AD11
A5	DDR3ADQS2P
A6	DDR3ADQM2
A7	DDR3ADQS3N
A8	DDR3AD27
A9	DDR3AA11
A10	DDR3AA13
A11	DDR3ACKE1
A12	DDR3ACLKOUTP0
A13	DDR3ACLKOUTP1
A14	$\overline{\text{DDR3ARAS}}$
A15	DDR3ADQS8N
A16	DDR3ACB00
A17	DDR3ADQS4P
A18	DDR3ADQM5
A19	DDR3ADQS5N
A20	DDR3AD48
A21	DDR3ADQS6P
A22	DDR3ADQM7
A23	DDR3ADQS7P
A24	RSV005
A25	DDR3ACLKN
A26	SPI0DIN
A27	SPI0DOUT
A28	SPI1DOUT
A29	SPI2SCS2
A30	GPIO08
A30	BOOTMODE07†
A31	GPIO13
A31	BOOTMODE12†
A32	GPIO17
A32	EMU19†
A33	GPIO20
A33	EMU22†
A34	GPIO26
A34	EMU28†
A35	GPIO03
A35	BOOTMODE02†
A36	GPIO16

Table 3-5 Terminal Functions — By Ball Number (Part 2 of 37)

Ball Number	Signal Name
A37	VSS
A38	VSS
A39	(nopin)
B1	VSS
B2	VSS
B3	DDR3ADQS1P
B4	DDR3AD12
B5	DDR3ADQS2N
B6	DDR3AD23
B7	DDR3ADQS3P
B8	DDR3AD28
B9	DDR3AA08
B10	DDR3AA14
B11	DDR3ABA0
B12	DDR3ACLKOUTN0
B13	DDR3ACLKOUTN1
B14	$\overline{\text{DDR3ARESET}}$
B15	DDR3ADQS8P
B16	DDR3ACB02
B17	DDR3ADQS4N
B18	DDR3AD45
B19	DDR3ADQS5P
B20	DDR3AD49
B21	DDR3ADQS6N
B22	DDR3AD61
B23	DDR3ADQS7N
B24	RSV004
B25	DDR3ACLKP
B26	SPI0CLK
B27	SPI1SCS0
B28	SPI2SCS0
B29	GPIO04
B29	BOOTMODE03†
B30	GPIO01
B30	BOOTMODE00†
B31	GPIO15
B32	GPIO19
B32	EMU21†
B33	GPIO24
B33	EMU26†
B34	GPIO31
B34	EMU33†

Table 3-5 Terminal Functions — By Ball Number (Part 3 of 37)

Ball Number	Signal Name
B35	GPIO23
B35	EMU25†
B36	GPIO30
B36	EMU32†
B37	RSV036
B38	VSS
B39	VSS
C1	VSS
C2	DDR3ADQM0
C3	DDR3ADQS1N
C4	VSS
C5	DDR3AD22
C6	VSS
C7	DDR3AD24
C8	VSS
C9	DDR3AA06
C10	VSS
C11	DDR3ABA1
C12	VSS
C13	$\overline{\text{DDR3ACAS}}$
C14	VSS
C15	DDR3ACB01
C16	VSS
C17	DDR3ADQM4
C18	VSS
C19	DDR3AD40
C20	VSS
C21	DDR3AD52
C22	VSS
C23	DDR3AD56
C24	VSS
C25	SPI0SCS1
C26	VSS
C27	SPI1SCS1
C28	SPI1CLK
C29	VSS
C30	GPIO07
C30	BOOTMODE06†
C31	GPIO18
C31	EMU20†
C32	VSS
C33	GPIO28

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Table 3-5 Terminal Functions — By Ball Number (Part 4 of 37)

Ball Number	Signal Name
C33	EMU30†
C34	GPIO29
C34	EMU31†
C35	EMIFA08
C36	EMIFA20
C37	RSV037
C38	RSV010
C39	VSS
D1	DDR3ADQS0N
D2	DDR3AD07
D3	DDR3AD14
D4	DDR3AD15
D5	DDR3AD18
D6	DDR3AD21
D7	DDR3AD31
D8	DDR3AA09
D9	DDR3AA07
D10	DDR3AA15
D11	$\overline{\text{DDR3ACE0}}$
D12	RSV027
D13	RSV028
D14	DDR3ACB06
D15	DDR3ACB04
D16	DDR3AD36
D17	DDR3AD37
D18	DDR3AD46
D19	DDR3AD41
D20	DDR3AD50
D21	DDR3ADQM6
D22	DDR3AD63
D23	DDR3AD58
D24	CORESEL2
D25	SPI2CLK
D26	SPI0SCS3
D27	SPI1SCS2
D28	SPI2SCS1
D29	GPIO02
D29	BOOTMODE01†
D30	GPIO06
D30	BOOTMODE05†
D31	GPIO22
D31	EMU24†

Table 3-5 Terminal Functions — By Ball Number (Part 5 of 37)

Ball Number	Signal Name
D32	GPIO27
D32	EMU29†
D33	GPIO21
D33	EMU23†
D34	VSS
D35	EMIFA11
D36	EMIFA23
D37	VSS
D38	RSV011
D39	EMIFWAIT1
E1	DDR3ADQS0P
E2	DDR3AD05
E3	VSS
E4	DDR3AD08
E5	VSS
E6	DDR3ADQM3
E7	VSS
E8	DDR3AA00
E9	VSS
E10	DDR3AA12
E11	VSS
E12	DDR3AODT0
E13	VSS
E14	DDR3ADQM8
E15	VSS
E16	DDR3AD32
E17	VSS
E18	DDR3AD39
E19	VSS
E20	DDR3AD53
E21	VSS
E22	DDR3AD60
E23	RSV014
E24	CORESEL1
E25	SPI2SCS3
E26	SPI0SCS2
E27	SPI1SCS3
E28	VSS
E29	GPIO05
E29	BOOTMODE04†
E30	GPIO11
E30	BOOTMODE10†

Table 3-5 Terminal Functions — By Ball Number (Part 6 of 37)

Ball Number	Signal Name
E31	GPIO25
E31	EMU27†
E32	GPIO14
E32	MAINPLLODSEL†
E33	RSV015
E34	EMIFA04
E35	EMIFA13
E36	$\overline{\text{EMIFCE3}}$
E37	$\overline{\text{EMIFOE}}$
E38	EMIFWAIT0
E39	EMIFA03
F1	DDR3AD02
F2	DDR3AD06
F3	DDR3ADQM1
F4	DDR3AD09
F5	DDR3AD19
F6	DDR3AD26
F7	DDR3AD25
F8	DDR3AA05
F9	DDR3AA04
F10	DDR3AA10
F11	$\overline{\text{DDR3ACE1}}$
F12	$\overline{\text{DDR3AWE}}$
F13	RSV029
F14	DDR3ACB05
F15	DDR3ACB03
F16	DDR3AD34
F17	DDR3AD38
F18	DDR3AD47
F19	DDR3AD43
F20	DDR3AD54
F21	DDR3AD62
F22	DDR3AD59
F23	RSV013
F24	CORESEL0
F25	SPI0SCS0
F26	RSV017
F27	SPI1DIN
F28	SPI2DIN
F29	GPIO00
F30	GPIO12
F30	BOOTMODE11†

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Table 3-5 Terminal Functions — By Ball Number (Part 7 of 37)

Ball Number	Signal Name
F31	GPIO10
F31	BOOTMODE09†
F32	RSV016
F33	EMIFRNW
F34	EMIFA00
F35	EMIFA17
F36	$\overline{\text{EMIFWE}}$
F37	EMIFA01
F38	EMIFA10
F39	EMIFA15
G1	DDR3AD00
G2	DDR3AD03
G3	DDR3AD10
G4	DDR3AD16
G5	DDR3AD20
G6	DDR3AD29
G7	DDR3AD30
G8	DDR3AA02
G9	DDR3AA01
G10	DDR3AA03
G11	DDR3ABA2
G12	DDR3ACKE0
G13	DDR3AODT1
G14	DDR3AVREFSSTL
G15	DDR3ACB07
G16	DDR3AD33
G17	DDR3AD35
G18	DDR3AD42
G19	DDR3AD44
G20	DDR3AD51
G21	DDR3AD55
G22	DDR3AD57
G23	VSS
G24	CORESEL3
G25	VSS
G26	RSV018
G27	VSS
G28	SPI2DOUT
G29	VSS
G30	GPIO09
G30	BOOTMODE08†
G31	VSS

Table 3-5 Terminal Functions — By Ball Number (Part 8 of 37)

Ball Number	Signal Name
G32	$\overline{\text{EMIFCE1}}$
G33	$\overline{\text{EMIFCE0}}$
G34	$\overline{\text{EMIFCE2}}$
G35	VSS
G36	EMIFA02
G37	EMIFA09
G38	EMIFA14
G39	EMIFA19
H1	DDR3AD04
H2	DDR3AD01
H3	DDR3AD13
H4	VSS
H5	DDR3AD17
H6	VSS
H7	DVDD15
H8	VSS
H9	DVDD15
H10	DDR3ARZQ1
H11	DVDD15
H12	VSS
H13	DVDD15
H14	VSS
H15	DVDD15
H16	DDR3ARZQ0
H17	DVDD15
H18	VSS
H19	DVDD15
H20	VSS
H21	DVDD15
H22	DDR3ARZQ2
H23	DVDD15
H24	VSS
H25	DVDD18
H26	VSS
H27	DVDD18
H28	VSS
H29	VSS
H30	VSS
H31	RSV047
H32	VSS
H33	$\overline{\text{EMIFBE1}}$
H34	$\overline{\text{EMIFBE0}}$

Table 3-5 Terminal Functions — By Ball Number (Part 9 of 37)

Ball Number	Signal Name
H35	EMIFA06
H36	EMIFA12
H37	VSS
H38	EMIFA22
H39	EMIFD04
J1	VSS
J2	VSS
J3	VSS
J4	VSS
J5	VSS
J6	DVDD15
J7	VSS
J8	DVDD15
J9	VSS
J10	DVDD15
J11	VSS
J12	DVDD15
J13	VSS
J14	DVDD15
J15	VSS
J16	DVDD15
J17	VSS
J18	DVDD15
J19	VSS
J20	DVDD15
J21	VSS
J22	DVDD15
J23	VSS
J24	VSS
J25	VSS
J26	DVDD18
J27	VSS
J28	DVDD18
J29	VSS
J30	RSV048
J31	VSS
J32	DVDD18
J33	VSS
J34	EMIFA05
J35	EMIFA18
J36	EMIFA21
J37	EMIFD01

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Table 3-5 Terminal Functions — By Ball Number (Part 10 of 37)

Ball Number	Signal Name
J38	EMIFD05
J39	EMIFD07
K1	UART1CTS
K2	UART0TXD
K3	UART1TXD
K4	UART0RXD
K5	VSS
K6	VSS
K7	DVDD15
K8	VSS
K9	DVDD15
K10	VSS
K11	DVDD15
K12	VSS
K13	DVDD15
K14	VSS
K15	DVDD15
K16	VSS
K17	DVDD15
K18	VSS
K19	DVDD15
K20	VSS
K21	DVDD15
K22	VSS
K23	DVDD15
K24	VSS
K25	DVDD18
K26	VSS
K27	DVDD18
K28	VSS
K29	RSV049
K30	VSS
K31	DVDD18
K32	VSS
K33	EMIFA07
K34	EMIFA16
K35	VSS
K36	EMIFD10
K37	EMIFD06
K38	EMIFD09
K39	EMIFD08
L1	UART0CTS

Table 3-5 Terminal Functions — By Ball Number (Part 11 of 37)

Ball Number	Signal Name
L2	UART1RXD
L3	USBDRVVBUS
L4	UART0RTS
L5	VSS
L6	CVDD
L7	VSS
L8	DVDD15
L9	VSS
L10	DVDD15
L11	VSS
L12	DVDD15
L13	VSS
L14	DVDD15
L15	VSS
L16	DVDD15
L17	VSS
L18	DVDD15
L19	VSS
L20	DVDD15
L21	VSS
L22	VPP
L23	VSS
L24	DVDD18
L25	VSS
L26	DVDD18
L27	VSS
L28	RSV050
L29	VSS
L30	DVDD18
L31	VSS
L32	DVDD15
L33	EMIFD02
L34	EMIFD03
L35	EMIFD12
L36	EMIFD11
L37	VSS
L38	DDR3BD00
L39	DDR3BD03
M1	TIMI1
M1	AVSIFSEL1†
M2	TIMI0
M2	AVSIFSEL0†

Table 3-5 Terminal Functions — By Ball Number (Part 12 of 37)

Ball Number	Signal Name
M3	TIMO0
M4	TIMO1
M5	UART1RTS
M6	VSS
M7	CVDD
M8	VSS
M9	CVDD
M10	VSS
M11	DVDD15
M12	VSS
M13	AVDDA7
M14	VSS
M15	AVDDA8
M16	VSS
M17	DVDD15
M18	AVDDA9
M19	DVDD15
M20	AVDDA10
M21	VPP
M22	VSS
M23	VNWA3
M24	VSS
M25	CVDD
M26	VSS
M27	RSV051
M28	VSS
M29	DVDD18
M30	VSS
M31	DVDD15
M32	EMIFD00
M33	VSS
M34	EMIFD13
M35	EMIFD15
M36	EMIFD14
M37	DDR3BD02
M38	DDR3BDQS0P
M39	DDR3BDQS0N
N1	SCL0
N2	SDA1
N3	SDA2
N4	SCL1
N5	VSS

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Table 3-5 Terminal Functions — By Ball Number (Part 13 of 37)

Ball Number	Signal Name
N6	CVDD
N7	VSS
N8	CVDD
N9	VSS
N10	CVDD
N11	VSS
N12	CVDD
N13	VSS
N14	CVDD
N15	VSS
N16	CVDD
N17	VSS
N18	CVDD
N19	VSS
N20	AVDDA2
N21	VSS
N22	CVDD
N23	VSS
N24	RSV052
N25	VSS
N26	RSV053
N27	VSS
N28	RSV046
N29	VSS
N30	DVDD18
N31	VSS
N32	DDR3BD13
N33	DDR3BD04
N34	DDR3BD01
N35	VSS
N36	DDR3BD06
N37	DDR3BD05
N38	DDR3BD07
N39	DDR3BDQM0
P1	RSV001
P2	RSV000
P3	SDA0
P4	SCL2
P5	VSS
P6	VSS
P7	CVDD
P8	VSS

Table 3-5 Terminal Functions — By Ball Number (Part 14 of 37)

Ball Number	Signal Name
P9	CVDD
P10	VSS
P11	AVDDA6
P12	VSS
P13	CVDD
P14	VSS
P15	CVDD
P16	VSS
P17	CVDD
P18	VSS
P19	CVDD
P20	VSS
P21	CVDD
P22	VSS
P23	RSV054
P24	VSS
P25	RSV055
P26	VSS
P27	CVDD
P28	VSS
P29	DVDD15
P30	VSS
P31	DVDD15
P32	DDR3BRZQ1
P33	VSS
P34	DDR3BDQM1
P35	DDR3BD10
P36	DDR3BD15
P37	VSS
P38	DDR3BDQS1N
P39	DDR3BDQS1P
R1	USBID0
R2	VSS
R3	EMU15
R4	EMU17
R5	VSS
R6	DVDD18
R7	VSS
R8	CVDD
R9	VSS
R10	CVDD
R11	VSS

Table 3-5 Terminal Functions — By Ball Number (Part 15 of 37)

Ball Number	Signal Name
R12	CVDD
R13	VSS
R14	CVDD
R15	VSS
R16	CVDD
R17	VSS
R18	CVDD
R19	VSS
R20	CVDD
R21	VSS
R22	RSV080
R23	VSS
R24	RSV056
R25	VSS
R26	RSV057
R27	VSS
R28	DVDD15
R29	VSS
R30	DVDD15
R31	VSS
R32	DDR3BD09
R33	DDR3BD14
R34	DDR3BD17
R35	VSS
R36	DDR3BD20
R37	DDR3BD19
R38	DDR3BD12
R39	DDR3BD11
T1	USBVBUS
T2	USBDM
T3	EMU09
T4	EMU13
T5	EMU16
T6	VSS
T7	DVDD18
T8	VSS
T9	CVDD
T10	VSS
T11	CVDD
T12	VSS
T13	CVDD1
T14	VSS

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Table 3-5 Terminal Functions — By Ball Number (Part 16 of 37)

Ball Number	Signal Name
T15	CVDD
T16	VSS
T17	CVDD
T18	VSS
T19	CVDD
T20	VSS
T21	CVDD1
T22	VSS
T23	RSV058
T24	VSS
T25	RSV059
T26	VSS
T27	CVDD
T28	VSS
T29	DVDD15
T30	VSS
T31	DVDD15
T32	DDR3BD08
T33	VSS
T34	DDR3BD16
T35	DDR3BD18
T36	DDR3BD22
T37	VSS
T38	DDR3BDQS2N
T39	DDR3BDQS2P
U1	USBTX0P
U2	USBDP
U3	EMU08
U4	EMU07
U5	EMU12
U6	DVDD18
U7	VSS
U8	CVDD
U9	VSS
U10	CVDD
U11	VSS
U12	CVDD
U13	VSS
U14	CVDD1
U15	VSS
U16	CVDD1
U17	VSS

Table 3-5 Terminal Functions — By Ball Number (Part 17 of 37)

Ball Number	Signal Name
U18	CVDD
U19	VSS
U20	CVDD1
U21	VSS
U22	RSV081
U23	VSS
U24	RSV074
U25	VSS
U26	RSV075
U27	VSS
U28	DVDD15
U29	VSS
U30	DVDD15
U31	VSS
U32	DDR3BDQM3
U33	DDR3BD29
U34	DDR3BD26
U35	VSS
U36	DDR3BD25
U37	DDR3BD21
U38	DDR3BD23
U39	DDR3BDQM2
V1	USBTX0M
V2	USBCLKM
V3	VSS
V4	EMU06
V5	DVDD18
V6	VSS
V7	DVDD18
V8	VSS
V9	CVDD
V10	VSS
V11	VNWA4
V12	VSS
V13	CVDD1
V14	VSS
V15	CVDD
V16	VSS
V17	CVDD1
V18	VSS
V19	CVDD
V20	VSS

Table 3-5 Terminal Functions — By Ball Number (Part 18 of 37)

Ball Number	Signal Name
V21	CVDD1
V22	VSS
V23	RSV076
V24	VSS
V25	RSV077
V26	VSS
V27	CVDD
V28	VSS
V29	DVDD15
V30	VSS
V31	DVDD15
V32	DDR3BD30
V33	VSS
V34	DDR3BA05
V35	DDR3BD24
V36	DDR3BD31
V37	VSS
V38	DDR3BDQS3N
V39	DDR3BDQS3P
W1	USBRX0P
W2	USBCLKP
W3	EMU04
W4	EMU05
W5	VSS
W6	DVDD18
W7	VSS
W8	CVDD
W9	VSS
W10	CVDD
W11	VSS
W12	CVDD
W13	VSS
W14	CVDD
W15	VSS
W16	CVDD1
W17	VSS
W18	CVDD
W19	VSS
W20	CVDD
W21	VSS
W22	RSV082
W23	VSS

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Table 3-5 Terminal Functions — By Ball Number (Part 19 of 37)

Ball Number	Signal Name
W24	RSV078
W25	VSS
W26	RSV079
W27	VSS
W28	DVDD15
W29	VSS
W30	DVDD15
W31	VSS
W32	DDR3BA02
W33	DDR3BA01
W34	DDR3BA04
W35	VSS
W36	DDR3BA06
W37	DDR3BA07
W38	DDR3BD27
W39	DDR3BD28
Y1	USBRX0M
Y2	VSS
Y3	EMU02
Y4	EMU03
Y5	DVDD18
Y6	VSS
Y7	DVDD18
Y8	VSS
Y9	CVDD
Y10	VSS
Y11	VPTX
Y12	VSS
Y13	VPH
Y14	VSS
Y15	CVDD
Y16	VSS
Y17	CVDD
Y18	VSS
Y19	CVDD
Y20	VSS
Y21	CVDD
Y22	VSS
Y23	CVDD
Y24	VSS
Y25	CVDD
Y26	VSS

Table 3-5 Terminal Functions — By Ball Number (Part 20 of 37)

Ball Number	Signal Name
Y27	CVDD
Y28	AVDDA11
Y29	DVDD15
Y30	VSS
Y31	DVDD15
Y32	DDR3BA09
Y33	VSS
Y34	DDR3BA03
Y35	DDR3BA12
Y36	DDR3BA15
Y37	VSS
Y38	DDR3BA10
Y39	DDR3BA13
AA1	USBRESREF
AA2	EMU00
AA3	EMU11
AA4	EMU18
AA5	VSS
AA6	DVDD18
AA7	VSS
AA8	CVDD
AA9	VSS
AA10	CVDD
AA11	VSS
AA12	VP
AA13	VSS
AA14	DVDD33
AA15	VSS
AA16	CVDD
AA17	VSS
AA18	CVDD
AA19	VSS
AA20	CVDD
AA21	VSS
AA22	CVDD
AA23	VSS
AA24	CVDD
AA25	VSS
AA26	CVDD
AA27	VSS
AA28	DVDD15
AA29	VSS

Table 3-5 Terminal Functions — By Ball Number (Part 21 of 37)

Ball Number	Signal Name
AA30	DVDD15
AA31	DDR3BRZQ0
AA32	DDR3BA00
AA33	DDR3BA08
AA34	DDR3BBA1
AA35	VSS
AA36	$\overline{\text{DDR3BCE1}}$
AA37	DDR3BBA0
AA38	DDR3BA14
AA39	DDR3BA11
AB1	TSCOMPOUT
AB2	EMU01
AB3	EMU14
AB4	EMU10
AB5	DVDD18
AB6	VSS
AB7	DVDD18
AB8	VSS
AB9	CVDD
AB10	VSS
AB11	CVDD
AB12	VSS
AB13	VDDUSB
AB14	VSS
AB15	CVDD
AB16	VSS
AB17	CVDD
AB18	VSS
AB19	CVDD
AB20	VSS
AB21	CVDD
AB22	VSS
AB23	CVDD
AB24	VSS
AB25	CVDD
AB26	VSS
AB27	CVDD
AB28	AVDDA12
AB29	DVDD15
AB30	VSS
AB31	DVDD15
AB32	RSV032

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Table 3-5 Terminal Functions — By Ball Number (Part 22 of 37)

Ball Number	Signal Name
AB33	VSS
AB34	DDR3BCE0
AB35	DDR3BBA2
AB36	VSS
AB37	VSS
AB38	DDR3BCKE1
AB39	DDR3BCKE0
AC1	TSPUSHEVT1
AC2	TSPUSHEVT0
AC3	TSSYNCEVT
AC4	EXTFRAMEEVENT
AC5	RESETSTAT
AC6	DVDD18
AC7	VSS
AC8	CVDD
AC9	VSS
AC10	CVDD
AC11	VSS
AC12	CVDD
AC13	VSS
AC14	CVDD
AC15	VSS
AC16	CVDD
AC17	VSS
AC18	CVDD1
AC19	VSS
AC20	CVDD
AC21	VSS
AC22	CVDD
AC23	VSS
AC24	CVDD
AC25	VSS
AC26	CVDD
AC27	VSS
AC28	AVDDA13
AC29	VSS
AC30	DVDD15
AC31	DDR3BVREFSSTL
AC32	DDR3BRESET
AC33	DDR3BODT0
AC34	RSV031
AC35	VSS

Table 3-5 Terminal Functions — By Ball Number (Part 23 of 37)

Ball Number	Signal Name
AC36	DDR3BCAS
AC37	DDR3BWE
AC38	DDR3BCLKOUTN1
AC39	DDR3BCLKOUTP1
AD1	TRST
AD2	RESET
AD3	RESETFULL
AD4	LRESETNMIEN
AD5	NMI
AD6	VSS
AD7	DVDD18
AD8	VSS
AD9	CVDD
AD10	VSS
AD11	VNWA2
AD12	VSS
AD13	CVDD
AD14	VSS
AD15	CVDD
AD16	VSS
AD17	CVDD1
AD18	VSS
AD19	CVDD1
AD20	VSS
AD21	CVDD
AD22	VSS
AD23	CVDD
AD24	VSS
AD25	CVDD
AD26	VSS
AD27	CVDD
AD28	AVDDA14
AD29	DVDD15
AD30	VSS
AD31	DVDD15
AD32	DDR3BRAS
AD33	VSS
AD34	DDR3BODT1
AD35	RSV030
AD36	DDR3BCB06
AD37	VSS
AD38	DDR3BCLKOUTP0

Table 3-5 Terminal Functions — By Ball Number (Part 24 of 37)

Ball Number	Signal Name
AD39	DDR3BCLKOUTN0
AE1	TCK
AE2	TMS
AE3	VSS
AE4	LRESET
AE5	HOUT
AE6	DVDD18
AE7	VSS
AE8	CVDD
AE9	VSS
AE10	CVDD
AE11	VSS
AE12	CVDD
AE13	VSS
AE14	CVDD
AE15	VSS
AE16	CVDD
AE17	VSS
AE18	CVDD
AE19	VSS
AE20	CVDD
AE21	VSS
AE22	CVDD
AE23	VSS
AE24	CVDD
AE25	VSS
AE26	CVDD
AE27	VSS
AE28	AVDDA15
AE29	VSS
AE30	DVDD15
AE31	VSS
AE32	DDR3BCB02
AE33	DDR3BCB04
AE34	DDR3BCB07
AE35	VSS
AE36	DDR3BCB05
AE37	DDR3BDQM8
AE38	DDR3BDQS8N
AE39	DDR3BDQS8P
AF1	TDO
AF2	HYP1TXPMDAT

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Table 3-5 Terminal Functions — By Ball Number (Part 25 of 37)

Ball Number	Signal Name
AF3	HYP1RXPMCLK
AF4	HYP1RXPMDAT
AF5	BOOTCOMPLETE
AF6	VSS
AF7	DVDD18
AF8	VSS
AF9	CVDD
AF10	VSS
AF11	AVDDA1
AF12	VSS
AF13	VDDALV
AF14	VSS
AF15	VDDALV
AF16	VSS
AF17	VDDALV
AF18	VSS
AF19	VDDALV
AF20	VSS
AF21	VDDALV
AF22	VSS
AF23	VDDALV
AF24	VSS
AF25	CVDD
AF26	VSS
AF27	CVDD
AF28	VSS
AF29	DVDD15
AF30	VSS
AF31	DVDD15
AF32	DDR3BCB00
AF33	VSS
AF34	DDR3BCB01
AF35	DDR3BCB03
AF36	DDR3BD33
AF37	VSS
AF38	DDR3BDQS4P
AF39	DDR3BDQS4N
AG1	TDI
AG2	HYP1RXFLDAT
AG3	HYP0RXPMDAT
AG4	VSS
AG5	HYP0TXFLDAT

Table 3-5 Terminal Functions — By Ball Number (Part 26 of 37)

Ball Number	Signal Name
AG6	DVDD18
AG7	VSS
AG8	CVDD
AG9	VSS
AG10	CVDD
AG11	VSS
AG12	VDDALV
AG13	VSS
AG14	VDDALV
AG15	VSS
AG16	VDDALV
AG17	VSS
AG18	VDDALV
AG19	VSS
AG20	VDDALV
AG21	VSS
AG22	VDDALV
AG23	VSS
AG24	VNWA1
AG25	VSS
AG26	AVDDA5
AG27	VSS
AG28	CVDD
AG29	VSS
AG30	DVDD15
AG31	VSS
AG32	DDR3BD39
AG33	DDR3BDQM4
AG34	DDR3BD35
AG35	VSS
AG36	DDR3BD36
AG37	DDR3BD32
AG38	DDR3BD34
AG39	DDR3BDQM5
AH1	HYP1TXPMCLK
AH2	HYP1TXFLDAT
AH3	HYP1TXFLCLK
AH4	HYP1RXFLCLK
AH5	HYP0TXPMCLK
AH6	VSS
AH7	VSS
AH8	VSS

Table 3-5 Terminal Functions — By Ball Number (Part 27 of 37)

Ball Number	Signal Name
AH9	CVDD
AH10	VSS
AH11	VDDALV
AH12	VSS
AH13	VDDALV
AH14	VSS
AH15	VDDALV
AH16	VSS
AH17	VDDALV
AH18	VSS
AH19	VDDALV
AH20	VSS
AH21	VDDALV
AH22	VSS
AH23	VDDALV
AH24	VSS
AH25	VDDALV
AH26	VSS
AH27	CVDD
AH28	VSS
AH29	AVDDA4
AH30	VSS
AH31	DVDD15
AH32	DDR3BD40
AH33	VSS
AH34	DDR3BD37
AH35	DDR3BD38
AH36	DDR3BD42
AH37	VSS
AH38	DDR3BD46
AH39	DDR3BD45
AJ1	HYP0TXPMDAT
AJ2	HYP0RXPMCLK
AJ3	HYP0TXFLCLK
AJ4	HYP0RXFLDAT
AJ5	HYP0RXFLCLK
AJ6	VSS
AJ7	VSS
AJ8	CVDD
AJ9	VSS
AJ10	CVDD
AJ11	VSS

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Table 3-5 Terminal Functions — By Ball Number (Part 28 of 37)

Ball Number	Signal Name
AJ12	VDDALV
AJ13	VSS
AJ14	VDDALV
AJ15	VSS
AJ16	VDDALV
AJ17	VSS
AJ18	VDDALV
AJ19	VSS
AJ20	VDDALV
AJ21	VSS
AJ22	VDDALV
AJ23	VSS
AJ24	VDDALV
AJ25	VSS
AJ26	DVDD18
AJ27	VSS
AJ28	CVDD
AJ29	VSS
AJ30	DVDD15
AJ31	VSS
AJ32	VSS
AJ33	DDR3BD41
AJ34	DDR3BD43
AJ35	VSS
AJ36	DDR3BD44
AJ37	DDR3BD47
AJ38	DDR3BDQS5N
AJ39	DDR3BDQS5P
AK1	SYSCLKOUT
AK2	VSS
AK3	SYSCLKN
AK4	$\overline{\text{POR}}$
AK5	RSV012
AK6	VSS
AK7	CVDD
AK8	VSS
AK9	CVDD
AK10	VSS
AK11	VDDAHV
AK12	VSS
AK13	VDDAHV
AK14	VSS

Table 3-5 Terminal Functions — By Ball Number (Part 29 of 37)

Ball Number	Signal Name
AK15	VDDAHV
AK16	VSS
AK17	VDDAHV
AK18	VSS
AK19	VDDAHV
AK20	VSS
AK21	VDDAHV
AK22	VSS
AK23	VDDAHV
AK24	VSS
AK25	VDDAHV
AK26	VSS
AK27	DVDD18
AK28	VSS
AK29	CVDD
AK30	VSS
AK31	DVDD15
AK32	DDR3BRZQ2
AK33	VSS
AK34	DDR3BDQM6
AK35	DDR3BD51
AK36	DDR3BD50
AK37	VSS
AK38	DDR3BD49
AK39	DDR3BD48
AL1	TSREFCLKN
AL2	ALTCORECLKN
AL3	SYSCLKP
AL4	CORECLKSEL
AL5	VSS
AL6	CVDD
AL7	VSS
AL8	CVDD
AL9	VSS
AL10	VDDAHV
AL11	VSS
AL12	VDDAHV
AL13	VSS
AL14	VDDAHV
AL15	VSS
AL16	VDDAHV
AL17	VSS

Table 3-5 Terminal Functions — By Ball Number (Part 30 of 37)

Ball Number	Signal Name
AL18	VDDAHV
AL19	VSS
AL20	VDDAHV
AL21	VSS
AL22	VDDAHV
AL23	VSS
AL24	VDDAHV
AL25	VSS
AL26	DVDD18
AL27	VSS
AL28	DVDD18
AL29	VSS
AL30	CVDD
AL31	VSS
AL32	DVDD15
AL33	DDR3BD55
AL34	DDR3BD52
AL35	VSS
AL36	DDR3BD53
AL37	DDR3BD54
AL38	DDR3BDQS6N
AL39	DDR3BDQS6P
AM1	TSREFCLKP
AM2	ALTCORECLKP
AM3	VSS
AM4	RSV003
AM5	CVDD
AM6	HYP1REFRES
AM7	RSV020
AM8	VSS
AM9	HYP0REFRES
AM10	VSS
AM11	AIFREFRES1
AM12	VSS
AM13	VSS
AM14	RSV025
AM15	AIFREFRES0
AM16	RSV024
AM17	VSS
AM18	VSS
AM19	XFIREFRES1
AM20	VSS

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Table 3-5 Terminal Functions — By Ball Number (Part 31 of 37)

Ball Number	Signal Name
AM21	RIOREFRES
AM22	VSS
AM23	RSV021
AM24	SGMIIREFRES
AM25	RSV023
AM26	PCIEREFRES
AM27	DVDD18
AM28	RSV022
AM29	DVDD18
AM30	RADSYNC
AM31	CVDD
AM32	VSS
AM33	VSS
AM34	DDR3BD59
AM35	DDR3BD60
AM36	DDR3BD62
AM37	VSS
AM38	DDR3BD61
AM39	DDR3BDQM7
AN1	TSRXCLKOUT0P
AN2	VSS
AN3	TSRXCLKOUT1P
AN4	RSV002
AN5	VSS
AN6	VSS
AN7	VSS
AN8	VSS
AN9	VSS
AN10	RSV019
AN11	VSS
AN12	VSS
AN13	VSS
AN14	VSS
AN15	VSS
AN16	XFIREFRES0
AN17	VSS
AN18	VSS
AN19	RSV026
AN20	VSS
AN21	VSS
AN22	VSS
AN23	VSS

Table 3-5 Terminal Functions — By Ball Number (Part 32 of 37)

Ball Number	Signal Name
AN24	VSS
AN25	VSS
AN26	VSS
AN27	VSS
AN28	VSS
AN29	VSS
AN30	PACLKSEL
AN31	VSS
AN32	RSV033
AN33	DDR3BD58
AN34	DDR3BD56
AN35	VSS
AN36	DDR3BD57
AN37	DDR3BD63
AN38	DDR3BDQS7P
AN39	DDR3BDQS7N
AP1	TSRXCLKOUT0N
AP2	RP1CLKN
AP3	TSRXCLKOUT1N
AP4	VSS
AP5	HYP1TXN1
AP6	HYP1TXP1
AP7	VSS
AP8	HYP0TXN2
AP9	HYP0TXP2
AP10	VSS
AP11	HYP0TXN0
AP12	HYP0TXP0
AP13	VSS
AP14	AIFTXN3
AP15	AIFTXP3
AP16	VSS
AP17	AIFTXN0
AP18	AIFTXP0
AP19	VSS
AP20	VSS
AP21	VSS
AP22	RIOTXN2
AP23	RIOTXP2
AP24	VSS
AP25	SGMII3TXN
AP26	SGMII3TXP

Table 3-5 Terminal Functions — By Ball Number (Part 33 of 37)

Ball Number	Signal Name
AP27	VSS
AP28	VSS
AP29	VSS
AP30	VSS
AP31	MDCLK
AP32	RSV034
AP33	RSV035
AP34	PHYSYNC
AP35	VD
AP36	VCL
AP37	VSS
AP38	RSV006
AP39	RSV007
AR1	RP1FBP
AR2	RP1CLKP
AR3	VSS
AR4	HYP1TXN2
AR5	HYP1TXP2
AR6	VSS
AR7	HYP0TXN3
AR8	HYP0TXP3
AR9	VSS
AR10	HYP0TXN1
AR11	HYP0TXP1
AR12	VSS
AR13	AIFTXN4
AR14	AIFTXP4
AR15	VSS
AR16	AIFTXN1
AR17	AIFTXP1
AR18	VSS
AR19	XFITXP1
AR20	XFITXN1
AR21	VSS
AR22	VSS
AR23	RIOTXN1
AR24	RIOTXP1
AR25	VSS
AR26	SGMII2TXN
AR27	SGMII2TXP
AR28	VSS
AR29	PCIETXN1

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Table 3-5 Terminal Functions — By Ball Number (Part 34 of 37)

Ball Number	Signal Name
AR30	PCIETXP1
AR31	VSS
AR32	MDIO
AR33	VSS
AR34	XFIMDCLK
AR35	VCNTL5
AR36	VCNTL2
AR37	VCNTL1
AR38	DDR3BCLKP
AR39	DDR3BCLKN
AT1	RP1FBN
AT2	VSS
AT3	HYP1TXN3
AT4	HYP1TXP3
AT5	VSS
AT6	HYP1TXN0
AT7	HYP1TXP0
AT8	VSS
AT9	HYP0CLKP
AT10	HYP0CLKN
AT11	VSS
AT12	AIFTXN5
AT13	AIFTXP5
AT14	VSS
AT15	AIFTXN2
AT16	AIFTXP2
AT17	VSS
AT18	XFITXP0
AT19	XFITXN0
AT20	VSS
AT21	RIOTXN3
AT22	RIOTXP3
AT23	VSS
AT24	RIOTXN0
AT25	RIOTXP0
AT26	VSS
AT27	SGMII1TXN
AT28	SGMII1TXP
AT29	VSS
AT30	PCIETXN0
AT31	PCIETXP0
AT32	VSS

Table 3-5 Terminal Functions — By Ball Number (Part 35 of 37)

Ball Number	Signal Name
AT33	XFIMDIO
AT34	RSV009
AT35	RSV045
AT36	VSS
AT37	RSV038
AT38	VCNTL3
AT39	VCNTL0
AU1	VSS
AU2	VSS
AU3	VSS
AU4	HYP1RXN2
AU5	HYP1RXP2
AU6	VSS
AU7	HYP1RXN0
AU8	HYP1RXP0
AU9	VSS
AU10	HYP0RXN1
AU11	HYP0RXP1
AU12	VSS
AU13	AIFRXN4
AU14	AIFRXP4
AU15	VSS
AU16	AIFRXN1
AU17	AIFRXP1
AU18	VSS
AU19	XFICLKP
AU20	XFICLKN
AU21	VSS
AU22	RIORXN1
AU23	RIORXP1
AU24	VSS
AU25	SGMII2RXN
AU26	SGMII2RXP
AU27	VSS
AU28	SGMII0TXN
AU29	SGMII0TXP
AU30	VSS
AU31	PCIERXN0
AU32	PCIERXP0
AU33	VSS
AU34	RSV008
AU35	RSV043

Table 3-5 Terminal Functions — By Ball Number (Part 36 of 37)

Ball Number	Signal Name
AU36	RSV039
AU37	RSV041
AU38	VCNTL4
AU39	VSS
AV1	VSS
AV2	VSS
AV3	HYP1RXN3
AV4	HYP1RXP3
AV5	VSS
AV6	HYP1RXN1
AV7	HYP1RXP1
AV8	VSS
AV9	HYP0RXN2
AV10	HYP0RXP2
AV11	VSS
AV12	AIFRXN5
AV13	AIFRXP5
AV14	VSS
AV15	AIFRXN2
AV16	AIFRXP2
AV17	VSS
AV18	XFIRXP0
AV19	XFIRXN0
AV20	VSS
AV21	RIORXN3
AV22	RIORXP3
AV23	VSS
AV24	RIORXN0
AV25	RIORXP0
AV26	VSS
AV27	SGMII1RXN
AV28	SGMII1RXP
AV29	VSS
AV30	PCIERXN1
AV31	PCIERXP1
AV32	VSS
AV33	PASSCLKP
AV34	PASSCLKN
AV35	VSS
AV36	RSV042
AV37	RSV040
AV38	VSS

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Table 3-5 Terminal Functions — By Ball Number (Part 37 of 37)

Ball Number	Signal Name
AV39	VSS
AW1	(nopin)
AW2	VSS
AW3	VSS
AW4	HYP1CLKP
AW5	HYP1CLKN
AW6	VSS
AW7	HYP0RXN3
AW8	HYP0RXP3
AW9	VSS
AW10	HYP0RXN0
AW11	HYP0RXP0
AW12	VSS
AW13	AIFRXN3
AW14	AIFRXP3
AW15	VSS
AW16	AIFRXN0
AW17	AIFRXP0
AW18	VSS
AW19	XFIRXP1
AW20	XFIRXN1
AW21	VSS
AW22	RIORXN2
AW23	RIORXP2
AW24	VSS
AW25	SGMII3RXN
AW26	SGMII3RXP
AW27	VSS
AW28	SGMII0RXN
AW29	SGMII0RXP
AW30	VSS
AW31	PCIECLKP
AW32	PCIECLKN
AW33	VSS
AW34	SRIOSGMIICLKP
AW35	SRIOSGMIICLKN
AW36	RSV044
AW37	VSS
AW38	VSS
AW39	(nopin)
End of Table 3-5	

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3.4 Pullup/Pulldown Resistors

Proper board design should ensure that input pins to the device always be at a valid logic level and not floating. This may be achieved via pullup/pulldown resistors. The device features internal pullup (IPU) and internal pulldown (IPD) resistors on most pins to eliminate the need, unless otherwise noted, for external pullup/pulldown resistors.

An external pullup/pulldown resistor needs to be used in the following situations:

- **Device Configuration Pins:** If the pin is both routed out and are not driven (in Hi-Z state), an external pullup/pulldown resistor must be used, even if the IPU/IPD matches the desired value/state.
- **Other Input Pins:** If the IPU/IPD does not match the desired value/state, use an external pullup/pulldown resistor to pull the signal to the opposite rail.

For the device configuration pins (listed in Table 6-13), if they are both routed out and are not driven (in Hi-Z state), it is strongly recommended that an external pullup/pulldown resistor be implemented. Although, internal pullup/pulldown resistors exist on these pins and they may match the desired configuration value, providing external connectivity can help ensure that valid logic levels are latched on these device configuration pins. In addition, applying external pullup/pulldown resistors on the device configuration pins adds convenience to the user in debugging and flexibility in switching operating modes.

Tips for choosing an external pullup/pulldown resistor:

- Consider the total amount of current that may pass through the pullup or pulldown resistor. Be sure to include the leakage currents of all the devices connected to the net, as well as any internal pullup or pulldown resistors.
- Decide a target value for the net. For a pulldown resistor, this should be below the lowest V_{IL} level of all inputs connected to the net. For a pullup resistor, this should be above the highest V_{IH} level of all inputs on the net. A reasonable choice would be to target the V_{OL} or V_{OH} levels for the logic family of the limiting device; which, by definition, have margin to the V_{IL} and V_{IH} levels.
- Select a pullup/pulldown resistor with the largest possible value that still ensures that the net will reach the target pulled value when maximum current from all devices on the net is flowing through the resistor. The current to be considered includes leakage current plus, any other internal and external pullup/pulldown resistors on the net.
- For bidirectional nets, there is an additional consideration that sets a lower limit on the resistance value of the external resistor. Verify that the resistance is small enough that the weakest output buffer can drive the net to the opposite logic level (including margin).
- Remember to include tolerances when selecting the resistor value.
- For pullup resistors, also remember to include tolerances on the DVDD rail.

For most systems:

- A 1-kΩ resistor can be used to oppose the IPU/IPD while meeting the above criteria. Users should confirm this resistor value is correct for their specific application.
- A 20-kΩ resistor can be used to compliment the IPU/IPD on the device configuration pins while meeting the above criteria. Users should confirm this resistor value is correct for their specific application.

For more detailed information on input current (I_I), and the low-level/high-level input voltages (V_{IL} and V_{IH}) for the TCI6634K2K device, see Section 7.3 "Electrical Characteristics" on page 214. To determine which pins on the device include internal pullup/pulldown resistors, see Table 3-3 "Terminal Functions — Power and Ground" on page 55.

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4 Memory, Interrupts, and EDMA for TCI6634K2K

4.1 Memory Map Summary for TCI6634K2K

The following table shows the memory map address ranges of the device.

Table 4-1 Device Memory Map Summary for TCI6634K2K (Part 1 of 12)

Physical 40 bit Address				
Start	**End**	**Bytes**	**DSP View**	**SOC View**
00 0000 0000	00 0003 FFFF	256K	Reserved	Reserved
00 0004 0000	00 007F FFFF	8M-256K	Reserved	Reserved
00 0080 0000	00 008F FFFF	1M	L2 SRAM	L2 SRAM
00 0090 0000	00 00DF FFFF	5M	Reserved	Reserved
00 00E0 0000	00 00E0 7FFF	32K	L1P SRAM	L1P SRAM
00 00E0 8000	00 00EF FFFF	1M-32K	Reserved	Reserved
00 00F0 0000	00 00F0 7FFF	32K	L1D SRAM	L1D SRAM
00 00F0 8000	00 00FF FFFF	1M-32K	Reserved	Reserved
00 0100 0000	00 0100 FFFF	64K	C66x CorePac registers	C66x CorePac registers
00 0101 0000	00 010F FFFF	1M-64K	C66x CorePac registers	C66x CorePac registers
00 0100 0000	00 0100 FFFF	64K	C66x CorePac registers	C66x CorePac registers
00 0101 0000	00 01BF FFFF	11M-64K	C66x CorePac registers	C66x CorePac registers
00 01C0 0000	00 01CF FFFF	1M	Reserved	Reserved
00 01D0 0000	00 01D0 007F	128	Tracer CFG0	Tracer CFG0
00 01D0 0080	00 01D0 7FFF	32K-128	Reserved	Reserved
00 01D0 8000	00 01D0 807F	128	Tracer CFG1	Tracer CFG1
00 01D0 8080	00 01D0 FFFF	32K-128	Reserved	Reserved
00 01D1 0000	00 01D1 007F	128	Tracer CFG2	Tracer CFG2
00 01D1 0080	00 01D1 7FFF	32K-128	Reserved	Reserved
00 01D1 8000	00 01D1 807F	128	Tracer CFG3	Tracer CFG3
00 01D1 8080	00 01D1 FFFF	32K-128	Reserved	Reserved
00 01D2 0000	00 01D2 007F	128	Tracer CFG4	Tracer CFG4
00 01D2 0080	00 01D2 7FFF	32K-128	Reserved	Reserved
00 01D2 8000	00 01D2 807F	128	Tracer CFG5	Tracer CFG5
00 01D2 8080	00 01D2 FFFF	32K-128	Reserved	Reserved
00 01D3 0000	00 01D3 007F	128	Tracer CFG6	Tracer CFG6
00 01D3 0080	00 01D3 7FFF	32K-128	Reserved	Reserved
00 01D3 8000	00 01D3 807F	128	Tracer CFG7	Tracer CFG7
00 01D3 8080	00 01D3 FFFF	32K-128	Reserved	Reserved
00 01D4 0000	00 01D4 007F	128	Tracer CFG8	Tracer CFG8
00 01D4 0080	00 01D4 7FFF	32K-128	Reserved	Reserved
00 01D4 8000	00 01D4 807F	128	Tracer CFG9	Tracer CFG9
00 01D4 8080	00 01D4 FFFF	32K-128	Reserved	Reserved
00 01D5 0000	00 01D5 007F	128	Tracer CFG10	Tracer CFG10
00 01D5 0080	00 01D5 7FFF	32K-128	Reserved	Reserved
00 01D5 8000	00 01D5 807F	128	Tracer CFG11	Tracer CFG11
00 01D5 8080	00 01D5 FFFF	32K-128	Reserved	Reserved
00 01D6 0000	00 01D6 007F	128	Tracer CFG12	Tracer CFG12
00 01D6 0080	00 01D6 7FFF	32K-128	Reserved	Reserved

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Table 4-1 Device Memory Map Summary for TCI6634K2K (Part 2 of 12)

Physical 40 bit Address		Bytes	DSP View	SOC View
Start	End			
00 01D6 8000	00 01D6 807F	128	Tracer CFG13	Tracer CFG13
00 01D6 8080	00 01D6 FFFF	32K-128	Reserved	Reserved
00 01D7 0000	00 01D7 007F	128	Tracer CFG14	Tracer CFG14
00 01D7 0080	00 01D7 7FFF	32K-128	Reserved	Reserved
00 01D7 8000	00 01D7 807F	128	Tracer CFG15	Tracer CFG15
00 01D7 8080	00 01D7 FFFF	32K-128	Reserved	Reserved
00 01D8 0000	00 01D8 007F	128	Tracer CFG16	Tracer CFG16
00 01D8 0080	00 01D8 7FFF	32K-128	Reserved	Reserved
00 01D8 8000	00 01D8 807F	128	Tracer CFG17	Tracer CFG17
00 01D8 8080	00 01D8 8FFF	32K-128	Reserved	Reserved
00 01D9 0000	00 01D9 007F	128	Tracer CFG18	Tracer CFG18
00 01D9 0080	00 01D9 7FFF	32K-128	Reserved	Reserved
00 01D9 8000	00 01D9 807F	128	Tracer CFG19	Tracer CFG19
00 01D9 8080	00 01D9 FFFF	32K-128	Reserved	Reserved
00 01DA 0000	00 01DA 007F	128	Tracer CFG20	Tracer CFG20
00 01DA 0080	00 01DA 7FFF	32K-128	Reserved	Reserved
00 01DA 8000	00 01DA 807F	128	Tracer CFG21	Tracer CFG21
00 01DA 8080	00 01DA FFFF	32K-128	Reserved	Reserved
00 01DB 0000	00 01DB 007F	128	Tracer CFG22	Tracer CFG22
00 01DB 0080	00 01DB 7FFF	32K-128	Reserved	Reserved
00 01DB 8000	00 01DB 807F	128	Tracer CFG23	Tracer CFG23
00 01DB 8080	00 01DB 8FFF	32K-128	Reserved	Reserved
00 01DC 0000	00 01DC 007F	128	Tracer CFG24	Tracer CFG24
00 01DC 0080	00 01DC 7FFF	32K-128	Reserved	Reserved
00 01DC 8000	00 01DC 807F	128	Tracer CFG25	Tracer CFG25
00 01DC 8080	00 01DC FFFF	32K-128	Reserved	Reserved
00 01DD 0000	00 01DD 007F	128	Tracer CFG26	Tracer CFG26
00 01DD 0080	00 01DD 7FFF	32K-128	Reserved	Reserved
00 01DD 8000	00 01DD 807F	128	Tracer CFG27	Tracer CFG27
00 01DD 8080	00 01DD FFFF	32K-128	Reserved	Reserved
00 01DE 0000	00 01DE 007F	128	Tracer CFG28	Tracer CFG28
00 01DE 0080	00 01DE 03FF	1K-128	Reserved	Reserved
00 01DE 0400	00 01DE 047F	128	Tracer CFG29	Tracer CFG29
00 01DD 0480	00 01DD 07FF	1K-128	Reserved	Reserved
00 01DE 0800	00 01DE 087F	128	Tracer CFG30	Tracer CFG30
00 01DE 0880	00 01DE 7FFF	30K-128	Reserved	Reserved
00 01DE 8000	00 01DE 807F	128	Tracer CFG31	Tracer CFG31
00 01DE 8080	00 01DF FFFF	64K-128	Reserved	Reserved
00 01E0 0000	00 01E3 FFFF	256K	Reserved	Reserved
00 01E4 0000	00 01E4 3FFF	16K	Reserved	Reserved
00 01E4 4000	00 01E7FFFF	240k	Reserved	Reserved
00 01E8 0000	00 01E8 3FFF	16K	Reserved	Reserved
00 01E8 4000	00 01EB FFFF	240k	Reserved	Reserved

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Table 4-1 Device Memory Map Summary for TCI6634K2K (Part 3 of 12)

Physical 40 bit Address		Bytes	DSP View	SOC View
Start	End			
00 01EC 0000	00 01EF FFFF	256K	Reserved	Reserved
00 01F0 0000	00 01F7 FFFF	512K	AIF2 control	AIF2 control
00 01F8 0000	00 01F8 FFFF	64K	RAC_1 - FEI control	RAC_1 - FEI control
00 01F9 0000	00 01F9 FFFF	64K	RAC_1 - BEI control	RAC_1 - BEI control
00 01FA 0000	00 01FB FFFF	128K	RAC_1 - GCCP 0 control	RAC_1 - GCCP 0 control
00 01FC 0000	00 01FD FFFF	128K	RAC_1 - GCCP 1 control	RAC_1 - GCCP 1 control
00 01FE 0000	00 01FF FFFF	128K	Reserved	Reserved
00 0200 0000	00 020F FFFF	1M	Network Coprocessor (Packet Accelerator, 1-gigabit Ethernet switch subsystem and Security Accelerator)	Network Coprocessor (Packet Accelerator, 1-gigabit Ethernet switch subsystem and Security Accelerator)
00 0210 0000	00 0210 FFFF	64K	RAC_0 - FEI control	RAC_0 - FEI control
00 0211 0000	00 0211 FFFF	64K	RAC_0 - BEI control	RAC_0 - BEI control
00 0212 0000	00 0213 FFFF	128K	RAC_0 - GCCP 0 control	RAC_0 - GCCP 0 control
00 0214 0000	00 0215 FFFF	128K	RAC_0 - GCCP 1 control	RAC_0 - GCCP 1 control
00 0216 0000	00 0217 FFFF	128K	Reserved	Reserved
00 0218 0000	00 0218 7FFF	32k	Reserved	Reserved
00 0218 8000	00 0218 FFFF	32k	Reserved	Reserved
00 0219 0000	00 0219 FFFF	64k	Reserved	Reserved
00 021A 0000	00 021A FFFF	64K	Reserved	Reserved
00 021B 0000	00 021B FFFF	64K	Reserved	Reserved
00 021C 0000	00 021C 03FF	1K	TCP3d_0	TCP3d_0
00 021C 0400	00 021C 3FFF	15K	Reserved	Reserved
00 021C 4000	00 021C 43FF	1K	TCP3d_2	TCP3d_2
00 021C 4400	00 021C 5FFF	7K	Reserved	Reserved
00 021C 6000	00 021C 63FF	1K	TCP3d_3	TCP3d_3
00 021C 6400	00 021C 7FFF	7K	Reserved	Reserved
00 021C 8000	00 021C 83FF	1K	TCP3d_1	TCP3d_1
00 021C 8400	00 021C FFFF	31K	Reserved	Reserved
00 021D 0000	00 021D 00FF	256	VCP2_0 configuration	VCP2_0 configuration
00 021D 0100	00 021D 3FFF	16K	Reserved	Reserved
00 021D 4000	00 021D 40FF	256	VCP2_1 configuration	VCP2_1 configuration
00 021D 4100	00 021D 7FFF	16K	Reserved	Reserved
00 021D 8000	00 021D 80FF	256	VCP2_2 configuration	VCP2_2 configuration
00 021D 8100	00 021D BFFF	16K	Reserved	Reserved
00 021D C000	00 021D C0FF	256	VCP2_3 configuration	VCP2_3 configuration
00 021D C100	00 021D EFFF	12K-256	Reserved	Reserved
00 021D F000	00 021D F07F	128	Reserved	Reserved
00 021D F080	00 021D FFFF	4K-128	Reserved	Reserved
00 021E 0000	00 021E FFFF	64K	Reserved	Reserved
00 021F 0000	00 021F 07FF	2K	FFTC_0 configuration	FFTC_0 configuration
00 021F 0800	00 021F 0FFF	2K	FFTC_4 configuration	FFTC_4 configuration
00 021F 1000	00 021F 17FF	2K	FFTC_5 configuration	FFTC_5 configuration
00 021F 1800	00 021F 3FFF	10K	Reserved	Reserved

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Table 4-1 Device Memory Map Summary for TCI6634K2K (Part 4 of 12)

Physical 40 bit Address		Bytes	DSP View	SOC View
Start	End			
00 021F 4000	00 021F 47FF	2K	FFTC_1 configuration	FFTC_1 configuration
00 021F 4800	00 021F 7FFF	14K	Reserved	Reserved
00 021F 8000	00 021F 87FF	2K	FFTC_2 configuration	FFTC_2 configuration
00 021F 8800	00 021F BFFF	14K	Reserved	Reserved
00 021F C000	00 021F C7FF	2K	FFTC_3 configuration	FFTC_3 configuration
00 021F C800	00 021F FFFF	14K	Reserved	Reserved
00 0220 0000	00 0220 007F	128	Timer0	Timer0
00 0220 0080	00 0220 FFFF	64K-128	Reserved	Reserved
00 0221 0000	00 0221 007F	128	Timer1	Timer1
00 0221 0080	00 0221 FFFF	64K-128	Reserved	Reserved
00 0222 0000	00 0222 007F	128	Timer2	Timer2
00 0222 0080	00 0222 FFFF	64K-128	Reserved	Reserved
00 0223 0000	00 0223 007F	128	Timer3	Timer3
00 0223 0080	00 0223 FFFF	64K-128	Reserved	Reserved
00 0224 0000	00 0224 007F	128	Timer4	Timer4
00 0224 0080	00 0224 FFFF	64K-128	Reserved	Reserved
00 0225 0000	00 0225 007F	128	Timer5	Timer5
00 0225 0080	00 0225 FFFF	64K-128	Reserved	Reserved
00 0226 0000	00 0226 007F	128	Timer6	Timer6
00 0226 0080	00 0226 FFFF	64K-128	Reserved	Reserved
00 0227 0000	00 0227 007F	128	Timer7	Timer7
00 0227 0080	00 0227 FFFF	64K-128	Reserved	Reserved
00 0228 0000	00 0228 007F	128	Timer 8	Timer 8
00 0228 0080	00 0228 FFFF	64K-128	Reserved	Reserved
00 0229 0000	00 0229 007F	128	Timer 9	Timer 9
00 0229 0080	00 0229 FFFF	64K-128	Reserved	Reserved
00 022A 0000	00 022A 007F	128	Timer 10	Timer 10
00 022A 0080	00 022A FFFF	64K-128	Reserved	Reserved
00 022B 0000	00 022B 007F	128	Timer 11	Timer 11
00 022B 0080	00 022B FFFF	64K-128	Reserved	Reserved
00 022C 0000	00 022C 007F	128	Timer 12	Timer 12
00 022C 0080	00 022C FFFF	64K-128	Reserved	Reserved
00 022D 0000	00 022D 007F	128	Timer 13	Timer 13
00 022D 0080	00 022D FFFF	64K-128	Reserved	Reserved
00 022E 0000	00 022E 007F	128	Timer 14	Timer 14
00 022E 0080	00 022E FFFF	64K-128	Reserved	Reserved
00 022F 0000	00 022F 007F	128	Timer 15	Timer 15
00 022F 0080	00 022F 00FF	128	Timer 16	Timer 16
00 022F 0100	00 022F 017F	128	Timer 17	Timer 17
00 022F 0180	00 022F 01FF	128	Timer 18	Timer 18
00 022F 0200	00 022F 027F	128	Timer 19	Timer 19
00 0230 0000	00 0230 FFFF	64K	Reserved	Reserved
00 0231 0000	00 0231 01FF	512	PLL Controller	PLL Controller

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Table 4-1 Device Memory Map Summary for TCI6634K2K (Part 5 of 12)

Physical 40 bit Address		Bytes	DSP View	SOC View
Start	End			
00 0231 0200	00 0231 9FFF	40K-512	Reserved	Reserved
00 0231 A000	00 0231 BFFF	8K	HyperLink0 SerDes Config	HyperLink0 SerDes Config
00 0231 C000	00 0231 DFFF	8K	HyperLink1 SerDes Config	HyperLink1 SerDes Config
00 0231 E000	00 0231 FFFF	8K	10GbE SerDes Config	10GbE SerDes Config
00 0232 0000	00 0232 3FFF	16K	PCIE SerDes Config	PCIE SerDes Config
00 0232 4000	00 0232 5FFF	8K	AIF2 SerDes B4 Config	AIF2 SerDes B4 Config
00 0232 5000	00 0232 7FFF	8K	AIF2 SerDes B8 Config	AIF2 SerDes B8 Config
00 0232 8000	00 0232 8FFF	4K	DDRB PHY Config	DDRB PHY Config
00 0232 9000	00 0232 9FFF	4K	DDRA PHY Config	DDRA PHY Config
00 0232 A000	00 0232 BFFF	8K	SGMII SerDes Config	SGMII SerDes Config
00 0232 C000	00 0232 CFFF	4K	SRIO SerDes Config	SRIO SerDes Config
00 0232 D000	00 0232 DFFF	4K	Reserved	Reserved
00 0232 E000	00 0232 EFFF	4K	Reserved	Reserved
00 0232 F000	00 0232 FFFF	4K	Reserved	Reserved
00 0233 0000	00 0233 03FF	1K	SmartReflex0	SmartReflex0
00 0233 0400	00 0233 07FF	1K	SmartReflex1	SmartReflex1
00 0233 0400	00 0233 FFFF	62K	Reserved	Reserved
00 0234 0000	00 0234 00FF	256	VCP2_4 configuration	VCP2_4 configuration
00 0234 0100	00 0234 3FFF	16K	Reserved	Reserved
00 0234 4000	00 0234 40FF	256	VCP2_5 configuration	VCP2_5 configuration
00 0234 4100	00 0234 7FFF	16K	Reserved	Reserved
00 0234 8000	00 0234 80FF	256	VCP2_6 configuration	VCP2_6 configuration
00 0234 8100	00 0234 BFFF	16K	Reserved	Reserved
00 0234 C000	00 0234 C0FF	256	VCP2_7 configuration	VCP2_7 configuration
00 0234 C100	00 0234 FFFF	16K	Reserved	Reserved
00 0235 0000	00 0235 0FFF	4K	Power sleep controller (PSC)	Power sleep controller (PSC)
00 0235 1000	00 0235 FFFF	64K-4K	Reserved	Reserved
00 0236 0000	00 0236 03FF	1K	Memory protection unit (MPU) 0	Memory protection unit (MPU) 0
00 0236 0400	00 0236 7FFF	31K	Reserved	Reserved
00 0236 8000	00 0236 83FF	1K	Memory protection unit (MPU) 1	Memory protection unit (MPU) 1
00 0236 8400	00 0236 FFFF	31K	Reserved	Reserved
00 0237 0000	00 0237 03FF	1K	Memory protection unit (MPU) 2	Memory protection unit (MPU) 2
00 0237 0400	00 0237 7FFF	31K	Reserved	Reserved
00 0237 8000	00 0237 83FF	1K	Memory protection unit (MPU) 3	Memory protection unit (MPU) 3
00 0237 8400	00 0237 FFFF	31K	Reserved	Reserved
00 0238 0000	00 0238 03FF	1K	Memory protection unit (MPU) 4	Memory protection unit (MPU) 4
00 0238 8000	00 0238 83FF	1K	Memory protection unit (MPU) 5	Memory protection unit (MPU) 5
00 0238 8400	00 0238 87FF	1K	Memory protection unit (MPU) 6	Memory protection unit (MPU) 6
00 0238 8800	00 0238 8BFF	1K	Memory protection unit (MPU) 7	Memory protection unit (MPU) 7
00 0238 8C00	00 0238 8FFF	1K	Memory protection unit (MPU) 8	Memory protection unit (MPU) 8
00 0238 9000	00 0238 93FF	1K	Memory protection unit (MPU) 9	Memory protection unit (MPU) 9
00 0238 9400	00 0238 97FF	1K	Memory protection unit (MPU) 10	Memory protection unit (MPU) 10
00 0238 9800	00 0238 9BFF	1K	Memory protection unit (MPU) 11	Memory protection unit (MPU) 11

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Table 4-1 Device Memory Map Summary for TCI6634K2K (Part 6 of 12)

Physical 40 bit Address		Bytes	DSP View	SOC View
Start	End			
00 0238 9C00	00 0238 9FFF	1K	Memory protection unit (MPU) 12	Memory protection unit (MPU) 12
00 0238 A000	00 0238 A3FF	1K	Memory protection unit (MPU) 13	Memory protection unit (MPU) 13
00 0238 A400	00 0238 A7FF	1K	Memory protection unit (MPU) 14	Memory protection unit (MPU) 14
00 0238 A800	00 023F FFFF	471K	Reserved	Reserved
00 0240 0000	00 0243 FFFF	256K	Reserved	Reserved
00 0244 0000	00 0244 3FFF	16K	DSP trace formatter 0	DSP trace formatter 0
00 0244 4000	00 0244 FFFF	48K	Reserved	Reserved
00 0245 0000	00 0245 3FFF	16K	DSP trace formatter 1	DSP trace formatter 1
00 0245 4000	00 0245 FFFF	48K	Reserved	Reserved
00 0246 0000	00 0246 3FFF	16K	DSP trace formatter 2	DSP trace formatter 2
00 0246 4000	00 0246 FFFF	48K	Reserved	Reserved
00 0247 0000	00 0247 3FFF	16K	DSP trace formatter 3	DSP trace formatter 3
00 0247 4000	00 0247 FFFF	48K	Reserved	Reserved
00 0248 0000	00 0248 3FFF	16K	DSP trace formatter 4	DSP trace formatter 4
00 0248 4000	00 0248 FFFF	48K	Reserved	Reserved
00 0249 0000	00 0249 3FFF	16K	DSP trace formatter 5	DSP trace formatter 5
00 0249 4000	00 0249 FFFF	48K	Reserved	Reserved
00 024A 0000	00 024A 3FFF	16K	DSP trace formatter 6	DSP trace formatter 6
00 024A 4000	00 024A FFFF	48K	Reserved	Reserved
00 024B 0000	00 024B 3FFF	16K	DSP trace formatter 7	DSP trace formatter 7
00 024B 4000	00 024B FFFF	48K	Reserved	Reserved
00 024C 0000	00 024C 01FF	512	Reserved	Reserved
00 024C 0200	00 024C 03FF	1K-512	Reserved	Reserved
00 024C 0400	00 024C 07FF	1K	Reserved	Reserved
00 024C 0800	00 024C FFFF	62K	Reserved	Reserved
00 024D 0000	00 024F FFFF	192K	Reserved	Reserved
00 0250 0000	00 0250 007F	128	Reserved	Reserved
00 0250 0080	00 0250 7FFF	32K-128	Reserved	Reserved
00 0250 8000	00 0250 FFFF	32K	Reserved	Reserved
00 0251 0000	00 0251 FFFF	64K	Reserved	Reserved
00 0252 0000	00 0252 03FF	1K	Reserved	Reserved
00 0252 0400	00 0252 FFFF	64K-1K	Reserved	Reserved
00 0253 0000	00 0253 007F	128	I^2C0	I^2C0
00 0253 0080	00 0253 03FF	1K-128	Reserved	Reserved
00 0253 0400	00 0253 047F	128	I^2C1	I^2C1
00 0253 0480	00 0253 07FF	1K-128	Reserved	Reserved
00 0253 0800	00 0253 087F	128	I^2C2	I^2C2
00 0253 0880	00 0253 0BFF	1K-128	Reserved	Reserved
00 0253 0C00	00 0253 0C3F	64	UART0	UART0
00 0253 0C40	00 0253 FFFF	1K-64	Reserved	Reserved
00 0253 1000	00 0253 103F	64	UART1	UART1
00 0253 1040	00 0253 FFFF	60K-64	Reserved	Reserved
00 0254 0000	00 0255 FFFF	128K	BCP	BCP

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Table 4-1 Device Memory Map Summary for TCI6634K2K (Part 7 of 12)

Physical 40 bit Address		Bytes	DSP View	SOC View
Start	End			
00 0256 0080	00 0257 FFFF	128K	Reserved	Reserved
00 0258 0000	00 025F FFFF	512K	TAC	TAC
00 0260 0000	00 0260 1FFF	8K	Secondary interrupt controller (INTC) 0	Secondary interrupt controller (INTC) 0
00 0260 2000	00 0260 3FFF	8K	Reserved	Reserved
00 0260 4000	00 0260 5FFF	8K	Secondary interrupt controller (INTC) 1	Secondary interrupt controller (INTC) 1
00 0260 6000	00 0260 7FFF	8K	Reserved	Reserved
00 0260 8000	00 0260 9FFF	8K	Secondary interrupt controller (INTC) 2	Secondary interrupt controller (INTC) 2
00 0260 A000	00 0260 BEFF	8K-256	Reserved	Reserved
00 0260 BF00	00 0260 BFFF	256	GPIO Config	GPIO Config
00 0260 C000	00 0261 BFFF	64K	Reserved	Reserved
00 0261 C000	00 0261 FFFF	16K	Reserved	Reserved
00 0262 0000	00 0262 0FFF	4K	BOOTCFG chip-level registers	BOOTCFG chip-level registers
00 0262 1000	00 0262 FFFF	60K	Reserved	Reserved
00 0263 0000	00 0263 FFFF	64K	USB PHY Config	USB PHY Config
00 0264 0000	00 0264 07FF	2K	Semaphore Config	Semaphore Config
00 0264 0800	00 0264 FFFF	62K	Reserved	Reserved
00 0265 0000	00 0267 FFFF	192K	Reserved	Reserved
00 0268 0000	00 0268 FFFF	512K	USB MMR Config	USB MMR Config
00 0270 0000	00 0270 7FFF	32K	EDMA channel controller (TPCC) 0	EDMA channel controller (TPCC) 0
00 0270 8000	00 0270 FFFF	32K	EDMA channel controller (TPCC) 4	EDMA channel controller (TPCC) 4
00 0271 0000	00 0271 FFFF	64K	Reserved	Reserved
00 0272 0000	00 0272 7FFF	32K	EDMA channel controller (TPCC) 1	EDMA channel controller (TPCC) 1
00 0272 8000	00 0272 FFFF	32K	EDMA channel controller (TPCC) 3	EDMA channel controller (TPCC) 3
00 0273 0000	00 0273 FFFF	64K	Reserved	Reserved
00 0274 0000	00 0274 7FFF	32K	EDMA channel controller (TPCC) 2	EDMA channel controller (TPCC) 2
00 0274 8000	00 0275 FFFF	96K	Reserved	Reserved
00 0276 0000	00 0276 03FF	1K	EDMA TPCC0 transfer controller (TPTC) 0	EDMA TPCC0 transfer controller (TPTC) 0
00 0276 0400	00 0276 7FFF	31K	Reserved	Reserved
00 0276 8000	00 0276 83FF	1K	EDMA TPCC0 transfer controller (TPTC) 1	EDMA TPCC0 transfer controller (TPTC) 1
00 0276 8400	00 0276 FFFF	31K	Reserved	Reserved
00 0277 0000	00 0277 03FF	1K	EDMA TPCC1 transfer controller (TPTC) 0	EDMA TPCC1 transfer controller (TPTC) 0
00 0277 0400	00 0277 7FFF	31K	Reserved	Reserved
00 0277 8000	00 0277 83FF	1K	EDMA TPCC1 transfer controller (TPTC) 1	EDMA TPCC1 transfer controller (TPTC) 1
00 0278 0400	00 0277 FFFF	31K	Reserved	Reserved
00 0278 0000	00 0278 03FF	1K	EDMA TPCC1 transfer controller (TPTC) 2	EDMA TPCC1 transfer controller (TPTC) 2
00 0278 0400	00 0278 7FFF	31K	Reserved	Reserved
00 0278 8000	00 0278 83FF	1K	EDMA TPCC1 transfer controller (TPTC) 3	EDMA TPCC1 transfer controller (TPTC) 3

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Table 4-1 Device Memory Map Summary for TCI6634K2K (Part 8 of 12)

Physical 40 bit Address		Bytes	DSP View	SOC View
Start	End			
00 0278 8400	00 0278 FFFF	31K	Reserved	Reserved
00 0279 0000	00 0279 03FF	1K	EDMA TPCC2 transfer controller (TPTC) 0	EDMA TPCC2 transfer controller (TPTC) 0
00 0279 0400	00 0279 7FFF	31K	Reserved	Reserved
00 0279 8000	00 0279 83FF	1K	EDMA TPCC2 transfer controller (TPTC) 1	EDMA TPCC2 transfer controller (TPTC) 1
00 0279 8400	00 0279 FFFF	31K	Reserved	Reserved
00 027A 0000	00 027A 03FF	1K	EDMA TPCC2 transfer controller (TPTC) 2	EDMA TPCC2 transfer controller (TPTC) 2
00 027A 0400	00 027A 7FFF	31K	Reserved	Reserved
00 027A 8000	00 027A 83FF	1K	EDMA TPCC2 transfer controller (TPTC) 3	EDMA TPCC2 transfer controller (TPTC) 3
00 027A 8400	00 027A FFFF	31K	Reserved	Reserved
00 027B 0000	00 027B 03FF	1K	EDMA TPCC3 transfer controller (TPTC) 0	EDMA TPCC3 transfer controller (TPTC) 0
00 027B 0400	00 027B 7FFF	31K	Reserved	Reserved
00 027B 8000	00 027B 83FF	1K	EDMA TPCC3 transfer controller (TPTC) 1	EDMA TPCC3 transfer controller (TPTC) 1
00 027B 8400	00 027B 87FF	1K	EDMA TPCC4 transfer controller (TPTC) 0	EDMA TPCC4 transfer controller (TPTC) 0
00 027B 8800	00 027B 8BFF	1K	EEDMA TPCC4 transfer controller (TPTC) 1	EEDMA TPCC4 transfer controller (TPTC) 1
00 027B 8C00	00 027B FFFF	29K	Reserved	Reserved
00 027C 0000	00 027C 03FF	1K	BCR config	BCR config
00 027C 0400	00 027C FFFF	63K	Reserved	Reserved
00 027D 0000	00 027D 3FFF	16K	TI embedded trace buffer (TETB) - CorePac0	TI embedded trace buffer (TETB) - CorePac0
00 027D 4000	00 027D 7FFF	16K	Reserved	Reserved
00 027D 8000	00 027D FFFF	32K	Reserved	Reserved
00 027E 0000	00 027E 3FFF	16K	TI embedded trace buffer (TETB) - CorePac1	TI embedded trace buffer (TETB) - CorePac1
00 027E 4000	00 027E FFFF	48K	Reserved	Reserved
00 027F 0000	00 027F 3FFF	16K	TI embedded trace buffer (TETB) - CorePac2	TI embedded trace buffer (TETB) - CorePac2
00 027F 4000	00 027F FFFF	48K	Reserved	Reserved
00 0280 0000	00 0280 3FFF	16K	TI embedded trace buffer (TETB) - CorePac3	TI embedded trace buffer (TETB) - CorePac3
00 0280 4000	00 0280 FFFF	48K	Reserved	Reserved
00 0281 0000	00 0281 3FFF	16K	TI embedded trace buffer (TETB) - CorePac4	TI embedded trace buffer (TETB) - CorePac4
00 0281 4000	00 0281 FFFF	48K	Reserved	Reserved
00 0282 0000	00 0282 3FFF	16K	TI embedded trace buffer (TETB) - CorePac5	TI embedded trace buffer (TETB) - CorePac5
00 0282 4000	00 0282 FFFF	48K	Reserved	Reserved
00 0283 0000	00 0283 3FFF	16K	TI embedded trace buffer (TETB) - CorePac6	TI embedded trace buffer (TETB) - CorePac6
00 0283 4000	00 0283 FFFF	48K	Reserved	Reserved
00 0284 0000	00 0284 3FFF	16K	TI embedded trace buffer (TETB) - CorePac7	TI embedded trace buffer (TETB) - CorePac7

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Table 4-1 Device Memory Map Summary for TCI6634K2K (Part 9 of 12)

Physical 40 bit Address		Bytes	DSP View	SOC View
Start	End			
00 0284 4000	00 0284 FFFF	48K	Reserved	Reserved
00 0285 0000	00 0285 7FFF	32K	TBR_SYS-Trace Buffer -System	TBR_SYS-Trace Buffer -System
00 0285 8000	00 0285 FFFF	32K	Reserved	Reserved
00 0286 0000	00 028F FFFF	640K	Reserved	Reserved
00 0290 0000	00 0293 FFFF	256K	Serial RapidIO configuration (SRIO)	Serial RapidIO configuration (SRIO)
00 0294 0000	00 029F FFFF	768K	Reserved	Reserved
00 02A0 0000	00 02AF FFFF	1M	Navigator configuration	Navigator configuration
00 02B0 0000	00 02BF FFFF	1M	Navigator linking RAM	Navigator linking RAM
00 02C0 0000	00 02C0 FFFF	64K	RAC_2 - FEI control	RAC_2 - FEI control
00 02C1 0000	00 02C1 FFFF	64K	RAC_2 - BEI control	RAC_2 - BEI control
00 02C2 0000	00 02C3 FFFF	128K	RAC_2 - GCCP 0 control	RAC_2 - GCCP 0 control
00 02C4 0000	00 02C5 FFFF	128K	RAC_2 - GCCP 1 control	RAC_2 - GCCP 1 control
00 02C6 0000	00 02C7 FFFF	128K	Reserved	Reserved
00 02C8 0000	00 02C8 FFFF	64K	RAC_3 - FEI control	RAC_3 - FEI control
00 02C9 0000	00 02C9 FFFF	64K	RAC_3 - BEI control	RAC_3 - BEI control
00 02CA 0000	00 02CB FFFF	128K	RAC_3 - GCCP 0 control	RAC_3 - GCCP 0 control
00 02CC 0000	00 02CD FFFF	128K	RAC_3 - GCCP 1 control	RAC_3 - GCCP 1 control
00 02CE 0000	00 02EF FFFF	15M-896K	Reserved	Reserved
00 02F0 0000	00 02FF FFFF	1M	10GbE Config	10GbE Config
00 0300 0000	00 030F FFFF	1M	DBG Config	DBG Config
00 0310 0000	00 07FF FFFF	79M	Reserved	Reserved
00 0800 0000	00 0801 FFFF	128K	Extended memory controller (XMC) configuration	Extended memory controller (XMC) configuration
00 0802 0000	00 0BBF FFFF	60M-128K	Reserved	Reserved
00 0BC0 0000	00 0BCF FFFF	1M	Multicore shared memory controller (MSMC) config	Multicore shared memory controller (MSMC) config
00 0BD0 0000	00 0BFF FFFF	3M	Reserved	Reserved
00 0C00 0000	00 0C5F FFFF	6M	Multicore shared memory (MSM)	Multicore shared memory (MSM)
00 0C60 0000	00 0FFF FFFF	58M	Reserved	Reserved
00 1000 0000	00 107F FFFF	8M	Reserved	Reserved
00 1080 0000	00 108F FFFF	1M	CorePac0 L2 SRAM	CorePac0 L2 SRAM
00 1090 0000	00 10DF FFFF	5M	Reserved	Reserved
00 10E0 0000	00 10E0 7FFF	32K	CorePac0 L1P SRAM	CorePac0 L1P SRAM
00 10E0 8000	00 10EF FFFF	1M-32K	Reserved	Reserved
00 10F0 0000	00 10F0 7FFF	32K	CorePac0 L1D SRAM	CorePac0 L1D SRAM
00 10F0 8000	00 117F FFFF	9M-32K	Reserved	Reserved
00 1180 0000	00 118F FFFF	1M	CorePac1 L2 SRAM	CorePac1 L2 SRAM
00 1190 0000	00 11DF FFFF	5M	Reserved	Reserved
00 11E0 0000	00 11E0 7FFF	32K	CorePac1 L1P SRAM	CorePac1 L1P SRAM
00 11E0 8000	00 11EF FFFF	1M-32K	Reserved	Reserved
00 11F0 0000	00 11F0 7FFF	32K	CorePac1 L1D SRAM	CorePac1 L1D SRAM
00 11F0 8000	00 127F FFFF	9M-32K	Reserved	Reserved
00 1280 0000	00 128F FFFF	1M	CorePac2 L2 SRAM	CorePac2 L2 SRAM
00 1290 0000	00 12DF FFFF	5M	Reserved	Reserved

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Table 4-1 Device Memory Map Summary for TCI6634K2K (Part 10 of 12)

Physical 40 bit Address		Bytes	DSP View	SOC View
Start	End			
00 12E0 0000	00 12E0 7FFF	32K	CorePac2 L1P SRAM	CorePac2 L1P SRAM
00 12E0 8000	00 12EF FFFF	1M-32K	Reserved	Reserved
00 12F0 0000	00 12F0 7FFF	32K	CorePac2 L1D SRAM	CorePac2 L1D SRAM
00 12F0 8000	00 137F FFFF	9M-32K	Reserved	Reserved
00 1380 0000	00 1388 FFFF	1M	CorePac3 L2 SRAM	CorePac3 L2 SRAM
00 1390 0000	00 13DF FFFF	5M	Reserved	Reserved
00 13E0 0000	00 13E0 7FFF	32K	CorePac3 L1P SRAM	CorePac3 L1P SRAM
00 13E0 8000	00 13EF FFFF	1M-32K	Reserved	Reserved
00 13F0 0000	00 13F0 7FFF	32K	CorePac3 L1D SRAM	CorePac3 L1D SRAM
00 13F0 8000	00 147F FFFF	9M-32K	Reserved	Reserved
00 1480 0000	00 148F FFFF	1M	CorePac4 L2 SRAM	CorePac4 L2 SRAM
00 1490 0000	00 14DF FFFF	5M	Reserved	Reserved
00 14E0 0000	00 14E0 7FFF	32K	CorePac4 L1P SRAM	CorePac4 L1P SRAM
00 14E0 8000	00 14EF FFFF	1M-32K	Reserved	Reserved
00 14F0 0000	00 14F0 7FFF	32K	CorePac4 L1D SRAM	CorePac4 L1D SRAM
00 14F0 8000	00 157F FFFF	9M-32K	Reserved	Reserved
00 1580 0000	00 158F FFFF	1M	CorePac5 L2 SRAM	CorePac5 L2 SRAM
00 1590 0000	00 15DF FFFF	5M	Reserved	Reserved
00 15E0 0000	00 15E0 7FFF	32K	CorePac5 L1P SRAM	CorePac5 L1P SRAM
00 15E0 8000	00 15EF FFFF	1M-32K	Reserved	Reserved
00 15F0 0000	00 15F0 7FFF	32K	CorePac5 L1D SRAM	CorePac5 L1D SRAM
00 15F0 8000	00 167F FFFF	9M-32K	Reserved	Reserved
00 1680 0000	00 168F FFFF	1M	CorePac6 L2 SRAM	CorePac6 L2 SRAM
00 1690 0000	00 16DF FFFF	5M	Reserved	Reserved
00 16E0 0000	00 16E0 7FFF	32K	CorePac6 L1P SRAM	CorePac6 L1P SRAM
00 16E0 8000	00 16EF FFFF	1M-32K	Reserved	Reserved
00 16F0 0000	00 16F0 7FFF	32K	CorePac6 L1D SRAM	CorePac6 L1D SRAM
00 16F0 8000	00 177F FFFF	9M-32K	Reserved	Reserved
00 1780 0000	00 178F FFFF	1M	CorePac7 L2 SRAM	CorePac7 L2 SRAM
00 1790 0000	00 17DF FFFF	5M	Reserved	Reserved
00 17E0 0000	00 17E0 7FFF	32K	CorePac7 L1P SRAM	CorePac7 L1P SRAM
00 17E0 8000	00 17EF FFFF	1M-32K	Reserved	Reserved
00 17F0 0000	00 17F0 7FFF	32K	CorePac7 L1D SRAM	CorePac7 L1D SRAM
00 17F0 8000	00 1FFF FFFF	129M-32K	Reserved	Reserved
00 2000 0000	00 200F FFFF	1M	System trace manager (STM) configuration	System trace manager (STM) configuration
00 2010 0000	00 201F FFFF	1M	Reserved	Reserved
00 2020 0000	00 205F FFFF	4M	Reserved	Reserved
00 2060 0000	00 206F FFFF	1M	TCP3d_1 data	TCP3d_1 data
00 2070 0000	00 207F FFFF	1M	TCP3d_2 data	TCP3d_2 data
00 2080 0000	00 208F FFFF	1M	TCP3d_0 data	TCP3d_0 data
00 2090 0000	00 209F FFFF	1M	TCP3d_3 data	TCP3d_3 data
00 20A0 0000	00 20A3 FFFF	256K	Reserved	Reserved

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Table 4-1 Device Memory Map Summary for TCI6634K2K (Part 11 of 12)

Physical 40 bit Address				
Start	End	Bytes	DSP View	SOC View
00 20A4 0000	00 20A4 FFFF	64K	Reserved	Reserved
00 20A5 0000	00 20AF FFFF	704K	Reserved	Reserved
00 20B0 0000	00 20B3 FFFF	256	Boot ROM	Boot ROM
00 20B4 0000	00 20BE FFFF	704K	Reserved	Reserved
00 20BF 0000	00 20BF 01FF	64K	Reserved	Reserved
00 20C0 0000	00 20FF FFFF	4M	Reserved	Reserved
00 2100 0000	00 2100 03FF	1K	Reserved	Reserved
00 2100 0400	00 2100 05FF	512	SPI0	SPI0
00 2100 0600	00 2100 07FF	512	SPI1	SPI1
00 2100 0800	00 2100 09FF	512	SPI2	SPI2
00 2100 0A00	00 2100 0AFF	256	AEMIF Config	AEMIF Config
00 2100 0B00	00 2100 FFFF	62K-768	Reserved	Reserved
00 2101 0000	00 2101 01FF	512	DDR3A EMIF Config	DDR3A EMIF Config
00 2101 0200	00 2101 07FF	2K-512	Reserved	Reserved
00 2101 0800	00 2101 09FF	512	Reserved	Reserved
00 2101 0A00	00 2101 0FFF	2K-512	Reserved	Reserved
00 2101 1000	00 2101 FFFF	60K	Reserved	Reserved
00 2102 0000	00 2103 FFFF	128K	DDR3B EMIF configuration	DDR3B EMIF configuration
00 2104 0000	00 217F FFFF	4M-256K	Reserved	Reserved
00 2140 0000	00 2140 00FF	256	HyperLink0 config	HyperLink0 config
00 2140 0100	00 2140 01FF	256	HyperLink1 config	HyperLink1 config
00 2140 0400	00 217F FFFF	4M-512	Reserved	Reserved
00 2180 0000	00 2180 7FFF	32K	PCIe config	PCIe config
00 2180 8000	00 21BF FFFF	4M-32K	Reserved	Reserved
00 21C0 0000	00 21FF FFFF	4M	Reserved	Reserved
00 2200 0000	00 229F FFFF	10M	Reserved	Reserved
00 22A0 0000	00 22A0 FFFF	64K	VCP2_0 Data	VCP2_0 Data
00 22A1 0000	00 22AF FFFF	1M-64K	Reserved	Reserved
00 22B0 0000	00 22B0 FFFF	64K	VCP2_1 Data	VCP2_1 Data
00 22B1 0000	00 22BF FFFF	1M-64K	Reserved	Reserved
00 22C0 0000	00 22C0 FFFF	64K	VCP2_2 Data	VCP2_2 Data
00 22C1 0000	00 22CF FFFF	1M-64K	Reserved	Reserved
00 22D0 0000	00 22D0 FFFF	64K	VCP2_3 Data	VCP2_3 Data
00 22D1 0000	00 22DF FFFF	1M-64K	Reserved	Reserved
00 22E0 0000	00 22E0 FFFF	64K	VCP2_4 Data	VCP2_4 Data
00 22E1 0000	00 22EF FFFF	1M-64K	Reserved	Reserved
00 22F0 0000	00 22F0 FFFF	64K	VCP2_5 Data	VCP2_5 Data
00 22F1 0000	00 22FF FFFF	1M-64K	Reserved	Reserved
00 2300 0000	00 2300 FFFF	64K	VCP2_6 Data	VCP2_6 Data
00 2301 0000	00 230F FFFF	1M-64K	Reserved	Reserved
00 2310 0000	00 2310 FFFF	64K	VCP2_7 Data	VCP2_7 Data
00 2311 0000	00 231F FFFF	1M-64K	Reserved	Reserved
00 2320 0000	00 2324 FFFF	384K	TAC BEI	TAC BEI

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Table 4-1 Device Memory Map Summary for TCI6634K2K (Part 12 of 12)

Physical 40 bit Address		Bytes	DSP View	SOC View
Start	**End**			
00 2325 0000	00 239F FFFF	8M-384K	Reserved	Reserved
00 23A0 0000	00 23BF FFFF	2M	Navigator	Navigator
00 23C0 0000	00 23FF FFFF	4M	BCR-RAC data	BCR-RAC data
00 2400 0000	00 27FF FFFF	64M	Reserved	Reserved
00 2800 0000	00 2FFF FFFF	128M	HyperLink1 data	HyperLink1 data
00 3000 0000	00 33FF FFFF	64M	EMIF16 CS2	EMIF16 CS2
00 3400 0000	00 37FF FFFF	64M	EMIF16 CS3	EMIF16 CS3
00 3800 0000	00 3BFF FFFF	64M	EMIF16 CS4	EMIF16 CS4
00 3C00 0000	00 3FFF FFFF	64M	EMIF16 CS5	EMIF16 CS5
00 4000 0000	00 4FFF FFFF	256M	HyperLink0 data	HyperLink0 data
00 5000 0000	00 5FFF FFFF	256M	PCIe data	PCIe data
00 6000 0000	00 7FFF FFFF	512M	DDR3B data (1)	DDR3B data (1)
00 8000 0000	00 FFFF FFFF	2G	DDR3B data	DDR3B data
01 0000 0000	01 20FF FFFF	528M	Reserved	Reserved
01 2100 0000	01 2100 01FF	512	DDR3A EMIF configuration (2)	DDR3A EMIF configuration (3)
01 2100 0200	07 FFFF FFFF	32G-512	Reserved	Reserved
08 0000 0000	09 FFFF FFFF	8G	DDR3A data (2)	DDR3A data (3)
0A 0000 0000	FF FFFF FFFF	984G	Reserved	Reserved
End of Table 4-1				

1 Address 00 6000 0000-00 7FFF FFFF is aliased to 00 8000 0000-00 9FFF FFFF (the first 512M DDR3B data space).
2 Access to 40-bit address requires XMC MPAX programmation.
3 Access to 40-bit address requires MSMC MPAX programmation.

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4.2 Memory Protection Unit (MPU) for TCI6634K2K

CFG (configuration) space of all slave devices on the TeraNet is protected by the MPU. The TCI6634K2K contains fifteen MPUs:

- MPU0 is used to protect main CORE/3 CFG TeraNet_3P_B (SCR_3P (B)).
- MPU1/2/5 are used for QM_SS (one for VBUSM port and one each for the two configuration VBUSP port).
- MPU3/4/6 are used for RAC_0/RAC_1, RAC_2/RAC_3 and BCR.
- MPU7 is used for DDR3_B.
- MPU8 is used for peripherals connected to TeraNet_6P_A (SCR_6P (A)).
- MPU9 is used for interrupt controllers connected to TeraNet_3P (SCR_3P).
- MPU10 is used for semaphore.
- MPU11 is used to protect TeraNet_6P_B (SCR_6P (B)) CPU/6 CFG TeraNet
- MPU12/13/14 are used for SPI0/1/2

This section contains MPU register map and details of device-specific MPU registers only. For MPU features and details of generic MPU registers, see the *Memory Protection Unit (MPU) for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

The following tables show the configuration of each MPU and the memory regions protected by each MPU.

Table 4-2 MPU0- MPU5 Default Configuration

Setting	MPU0 Main SCR_3P (B)	MPU1 (QM_SS DATA PORT)	MPU2 (QM_SS CFG1 PORT)	MPU3 BCR CFG	MPU4 RAC 0/1	MPU5 (QM_SS CFG1 PORT)
Default permission	Assume allowed	Assume allowed	Assume allowed	Assume allowed	Assume allowed	Assume allowed
Number of allowed IDs supported	16	16	16	16	16	16
Number of programmable ranges supported	16	16	16	2	4	16
Compare width	1KB granularity	1KB granularity	1KB granularity	1KB granularity	1KB granularity	1KB granularity
End of Table 4-2						

Table 4-3 MPU6-MPU11 Default Configuration

Setting	MPU6 RAC 2/3	MPU7 DDR3B)	MPU8 EMIF16	MPU9 INTC	MPU10 SM	MPU11 SCR_6P (B)
Default permission	Assume allowed	Assume allowed	Assume allowed	Assume allowed	Assume allowed	Assume allowed
Number of allowed IDs supported	16	16	16	16	16	16
Number of programmable ranges supported	4	16	8	4	2	16
Compare width	1KB granularity	1KB granularity	1KB granularity	1KB granularity	1KB granularity	1KB granularity
End of Table 4-3						

Table 4-4 MPU12- MPU14 Default Configuration (Part 1 of 2)

Setting	MPU12 SPI0	MPU13 SPI1	MPU14 SPI2
Default permission	Assume allowed	Assume allowed	Assume allowed
Number of allowed IDs supported	16	16	16

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Table 4-4 MPU12- MPU14 Default Configuration (Part 2 of 2)

Setting	MPU12 SPI0	MPU13 SPI1	MPU14 SPI2
Number of programmable ranges supported	2	2	2
Compare width	1KB granularity	1KB granularity	1KB granularity
End of Table 4-4			

Table 4-5 MPU Memory Regions

	Memory Protection	Start Address	End Address
MPU0	Main CFG SCR	0x01D0_0000	0x01e7_FFFF
MPU1	QM_SS DATA PORT	0x23A0_0000	0x23BF_FFFF
MPU2	QM_SS CFG1 PORT	0x02A0_0000	0x02AF_FFFF
MPU3	BCR	0x027C_0000	0x027C_03FF
MPU4	RAC 0/1	0x0210_0000	0x0215_FFFF
MPU5	QM_SS CFG2 PORT	0x02A0_4000	0x02BF_FFFF
MPU6	RAC 2/3	0x02C0_0000	0x02CD_FFFF
MPU7	DDR3B	0x2101_0000	0xFFFF_FFFF
MPU8	SPIROM/EMIF16	0x20B0_0000	0x3FFF_FFFF
MPU9	INTC/AINTC	0x0264_0000	0x0264_07FF
MPU10	Semaphore	0x0260_0000	0x0260_9FFF
MPU11	SCR_6 and CPU/6 CFG SCR	0x0220_0000	0x03FF_FFFF
MPU12	SPI0	0x2100_0400	0x2100_07FF
MPU13	SPI1	0x2100_0400	0x2100_07FF
MPU14	SPI2	0x2100_0800	0x2100_0AFF
End of Table 4-5			

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Table 4-6 shows the unique Master ID assigned to each C66x CorePac and peripherals on the device.

Table 4-6 Master ID Settings (Part 1 of 4)

Master ID	TCI6634
0	C66x CorePac0
1	C66x CorePac1
2	C66x CorePac2
3	C66x CorePac3
4	C66x CorePac4
5	C66x CorePac5
6	C66x CorePac6
7	C66x CorePac7
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	C66x CorePac0 CFG
17	C66x CorePac1 CFG
18	C66x CorePac2 CFG
19	C66x CorePac3 CFG

Table 4-6 Master ID Settings (Part 2 of 4)

Master ID	TCI6634
20	C66x CorePac4 CFG
21	C66x CorePac5 CFG
22	C66x CorePac6 CFG
23	C66x CorePac7 CFG
24	Reserved
25	EDMA0_TC0 read
26	EDMA0_TC0 write
27	EDMA0_TC1 read
28	HyperLink0
29	HyperLink1
30	SRIO
31	PCIE
32	EDMA0_TC1 write
33	EDMA1_TC0 read
34	EDMA1_TC0 write
35	EDMA1_TC1 read
36	EDMA1_TC1write
37	EDMA1_TC2 read
38	EDMA1_TC2 write
39	EDMA1_TC3 read
40	EDMA1_TC3 write
41	EDMA2_TC0 read
42	EDMA2_TC0 write
43	EDMA2_TC1 read
44	EDMA2_TC1 write
45	EDMA2_TC2 read
46	EDMA2_TC2 write
47	EDMA2_TC3 read
48	EDMA2_TC3 write
49	EDMA3_TC0 read
50	EDMA3_TC0 write
51	EDMA3_TC1 read
52	Reserved
53	EDMA3_TC1 write
54 to 55	SRIO PKTDMA
56	FFTC_0
57	FFTC_1
58	RAC_1_BE0
59	RAC_1_BE1
60	RAC_0_BE0
61	RAC_0_BE1
62	EDMA3CC0
63	EDMA3CC1
64	EDMA3CC2

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Table 4-6 Master ID Settings (Part 3 of 4)

Master ID	TCI6634
65	FFTC_2
66	Reserved
67	FFTC_3
68 to 71	Queue Manager
72 to 79	AIF2
80	Reserved1
81	BCP_DIO0
82	BCP_DIO1
83	Reserved
84 to 87	10GbE
88	RAC_2_BE0
89	RAC_2_BE1
90	RAC_3_BE0
91	RAC_3_BE1
92 to 95	Packet Coprocessor MST2
96 to 99	Packet Coprocessor MST1
100 to 101	Reserved
102	BCP
103	TAC_FEI0
104	TAC_FEI1
105	FFTC_4_CDMA
106	FFTC_5_CDMA
107	DBG_DAP
108-139	Reserved
140	CPT_L2_0
141	CPT_L2_1
142	CPT_L2_2
143	CPT_L2_3
144	CPT_L2_4
145	CPT_L2_5
146	CPT_L2_6
147	CPT_L2_7
148	CPT_MSMC0
149	CPT_MSMC1
150	CPT_MSMC2
151	CPT_MSMC3
152	CPT_DDR3A
153	CPT_SM
154	CPT_QM_CFG1
155	CPT_QM_M
156	CPT_CFG
157	CPT_RAC_FEI
158	CPT_RAC_2FG1
159	CPT_TAC_BE

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Table 4-6 Master ID Settings (Part 4 of 4)

Master ID	TCI6634
160	CPT_QM_CFG2
161	CPT_DDR3B
162	CPT_RAC_2FG2
163	CPT_BCR_CFG
164	CPT_EDMA3CC0_4
165	CPT_EDMA3CC1_2_3
166	CPT_INTC
167	CPT_SPI_ROM
168	Reserved
169	EDMA4_TC0 read
170	EDMA4_TC0 write
171	EDMA4_TC1 read
172	EDMA4_TC1 write
173	EDMA4_CC_TR
174	CPT_MSMC0
175	CPT_MSMC1
176	CPT_MSMC2
177	CPT_MSMC3
178	Reserved
179	TAC FEI2
180-183	NETCP
184-255	Reserved
End of Table 4-6	

Note—Some of the PKTDMA based-peripherals require multiple master IDs. Queue Manager Packet DMA is assigned with 88, 89, 90, 91, but only 88-89 are actually used. For Queue Manager port, 56, 57, 58, 59 are assigned while only 1 (56) is actually used. For AIF2, 64, 65, 66, 67, 68, 69, 70, 71 are assigned while only 4 (64-67) are actually used. There are two master ID values assigned to the Queue Manager_second master port, one master ID for external linking RAM and the other one for the PDSP/MCDM accesses.

Table 4-7 shows the privilege ID of each C66x CorePac and every mastering peripheral. The table also shows the privilege level (supervisor vs. user), security level (secure vs. non-secure), and access type (instruction read vs. data/DMA read or write) of each master on the device. In some cases, a particular setting depends on software being executed at the time of the access or the configuration of the master peripheral.

Table 4-7 Privilege ID Settings (Part 1 of 2)

Privilege ID	Master	Privilege Level	Security Level	Access Type
0	C66x CorePac0	SW dependant, driven by MSMC	Non-secure	DMA
1	C66x CorePac1	SW dependant, driven by MSMC	Non-secure	DMA
2	C66x CorePac2	SW dependant, driven by MSMC	Non-secure	DMA
3	C66x CorePac3	SW dependant, driven by MSMC	Non-secure	DMA
4	C66x CorePac3	SW dependant, driven by MSMC	Non-secure	DMA
5	C66x CorePac3	SW dependant, driven by MSMC	Non-secure	DMA
6	C66x CorePac3	SW dependant, driven by MSMC	Non-secure	DMA

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Table 4-7 Privilege ID Settings (Part 2 of 2)

Privilege ID	Master	Privilege Level	Security Level	Access Type
7	C66x CorePac3	SW dependant, driven by MSMC	Non-secure	DMA
9	SRIO_M and all CPPI masters (NetCP, Both QM_CDMA, FFTC, BCP_CDMA, AIF, SRIO_CDMA, 10GbE), USB	User/driven by SRIO block, user mode and supervisor mode is determined by per transaction basis. Only the transaction with source ID matching the value in SupervisorID register is granted supervisor mode.	Non-secure	DMA
10	QM_CDMA/Network Coprocessor Packet DMA	User	Non-secure	DMA
11	PCIe	Supervisor	Non-secure	DMA
12	DAP	Driven by Emulation SW	Driven by Emulation SW	DMA
13	RAC_TAC/BCP_DIO	Supervisor	Non-secure	DMA
14	HyperLink	Supervisor	Non-secure	DMA
15	Reserved			
End of Table 4-7				

4.2.1 MPU Registers

This section includes the offsets for MPU registers and definitions for device-specific MPU registers. For Number of Programmable Ranges supported (PROGx_MPSA, PROGxMPEA) refer to the following tables.

4.2.1.1 MPU Register Map

Table 4-8 MPU Registers (Part 1 of 2)

Offset	Name	Description
0h	REVID	Revision ID
4h	CONFIG	Configuration
10h	IRAWSTAT	Interrupt raw status/set
14h	IENSTAT	Interrupt enable status/clear
18h	IENSET	Interrupt enable
1Ch	IENCLR	Interrupt enable clear
20h	EOI	End of interrupt
200h	PROG0_MPSAR	Programmable range 0, start address
204h	PROG0_MPEAR	Programmable range 0, end address
208h	PROG0_MPPAR	Programmable range 0, memory page protection attributes
210h	PROG1_MPSAR	Programmable range 1, start address
214h	PROG1_MPEAR	Programmable range 1, end address
218h	PROG1_MPPAR	Programmable range 1, memory page protection attributes
220h	PROG2_MPSAR	Programmable range 2, start address
224h	PROG2_MPEAR	Programmable range 2, end address
228h	PROG2_MPPAR	Programmable range 2, memory page protection attributes
230h	PROG3_MPSAR	Programmable range 3, start address
234h	PROG3_MPEAR	Programmable range 3, end address
238h	PROG3_MPPAR	Programmable range 3, memory page protection attributes
240h	PROG4_MPSAR	Programmable range 4, start address
244h	PROG4_MPEAR	Programmable range 4, end address
248h	PROG4_MPPAR	Programmable range 4, memory page protection attributes

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Table 4-8 MPU Registers (Part 2 of 2)

Offset	Name	Description
250h	PROG5_MPSAR	Programmable range 5, start address
254h	PROG5_MPEAR	Programmable range 5, end address
258h	PROG5_MPPAR	Programmable range 5, memory page protection attributes
260h	PROG6_MPSAR	Programmable range 6, start address
264h	PROG6_MPEAR	Programmable range 6, end address
268h	PROG6_MPPAR	Programmable range 6, memory page protection attributes
270h	PROG7_MPSAR	Programmable range 7, start address
274h	PROG7_MPEAR	Programmable range 7, end address
278h	PROG7_MPPAR	Programmable range 7, memory page protection attributes
280h	PROG8_MPSAR	Programmable range 8, start address
284h	PROG8_MPEAR	Programmable range 8, end address
288h	PROG8_MPPAR	Programmable range 8, memory page protection attributes
290h	PROG9_MPSAR	Programmable range 9, start address
294h	PROG9_MPEAR	Programmable range 9, end address
298h	PROG9_MPPAR	Programmable range 9, memory page protection attributes
2A0h	PROG10_MPSAR	Programmable range 10, start address
2A4h	PROG10_MPEAR	Programmable range 10, end address
2A8h	PROG10_MPPAR	Programmable range 10, memory page protection attributes
2B0h	PROG11_MPSAR	Programmable range 11, start address
2B4h	PROG11_MPEAR	Programmable range 11, end address
2B8h	PROG11_MPPAR	Programmable range 11, memory page protection attributes
2C0h	PROG12_MPSAR	Programmable range 12, start address
2C4h	PROG12_MPEAR	Programmable range 12, end address
2C8h	PROG12_MPPAR	Programmable range 12, memory page protection attributes
2D0h	PROG13_MPSAR	Programmable range 13, start address
2D4h	PROG13_MPEAR	Programmable range 13, end address
2Dh	PROG13_MPPAR	Programmable range 13, memory page protection attributes
2E0h	PROG14_MPSAR	Programmable range 14, start address
2E4h	PROG14_MPEAR	Programmable range 14, end address
2E8h	PROG14_MPPAR	Programmable range 14, memory page protection attributes
2F0h	PROG15_MPSAR	Programmable range 15, start address
2F4h	PROG15_MPEAR	Programmable range 15, end address
2F8h	PROG15_MPPAR	Programmable range 15, memory page protection attributes
300h	FLTADDRR	Fault address
304h	FLTSTAT	Fault status
308h	FLTCLR	Fault clear
End of Table 4-8		

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4.2.1.2 Device-Specific MPU Registers

4.2.1.2.1 Configuration Register (CONFIG)

The configuration register (CONFIG) contains the configuration value of the MPU.

Figure 4-1 Configuration Register (CONFIG)

	31–24	23–20	19–16	15–12	11–1	0
	ADDR_WIDTH	NUM_FIXED	NUM_PROG	NUM_AIDS	Reserved	ASSUME_ALLOWED
Reset Values						
MPU0	R-0	R-0	R-16	R-16	R-0	R-1
MPU1	R-0	R-0	R-16	R-16	R-0	R-1
MPU2	R-0	R-0	R-16	R-16	R-0	R-1
MPU3	R-0	R-0	R-2	R-16	R-0	R-1
MPU4	R-0	R-0	R-4	R-16	R-0	R-1
MPU5	R-0	R-0	R-16	R-16	R-0	R-1
MPU6	R-0	R-0	R-4	R-16	R-0	R-1
MPU7	R-0	R-0	R-16	R-16	R-0	R-1
MPU8	R-0	R-0	R-8	R-16	R-0	R-1
MPU9	R-0	R-0	R-4	R-16	R-0	R-1
MPU10	R-0	R-0	R-2	R-16	R-0	R-1
MPU11	R-0	R-0	R-16	R-16	R-0	R-1
MPU12	R-0	R-0	R-2	R-16	R-0	R-1
MPU13	R-0	R-0	R-2	R-16	R-0	R-1
MPU14	R-0	R-0	R-2	R-16	R-0	R-1

Legend: R = Read only; -*n* = value after reset

Table 4-9 Configuration Register Field Descriptions

Bits	Field	Description
31 – 24	ADDR_WIDTH	Address alignment for range checking 0 = 1KB alignment 6 = 64KB alignment
23 – 20	NUM_FIXED	Number of fixed address ranges
19 – 16	NUM_PROG	Number of programmable address ranges
15 – 12	NUM_AIDS	Number of supported AIDs
11 – 1	Reserved	Reserved. Always read as 0.
0	ASSUME_ALLOWED	Assume allowed bit. When an address is not covered by any MPU protection range, this bit determines whether the transfer is assumed to be allowed or not. 0 = Assume disallowed 1 = Assume allowed
End of Table 4-9		

4.2.2 MPU Programmable Range Registers

4.2.2.1 Programmable Range *n* Start Address Register (PROG*n*_MPSAR)

The Programmable Address Start Register holds the start address for the range. This register is writeable by a supervisor entity only. If NS = 0 (non-secure mode) in the associated MPPAR register, then the register is also writeable only by a secure entity.

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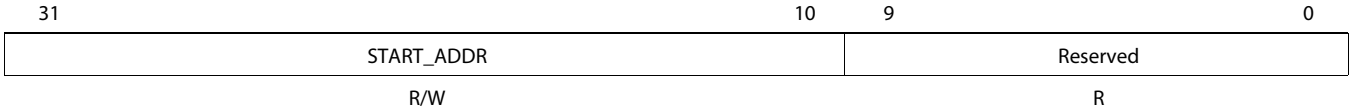
The start address must be aligned on a page boundary. The size of the page is 1K byte. The size of the page determines the width of the address field in MPSAR and MPEAR.

Figure 4-2 Programmable Range *n* Start Address Register (PROG*n*_MPSAR)



Legend: R = Read only; R/W = Read/Write

Table 4-10 Programmable Range *n* Start Address Register Field Descriptions

Bit	Field	Description
31 – 10	START_ADDR	Start address for range n
9 – 0	Reserved	Reserved. Always read as 0.
End of Table 4-10		

Table 4-11 MPU0-MPU5 Programmable Range *n* Start Address Register (PROG*n*_MPSAR) Reset Values

Register	MPU0	MPU1	MPU2	MPU3	MPU4	MPU5
PROG0_MPSAR	0x01D0_0000	0x23A0_0000	0x02A0_0000	0x027C_0000	0x0210_0000	0x02A0_4000
PROG1_MPSAR	0x01F0_0000	0x23A0_2000	0x02A0_2000	N/A	0x01F8_0000	0x02A0_5000
PROG2_MPSAR	0x02F0_0000	0x023A_6000	0x02A0_6000	N/A	Reserved	0x02A0_6400
PROG3_MPSAR	0x0200_0000	0x23A0_6800	0x02A0_6800	N/A	Reserved	0x02A0_7400
PROG4_MPSAR	0x020C_0000	0x23A0_7000	0x02A0_7000	N/A	N/A	0x02A0_A000
PROG5_MPSAR	0x021C_0000	0x23A0_8000	0x02A0_8000	N/A	N/A	0x02A0_D000
PROG6_MPSAR	0x021D_0000	0x23A0_C000	0x02A0_C000	N/A	N/A	0x02A0_E000
PROG7_MPSAR	0x021F_0000	0x23A0_E000	0x02A0_E000	N/A	N/A	0x02A0_F000
PROG8_MPSAR	0x0234_0000	0x23A0_F000	0x02A0_F000	N/A	N/A	0x02A0_F800
PROG9_MPSAR	0x0254_0000	0x23A0_F800	0x02A0_F800	N/A	N/A	0x02A1_2000
PROG10_MPSAR	0x0258_0000	0x23A1_0000	0x02A1_0000	N/A	N/A	0x02A1_C000
PROG11_MPSAR	Reserved	0x23A1_C000	0x02A2_0000	N/A	N/A	0x02A2_8000
PROG12_MPSAR	0x0290_0000	0x23A4_0000	0x02A4_0000	N/A	N/A	0x02A6_0000
PROG13_MPSAR	0x01E8_0000	0x23A8_0000	0x02A8_0000	N/A	N/A	0x02AA_0000
PROG14_MPSAR	0x01E8_0800	0x23B0_0000	0x02AC_0000	N/A	N/A	0x02B0_0000
PROG15_MPSAR	0x01E0_0000	0x23B8_0000	0x02AE_0000	N/A	N/A	0x02B8_0000
End of Table 4-11						

Table 4-12 MPU6-MPU11Programmable Range *n* Start Address Register (PROG*n*_MPSAR) Reset Values (Part 1 of 2)

Register	MPU6	MPU7	MPU8	MPU9	MPU10	MPU11
PROG0_MPSAR	0x02C0_0000	0x2101_0000	0x3000_0000	0x0260_0000	0x0264_0000	0x0220_0000
PROG1_MPSAR	0x02C8_0000	0x0000_0000	0x3200_0000	0x0260_4000	Reserved	0x0231_0000
PROG2_MPSAR	Reserved	0x0800_0000	0x3400_0000	Reserved	N/A	0x0231_A000
PROG3_MPSAR	Reserved	0x1000_0000	0x3600_0000	N/A	N/A	0x0233_0000
PROG4_MPSAR	N/A	0x1800_0000	0x3800_0000	N/A	N/A	0x0235_0000
PROG5_MPSAR	N/A	0x2000_0000	0x3A00_0000	N/A	N/A	0x0263_0000
PROG6_MPSAR	N/A	0x2800_0000	0x3C00_0000	N/A	N/A	0x0244_0000
PROG7_MPSAR	N/A	0x3000_0000	0x2100_0800	N/A	N/A	0x024C_0000
PROG8_MPSAR	N/A	0x3800_0000	N/A	N/A	N/A	0x0250_0000

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Table 4-12 MPU6-MPU11Programmable Range *n* Start Address Register (PROG*n*_MPSAR) Reset Values (Part 2 of 2)

Register	MPU6	MPU7	MPU8	MPU9	MPU10	MPU11
PROG9_MPSAR	N/A	0x4000_0000	N/A	N/A	N/A	0x0253_0000
PROG10_MPSAR	N/A	0x4800_0000	N/A	N/A	N/A	0x0253_0C00
PROG11_MPSAR	N/A	0x5000_0000	N/A	N/A	N/A	0x0260_B000
PROG12_MPSAR	N/A	0x5800_0000	N/A	N/A	N/A	0x0262_0000
PROG13_MPSAR	N/A	0x6000_0000	N/A	N/A	N/A	0x0300_0000
PROG14_MPSAR	N/A	0x6800_0000	N/A	N/A	N/A	0x021E_0000
PROG15_MPSAR	N/A	0x7000_0000	N/A	N/A	N/A	0x0268_0000
End of Table 4-12						

Table 4-13 MPU12-MPU14 Programmable Range *n* Start Address Register (PROG*n*_MPSAR) Reset Values

Register	MPU12	MPU13	MPU14
PROG0_MPSAR	0x2100_0400	0x2100_0400	0x2100_0800
PROG1_MPSAR	Reserved	Reserved	Reserved
PROG2_MPSAR	N/A	N/A	N/A
PROG3_MPSAR	N/A	N/A	N/A
PROG4_MPSAR	N/A	N/A	N/A
PROG5_MPSAR	N/A	N/A	N/A
PROG6_MPSAR	N/A	N/A	N/A
PROG7_MPSAR	N/A	N/A	N/A
PROG8_MPSAR	N/A	N/A	N/A
PROG9_MPSAR	N/A	N/A	N/A
PROG10_MPSAR	N/A	N/A	N/A
PROG11_MPSAR	N/A	N/A	N/A
PROG12_MPSAR	N/A	N/A	N/A
PROG13_MPSAR	N/A	N/A	N/A
PROG14_MPSAR	N/A	N/A	N/A
PROG15_MPSAR	N/A	N/A	N/A
End of Table 4-13			

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4.2.2.2 Programmable Range *n* - End Address Register (PROG*n*_MPEAR)

The programmable address end register holds the end address for the range. This register is writeable by a supervisor entity only. If NS = 0 (non-secure mode) in the associated MPPAR register then the register is also writeable only by a secure entity.

The end address must be aligned on a page boundary. The size of the page depends on the MPU number. The page size for MPU1 is 1K byte and for MPU2 it is 64K bytes. The size of the page determines the width of the address field in MPSAR and MPEAR

Figure 4-3 Programmable Range *n* End Address Register (PROG*n*_MPEAR)

Legend: R = Read only; R/W = Read/Write

Table 4-14 Programmable Range *n* End Address Register Field Descriptions

Bit	Field	Description
31 – 10	END_ADDR	End address for range n
9 – 0	Reserved	Reserved. Always read as 3FFh.
End of Table 4-14		

Table 4-15 MPU0-MPU5 Programmable Range *n* End Address Register (PROG*n*_MPEAR) Reset Values

Register	MPU0	MPU1	MPU2	MPU3	MPU4	MPU5
PROG0_MPEAR	0x01DF_FFFF	0x23A0_1FFF	0x02A0_00FF	0x027C_03FF	0x0215_FFFF	0x02A0_4FFF
PROG1_MPEAR	0x01F7_FFFF	0x23A0_5FFF	0x02A0_3FFF	Reserved	0x01FD_FFFF	0x02A0_5FFF
PROG2_MPEAR	0x02FF_FFFF	0x23A0_67FF	0x02A0_63FF	N/A	Reserved	0x02A0_67FF
PROG3_MPEAR	0x020B_FFFF	0x23A0_6FFF	0x02A0_6FFF	N/A	N/A	0x02A0_7FFF
PROG4_MPEAR	0x020F_FFFF	0x23A0_7FFF	0x02A0_73FF	N/A	N/A	0x02A0_BFFF
PROG5_MPEAR	0x021C_83FF	0x23A0_BFFF	0x02A0_9FFF	N/A	N/A	0x02A0_DFFF
PROG6_MPEAR	0x021D_C0FF	0x23A0_DFFF	0x02A0_CFFF	N/A	N/A	0x02A0_E7FF
PROG7_MPEAR	0x021F_C7FF	0x23A0_EFFF	0x02A0_E7FF	N/A	N/A	0x02A0_F7FF
PROG8_MPEAR	0x0234_C0FF	0x23A0_F7FF	0x02A0_F7FF	N/A	N/A	0x02A0_FFFF
PROG9_MPEAR	0x0255_FFFF	0x23A0_FFFF	0x02A0_FFFF	N/A	N/A	0x02A1_7FFF
PROG10_MPEAR	0x025F_FFFF	0x23A1_BFFF	0x02A1_1FFF	N/A	N/A	0x02A1_FFFF
PROG11_MPEAR	Reserved	0x23A3_FFFF	0x02A2_5FFF	N/A	N/A	0x02A3_FFFF
PROG12_MPEAR	0x029F_FFFF	0x23A7_FFFF	0x02A5_FFFF	N/A	N/A	0x02A7_FFFF
PROG13_MPEAR	0x01E8_07FF	0x23AF_FFFF	0x02A9_FFFF	N/A	N/A	0x02AB_FFFF
PROG14_MPEAR	0x01E8_43FF	0x23B7_FFFF	0x02AD_FFFF	N/A	N/A	0x02B7_FFFF
PROG15_MPEAR	0x01E7_FFFF	0x23BF_FFFF	0x02AF_FFFF	N/A	N/A	0x02BF_FFFF
End of Table 4-15						

Table 4-16 MPU6-MPU11 Programmable Range *n* End Address Register (PROG*n*_MPEAR) Reset Values

Register	MPU6	MPU7	MPU8	MPU9	MPU10	MPU11
PROG0_MPEAR	0x02C5_FFFF	0x2103_FFFF	0x31FF_FFFF	0x0260_1FFF	0x0264_07FF	0x022F_027F
PROG1_MPEAR	0x02CD_FFFF	0x07FF_FFFF	0x33FF_FFFF	0x0260_5FFF	Reserved	0x0231_01FF
PROG2_MPEAR	Reserved	0x0FFF_FFFF	0x35FF_FFFF	0x0260_9FFF	N/A	0x0232_FFFF
PROG3_MPEAR	Reserved	0x17FF_FFFF	0x37FF_FFFF	0x0257_FFFF	N/A	0x0233_07FF
PROG4_MPEAR	N/A	0x1FFF_FFFF	0x39FF_FFFF	Reserved	N/A	0x0235_0FFF
PROG5_MPEAR	N/A	0x27FF_FFFF	0x3BFF_FFFF	Reserved	N/A	0x0263_FFFF
PROG6_MPEAR	N/A	0x2FFF_FFFF	0x3FFF_FFFF	Reserved	N/A	0x024B_3FFF
PROG7_MPEAR	N/A	0x37FF_FFFF	0x2100_0AFF	Reserved	N/A	0x024C_0BFF
PROG8_MPEAR	N/A	0x3FFF_FFFF	N/A	Reserved	N/A	0x0250_7FFF
PROG9_MPEAR	N/A	0x47FF_FFFF	N/A	Reserved	N/A	0x0253_0BFF
PROG10_MPEAR	N/A	0x4FFF_FFFF	N/A	Reserved	N/A	0x0253_FFFF
PROG11_MPEAR	N/A	0x57FF_FFFF	N/A	Reserved	N/A	0x0260_BFFF
PROG12_MPEAR	N/A	0x5FFF_FFFF	N/A	Reserved	N/A	0x0262_0FFF
PROG13_MPEAR	N/A	0x67FF_FFFF	N/A	Reserved	N/A	0x03FF_FFFF
PROG14_MPEAR	N/A	0x6FFF_FFFF	N/A	Reserved	N/A	0x021E_1FFF
PROG15_MPEAR	N/A	0x7FFF_FFFF	N/A	Reserved	N/A	0x026F_FFFF
End of Table 4-16						

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Table 4-17 MPU12-MPU14 Programmable Range *n* End Address Register (PROG*n*_MPEAR) Reset Values

Register	MPU12	MPU13	MPU14
PROG0_MPEAR	0x2100_07FF	0x2100_07FF	0x2100_0AFF
PROG1_MPEAR	Reserved	Reserved	Reserved
PROG2_MPEAR	N/A	N/A	N/A
PROG3_MPEAR	N/A	N/A	N/A
PROG4_MPEAR	N/A	N/A	N/A
PROG5_MPEAR	N/A	N/A	N/A
PROG6_MPEAR	N/A	N/A	N/A
PROG7_MPEAR	N/A	N/A	N/A
PROG8_MPEAR	N/A	N/A	N/A
PROG9_MPEAR	N/A	N/A	N/A
PROG10_MPEAR	N/A	N/A	N/A
PROG11_MPEAR	N/A	N/A	N/A
PROG12_MPEAR	N/A	N/A	N/A
PROG13_MPEAR	N/A	N/A	N/A
PROG14_MPEAR	N/A	N/A	N/A
PROG15_MPEAR	N/A	N/A	N/A
End of Table 4-17			

4.2.2.3 Programmable Range *n* Memory Protection Page Attribute Register (PROG*n*_MPPAR)

The programmable address memory protection page attribute register holds the permissions for the region. This register is writeable only by a non-debug supervisor entity. If NS = 0 (secure mode) then the register is also writeable only by a non-debug secure entity. The NS bit is writeable only by a non-debug secure entity. For debug accesses, the register is writeable only when NS = 1 or EMU = 1.

Figure 4-4 Programmable Range *n* Memory Protection Page Attribute Register (PROG*n*_MPPAR)

31	26	25	24	23	22	21	20	19	18	17	16	15
Reserved		AID15	AID14	AID13	AID12	AID11	AID10	AID9	AID8	AID7	AID6	AID5
R		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AID4	AID3	AID2	AID1	AID0	AIDX	Reserved	NS	EMU	SR	SW	SX	UR	UW	UX
R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Legend: R = Read only; R/W = Read/Write

Table 4-18 Programmable Range *n* Memory Protection Page Attribute Register Field Descriptions (Part 1 of 3)

Bits	Name	Description
31 – 26	Reserved	Reserved. Always read as 0.
25	AID15	Controls access from ID = 15 0 = Access denied 1 = Access granted
24	AID14	Controls access from ID = 14 0 = Access denied 1 = Access granted

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Table 4-18 Programmable Range *n* Memory Protection Page Attribute Register Field Descriptions (Part 2 of 3)

Bits	Name	Description
23	AID13	Controls access from ID = 13 0 = Access denied 1 = Access granted
22	AID12	Controls access from ID = 12 0 = Access denied 1 = Access granted
21	AID11	Controls access from ID = 11 0 = Access denied 1 = Access granted
20	AID10	Controls access from ID = 10 0 = Access denied 1 = Access granted
19	AID9	Controls access from ID = 9 0 = Access denied 1 = Access granted
18	AID8	Controls access from ID = 8 0 = Access denied 1 = Access granted
17	AID7	Controls access from ID = 7 0 = Access denied 1 = Access granted
16	AID6	Controls access from ID = 6 0 = Access denied 1 = Access granted
15	AID5	Controls access from ID = 5 0 = Access denied 1 = Access granted
14	AID4	Controls access from ID = 4 0 = Access denied 1 = Access granted
13	AID3	Controls access from ID = 3 0 = Access denied 1 = Access granted
12	AID2	Controls access from ID = 2 0 = Access denied 1 = Access granted
11	AID1	Controls access from ID = 1 0 = Access denied 1 = Access granted
10	AID0	Controls access from ID = 0 0 = Access denied 1 = Access granted
9	AIDX	Controls access from ID > 15 0 = Access denied 1 = Access granted
8	Reserved	Reserved. Always reads as 0.
7	NS	Non-secure access permission 0 = Only secure access allowed 1 = Non-secure access allowed
6	EMU	Emulation (debug) access permission. This bit is ignored if NS = 1 0 = Debug access not allowed 1 = Debug access allowed

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Table 4-18 Programmable Range *n* Memory Protection Page Attribute Register Field Descriptions (Part 3 of 3)

Bits	Name	Description
5	SR	Supervisor Read permission 0 = Access not allowed 1 = Access allowed
4	SW	Supervisor Write permission 0 = Access not allowed 1 = Access allowed
3	SX	Supervisor Execute permission 0 = Access not allowed 1 = Access allowed
2	UR	User Read permission 0 = Access not allowed 1 = Access allowed
1	UW	User Write permission 0 = Access not allowed 1 = Access allowed
0	UX	User Execute permission 0 = Access not allowed 1 = Access allowed
End of Table 4-181		

Table 4-19 MPU0-MPU5 Programmable Range *n* Memory Protection Page Attribute Register (PROG*n*_MPPAR) Reset Values

Register	MPU0	MPU1	MPU2	MPU3	MPU4	MPU5
PROG0_MPPAR	0x03FF_FCB6	0x03FF_FCB6	0x03FF_FCB6	0x03FF_FCB6	0x03FF_FCB6	0x03FF_FCB4
PROG1_MPPAR	0x03FF_FCB6	0x03FF_FCB4	0x03FF_FCB4	0x03FF_FCB6	0x03FF_FCB6	0x03FF_FCB4
PROG2_MPPAR	0x03FF_FCB6	0x03FF_FCA4	0x03FF_FCA4	N/A	0x03FF_FCB6	0x03FF_FCA4
PROG3_MPPAR	0x03FF_FCB6	0x03FF_FCB4	0x03FF_FCB4	N/A	0x03FF_FCB6	0x03FF_FCF4
PROG4_MPPAR	0x03FF_FCB6	0x03FF_FCF4	0x03FF_FCF4	N/A	N/A	0x03FF_FCB4
PROG5_MPPAR	0x03FF_FCB6	0x03FF_FCB4	0x03FF_FCB4	N/A	N/A	0x03FF_FCB4
PROG6_MPPAR	0x03FF_FCB6	0x03FF_FCB4	0x03FF_FCB4	N/A	N/A	0x03FF_FCB4
PROG7_MPPAR	0x03FF_FCB6	0x03FF_FCB4	0x03FF_FCB4	N/A	N/A	0x03FF_FCB4
PROG8_MPPAR	0x03FF_FCB6	0x03FF_FCB4	0x03FF_FCB4	N/A	N/A	0x03FF_FCF4
PROG9_MPPAR	0x03FF_FCB6	0x03FF_FCF4	0x03FF_FCF4	N/A	N/A	0x03FF_FCB4
PROG10_MPPAR	0x03FF_FCB6	0x03FF_FCB4	0x03FF_FCB4	N/A	N/A	0x03FF_FCF4
PROG11_MPPAR	0x03FF_FCB6	0x03FF_FCF4	0x03FF_FCF4	N/A	N/A	0x03FF_FCF4
PROG12_MPPAR	0x03FF_FCB4	0x03FF_FCA4	0x03FF_FCA4	N/A	N/A	0x03FF_FCA4
PROG13_MPPAR	0x03FF_FCB6	0x03FF_FCB6	0x03FF_FCB6	N/A	N/A	0x03FF_FCB6
PROG14_MPPAR	0x03FF_FCB0	0x03FF_FCA4	0x03FF_FCB6	N/A	N/A	0x03FF_FCA4
PROG15_MPPAR	0x03FF_FCB6	0x03FF_FCA4	0x03FF_FCB6	N/A	N/A	0x03FF_FCA4
End of Table 4-19						

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Table 4-20 MPU6-MPU11 Programmable Range *n* Memory Protection Page Attribute Register (PROG*n*_MPPAR) Reset Values

Register	MPU6	MPU7	MPU8	MPU9	MPU10	MPU11
PROG0_MPPAR	0x03FF_FCB6	0x03FF_FCB6	0x03FF_FCBF	0x03FF_FCB6	0x03FF_FCB6	0x03FF_FCB6
PROG1_MPPAR	0x03FF_FCB6	0x03FF_FCBF	0x03FF_FCBF	0x03FF_FCB6	0x03FF_FCB6	0x03FF_FCB0
PROG2_MPPAR	0x03FF_FCB6	0x03FF_FCBF	0x03FF_FCBF	0x03FF_FCB6	N/A	0x03FF_FCB6
PROG3_MPPAR	0x03FF_FCB6	0x03FF_FCBF	0x03FF_FCBF	0x03FF_FCB6	N/A	0x03FF_FCB0
PROG4_MPPAR	N/A	0x03FF_FCBF	0x03FF_FCBF	0x03FF_FCB6	N/A	0x03FF_FCB0
PROG5_MPPAR	N/A	0x03FF_FCBF	0x03FF_FCBF	0x03FF_FCB6	N/A	0x03FF_FCB6
PROG6_MPPAR	N/A	0x03FF_FCBF	0x03FF_FCBF	0x03FF_FCB6	N/A	0x03FF_FCB6
PROG7_MPPAR	N/A	0x03FF_FCBF	0x03FF_FCB6	0x03FF_FCB6	N/A	0x03FF_FCB0
PROG8_MPPAR	N/A	0x03FF_FCBF	N/A	0x03FF_FCB6	N/A	0x03FF_FCB0
PROG9_MPPAR	N/A	0x03FF_FCBF	N/A	0x03FF_FCB6	N/A	0x03FF_FCB6
PROG10_MPPAR	N/A	0x03FF_FCBF	N/A	0x03FF_FCB6	N/A	0x03FF_FCB6
PROG11_MPPAR	N/A	0x03FF_FCBF	N/A	0x03FF_FCB6	N/A	0x03FF_FCB6
PROG12_MPPAR	N/A	0x03FF_FCBF	N/A	0x03FF_FCB6	N/A	0x03FF_FCB0
PROG13_MPPAR	N/A	0x03FF_FCBF	N/A	0x03FF_FCB6	N/A	0x03FF_FCB6
PROG14_MPPAR	N/A	0x03FF_FCBF	N/A	0x03FF_FCB6	N/A	0x03FF_FCB0
PROG15_MPPAR	N/A	0x03FF_FCBF	N/A	0x03FF_FCB6	N/A	0x03FF_FCB6
End of Table 4-20						

Table 4-21 MPU12-MPU14 Programmable Range *n* Memory Protection Page Attribute Register (PROG*n*_MPPAR) Reset Values

Register	MPU12	MPU13	MPU14
PROG0_MPPAR	0x03FF_FCBF	0x03FF_FCBF	0x03FF_FCBF
PROG1_MPPAR	0x03FF_FCBF	0x03FF_FCBF	0x03FF_FCBF
PROG2_MPPAR	Reserved	Reserved	Reserved
PROG3_MPPAR	N/A	N/A	N/A
PROG4_MPPAR	N/A	N/A	N/A
PROG5_MPPAR	N/A	N/A	N/A
PROG6_MPPAR	N/A	N/A	N/A
PROG7_MPPAR	N/A	N/A	N/A
PROG8_MPPAR	N/A	N/A	N/A
PROG9_MPPAR	N/A	N/A	N/A
PROG10_MPPAR	N/A	N/A	N/A
PROG11_MPPAR	N/A	N/A	N/A
PROG12_MPPAR	N/A	N/A	N/A
PROG13_MPPAR	N/A	N/A	N/A
PROG14_MPPAR	N/A	N/A	N/A
PROG15_MPPAR	N/A	N/A	N/A
End of Table 4-21			

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4.3 Interrupts for TCI6634K2K

This section discusses the interrupt sources, controller, and topology. Also provided are tables describing the interrupt events.

4.3.1 Interrupt Sources and Interrupt Controller

The CPU interrupts on the TCI6634K2K device are configured through the C66x CorePac Interrupt Controller. The Interrupt Controller allows for up to 128 system events to be programmed to any of the 12 CPU interrupt inputs (CPUINT4 - CPUINT15), the CPU exception input (EXCEP), or the advanced emulation logic. The 128 system events consist of both internally-generated events (within the CorePac) and chip-level events.

Additional system events are routed to each of the C66x CorePacs to provide chip-level events that are not required as CPU interrupts/exceptions to be routed to the Interrupt Controller as emulation events. In addition, error-class events or infrequently used events are also routed through the system event router to offload the C66x CorePac interrupt selector. This is accomplished through the CorePac Interrupt Controller blocks, CIC[2:0]. This is clocked using CPU/6.

The event controllers consist of simple combination logic to provide additional events to each C66x CorePac, plus the EDMA3CC. CIC0 provides 8 broadcast events and 18 additional events to each of the C66x CorePacs, 0 through 3. Similarly, CIC1 provides 8 broadcast events and 18 additional events to each of the C66x CorePacs, 4 through 7. CIC2 provides 17, 26, 8, 8, 8, and 8 events to EDMA3CC0, EDMA3CC1, EDMA3C2, EDMA3CC3, EDMA3CC4, and HyperLink respectively.

The events that are routed to the C66x CorePacs for Advanced Event Triggering (AET) purposes, from those EDMA3CC and FSYNC events that are not otherwise provided to each C66x CorePac.

Modules such as FFTC, TCP3d, TAC, AIF, CP_MPU, BOOT_CFG, and CP_Tracer have level interrupts and EOI handshaking interface. The EOI value is 0 for TCP3d_x, TAC, AIF, CP_MPU, BOOT_CFG, and CP_Tracer.

For FFTC:

- the EOI value is 0 for FFTC_x_INTD_INTR0,
- the EOI value is 1 for FFTC_x_INTD_INTR1,
- the EOI value is 2 for FFTC_x_INTD_INTR2
- the EOI value is 3 for FFTC_x_INTD_INTR3 (where FFTC_x can be FFTC_0, FFTC_1, FFTC_2 , FFTC_3, FFTC_4 or FFTC_5)

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Figure 4-5 shows the TCI6634 interrupt topology.

Figure 4-5 Interrupt Topology

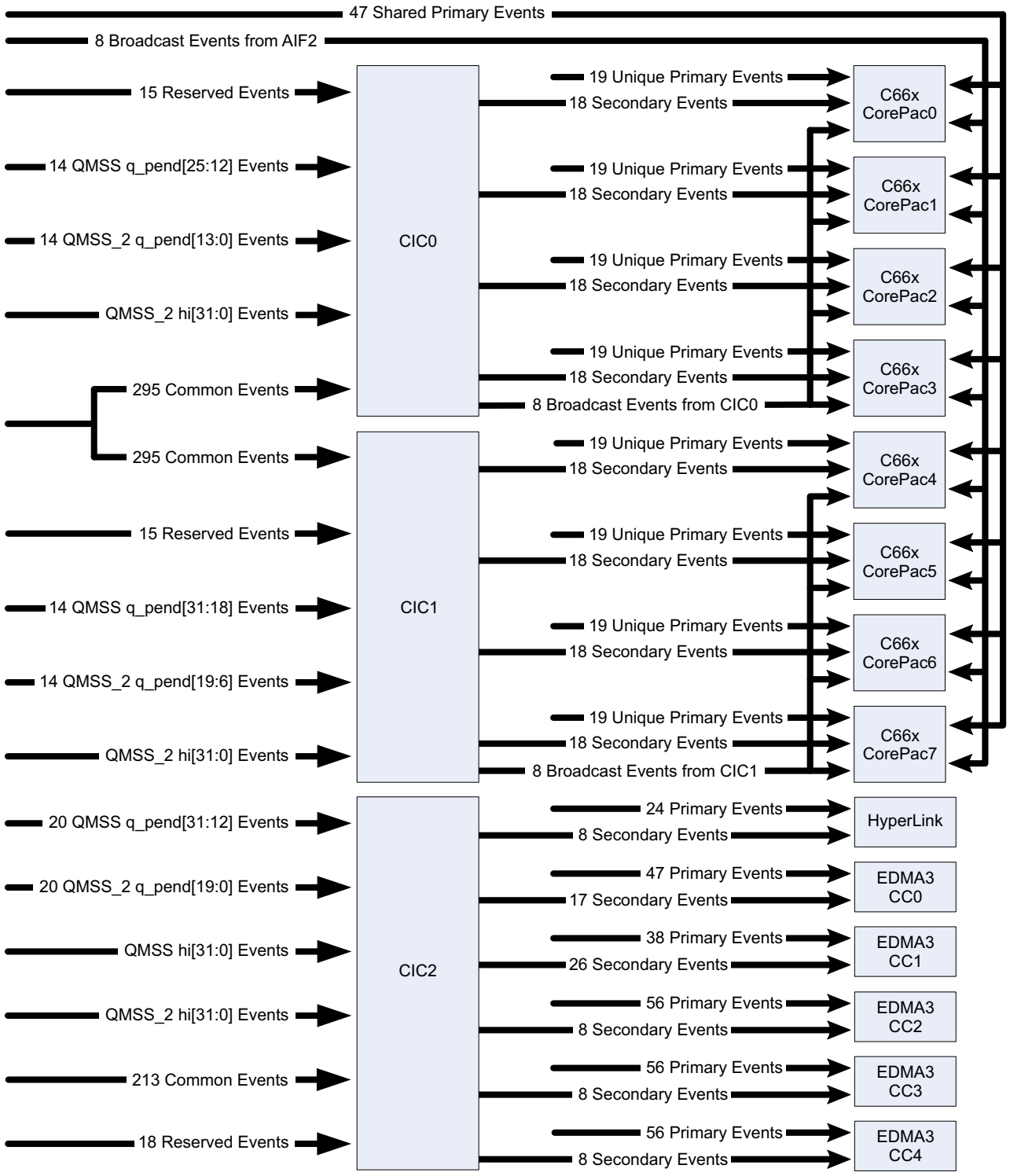

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Table 4-22 shows the mapping of system events.

Table 4-22 System Event Mapping — C66x CorePac Primary Interrupts (Part 1 of 3)

Event No.	Event Name	Description
0	EVT0	Event combiner 0 output
1	EVT1	Event combiner 1 output
2	EVT2	Event combiner 2 output
3	EVT3	Event combiner 3 output
4	TETB_HFULLINTN	TETB is half full
5	TETB_FULLINTN	TETB is full
6	TETB_ACQINTN	TETB Acquisition complete interrupt
7	TETB_OVFLINTN	TETB Overflow condition interrupt
8	TETB_UNFLINTN	TETB Underflow condition interrupt
9	EMU_DTDMA	Emulation interrupt for host scan, DTDMA transfer complete and AET
10	MSMC_MPF_ERRORN	Memory protection fault indicators for system master PrivID = 0 (C66x CorePac)
11	EMU_RTDXRX	Reserved
12	EMU_RTDXTX	Reserved
13	IDMA0	IDMA channel 0 interrupt
14	IDMA1	IDMA channel 1 interrupt
15	SEM_ERRN	Semaphore error interrupt
16	SEM_INTN	Semaphore interrupt
17	PCIE_INT4_PLUS_N	PCIE0 MSI interrupt
18	RAC_2_INT	RAC interrupt
19	RAC_0_INT	RAC interrupt
20	SRIO_INTDST16_PLUS_N	SRIO interrupt
21	RAC_3_INT	RAC interrupt
22	RAC_1_INT	RAC interrupt
23	CIC_OUT35	C66x CorePac Interrupt Controller output
24	CIC_2_OUT102	C66x CorePac Interrupt Controller output
25	CIC_2_OUT94_PLUS_N	C66x CorePac Interrupt Controller output
26	CIC_OUT68_PLUS_10_MUL_N	C66x CorePac Interrupt Controller output
27	CIC_OUT69_PLUS_10_MUL_N	C66x CorePac Interrupt Controller output
28	CIC_OUT70_PLUS_10_MUL_N	C66x CorePac Interrupt Controller output
29	CIC_OUT71_PLUS_10_MUL_N	C66x CorePac Interrupt Controller output
30	CIC_OUT72_PLUS_10_MUL_N	C66x CorePac Interrupt Controller output
31	CIC_OUT73_PLUS_10_MUL_N	C66x CorePac Interrupt Controller output
32	CIC_OUT16	C66x CorePac Interrupt Controller output
33	CIC_OUT17	C66x CorePac Interrupt Controller output
34	CIC_OUT18	C66x CorePac Interrupt Controller output
35	CIC_OUT19	C66x CorePac Interrupt Controller output
36	CIC_OUT20	C66x CorePac Interrupt Controller output
37	CIC_OUT21	C66x CorePac Interrupt Controller output
38	CIC_OUT22	C66x CorePac Interrupt Controller output
39	CIC_OUT23	C66x CorePac Interrupt Controller output
40	CIC_OUT32	C66x CorePac Interrupt Controller output
41	CIC_OUT33	C66x CorePac Interrupt Controller output
42	CIC_OUT13_PLUS_16_MUL_N	C66x CorePac Interrupt Controller output

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Table 4-22 System Event Mapping — C66x CorePac Primary Interrupts (Part 2 of 3)

Event No.	Event Name	Description
43	CIC_OUT14_PLUS_16_MUL_N	C66x CorePac Interrupt Controller output
44	CIC_OUT15_PLUS_16_MUL_N	C66x CorePac Interrupt Controller output
45	CIC_OUT64_PLUS_10_MUL_N	C66x CorePac Interrupt Controller output
46	CIC_OUT65_PLUS_10_MUL_N	C66x CorePac Interrupt Controller output
47	CIC_OUT66_PLUS_10_MUL_N	C66x CorePac Interrupt Controller output
48	QMSS_INTD_1_HIGH_N	Navigator 1 accumulated hi-priority interrupt 0
49	QMSS_INTD_1_HIGH_8_PLUS_N	Navigator 1 accumulated hi-priority interrupt 8
50	QMSS_INTD_1_HIGH_16_PLUS_N	Navigator 1 accumulated hi-priority interrupt 16
51	QMSS_INTD_1_HIGH_24_PLUS_N	Navigator 1 accumulated hi-priority interrupt 24
52	QMSS_INTD_2_HIGH_N	Navigator 2 accumulated hi-priority interrupt 0
53	QMSS_INTD_2_HIGH_8_PLUS_N	Navigator 2 accumulated hi-priority interrupt 8
54	QMSS_INTD_2_HIGH_16_PLUS_N	Navigator 2 accumulated hi-priority interrupt 16
55	QMSS_INTD_2_HIGH_24_PLUS_N	Navigator 2 accumulated hi-priority interrupt 24
56	CIC_OUT0	C66x CorePac Interrupt Controller output
57	CIC_OUT1	C66x CorePac Interrupt Controller output
58	CIC_OUT2	C66x CorePac Interrupt Controller output
59	CIC_OUT3	C66x CorePac Interrupt Controller output
60	CIC_OUT4	C66x CorePac Interrupt Controller output
61	CIC_OUT5	C66x CorePac Interrupt Controller output
62	CIC_OUT6	C66x CorePac Interrupt Controller output
63	CIC_OUT7	C66x CorePac Interrupt Controller output
64	TIMER_N_INTL	Local timer interrupt low
65	TIMER_N_INTH	Local timer interrupt high
66	TIMER_8_INTL	Timer interrupt low
67	TIMER_8_INTH	Timer interrupt high
68	TIMER_9_INTL	Timer interrupt low
69	TIMER_9_INTH	Timer interrupt high
70	TIMER_10_INTL	Timer interrupt low
71	TIMER_10_INTH	Timer interrupt high
72	TIMER_11_INTL	Timer interrupt low
73	TIMER_11_INTH	Timer interrupt high
74	CIC_OUT8_PLUS_16_MUL_N	C66x CorePac Interrupt Controller output
75	CIC_OUT9_PLUS_16_MUL_N	C66x CorePac Interrupt Controller output
76	CIC_OUT10_PLUS_16_MUL_N	C66x CorePac Interrupt Controller output
77	CIC_OUT11_PLUS_16_MUL_N	C66x CorePac Interrupt Controller output
78	TIMER_14_INTL	Timer interrupt low
79	TIMER_14_INTH	Timer interrupt high
80	TIMER_15_INTL	Timer interrupt low
81	TIMER_15_INTH	Timer interrupt high
82	GPIO_INT8	Local GPIO interrupt
83	GPIO_INT9	Local GPIO interrupt
84	GPIO_INT10	Local GPIO interrupt
85	GPIO_INT11	Local GPIO interrupt
86	GPIO_INT12	Local GPIO interrupt

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Table 4-22 System Event Mapping — C66x CorePac Primary Interrupts (Part 3 of 3)

Event No.	Event Name	Description
87	AIF_ATEVT0	AIF Timer event
88	AIF_ATEVT1	AIF Timer event
89	AIF_ATEVT2	AIF Timer event
90	AIF_ATEVT3	AIF Timer event
91	AIF_ATEVT4	AIF Timer event
92	AIF_ATEVT5	AIF Timer event
93	AIF_ATEVT6	AIF Timer event
94	AIF_ATEVT7	AIF Timer event
95	CIC_OUT67_PLUS_10_MUL_N	C66x CorePac Interrupt Controller output
96	INTERR	Dropped C66x CorePac interrupt event
97	EMC_IDMAERR	Invalid IDMA parameters
98	Reserved	Reserved
99	CIC_2_SPECIAL_BROADCAST	C66x CorePac Interrupt Controller output
100	EFIINT0	EFI interrupt from Side A
101	EFIINT1	EFI interrupt from Side B
102	GPIO_INT13	Local GPIO interrupt
103	GPIO_INT14	Local GPIO interrupt
104	GPIO_INT15	Local GPIO interrupt
105	IPC_GRN	Boot CFG
106	GPIO_INTN	GPIO interrupt
107	CIC_OUT12_PLUS_16_MUL_N	C66x CorePac Interrupt Controller output
108	CIC_OUT34	C66x CorePac Interrupt Controller output
109	CIC_2_OUT13	C66x CorePac Interrupt Controller output
110	MDMAERREVT	VbusM error event
111	Reserved	Reserved
112	EDMACC_0_4_TC_AET_INT	EDMA3CC0_4 AET event
113	PMC_ED	Single bit error detected during DMA read
114	EDMACC_1_2_TC_AET_INT	EDMA3CC1_2 AET event
115	EDMACC_1_3_TC_AET_INT	EDMA3CC3_4 AET event
116	UMC_ED1	Corrected bit error detected
117	UMC_ED2	Uncorrected bit error detected
118	PDC_INT	Power down sleep interrupt
119	SYS_CMPA	SYS CPU MP fault event
120	PMC_CMPA	CPU memory protection fault
121	PMC_DMPA	DMA memory protection fault
122	DMC_CMPA	CPU memory protection fault
123	DMC_DMPA	DMA memory protection fault
124	UMC_CMPA	CPU memory protection fault
125	UMC_DMPA	DMA memory protection fault
126	EMC_CMPA	CPU memory protection fault
127	EMC_BUSERR	Bus error interrupt
End of Table 4-22		

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Table 4-23, Table 4-24, and Table 4-25 list the CIC0, CIC1, and CIC2 event inputs.

Table 4-23 CIC0 Event Inputs — C66x CorePac Secondary Interrupts (Part 1 of 11)

Event No.	Event Name	Description
0	EDMACC_1_ERRINT	EDMA3CC1 error interrupt
1	EDMACC_1_MPINT	EDMA3CC1 memory protection interrupt
2	EDMACC_1_TC_0_ERRINT	EDMA3CC1 TPTC0 error interrupt
3	EDMACC_1_TC_1_ERRINT	EDMA3CC1 TPTC1 error interrupt
4	EDMACC_1_TC_2_ERRINT	EDMA3CC1 TPTC2 error interrupt
5	EDMACC_1_TC_3_ERRINT	EDMA3CC1 TPTC3 error interrupt
6	EDMACC_1_GINT	EDMA3CC1 GINT
7	Reserved	Reserved
8	EDMACC_1_TC_0_INT	EDMA3CC1 individual completion interrupt
9	EDMACC_1_TC_1_INT	EDMA3CC1 individual completion interrupt
10	EDMACC_1_TC_2_INT	EDMA3CC1 individual completion interrupt
11	EDMACC_1_TC_3_INT	EDMA3CC1 individual completion interrupt
12	EDMACC_1_TC_4_INT	EDMA3CC1 individual completion interrupt
13	EDMACC_1_TC_5_INT	EDMA3CC1 individual completion interrupt
14	EDMACC_1_TC_6_INT	EDMA3CC1 individual completion interrupt
15	EDMACC_1_TC_7_INT	EDMA3CC1 individual completion interrupt
16	EDMACC_2_ERRINT	EDMA3CC2 error interrupt
17	EDMACC_2_MPINT	EDMA3CC2 memory protection interrupt
18	EDMACC_2_TC_0_ERRINT	EDMA3CC2 TPTC0 error interrupt
19	EDMACC_2_TC_1_ERRINT	EDMA3CC2 TPTC1 error interrupt
20	EDMACC_2_TC_2_ERRINT	EDMA3CC2 TPTC2 error interrupt
21	EDMACC_2_TC_3_ERRINT	EDMA3CC2 TPTC3 error interrupt
22	EDMACC_2_GINT	EDMA3CC2 GINT
23	Reserved	Reserved
24	EDMACC_2_TC_0_INT	EDMA3CC2 individual completion interrupt
25	EDMACC_2_TC_1_INT	EDMA3CC2 individual completion interrupt
26	EDMACC_2_TC_2_INT	EDMA3CC2 individual completion interrupt
27	EDMACC_2_TC_3_INT	EDMA3CC2 individual completion interrupt
28	EDMACC_2_TC_4_INT	EDMA3CC2 individual completion interrupt
29	EDMACC_2_TC_5_INT	EDMA3CC2 individual completion interrupt
30	EDMACC_2_TC_6_INT	EDMA3CC2 individual completion interrupt
31	EDMACC_2_TC_7_INT	EDMA3CC2 individual completion interrupt
32	EDMACC_0_ERRINT	EDMA3CC0 error interrupt
33	EDMACC_0_MPINT	EDMA3CC0 memory protection interrupt
34	EDMACC_0_TC_0_ERRINT	EDMA3CC0 TPTC0 error interrupt
35	EDMACC_0_TC_1_ERRINT	EDMA3CC0 TPTC1 error interrupt
36	EDMACC_0_GINT	EDMA3CC0 global completion interrupt
37	Reserved	Reserved
38	EDMACC_0_TC_0_INT	EDMA3CC0 individual completion interrupt
39	EDMACC_0_TC_1_INT	EDMA3CC0 individual completion interrupt
40	EDMACC_0_TC_2_INT	EDMA3CC0 individual completion interrupt
41	EDMACC_0_TC_3_INT	EDMA3CC0 individual completion interrupt
42	EDMACC_0_TC_4_INT	EDMA3CC0 individual completion interrupt

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Table 4-23 CIC0 Event Inputs — C66x CorePac Secondary Interrupts (Part 2 of 11)

Event No.	Event Name	Description
43	EDMACC_0_TC_5_INT	EDMA3CC0 individual completion interrupt
44	EDMACC_0_TC_6_INT	EDMA3CC0 individual completion interrupt
45	EDMACC_0_TC_7_INT	EDMA3CC0 individual completion interrupt
46	Reserved	Reserved
47	QMSS_QUE_PEND_652	Navigator transmit queue pending event for indicated queue
48	PCIE_INT12	PCIE protocol error interrupt
49	PCIE_INT13	PCIE power management interrupt
50	PCIE_INT0	PCIE legacy INTA interrupt
51	PCIE_INT1	PCIE legacy INTB interrupt
52	PCIE_INT2	PCIE legacy INTC interrupt
53	PCIE_INT3	PCIE legacy INTD interrupt
54	SPI_0_INT0	SPI0 interrupt0
55	SPI_0_INT1	SPI0 interrupt1
56	SPI_0_XEVT	SPI0 transmit event
57	SPI_0_REVT	SPI0 receive event
58	I2C_0_INT	I2C0 interrupt
59	I2C_0_REVT	I2C0 receive event
60	I2C_0_XEVT	I2C0 transmit event
61	Reserved	Reserved
62	Reserved	Reserved
63	DBGTBR_DMAINT	Debug trace buffer (TBR) DMA event
64	MPU_12_INT	MPU12 addressing violation interrupt and protection violation interrupt
65	DBGTBR_ACQCOMP	Debug trace buffer (TBR) acquisition has been completed
66	MPU_13_INT	MPU13 addressing violation interrupt and protection violation interrupt
67	MPU_14_INT	MPU14 addressing violation interrupt and protection violation interrupt
68	NETCP_MDIO_LINK_INT0	Packet Accelerator 0 subsystem MDIO interrupt
69	NETCP_MDIO_LINK_INT1	Packet Accelerator 0 subsystem MDIO interrupt
70	NETCP_MDIO_USER_INT0	Packet Accelerator 0 subsystem MDIO interrupt
71	NETCP_MDIO_USER_INT1	Packet Accelerator 0 subsystem MDIO interrupt
72	NETCP_MISC_INT	Packet Accelerator 0 subsystem misc interrupt
73	TRACER_CORE_0_INT	Tracer sliding time window interrupt for DSP0 L2
74	TRACER_CORE_1_INT	Tracer sliding time window interrupt for DSP1 L2
75	TRACER_CORE_2_INT	Tracer sliding time window interrupt for DSP2 L2
76	TRACER_CORE_3_INT	Tracer sliding time window interrupt for DSP3 L2
77	TRACER_DDR_INT	Tracer sliding time window interrupt for MSMC-DDR3A
78	TRACER_MSMC_0_INT	Tracer sliding time window interrupt for MSMC SRAM bank0
79	TRACER_MSMC_1_INT	Tracer sliding time window interrupt for MSMC SRAM bank1
80	TRACER_MSMC_2_INT	Tracer sliding time window interrupt for MSMC SRAM bank2
81	TRACER_MSMC_3_INT	Tracer sliding time window interrupt for MSMC SRAM bank3
82	TRACER_CFG_INT	Tracer sliding time window interrupt for CFG0 TeraNet
83	TRACER_QMSS_QM_CFG1_INT	Tracer sliding time window interrupt for Navigator CFG1 slave port
84	TRACER_QMSS_DMA_INT	Tracer sliding time window interrupt for Navigator VBUSM slave port
85	TRACER_SEM_INT	Tracer sliding time window interrupt for Semaphore
86	PSC_ALLINT	Power & Sleep Controller interrupt

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Table 4-23 CIC0 Event Inputs — C66x CorePac Secondary Interrupts (Part 3 of 11)

Event No.	Event Name	Description
87	MSMC_SCRUB_CERROR	Correctable (1-bit) soft error detected during scrub cycle
88	BOOTCFG_INT	Chip-level MMR Error Register
89	SR_0_PO_VCON_SMPSERR_INT	SmartReflex SMPS error interrupt
90	MPU_0_INT	MPU0 addressing violation interrupt and protection violation interrupt
91	QMSS_QUE_PEND_653	Navigator transmit queue pending event for indicated queue
92	MPU_1_INT	MPU1 addressing violation interrupt and protection violation interrupt.
93	QMSS_QUE_PEND_654	Navigator transmit queue pending event for indicated queue
94	MPU_2_INT	MPU2 addressing violation interrupt and protection violation interrupt.
95	QMSS_QUE_PEND_655	Navigator transmit queue pending event for indicated queue
96	MPU_3_INT	MPU3 addressing violation interrupt and protection violation interrupt.
97	QMSS_QUE_PEND_656	Navigator transmit queue pending event for indicated queue
98	MSMC_DEDC_CERROR	Correctable (1-bit) soft error detected on SRAM read
99	MSMC_DEDC_NC_ERROR	Non-correctable (2-bit) soft error detected on SRAM read
100	MSMC_SCRUB_NC_ERROR	Non-correctable (2-bit) soft error detected during scrub cycle
101	MSMC_MPF_ERROR0	Memory protection fault indicators for system master PrivID = 0
102	MSMC_MPF_ERROR8	Memory protection fault indicators for system master PrivID = 8
103	MSMC_MPF_ERROR9	Memory protection fault indicators for system master PrivID = 9
104	MSMC_MPF_ERROR10	Memory protection fault indicators for system master PrivID = 10
105	MSMC_MPF_ERROR11	Memory protection fault indicators for system master PrivID = 11
106	MSMC_MPF_ERROR12	Memory protection fault indicators for system master PrivID = 12
107	MSMC_MPF_ERROR13	Memory protection fault indicators for system master PrivID = 13
108	MSMC_MPF_ERROR14	Memory protection fault indicators for system master PrivID = 14
109	MSMC_MPF_ERROR15	Memory protection fault indicators for system master PrivID = 15
110	DDR3_0_ERR	DDR3A_EMIF error interrupt
111	HYPERLINK_0_INT	HyperLink 0 interrupt
112	SRIO_INTDST0	SRIO interrupt
113	SRIO_INTDST1	SRIO interrupt
114	SRIO_INTDST2	SRIO interrupt
115	SRIO_INTDST3	SRIO interrupt
116	SRIO_INTDST4	SRIO interrupt
117	SRIO_INTDST5	SRIO interrupt
118	SRIO_INTDST6	SRIO interrupt
119	SRIO_INTDST7	SRIO interrupt
120	SRIO_INTDST8	SRIO interrupt
121	SRIO_INTDST9	SRIO interrupt
122	SRIO_INTDST10	SRIO interrupt
123	SRIO_INTDST11	SRIO interrupt
124	SRIO_INTDST12	SRIO interrupt
125	SRIO_INTDST13	SRIO interrupt
126	SRIO_INTDST14	SRIO interrupt
127	SRIO_INTDST15	SRIO interrupt
128	AEMIF_EASYNCERR	Asynchronous EMIF16 error interrupt
129	TRACER_CORE_4_INT	Tracer sliding time window interrupt for DSP4 L2
130	TRACER_CORE_5_INT	Tracer sliding time window interrupt for DSP5 L2

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Table 4-23 CIC0 Event Inputs — C66x CorePac Secondary Interrupts (Part 4 of 11)

Event No.	Event Name	Description
131	TRACER_CORE_6_INT	Tracer sliding time window interrupt for DSP6 L2
132	TRACER_CORE_7_INT	Tracer sliding time window interrupt for DSP7 L2
133	QMSS_INTD_1_PKTDMA_0	Navigator interrupt for Packet DMA starvation
134	QMSS_INTD_1_PKTDMA_1	Navigator interrupt for Packet DMA starvation
135	SRIO_INT_PKTDMA_0	IPC interrupt generation
136	NETCP_PKTDMA_INT0	Packet Accelerator0 Packet DMA starvation interrupt
137	SR_0_SMARTREFLEX_INTREQ0	SmartReflex controller interrupt
138	SR_0_SMARTREFLEX_INTREQ1	SmartReflex controller interrupt
139	SR_0_SMARTREFLEX_INTREQ2	SmartReflex controller interrupt
140	SR_0_SMARTREFLEX_INTREQ3	SmartReflex controller interrupt
141	SR_0_VPNOSMPSACK	SmartReflex VPVOLTUPDATE has been asserted but SMPS has not been responded to in a defined time interval
142	SR_0_VPEQVALUE	SmartReflex SRSINTERUPT is asserted, but the new voltage is not different from the current SMPS voltage
143	SR_0_VPMAXVDD	SmartReflex. The new voltage required is equal to or greater than MaxVdd
144	SR_0_VPMINVDD	SmartReflex. The new voltage required is equal to or less than MinVdd
145	SR_0_VPINIDLE	SmartReflex indicating that the FSM of voltage processor is in idle
146	SR_0_VPOPPCHANGEDONE	SmartReflex indicating that the average frequency error is within the desired limit
147	Reserved	Reserved
148	UART_0_UARTINT	UART0 interrupt
149	UART_0_URXEVT	UART0 receive event
150	UART_0_UTXEVT	UART0 transmit event
151	QMSS_QUE_PEND_657	Navigator transmit queue pending event for indicated queue
152	QMSS_QUE_PEND_658	Navigator transmit queue pending event for indicated queue
153	QMSS_QUE_PEND_659	Navigator transmit queue pending event for indicated queue
154	QMSS_QUE_PEND_660	Navigator transmit queue pending event for indicated queue
155	QMSS_QUE_PEND_661	Navigator transmit queue pending event for indicated queue
156	QMSS_QUE_PEND_662	Navigator transmit queue pending event for indicated queue
157	QMSS_QUE_PEND_663	Navigator transmit queue pending event for indicated queue
158	QMSS_QUE_PEND_664	Navigator transmit queue pending event for indicated queue
159	QMSS_QUE_PEND_665	Navigator transmit queue pending event for indicated queue
160	SR_0_VPSMPSACK	SmartReflex VPVOLTUPDATE asserted and SMPS has acknowledged in a defined time interval
161	Reserved	Reserved
162	Reserved	Reserved
163	Reserved	Reserved
164	Reserved	Reserved
165	SR_0_SR_TEMPSENSOR	SmartReflex temperature threshold crossing interrupt
166	SR_0_SR_TIMERINT	SmartReflex internal timer expiration interrupt
167	AIF_ATEVT8	AIF timer event
168	AIF_ATEVT9	AIF timer event
169	AIF_ATEVT10	AIF timer event
170	AIF_ATEVT11	AIF timer event
171	AIF_ATEVT12	AIF timer event
172	AIF_ATEVT13	AIF timer event
173	AIF_ATEVT14	AIF timer event

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Table 4-23 CIC0 Event Inputs — C66x CorePac Secondary Interrupts (Part 5 of 11)

Event No.	Event Name	Description
174	AIF_ATEVT15	AIF timer event
175	TIMER_7_INTL	Timer interrupt low
176	TIMER_7_INTH	Timer interrupt high
177	TIMER_6_INTL	Timer interrupt low
178	TIMER_6_INTH	Timer interrupt high
179	TIMER_5_INTL	Timer interrupt low
180	TIMER_5_INTH	Timer interrupt high
181	TIMER_4_INTL	Timer interrupt low
182	TIMER_4_INTH	Timer interrupt high
183	TIMER_3_INTL	Timer interrupt low
184	TIMER_3_INTH	Timer interrupt high
185	TIMER_2_INTL	Timer interrupt low
186	TIMER_2_INTH	Timer interrupt high
187	TIMER_1_INTL	Timer interrupt low
188	TIMER_1_INTH	Timer interrupt high
189	TIMER_0_INTL	Timer interrupt low
190	TIMER_0_INTH	Timer interrupt high
191	TCP3D_0_INT	TCP3d interrupt
192	TCP3D_1_INT	TCP3d interrupt
193	TCP3D_2_INT	TCP3d interrupt
194	TCP3D_3_INT	TCP3d interrupt
195	TCP3D_0_REVT0	TCP3d event
196	TCP3D_0_REVT1	TCP3d event
197	TCP3D_1_REVT0	TCP3d event
198	TCP3D_1_REVT1	TCP3d event
199	TCP3D_2_REVT0	TCP3d event
200	TCP3D_2_REVT1	TCP3d event
201	TCP3D_3_REVT0	TCP3d event
202	TCP3D_3_REVT1	TCP3d event
203	TAC_INT	TAC interrupt
204	TAC_DEVT0	TAC debug event
205	TAC_DEVT1	TAC debug event
206	AIF_INT	AIF interrupt
207	EDMACC_4_ERRINT	EDMA3CC4 error interrupt
208	EDMACC_4_MPINT	EDMA3CC4 memory protection interrupt
209	EDMACC_4_TC_0_ERRINT	EDMA3CC4 TPTC0 error interrupt
210	EDMACC_4_TC_1_ERRINT	EDMA3CC4 TPTC1 error interrupt
211	EDMACC_4_GINT	EDMA3CC4 GINT
212	EDMACC_4_TC_0_INT	EDMA3CC4 individual completion interrupt
213	EDMACC_4_TC_1_INT	EDMA3CC4 individual completion interrupt
214	EDMACC_4_TC_2_INT	EDMA3CC4 individual completion interrupt
215	EDMACC_4_TC_3_INT	EDMA3CC4 individual completion interrupt
216	EDMACC_4_TC_4_INT	EDMA3CC4 individual completion interrupt
217	EDMACC_4_TC_5_INT	EDMA3CC4 individual completion interrupt

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Table 4-23 CIC0 Event Inputs — C66x CorePac Secondary Interrupts (Part 6 of 11)

Event No.	Event Name	Description
218	EDMACC_4_TC_6_INT	EDMA3CC4 individual completion interrupt
219	EDMACC_4_TC_7_INT	EDMA3CC4 individual completion interrupt
220	EDMACC_3_ERRINT	EDMA3CC3 error interrupt
221	EDMACC_3_MPINT	EDMA3CC3 memory protection interrupt
222	EDMACC_3_TC_0_ERRINT	EDMA3CC3 TPTC0 error interrupt
223	EDMACC_3_TC_1_ERRINT	EDMA3CC3 TPTC1 error interrupt
224	EDMACC_3_GINT	EDMA3CC3 GINT
225	EDMACC_3_TC_0_INT	EDMA3CC3 individual completion interrupt
226	EDMACC_3_TC_1_INT	EDMA3CC3 individual completion interrupt
227	EDMACC_3_TC_2_INT	EDMA3CC3 individual completion interrupt
228	EDMACC_3_TC_3_INT	EDMA3CC3 individual completion interrupt
229	EDMACC_3_TC_4_INT	EDMA3CC3 individual completion interrupt
230	EDMACC_3_TC_5_INT	EDMA3CC3 individual completion interrupt
231	EDMACC_3_TC_6_INT	EDMA3CC3 individual completion interrupt
232	EDMACC_3_TC_7_INT	EDMA3CC3 individual completion interrupt
233	UART_1_UARTINT	UART1 interrupt
234	UART_1_URXEVT	UART1 receive event
235	UART_1_UTXEVT	UART1 transmit event
236	I2C_1_INT	I2C1 interrupt
237	I2C_1_REVT	I2C1 receive event
238	I2C_1_XEVT	I2C1 transmit event
239	SPI_1_INT0	SPI1 interrupt0
240	SPI_1_INT1	SPI1 interrupt1
241	SPI_1_XEVT	SPI1 transmit event
242	SPI_1_REVT	SPI1 receive event
243	MPU_5_INT	MPU5 addressing violation interrupt and protection violation interrupt
244	MPU_8_INT	MPU8 addressing violation interrupt and protection violation interrupt
245	MPU_9_INT	MPU9 addressing violation interrupt and protection violation interrupt
246	MPU_11_INT	MPU11 addressing violation interrupt and protection violation interrupt
247	MPU_4_INT	MPU4 addressing violation interrupt and protection violation interrupt
248	MPU_6_INT	MPU6 addressing violation interrupt and protection violation interrupt
249	MPU_7_INT	MPU7 addressing violation interrupt and protection violation interrupt
250	MPU_10_INT	MPU10 addressing violation interrupt and protection violation interrupt
251	SPI_2_INT0	SPI2 interrupt0
252	SPI_2_INT1	SPI2 interrupt1
253	SPI_2_XEVT	SPI2 transmit event
254	SPI_2_REVT	SPI2 receive event
255	I2C_2_INT	I2C2 interrupt
256	I2C_2_REVT	I2C2 receive event
257	I2C_2_XEVT	I2C2 transmit event
258	10GbE_LINK_INT0	10 Gigabit Ethernet subsystem MDIO interrupt
259	10GbE_LINK_INT1	10 Gigabit Ethernet subsystem MDIO interrupt
260	10GbE_USER_INT0	10 Gigabit Ethernet subsystem MDIO interrupt
261	10GbE_USER_INT1	10 Gigabit Ethernet subsystem MDIO interrupt

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Table 4-23 CIC0 Event Inputs — C66x CorePac Secondary Interrupts (Part 7 of 11)

Event No.	Event Name	Description
262	10GbE_MISC_INT	10 Gigabit Ethernet subsystem MDIO interrupt
263	10GbE_INT_PKTDMA_0	10 Gigabit Ethernet Packet DMA starvation interrupt
264	Reserved	Reserved
265	Reserved	Reserved
266	Reserved	Reserved
267	BCP_INT0	BCP interrupt
268	BCP_INT1	BCP interrupt
269	BCP_INT2	BCP interrupt
270	BCP_INT3	BCP interrupt
271	RAC_0_TRACE_GCCP0	RAC trace
272	RAC_0_TRACE_GCCP1	RAC trace
273	RAC_1_TRACE_GCCP0	RAC trace
274	RAC_1_TRACE_GCCP1	RAC trace
275	RAC_2_TRACE_GCCP0	RAC trace
276	RAC_2_TRACE_GCCP1	RAC trace
277	RAC_3_TRACE_GCCP0	RAC trace
278	RAC_3_TRACE_GCCP1	RAC trace
279	TAC_DEVT2	TAC debug
280	TAC_DEVT3	TAC debug
281	TAC_DEVT4	TAC debug
282	TAC_DEVT5	TAC debug
283	Reserved	Reserved
284	Reserved	Reserved
285	Reserved	Reserved
286	Reserved	Reserved
287	Reserved	Reserved
288	Reserved	Reserved
289	Reserved	Reserved
290	TRACER_RAC_1_INT	Tracer RAC interrupt
291	TRACER_RAC_FE_INT	Tracer RAC interrupt
292	QMSS_QUE_PEND_666	Navigator transmit queue pending event for indicated queue
293	QMSS_QUE_PEND_667	Navigator transmit queue pending event for indicated queue
294	QMSS_QUE_PEND_668	Navigator transmit queue pending event for indicated queue
295	QMSS_QUE_PEND_669	Navigator transmit queue pending event for indicated queue
296	QMSS_QUE_PEND_670	Navigator transmit queue pending event for indicated queue
297	QMSS_QUE_PEND_671	Navigator transmit queue pending event for indicated queue
298	QMSS_QUE_PEND_8844	Navigator transmit queue pending event for indicated queue
299	QMSS_QUE_PEND_8845	Navigator transmit queue pending event for indicated queue
300	QMSS_QUE_PEND_8846	Navigator transmit queue pending event for indicated queue
301	QMSS_QUE_PEND_8847	Navigator transmit queue pending event for indicated queue
302	QMSS_QUE_PEND_8848	Navigator transmit queue pending event for indicated queue
303	QMSS_QUE_PEND_8849	Navigator transmit queue pending event for indicated queue
304	QMSS_QUE_PEND_8850	Navigator transmit queue pending event for indicated queue
305	QMSS_QUE_PEND_8851	Navigator transmit queue pending event for indicated queue

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Table 4-23 CIC0 Event Inputs — C66x CorePac Secondary Interrupts (Part 8 of 11)

Event No.	Event Name	Description
306	QMSS_QUE_PEND_8852	Navigator transmit queue pending event for indicated queue
307	QMSS_QUE_PEND_8853	Navigator transmit queue pending event for indicated queue
308	QMSS_QUE_PEND_8854	Navigator transmit queue pending event for indicated queue
309	QMSS_QUE_PEND_8855	Navigator transmit queue pending event for indicated queue
310	QMSS_QUE_PEND_8856	Navigator transmit queue pending event for indicated queue
311	QMSS_QUE_PEND_8857	Navigator transmit queue pending event for indicated queue
312	QMSS_QUE_PEND_8858	Navigator transmit queue pending event for indicated queue
313	QMSS_QUE_PEND_8859	Navigator transmit queue pending event for indicated queue
314	QMSS_QUE_PEND_8860	Navigator transmit queue pending event for indicated queue
315	QMSS_QUE_PEND_8861	Navigator transmit queue pending event for indicated queue
316	QMSS_QUE_PEND_8862	Navigator transmit queue pending event for indicated queue
317	QMSS_QUE_PEND_8863	Navigator transmit queue pending event for indicated queue
318	QMSS_INTD_2_PKTDMA_0	Navigator ECC error interrupt
319	QMSS_INTD_2_PKTDMA_1	Navigator ECC error interrupt
320	QMSS_INTD_1_LOW_0	Navigator interrupt low
321	QMSS_INTD_1_LOW_1	Navigator interrupt low
322	QMSS_INTD_1_LOW_2	Navigator interrupt low
323	QMSS_INTD_1_LOW_3	Navigator interrupt low
324	QMSS_INTD_1_LOW_4	Navigator interrupt low
325	QMSS_INTD_1_LOW_5	Navigator interrupt low
326	QMSS_INTD_1_LOW_6	Navigator interrupt low
327	QMSS_INTD_1_LOW_7	Navigator interrupt low
328	QMSS_INTD_1_LOW_8	Navigator interrupt low
329	QMSS_INTD_1_LOW_9	Navigator interrupt low
330	QMSS_INTD_1_LOW_10	Navigator interrupt low
331	QMSS_INTD_1_LOW_11	Navigator interrupt low
332	QMSS_INTD_1_LOW_12	Navigator interrupt low
333	QMSS_INTD_1_LOW_13	Navigator interrupt low
334	QMSS_INTD_1_LOW_14	Navigator interrupt low
335	QMSS_INTD_1_LOW_15	Navigator interrupt low
336	QMSS_INTD_2_LOW_0	Navigator second interrupt low
337	QMSS_INTD_2_LOW_1	Navigator second interrupt low
338	QMSS_INTD_2_LOW_2	Navigator second interrupt low
339	QMSS_INTD_2_LOW_3	Navigator second interrupt low
340	QMSS_INTD_2_LOW_4	Navigator second interrupt low
341	QMSS_INTD_2_LOW_5	Navigator second interrupt low
342	QMSS_INTD_2_LOW_6	Navigator second interrupt low
343	QMSS_INTD_2_LOW_7	Navigator second interrupt low
344	QMSS_INTD_2_LOW_8	Navigator second interrupt low
345	QMSS_INTD_2_LOW_9	Navigator second interrupt low
346	QMSS_INTD_2_LOW_10	Navigator second interrupt low
347	QMSS_INTD_2_LOW_11	Navigator second interrupt low
348	QMSS_INTD_2_LOW_12	Navigator second interrupt low
349	QMSS_INTD_2_LOW_13	Navigator second interrupt low

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Table 4-23 CIC0 Event Inputs — C66x CorePac Secondary Interrupts (Part 9 of 11)

Event No.	Event Name	Description
350	QMSS_INTD_2_LOW_14	Navigator second interrupt low
351	QMSS_INTD_2_LOW_15	Navigator second interrupt low
352	TRACER_EDMACC_0	Tracer sliding time window interrupt for EDMA3CC0
353	TRACER_EDMACC_123_INT	Tracer sliding time window interrupt for EDMA3CC1, EDMA3CC2 and EDMA3CC3
354	TRACER_CIC_INT	Tracer sliding time window interrupt for interrupt controllers (CIC)
355	TRACER_MSMC_4_INT	Tracer sliding time window interrupt for MSMC SRAM bank4
356	TRACER_MSMC_5_INT	Tracer sliding time window interrupt for MSMC SRAM bank5
357	TRACER_MSMC_6_INT	Tracer sliding time window interrupt for MSMC SRAM bank6
358	TRACER_MSMC_7_INT	Tracer sliding time window interrupt for MSMC SRAM bank7
359	TRACER_SPI_ROM_EMIF_INT	Tracer sliding time window interrupt for SPI/ROM/EMIF16 modules
360	TRACER_QMSS_QM_CFG2_INT	Tracer sliding time window interrupt for QM2
361	TRACER_TAC_BE_INT	Tracer TAC interrupt
362	TRACER_RAC_2_INT	Tracer RAC interrupt
363	TRACER_DDR_1_INT	Tracer sliding time window interrupt for DDR3B
364	TRACER_BCR_INT	Tracer sliding time window interrupt for BCR
365	HYPERLINK_1_INT	HyperLink 1 interrupt
366	VCP_0_INT0	VCP interrupt
367	VCP_0_INT1	VCP interrupt
368	VCP_0_INT2	VCP interrupt
369	VCP_0_INT3	VCP interrupt
370	VCP_1_INT0	VCP interrupt
371	VCP_1_INT1	VCP interrupt
372	VCP_1_INT2	VCP interrupt
373	VCP_1_INT3	VCP interrupt
374	VCP_0_REVT0	VCP event
375	VCP_0_XEVT0	VCP event
376	VCP_0_REVT1	VCP event
377	VCP_0_XEVT1	VCP event
378	VCP_0_REVT2	VCP event
379	VCP_0_XEVT2	VCP event
380	VCP_0_REVT3	VCP event
381	VCP_0_XEVT3	VCP event
382	VCP_1_REVT0	VCP event
383	VCP_1_XEVT0	VCP event
384	VCP_1_REVT1	VCP event
385	VCP_1_XEVT1	VCP event
386	VCP_1_REVT2	VCP event
387	VCP_1_XEVT2	VCP event
388	VCP_1_REVT3	VCP event
389	VCP_1_XEVT3	VCP event
390	FFTC_0_INT0	FFTC interrupt
391	FFTC_0_INT1	FFTC interrupt
392	FFTC_0_INT2	FFTC interrupt
393	FFTC_0_INT3	FFTC interrupt

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Table 4-23 CIC0 Event Inputs — C66x CorePac Secondary Interrupts (Part 10 of 11)

Event No.	Event Name	Description
394	FFTC_1_INT0	FFTC interrupt
395	FFTC_1_INT1	FFTC interrupt
396	FFTC_1_INT2	FFTC interrupt
397	FFTC_1_INT3	FFTC interrupt
398	FFTC_2_INT0	FFTC interrupt
399	FFTC_2_INT1	FFTC interrupt
400	FFTC_2_INT2	FFTC interrupt
401	FFTC_2_INT3	FFTC interrupt
402	FFTC_3_INT0	FFTC interrupt
403	FFTC_3_INT1	FFTC interrupt
404	FFTC_3_INT2	FFTC interrupt
405	FFTC_3_INT3	FFTC interrupt
406	FFTC_4_INT0	FFTC interrupt
407	FFTC_4_INT1	FFTC interrupt
408	FFTC_4_INT2	FFTC interrupt
409	FFTC_4_INT3	FFTC interrupt
410	FFTC_5_INT0	FFTC interrupt
411	FFTC_5_INT1	FFTC interrupt
412	FFTC_5_INT2	FFTC interrupt
413	FFTC_5_INT3	FFTC interrupt
414	AIF_ATEVT16	AIF timer event
415	AIF_ATEVT17	AIF timer event
416	AIF_ATEVT18	AIF timer event
417	AIF_ATEVT19	AIF timer event
418	AIF_ATEVT20	AIF timer event
419	AIF_ATEVT21	AIF timer event
420	AIF_ATEVT22	AIF timer event
421	AIF_ATEVT23	AIF timer event
422	USB_INT00	USB interrupt
423	USB_INT04	USB interrupt
424	USB_INT05	USB interrupt
425	USB_INT06	USB interrupt
426	USB_INT07	USB interrupt
427	USB_INT08	USB interrupt
428	USB_INT09	USB interrupt
429	USB_INT10	USB interrupt
430	USB_INT11	USB interrupt
431	USB_MISCINT	USB miscellaneous interrupt
432	USB_OABSINT	USB OABS interrupt
433	TIMER_12_INTL	Timer interrupt low
434	TIMER_12_INTH	Timer interrupt high
435	TIMER_13_INTL	Timer interrupt low
436	TIMER_13_INTH	Timer interrupt high
437	TIMER_14_INTL	Timer interrupt low

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Table 4-23 CIC0 Event Inputs — C66x CorePac Secondary Interrupts (Part 11 of 11)

Event No.	Event Name	Description
438	TIMER_14_INTH	Timer interrupt high
439	TIMER_15_INTL	Timer interrupt low
440	TIMER_15_INTH	Timer interrupt high
441	TIMER_16_INTL	Timer interrupt low
442	TIMER_17_INTL	Timer interrupt high
443	TIMER_18_INTL	Timer interrupt low
444	TIMER_19_INTL	Timer interrupt high
445	DDR3_1_ERR	DDR3B_EMIF error interrupt
446	GPIO_INT16	GPIO interrupt
447	GPIO_INT17	GPIO interrupt
448	GPIO_INT18	GPIO interrupt
449	GPIO_INT19	GPIO interrupt
450	GPIO_INT20	GPIO interrupt
451	GPIO_INT21	GPIO interrupt
452	GPIO_INT22	GPIO interrupt
453	GPIO_INT23	GPIO interrupt
454	GPIO_INT24	GPIO interrupt
455	GPIO_INT25	GPIO interrupt
456	GPIO_INT26	GPIO interrupt
457	GPIO_INT27	GPIO interrupt
458	GPIO_INT28	GPIO interrupt
459	GPIO_INT29	GPIO interrupt
460	GPIO_INT30	GPIO interrupt
461	GPIO_INT31	GPIO interrupt
462	SRIO_INTDST16	SRIOI interrupt
463	SRIO_INTDST17	SRIOI interrupt
464	SRIO_INTDST18	SRIOI interrupt
465	SRIO_INTDST19	SRIOI interrupt
466	PCIE_INT4	PCIE MSI interrupt
467	PCIE_INT5	PCIE MSI interrupt
468	PCIE_INT6	PCIE MSI interrupt
469	PCIE_INT7	PCIE MSI interrupt
470	SEM_INT12	Semaphore interrupt
471	SEM_INT13	Semaphore interrupt
472	SEM_ERR12	Semaphore error interrupt
473	SEM_ERR13	Semaphore error interrupt
End of Table 4-23		

Table 4-24 CIC1 Event Inputs — C66x CorePac Secondary Interrupts (Part 1 of 12)

Event No.	Event Name	Description
0	EDMACC_1_ERRINT	EDMA3CC1 error interrupt
1	EDMACC_1_MPINT	EDMA3CC1 memory protection interrupt
2	EDMACC_1_TC_0_ERRINT	EDMA3CC1 TPTC0 error interrupt

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Table 4-24 CIC1 Event Inputs — C66x CorePac Secondary Interrupts (Part 2 of 12)

Event No.	Event Name	Description
3	EDMACC_1_TC_1_ERRINT	EDMA3CC1 TPTC1 error interrupt
4	EDMACC_1_TC_2_ERRINT	EDMA3CC1 TPTC2 error interrupt
5	EDMACC_1_TC_3_ERRINT	EDMA3CC1 TPTC3 error interrupt
6	EDMACC_1_GINT	EDMA3CC1 GINT
7	Reserved	Reserved
8	EDMACC_1_TC_0_INT	EDMA3CC1 individual completion interrupt
9	EDMACC_1_TC_1_INT	EDMA3CC1 individual completion interrupt
10	EDMACC_1_TC_2_INT	EDMA3CC1 individual completion interrupt
11	EDMACC_1_TC_3_INT	EDMA3CC1 individual completion interrupt
12	EDMACC_1_TC_4_INT	EDMA3CC1 individual completion interrupt
13	EDMACC_1_TC_5_INT	EDMA3CC1 individual completion interrupt
14	EDMACC_1_TC_6_INT	EDMA3CC1 individual completion interrupt
15	EDMACC_1_TC_7_INT	EDMA3CC1 individual completion interrupt
16	EDMACC_2_ERRINT	EDMA3CC2 error interrupt
17	EDMACC_2_MPINT	EDMA3CC2 memory protection interrupt
18	EDMACC_2_TC_0_ERRINT	EDMA3CC2 TPTC0 error interrupt
19	EDMACC_2_TC_1_ERRINT	EDMA3CC2 TPTC1 error interrupt
20	EDMACC_2_TC_2_ERRINT	EDMA3CC2 TPTC2 error interrupt
21	EDMACC_2_TC_3_ERRINT	EDMA3CC2 TPTC3 error interrupt
22	EDMACC_2_GINT	EDMA3CC2 GINT
23	Reserved	Reserved
24	EDMACC_2_TC_0_INT	EDMA3CC2 individual completion interrupt
25	EDMACC_2_TC_1_INT	EDMA3CC2 individual completion interrupt
26	EDMACC_2_TC_2_INT	EDMA3CC2 individual completion interrupt
27	EDMACC_2_TC_3_INT	EDMA3CC2 individual completion interrupt
28	EDMACC_2_TC_4_INT	EDMA3CC2 individual completion interrupt
29	EDMACC_2_TC_5_INT	EDMA3CC2 individual completion interrupt
30	EDMACC_2_TC_6_INT	EDMA3CC2 individual completion interrupt
31	EDMACC_2_TC_7_INT	EDMA3CC2 individual completion interrupt
32	EDMACC_0_ERRINT	EDMA3CC0 error interrupt
33	EDMACC_0_MPINT	EDMA3CC0 memory protection interrupt
34	EDMACC_0_TC_0_ERRINT	EDMA3CC0 TPTC0 error interrupt
35	EDMACC_0_TC_1_ERRINT	EDMA3CC0 TPTC1 error interrupt
36	EDMACC_0_GINT	EDMA3CC0 GINT
37	Reserved	Reserved
38	EDMACC_0_TC_0_INT	EDMA3CC0 individual completion interrupt
39	EDMACC_0_TC_1_INT	EDMA3CC0 individual completion interrupt
40	EDMACC_0_TC_2_INT	EDMA3CC0 individual completion interrupt
41	EDMACC_0_TC_3_INT	EDMA3CC0 individual completion interrupt
42	EDMACC_0_TC_4_INT	EDMA3CC0 individual completion interrupt
43	EDMACC_0_TC_5_INT	EDMA3CC0 individual completion interrupt
44	EDMACC_0_TC_6_INT	EDMA3CC0 individual completion interrupt
45	EDMACC_0_TC_7_INT	EDMA3CC0 individual completion interrupt
46	Reserved	Reserved

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Table 4-24 CIC1 Event Inputs — C66x CorePac Secondary Interrupts (Part 3 of 12)

Event No.	Event Name	Description
47	QMSS_QUE_PEND_658	Navigator transmit queue pending event for indicated queue
48	PCIE_INT12	PCIE interrupt
49	PCIE_INT13	PCIE interrupt
50	PCIE_INT0	PCIE interrupt
51	PCIE_INT1	PCIE interrupt
52	PCIE_INT2	PCIE interrupt
53	PCIE_INT3	PCIE interrupt
54	SPI_0_INT0	SPI0 interrupt
55	SPI_0_INT1	SPI0 interrupt
56	SPI_0_XEVT	SPI0 transmit event
57	SPI_0_REVT	SPI0 receive event
58	I2C_0_INT	I2C0 interrupt
59	I2C_0_REVT	I2C0 receive event
60	I2C_0_XEVT	I2C0 transmit event
61	Reserved	Reserved
62	Reserved	Reserved
63	DBGTBR_DMAINT	Debug trace buffer (TBR) DMA event
64	MPU_12_INT	MPU12 interrupt
65	DBGTBR_ACQCOMP	Debug trace buffer (TBR) acquisition has been completed
66	MPU_13_INT	MPU13 interrupt
67	MPU_14_INT	MPU14 interrupt
68	NETCP_MDIO_LINK_INT0	Packet Accelerator 0 subsystem MDIO interrupt
69	NETCP_MDIO_LINK_INT1	Packet Accelerator 0 subsystem MDIO interrupt
70	NETCP_MDIO_USER_INT0	Packet Accelerator 0 subsystem MDIO interrupt
71	NETCP_MDIO_USER_INT1	Packet Accelerator 0 subsystem MDIO interrupt
72	NETCP_MISC_INT	Packet Accelerator 0 subsystem misc interrupt
73	TRACER_CORE_0_INT	Tracer sliding time window interrupt for DSP0 L2
74	TRACER_CORE_1_INT	Tracer sliding time window interrupt for DSP1 L2
75	TRACER_CORE_2_INT	Tracer sliding time window interrupt for DSP2 L2
76	TRACER_CORE_3_INT	Tracer sliding time window interrupt for DSP3 L2
77	TRACER_DDR_INT	Tracer sliding time window interrupt for MSMC-DDR3A
78	TRACER_MSMC_0_INT	Tracer sliding time window interrupt for MSMC SRAM bank0
79	TRACER_MSMC_1_INT	Tracer sliding time window interrupt for MSMC SRAM bank1
80	TRACER_MSMC_2_INT	Tracer sliding time window interrupt for MSMC SRAM bank2
81	TRACER_MSMC_3_INT	Tracer sliding time window interrupt for MSMC SRAM bank3
82	TRACER_CFG_INT	Tracer sliding time window interrupt for CFG0 TeraNet
83	TRACER_QMSS_QM_CFG1_INT	Tracer sliding time window interrupt for Navigator CFG1 slave port
84	TRACER_QMSS_DMA_INT	Tracer sliding time window interrupt for Navigator VBUSM slave port
85	TRACER_SEM_INT	Tracer sliding time window interrupt for Semaphore
86	PSC_ALLINT	Power & Sleep Controller interrupt
87	MSMC_SCRUB_CERROR	Correctable (1-bit) soft error detected during scrub cycle
88	BOOTCFG_INT	Chip-level MMR Error Register
89	SR_0_PO_VCON_SMPSERR_INT	SmartReflex SMPS error interrupt
90	MPU_0_INT	MPU0 addressing violation interrupt and protection violation interrupt.

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Table 4-24 CIC1 Event Inputs — C66x CorePac Secondary Interrupts (Part 4 of 12)

Event No.	Event Name	Description
91	QMSS_QUE_PEND_659	Navigator transmit queue pending event for indicated queue
92	MPU_1_INT	MPU1 addressing violation interrupt and protection violation interrupt.
93	QMSS_QUE_PEND_660	Navigator transmit queue pending event for indicated queue
94	MPU_2_INT	MPU2 addressing violation interrupt and protection violation interrupt.
95	QMSS_QUE_PEND_661	Navigator transmit queue pending event for indicated queue
96	MPU_3_INT	MPU3 addressing violation interrupt and protection violation interrupt.
97	QMSS_QUE_PEND_662	Navigator transmit queue pending event for indicated queue
98	MSMC_DEDC_CERROR	Correctable (1-bit) soft error detected on SRAM read
99	MSMC_DEDC_NC_ERROR	Non-correctable (2-bit) soft error detected on SRAM read
100	MSMC_SCRUB_NC_ERROR	Non-correctable (2-bit) soft error detected during scrub cycle
101	Reserved	Reserved
102	MSMC_MPF_ERROR8	Memory protection fault indicators for system master PrivID = 8
103	MSMC_MPF_ERROR9	Memory protection fault indicators for system master PrivID = 9
104	MSMC_MPF_ERROR10	Memory protection fault indicators for system master PrivID = 10
105	MSMC_MPF_ERROR11	Memory protection fault indicators for system master PrivID = 11
106	MSMC_MPF_ERROR12	Memory protection fault indicators for system master PrivID = 12
107	MSMC_MPF_ERROR13	Memory protection fault indicators for system master PrivID = 13
108	MSMC_MPF_ERROR14	Memory protection fault indicators for system master PrivID = 14
109	MSMC_MPF_ERROR15	Memory protection fault indicators for system master PrivID = 15
110	DDR3_0_ERR	DDR3A_EMIF Error interrupt
111	HYPERLINK_0_INT	HyperLink 0 interrupt
112	SRIO_INTDST0	SRIO interrupt
113	SRIO_INTDST1	SRIO interrupt
114	SRIO_INTDST2	SRIO interrupt
115	SRIO_INTDST3	SRIO interrupt
116	SRIO_INTDST4	SRIO interrupt
117	SRIO_INTDST5	SRIO interrupt
118	SRIO_INTDST6	SRIO interrupt
119	SRIO_INTDST7	SRIO interrupt
120	SRIO_INTDST8	SRIO interrupt
121	SRIO_INTDST9	SRIO interrupt
122	SRIO_INTDST10	SRIO interrupt
123	SRIO_INTDST11	SRIO interrupt
124	SRIO_INTDST12	SRIO interrupt
125	SRIO_INTDST13	SRIO interrupt
126	SRIO_INTDST14	SRIO interrupt
127	SRIO_INTDST15	SRIO interrupt
128	AEMIF_EASYNCERR	Asynchronous EMIF16 error interrupt
129	TRACER_CORE_4_INT	Tracer sliding time window interrupt for DSP4 L2
130	TRACER_CORE_5_INT	Tracer sliding time window interrupt for DSP5 L2
131	TRACER_CORE_6_INT	Tracer sliding time window interrupt for DSP6 L2
132	TRACER_CORE_7_INT	Tracer sliding time window interrupt for DSP7 L2
133	QMSS_INTD_1_PKTDMA_0	Navigator interrupt for Packet DMA starvation
134	QMSS_INTD_1_PKTDMA_1	Navigator interrupt for Packet DMA starvation

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Table 4-24 CIC1 Event Inputs — C66x CorePac Secondary Interrupts (Part 5 of 12)

Event No.	Event Name	Description
135	SRIO_INT_PKTDMA_0	IPC interrupt generation
136	NETCP_PKTDMA_INT0	Packet Accelerator0 Packet DMA starvation interrupt
137	SR_0_SMARTREFLEX_INTREQ0	SmartReflex controller interrupt
138	SR_0_SMARTREFLEX_INTREQ1	SmartReflex controller interrupt
139	SR_0_SMARTREFLEX_INTREQ2	SmartReflex controller interrupt
140	SR_0_SMARTREFLEX_INTREQ3	SmartReflex controller interrupt
141	SR_0_VPNOSMPSACK	SmartReflex VPVOLTUPDATE has been asserted but SMPS has not been responded to in a defined time interval
142	SR_0_VPEQVALUE	SmartReflex SRSINTERUPT is asserted, but the new voltage is not different from the current SMPS voltage
143	SR_0_VPMAXVDD	SmartReflex. The new voltage required is equal to or greater than MaxVdd
144	SR_0_VPMINVDD	SmartReflex. The new voltage required is equal to or less than MinVdd
145	SR_0_VPINIDLE	SmartReflex indicating that the FSM of voltage processor is in idle
146	SR_0_VPOPPCHANGEDONE	SmartReflex indicating that the average frequency error is within the desired limit
147	Reserved	Reserved
148	UART_0_UARTINT	UART0 interrupt
149	UART_0_URXEVT	UART0 receive event
150	UART_0_UTXEVT	UART0 transmit event
151	QMSS_QUE_PEND_663	Navigator transmit queue pending event for indicated queue
152	QMSS_QUE_PEND_664	Navigator transmit queue pending event for indicated queue
153	QMSS_QUE_PEND_665	Navigator transmit queue pending event for indicated queue
154	QMSS_QUE_PEND_666	Navigator transmit queue pending event for indicated queue
155	QMSS_QUE_PEND_667	Navigator transmit queue pending event for indicated queue
156	QMSS_QUE_PEND_668	Navigator transmit queue pending event for indicated queue
157	QMSS_QUE_PEND_669	Navigator transmit queue pending event for indicated queue
158	QMSS_QUE_PEND_670	Navigator transmit queue pending event for indicated queue
159	QMSS_QUE_PEND_671	Navigator transmit queue pending event for indicated queue
160	SR_0_VPSMPSACK	SmartReflex VPVOLTUPDATE asserted and SMPS has acknowledged in a defined time interval
161	Reserved	Reserved
162	Reserved	Reserved
163	Reserved	Reserved
164	Reserved	Reserved
165	SR_0_SR_TEMPSENSOR	SmartReflex temperature threshold crossing interrupt
166	SR_0_SR_TIMERINT	SmartReflex internal timer expiration interrupt
167	AIF_ATEVT8	AIF timer event
168	AIF_ATEVT9	AIF timer event
169	AIF_ATEVT10	AIF timer event
170	AIF_ATEVT11	AIF timer event
171	AIF_ATEVT12	AIF timer event
172	AIF_ATEVT13	AIF timer event
173	AIF_ATEVT14	AIF timer event
174	AIF_ATEVT15	AIF timer event
175	TIMER_7_INTL	Timer interrupt low
176	TIMER_7_INTH	Timer interrupt high
177	TIMER_6_INTL	Timer interrupt low

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Table 4-24 CIC1 Event Inputs — C66x CorePac Secondary Interrupts (Part 6 of 12)

Event No.	Event Name	Description
178	TIMER_6_INTH	Timer interrupt high
179	TIMER_5_INTL	Timer interrupt low
180	TIMER_5_INTH	Timer interrupt high
181	TIMER_4_INTL	Timer interrupt low
182	TIMER_4_INTH	Timer interrupt high
183	TIMER_3_INTL	Timer interrupt low
184	TIMER_3_INTH	Timer interrupt high
185	TIMER_2_INTL	Timer interrupt low
186	TIMER_2_INTH	Timer interrupt high
187	TIMER_1_INTL	Timer interrupt low
188	TIMER_1_INTH	Timer interrupt high
189	TIMER_0_INTL	Timer interrupt low
190	TIMER_0_INTH	Timer interrupt high
191	TCP3D_0_INT	TCP3d interrupt
192	TCP3D_1_INT	TCP3d interrupt
193	TCP3D_2_INT	TCP3d interrupt
194	TCP3D_3_INT	TCP3d interrupt
195	TCP3D_0_REVT0	TCP3d event
196	TCP3D_0_REVT1	TCP3d event
197	TCP3D_1_REVT0	TCP3d event
198	TCP3D_1_REVT1	TCP3d event
199	TCP3D_2_REVT0	TCP3d event
200	TCP3D_2_REVT1	TCP3d event
201	TCP3D_3_REVT0	TCP3d event
202	TCP3D_3_REVT1	TCP3d event
203	TAC_INT	TAC interrupt
204	TAC_DEVT0	TAC debug event
205	TAC_DEVT1	TAC debug event
206	AIF_INT	AIF interrupt
207	EDMACC_4_ERRINT	EDMA3CC4 error interrupt
208	EDMACC_4_MPINT	EDMA3CC4 memory protection interrupt
209	EDMACC_4_TC_0_ERRINT	EDMA3CC4 TPTC0 error interrupt
210	EDMACC_4_TC_1_ERRINT	EDMA3CC4 TPTC1 error interrupt
211	EDMACC_4_GINT	EDMA3CC4 GINT
212	EDMACC_4_TC_0_INT	EDMA3CC4 individual completion interrupt
213	EDMACC_4_TC_1_INT	EDMA3CC4 individual completion interrupt
214	EDMACC_4_TC_2_INT	EDMA3CC4 individual completion interrupt
215	EDMACC_4_TC_3_INT	EDMA3CC4 individual completion interrupt
216	EDMACC_4_TC_4_INT	EDMA3CC4 individual completion interrupt
217	EDMACC_4_TC_5_INT	EDMA3CC4 individual completion interrupt
218	EDMACC_4_TC_6_INT	EDMA3CC4 individual completion interrupt
219	EDMACC_4_TC_7_INT	EDMA3CC4 individual completion interrupt
220	EDMACC_3_ERRINT	EDMA3CC3 error interrupt
221	EDMACC_3_MPINT	EDMA3CC3 memory protection interrupt

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Table 4-24 CIC1 Event Inputs — C66x CorePac Secondary Interrupts (Part 7 of 12)

Event No.	Event Name	Description
222	EDMACC_3_TC_0_ERRINT	EDMA3CC3 TPTC0 error interrupt
223	EDMACC_3_TC_1_ERRINT	EDMA3CC3 TPTC1 error interrupt
224	EDMACC_3_GINT	EDMA3CC3 GINT
225	EDMACC_3_TC_0_INT	EDMA3CC3 individual completion interrupt
226	EDMACC_3_TC_1_INT	EDMA3CC3 individual completion interrupt
227	EDMACC_3_TC_2_INT	EDMA3CC3 individual completion interrupt
228	EDMACC_3_TC_3_INT	EDMA3CC3 individual completion interrupt
229	EDMACC_3_TC_4_INT	EDMA3CC3 individual completion interrupt
230	EDMACC_3_TC_5_INT	EDMA3CC3 individual completion interrupt
231	EDMACC_3_TC_6_INT	EDMA3CC3 individual completion interrupt
232	EDMACC_3_TC_7_INT	EDMA3CC3 individual completion interrupt
233	UART_1_UARTINT	UART1 interrupt
234	UART_1_URXEVT	UART1 receive event
235	UART_1_UTXEVT	UART1 transmit event
236	I2C_1_INT	I2C1 interrupt
237	I2C_1_REVT	I2C1 receive event
238	I2C_1_XEVT	I2C1 transmit event
239	SPI_1_INT0	SPI1 interrupt0
240	SPI_1_INT1	SPI1 interrupt1
241	SPI_1_XEVT	SPI1 transmit event
242	SPI_1_REVT	SPI1 receive event
243	MPU_5_INT	MPU5 addressing violation interrupt and protection violation interrupt
244	MPU_8_INT	MPU8 addressing violation interrupt and protection violation interrupt
245	MPU_9_INT	MPU9 addressing violation interrupt and protection violation interrupt
246	MPU_11_INT	MPU11 addressing violation interrupt and protection violation interrupt
247	MPU_4_INT	MPU4 addressing violation interrupt and protection violation interrupt
248	MPU_6_INT	MPU6 addressing violation interrupt and protection violation interrupt
249	MPU_7_INT	MPU7 addressing violation interrupt and protection violation interrupt
250	MPU_10_INT	MPU10 addressing violation interrupt and protection violation interrupt
251	SPI_2_INT0	SPI2 interrupt0
252	SPI_2_INT1	SPI2 interrupt1
253	SPI_2_XEVT	SPI2 transmit event
254	SPI_2_REVT	SPI2 receive event
255	I2C_2_INT	I2C2 interrupt
256	I2C_2_REVT	I2C2 receive event
257	I2C_2_XEVT	I2C2 transmit event
258	10GbE_LINK_INT0	10 Gigabit Ethernet subsystem MDIO interrupt
259	10GbE_LINK_INT1	10 Gigabit Ethernet subsystem MDIO interrupt
260	10GbE_USER_INT0	10 Gigabit Ethernet subsystem MDIO interrupt
261	10GbE_USER_INT1	10 Gigabit Ethernet subsystem MDIO interrupt
262	10GbE_MISC_INT	10 Gigabit Ethernet subsystem MDIO interrupt
263	10GbE_INT_PKTDMA_0	10 Gigabit Ethernet Packet DMA starvation interrupt
264	Reserved	Reserved
265	Reserved	Reserved

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Table 4-24 CIC1 Event Inputs — C66x CorePac Secondary Interrupts (Part 8 of 12)

Event No.	Event Name	Description
266	Reserved	Reserved
267	BCP_INT0	BCP interrupt
268	BCP_INT1	BCP interrupt
269	BCP_INT2	BCP interrupt
270	BCP_INT3	BCP interrupt
271	RAC_0_TRACE_GCCP0	RAC trace
272	RAC_0_TRACE_GCCP1	RAC trace
273	RAC_1_TRACE_GCCP0	RAC trace
274	RAC_1_TRACE_GCCP1	RAC trace
275	RAC_2_TRACE_GCCP0	RAC trace
276	RAC_2_TRACE_GCCP1	RAC trace
277	RAC_3_TRACE_GCCP0	RAC trace
278	RAC_3_TRACE_GCCP1	RAC trace
279	TAC_DEVT2	TAC debug
280	TAC_DEVT3	TAC debug
281	TAC_DEVT4	TAC debug
282	TAC_DEVT5	TAC debug
283	Reserved	Reserved
284	Reserved	Reserved
285	Reserved	Reserved
286	Reserved	Reserved
287	Reserved	Reserved
288	Reserved	Reserved
289	Reserved	Reserved
290	TRACER_RAC_1_INT	Tracer RAC interrupt
291	TRACER_RAC_FE_INT	Tracer RAC interrupt
292	QMSS_QUE_PEND_652	Navigator transmit queue pending event for indicated queue
293	QMSS_QUE_PEND_653	Navigator transmit queue pending event for indicated queue
294	QMSS_QUE_PEND_654	Navigator transmit queue pending event for indicated queue
295	QMSS_QUE_PEND_655	Navigator transmit queue pending event for indicated queue
296	QMSS_QUE_PEND_656	Navigator transmit queue pending event for indicated queue
297	QMSS_QUE_PEND_657	Navigator transmit queue pending event for indicated queue
298	QMSS_QUE_PEND_8844	Navigator transmit queue pending event for indicated queue
299	QMSS_QUE_PEND_8845	Navigator transmit queue pending event for indicated queue
300	QMSS_QUE_PEND_8846	Navigator transmit queue pending event for indicated queue
301	QMSS_QUE_PEND_8847	Navigator transmit queue pending event for indicated queue
302	QMSS_QUE_PEND_8848	Navigator transmit queue pending event for indicated queue
303	QMSS_QUE_PEND_8849	Navigator transmit queue pending event for indicated queue
304	QMSS_QUE_PEND_8850	Navigator transmit queue pending event for indicated queue
305	QMSS_QUE_PEND_8851	Navigator transmit queue pending event for indicated queue
306	QMSS_QUE_PEND_8852	Navigator transmit queue pending event for indicated queue
307	QMSS_QUE_PEND_8853	Navigator transmit queue pending event for indicated queue
308	QMSS_QUE_PEND_8854	Navigator transmit queue pending event for indicated queue
309	QMSS_QUE_PEND_8855	Navigator transmit queue pending event for indicated queue

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Table 4-24 CIC1 Event Inputs — C66x CorePac Secondary Interrupts (Part 9 of 12)

Event No.	Event Name	Description
310	QMSS_QUE_PEND_8856	Navigator transmit queue pending event for indicated queue
311	QMSS_QUE_PEND_8857	Navigator transmit queue pending event for indicated queue
312	QMSS_QUE_PEND_8858	Navigator transmit queue pending event for indicated queue
313	QMSS_QUE_PEND_8859	Navigator transmit queue pending event for indicated queue
314	QMSS_QUE_PEND_8860	Navigator transmit queue pending event for indicated queue
315	QMSS_QUE_PEND_8861	Navigator transmit queue pending event for indicated queue
316	QMSS_QUE_PEND_8862	Navigator transmit queue pending event for indicated queue
317	QMSS_QUE_PEND_8863	Navigator transmit queue pending event for indicated queue
318	QMSS_INTD_2_PKTDMA_0	Navigator ECC error interrupt
319	QMSS_INTD_2_PKTDMA_1	Navigator ECC error interrupt
320	QMSS_INTD_1_LOW_0	Navigator interrupt low
321	QMSS_INTD_1_LOW_1	Navigator interrupt low
322	QMSS_INTD_1_LOW_2	Navigator interrupt low
323	QMSS_INTD_1_LOW_3	Navigator interrupt low
324	QMSS_INTD_1_LOW_4	Navigator interrupt low
325	QMSS_INTD_1_LOW_5	Navigator interrupt low
326	QMSS_INTD_1_LOW_6	Navigator interrupt low
327	QMSS_INTD_1_LOW_7	Navigator interrupt low
328	QMSS_INTD_1_LOW_8	Navigator interrupt low
329	QMSS_INTD_1_LOW_9	Navigator interrupt low
330	QMSS_INTD_1_LOW_10	Navigator interrupt low
331	QMSS_INTD_1_LOW_11	Navigator interrupt low
332	QMSS_INTD_1_LOW_12	Navigator interrupt low
333	QMSS_INTD_1_LOW_13	Navigator interrupt low
334	QMSS_INTD_1_LOW_14	Navigator interrupt low
335	QMSS_INTD_1_LOW_15	Navigator interrupt low
336	QMSS_INTD_2_LOW_0	Navigator second interrupt low
337	QMSS_INTD_2_LOW_1	Navigator second interrupt low
338	QMSS_INTD_2_LOW_2	Navigator second interrupt low
339	QMSS_INTD_2_LOW_3	Navigator second interrupt low
340	QMSS_INTD_2_LOW_4	Navigator second interrupt low
341	QMSS_INTD_2_LOW_5	Navigator second interrupt low
342	QMSS_INTD_2_LOW_6	Navigator second interrupt low
343	QMSS_INTD_2_LOW_7	Navigator second interrupt low
344	QMSS_INTD_2_LOW_8	Navigator second interrupt low
345	QMSS_INTD_2_LOW_9	Navigator second interrupt low
346	QMSS_INTD_2_LOW_10	Navigator second interrupt low
347	QMSS_INTD_2_LOW_11	Navigator second interrupt low
348	QMSS_INTD_2_LOW_12	Navigator second interrupt low
349	QMSS_INTD_2_LOW_13	Navigator second interrupt low
350	QMSS_INTD_2_LOW_14	Navigator second interrupt low
351	QMSS_INTD_2_LOW_15	Navigator second interrupt low
352	TRACER_EDMACC_0	Tracer sliding time window interrupt for EDMA3CC0
353	TRACER_EDMACC_123_INT	Tracer sliding time window interrupt for EDMA3CC1, EDMA3CC2 and EDMA3CC3

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Table 4-24 CIC1 Event Inputs — C66x CorePac Secondary Interrupts (Part 10 of 12)

Event No.	Event Name	Description
354	TRACER_CIC_INT	Tracer sliding time window interrupt for interrupt controllers (CIC)
355	TRACER_MSMC_4_INT	Tracer sliding time window interrupt for MSMC SRAM bank4
356	TRACER_MSMC_5_INT	Tracer sliding time window interrupt for MSMC SRAM bank5
357	TRACER_MSMC_6_INT	Tracer sliding time window interrupt for MSMC SRAM bank6
358	TRACER_MSMC_7_INT	Tracer sliding time window interrupt for MSMC SRAM bank7
359	TRACER_SPI_ROM_EMIF_INT	Tracer sliding time window interrupt for SPI/ROM/EMIF16 modules
360	TRACER_QMSS_QM_CFG2_INT	Tracer sliding time window interrupt for QM2
361	TRACER_TAC_BE_INT	Tracer TAC interrupt
362	TRACER_RAC_2_INT	Tracer RAC interrupt
363	TRACER_DDR_1_INT	Tracer sliding time window interrupt for DDR3B
364	TRACER_BCR_INT	Tracer sliding time window interrupt for BCR
365	HYPERLINK_1_INT	HyperLink 1 interrupt
366	VCP_0_INT0	VCP interrupt
367	VCP_0_INT1	VCP interrupt
368	VCP_0_INT2	VCP interrupt
369	VCP_0_INT3	VCP interrupt
370	VCP_1_INT0	VCP interrupt
371	VCP_1_INT1	VCP interrupt
372	VCP_1_INT2	VCP interrupt
373	VCP_1_INT3	VCP interrupt
374	VCP_0_REVT0	VCP event
375	VCP_0_XEVT0	VCP event
376	VCP_0_REVT1	VCP event
377	VCP_0_XEVT1	VCP event
378	VCP_0_REVT2	VCP event
379	VCP_0_XEVT2	VCP event
380	VCP_0_REVT3	VCP event
381	VCP_0_XEVT3	VCP event
382	VCP_1_REVT0	VCP event
383	VCP_1_XEVT0	VCP event
384	VCP_1_REVT1	VCP event
385	VCP_1_XEVT1	VCP event
386	VCP_1_REVT2	VCP event
387	VCP_1_XEVT2	VCP event
388	VCP_1_REVT3	VCP event
389	VCP_1_XEVT3	VCP event
390	FFTC_0_INT0	FFTC interrupt
391	FFTC_0_INT1	FFTC interrupt
392	FFTC_0_INT2	FFTC interrupt
393	FFTC_0_INT3	FFTC interrupt
394	FFTC_1_INT0	FFTC interrupt
395	FFTC_1_INT1	FFTC interrupt
396	FFTC_1_INT2	FFTC interrupt
397	FFTC_1_INT3	FFTC interrupt

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Table 4-24 CIC1 Event Inputs — C66x CorePac Secondary Interrupts (Part 11 of 12)

Event No.	Event Name	Description
398	FFTC_2_INT0	FFTC interrupt
399	FFTC_2_INT1	FFTC interrupt
400	FFTC_2_INT2	FFTC interrupt
401	FFTC_2_INT3	FFTC interrupt
402	FFTC_3_INT0	FFTC interrupt
403	FFTC_3_INT1	FFTC interrupt
404	FFTC_3_INT2	FFTC interrupt
405	FFTC_3_INT3	FFTC interrupt
406	FFTC_4_INT0	FFTC interrupt
407	FFTC_4_INT1	FFTC interrupt
408	FFTC_4_INT2	FFTC interrupt
409	FFTC_4_INT3	FFTC interrupt
410	FFTC_5_INT0	FFTC interrupt
411	FFTC_5_INT1	FFTC interrupt
412	FFTC_5_INT2	FFTC interrupt
413	FFTC_5_INT3	FFTC interrupt
414	AIF_ATEVT16	AIF timer event
415	AIF_ATEVT17	AIF timer event
416	AIF_ATEVT18	AIF timer event
417	AIF_ATEVT19	AIF timer event
418	AIF_ATEVT20	AIF timer event
419	AIF_ATEVT21	AIF timer event
420	AIF_ATEVT22	AIF timer event
421	AIF_ATEVT23	AIF timer event
422	USB_INT00	USB interrupt
423	USB_INT04	USB interrupt
424	USB_INT05	USB interrupt
425	USB_INT06	USB interrupt
426	USB_INT07	USB interrupt
427	USB_INT08	USB interrupt
428	USB_INT09	USB interrupt
429	USB_INT10	USB interrupt
430	USB_INT11	USB interrupt
431	USB_MISCINT	USB miscellaneous interrupt
432	USB_OABSINT	USB OABS interrupt
433	TIMER_12_INTL	Timer interrupt low
434	TIMER_12_INTH	Timer interrupt high
435	TIMER_13_INTL	Timer interrupt low
436	TIMER_13_INTH	Timer interrupt high
437	TIMER_14_INTL	Timer interrupt low
438	TIMER_14_INTH	Timer interrupt high
439	TIMER_15_INTL	Timer interrupt low
440	TIMER_15_INTH	Timer interrupt high
441	TIMER_16_INTL	Timer interrupt low

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Table 4-24 CIC1 Event Inputs — C66x CorePac Secondary Interrupts (Part 12 of 12)

Event No.	Event Name	Description
442	TIMER_17_INTL	Timer interrupt high
443	TIMER_18_INTL	Timer interrupt low
444	TIMER_19_INTL	Timer interrupt high
445	DDR3_1_ERR	DDR3B_EMIF error interrupt
446	GPIO_INT16	GPIO interrupt
447	GPIO_INT17	GPIO interrupt
448	GPIO_INT18	GPIO interrupt
449	GPIO_INT19	GPIO interrupt
450	GPIO_INT20	GPIO interrupt
451	GPIO_INT21	GPIO interrupt
452	GPIO_INT22	GPIO interrupt
453	GPIO_INT23	GPIO interrupt
454	GPIO_INT24	GPIO interrupt
455	GPIO_INT25	GPIO interrupt
456	GPIO_INT26	GPIO interrupt
457	GPIO_INT27	GPIO interrupt
458	GPIO_INT28	GPIO interrupt
459	GPIO_INT29	GPIO interrupt
460	GPIO_INT30	GPIO interrupt
461	GPIO_INT31	GPIO interrupt
462	SRIO_INTDST20	SRIOI interrupt
463	SRIO_INTDST21	SRIOI interrupt
464	SRIO_INTDST22	SRIOI interrupt
465	SRIO_INTDST23	SRIOI interrupt
466	PCIE_INT8	PCIE MSI interrupt
467	PCIE_INT9	PCIE MSI interrupt
468	PCIE_INT10	PCIE MSI interrupt
469	PCIE_INT11	PCIE MSI interrupt
470	SEM_INT12	Semaphore interrupt
471	SEM_INT13	Semaphore interrupt
472	SEM_ERR12	Semaphore error interrupt
473	SEM_ERR13	Semaphore error interrupt
474	Reserved	Reserved
End of Table 4-24		

Table 4-25 CIC2 Event Inputs (Secondary Events for EDMA3CC0 and HyperLinks) (Part 1 of 12)

Event No.	Event Name	Description
0	GPIO_INT8	GPIO interrupt
1	GPIO_INT9	GPIO interrupt
2	GPIO_INT10	GPIO interrupt
3	GPIO_INT11	GPIO interrupt
4	GPIO_INT12	GPIO interrupt
5	GPIO_INT13	GPIO interrupt

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Table 4-25 CIC2 Event Inputs (Secondary Events for EDMA3CC0 and HyperLinks) (Part 2 of 12)

Event No.	Event Name	Description
6	GPIO_INT14	GPIO interrupt
7	GPIO_INT15	GPIO interrupt
8	DBGTBR_DMAINT	Debug trace buffer (TBR) DMA event
9	Reserved	Reserved
10	Reserved	Reserved
11	TETB_FULLINT0	TETB0 is full
12	TETB_HFULLINT0	TETB0 is half full
13	TETB_ACQINT0	TETB0 acquisition has been completed
14	TETB_FULLINT1	TETB1 is full
15	TETB_HFULLINT1	TETB1 is half full
16	TETB_ACQINT1	TETB1 acquisition has been completed
17	TETB_FULLINT2	TETB2 is full
18	TETB_HFULLINT2	TETB2 is half full
19	TETB_ACQINT2	TETB2 acquisition has been completed
20	TETB_FULLINT3	TETB3 is full
21	TETB_HFULLINT3	TETB3 is half full
22	TETB_ACQINT3	TETB3 acquisition has been completed
23	Reserved	Reserved
24	QMSS_INTD_1_HIGH_16	Navigator hi interrupt
25	QMSS_INTD_1_HIGH_17	Navigator hi interrupt
26	QMSS_INTD_1_HIGH_18	Navigator hi interrupt
27	QMSS_INTD_1_HIGH_19	Navigator hi interrupt
28	QMSS_INTD_1_HIGH_20	Navigator hi interrupt
29	QMSS_INTD_1_HIGH_21	Navigator hi interrupt
30	QMSS_INTD_1_HIGH_22	Navigator hi interrupt
31	QMSS_INTD_1_HIGH_23	Navigator hi interrupt
32	QMSS_INTD_1_HIGH_24	Navigator hi interrupt
33	QMSS_INTD_1_HIGH_25	Navigator hi interrupt
34	QMSS_INTD_1_HIGH_26	Navigator hi interrupt
35	QMSS_INTD_1_HIGH_27	Navigator hi interrupt
36	QMSS_INTD_1_HIGH_28	Navigator hi interrupt
37	QMSS_INTD_1_HIGH_29	Navigator hi interrupt
38	QMSS_INTD_1_HIGH_30	Navigator hi interrupt
39	QMSS_INTD_1_HIGH_31	Navigator hi interrupt
40	NETCP_MDIO_LINK_INT0	Packet Accelerator 0 subsystem MDIO interrupt
41	NETCP_MDIO_LINK_INT1	Packet Accelerator 0 subsystem MDIO interrupt
42	NETCP_MDIO_USER_INT0	Packet Accelerator 0 subsystem MDIO interrupt
43	NETCP_MDIO_USER_INT1	Packet Accelerator 0 subsystem MDIO interrupt
44	NETCP_MISC_INT	Packet Accelerator 0 subsystem MDIO interrupt
45	TRACER_CORE_0_INT	Tracer sliding time window interrupt for DSP0 L2
46	TRACER_CORE_1_INT	Tracer sliding time window interrupt for DSP1 L2
47	TRACER_CORE_2_INT	Tracer sliding time window interrupt for DSP2 L2
48	TRACER_CORE_3_INT	Tracer sliding time window interrupt for DSP3 L2
49	TRACER_DDR_INT	Tracer sliding time window interrupt for MSMC-DDR3A

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Table 4-25 CIC2 Event Inputs (Secondary Events for EDMA3CC0 and HyperLinks) (Part 3 of 12)

Event No.	Event Name	Description
50	TRACER_MSMC_0_INT	Tracer sliding time window interrupt for MSMC SRAM bank0
51	TRACER_MSMC_1_INT	Tracer sliding time window interrupt for MSMC SRAM bank1
52	TRACER_MSMC_2_INT	Tracer sliding time window interrupt for MSMC SRAM bank2
53	TRACER_MSMC_3_INT	Tracer sliding time window interrupt for MSMC SRAM bank3
54	TRACER_CFG_INT	Tracer sliding time window interrupt for TeraNet CFG
55	TRACER_QMSS_QM_CFG1_INT	Tracer sliding time window interrupt for Navigator CFG1 slave port
56	TRACER_QMSS_DMA_INT	Tracer sliding time window interrupt for Navigator VBUSM slave port
57	TRACER_SEM_INT	Tracer sliding time window interrupt for Semaphore interrupt
58	SEM_ERR0	Semaphore error interrupt
59	SEM_ERR1	Semaphore error interrupt
60	SEM_ERR2	Semaphore error interrupt
61	SEM_ERR3	Semaphore error interrupt
62	BOOTCFG_INT	BOOTCFG error interrupt
63	NETCP_PKTDMA_INT0	Packet Accelerator0 Packet DMA starvation interrupt
64	MPU_0_INT	MPU0 interrupt
65	MSMC_SCRUB_CERROR	MSMC error interrupt
66	MPU_1_INT	MPU1 interrupt
67	SRIO_INT_PKTDMA_0	Packet Accelerator0 Packet DMA interrupt
68	MPU_2_INT	MPU2 interrupt
69	QMSS_INTD_1_PKTDMA_0	Navigator Packet DMA interrupt
70	MPU_3_INT	MPU3 interrupt
71	QMSS_INTD_1_PKTDMA_1	Navigator Packet DMA interrupt
72	MSMC_DEDC_CERROR	MSMC error interrupt
73	MSMC_DEDC_NC_ERROR	MSMC error interrupt
74	MSMC_SCRUB_NC_ERROR	MSMC error interrupt
75	Reserved	Reserved
76	MSMC_MPF_ERROR0	Memory protection fault indicators for system master PrivID = 0
77	MSMC_MPF_ERROR1	Memory protection fault indicators for system master PrivID = 1
78	MSMC_MPF_ERROR2	Memory protection fault indicators for system master PrivID = 2
79	MSMC_MPF_ERROR3	Memory protection fault indicators for system master PrivID = 3
80	MSMC_MPF_ERROR4	Memory protection fault indicators for system master PrivID = 4
81	MSMC_MPF_ERROR5	Memory protection fault indicators for system master PrivID = 5
82	MSMC_MPF_ERROR6	Memory protection fault indicators for system master PrivID = 6
83	MSMC_MPF_ERROR7	Memory protection fault indicators for system master PrivID = 7
84	MSMC_MPF_ERROR8	Memory protection fault indicators for system master PrivID = 8
85	MSMC_MPF_ERROR9	Memory protection fault indicators for system master PrivID = 9
86	MSMC_MPF_ERROR10	Memory protection fault indicators for system master PrivID = 10
87	MSMC_MPF_ERROR11	Memory protection fault indicators for system master PrivID = 11
88	MSMC_MPF_ERROR12	Memory protection fault indicators for system master PrivID = 12
89	MSMC_MPF_ERROR13	Memory protection fault indicators for system master PrivID = 13
90	MSMC_MPF_ERROR14	Memory protection fault indicators for system master PrivID = 14
91	MSMC_MPF_ERROR15	Memory protection fault indicators for system master PrivID = 15
92	Reserved	Reserved
93	SRIO_INTDST0	SRIO interrupt

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Table 4-25 CIC2 Event Inputs (Secondary Events for EDMA3CC0 and HyperLinks) (Part 4 of 12)

Event No.	Event Name	Description
94	SRIO_INTDST1	SRIO interrupt
95	SRIO_INTDST2	SRIO interrupt
96	SRIO_INTDST3	SRIO interrupt
97	SRIO_INTDST4	SRIO interrupt
98	SRIO_INTDST5	SRIO interrupt
99	SRIO_INTDST6	SRIO interrupt
100	SRIO_INTDST7	SRIO interrupt
101	SRIO_INTDST8	SRIO interrupt
102	SRIO_INTDST9	SRIO interrupt
103	SRIO_INTDST10	SRIO interrupt
104	SRIO_INTDST11	SRIO interrupt
105	SRIO_INTDST12	SRIO interrupt
106	SRIO_INTDST13	SRIO interrupt
107	SRIO_INTDST14	SRIO interrupt
108	SRIO_INTDST15	SRIO interrupt
109	SRIO_INTDST16	SRIO interrupt
110	SRIO_INTDST17	SRIO interrupt
111	SRIO_INTDST18	SRIO interrupt
112	SRIO_INTDST19	SRIO interrupt
113	SRIO_INTDST20	SRIO interrupt
114	SRIO_INTDST21	SRIO interrupt
115	SRIO_INTDST22	SRIO interrupt
116	SRIO_INTDST23	SRIO interrupt
117	AEMIF_EASYNCERR	Asynchronous EMIF16 error interrupt
118	TETB_FULLINT4	TETB4 is full
119	TETB_HFULLINT4	TETB4 is half full
120	TETB_ACQINT4	TETB4 acquisition has been completed
121	TETB_FULLINT5	TETB5 is full
122	TETB_HFULLINT5	TETB5 is half full
123	TETB_ACQINT5	TETB5 acquisition has been completed
124	TETB_FULLINT6	TETB6 is full
125	TETB_HFULLINT6	TETB6 is half full
126	TETB_ACQINT6	TETB6 acquisition has been completed
127	TETB_FULLINT7	TETB7 is full
128	TETB_HFULLINT7	TETB7 is half full
129	TETB_ACQINT7	TETB7 acquisition has been completed
130	TRACER_CORE_4_INT	Tracer sliding time window interrupt for DSP4 L2
131	TRACER_CORE_5_INT	Tracer sliding time window interrupt for DSP5 L2
132	TRACER_CORE_6_INT	Tracer sliding time window interrupt for DSP6 L2
133	TRACER_CORE_7_INT	Tracer sliding time window interrupt for DSP7 L2
134	SEM_ERR4	Semaphore error interrupt
135	SEM_ERR5	Semaphore error interrupt
136	SEM_ERR6	Semaphore error interrupt
137	SEM_ERR7	Semaphore error interrupt

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Table 4-25 CIC2 Event Inputs (Secondary Events for EDMA3CC0 and HyperLinks) (Part 5 of 12)

Event No.	Event Name	Description
138	QMSS_INTD_1_HIGH_0	Navigator hi interrupt
139	QMSS_INTD_1_HIGH_1	Navigator hi interrupt
140	QMSS_INTD_1_HIGH_2	Navigator hi interrupt
141	QMSS_INTD_1_HIGH_3	Navigator hi interrupt
142	QMSS_INTD_1_HIGH_4	Navigator hi interrupt
143	QMSS_INTD_1_HIGH_5	Navigator hi interrupt
144	QMSS_INTD_1_HIGH_6	Navigator hi interrupt
145	QMSS_INTD_1_HIGH_7	Navigator hi interrupt
146	QMSS_INTD_1_HIGH_8	Navigator hi interrupt
147	QMSS_INTD_1_HIGH_9	Navigator hi interrupt
148	QMSS_INTD_1_HIGH_10	Navigator hi interrupt
149	QMSS_INTD_1_HIGH_11	Navigator hi interrupt
150	QMSS_INTD_1_HIGH_12	Navigator hi interrupt
151	QMSS_INTD_1_HIGH_13	Navigator hi interrupt
152	QMSS_INTD_1_HIGH_14	Navigator hi interrupt
153	QMSS_INTD_1_HIGH_15	Navigator hi interrupt
154	QMSS_INTD_2_HIGH_0	Navigator second hi interrupt
155	QMSS_INTD_2_HIGH_1	Navigator second hi interrupt
156	QMSS_INTD_2_HIGH_2	Navigator second hi interrupt
157	QMSS_INTD_2_HIGH_3	Navigator second hi interrupt
158	QMSS_INTD_2_HIGH_4	Navigator second hi interrupt
159	QMSS_INTD_2_HIGH_5	Navigator second hi interrupt
160	QMSS_INTD_2_HIGH_6	Navigator second hi interrupt
161	QMSS_INTD_2_HIGH_7	Navigator second hi interrupt
162	QMSS_INTD_2_HIGH_8	Navigator second hi interrupt
163	QMSS_INTD_2_HIGH_9	Navigator second hi interrupt
164	QMSS_INTD_2_HIGH_10	Navigator second hi interrupt
165	QMSS_INTD_2_HIGH_11	Navigator second hi interrupt
166	QMSS_INTD_2_HIGH_12	Navigator second hi interrupt
167	QMSS_INTD_2_HIGH_13	Navigator second hi interrupt
168	QMSS_INTD_2_HIGH_14	Navigator second hi interrupt
169	QMSS_INTD_2_HIGH_15	Navigator second hi interrupt
170	QMSS_INTD_2_HIGH_16	Navigator second hi interrupt
171	QMSS_INTD_2_HIGH_17	Navigator second hi interrupt
172	QMSS_INTD_2_HIGH_18	Navigator second hi interrupt
173	QMSS_INTD_2_HIGH_19	Navigator second hi interrupt
174	QMSS_INTD_2_HIGH_20	Navigator second hi interrupt
175	QMSS_INTD_2_HIGH_21	Navigator second hi interrupt
176	QMSS_INTD_2_HIGH_22	Navigator second hi interrupt
177	QMSS_INTD_2_HIGH_23	Navigator second hi interrupt
178	QMSS_INTD_2_HIGH_24	Navigator second hi interrupt
179	QMSS_INTD_2_HIGH_25	Navigator second hi interrupt
180	QMSS_INTD_2_HIGH_26	Navigator second hi interrupt
181	QMSS_INTD_2_HIGH_27	Navigator second hi interrupt

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Table 4-25 CIC2 Event Inputs (Secondary Events for EDMA3CC0 and HyperLinks) (Part 6 of 12)

Event No.	Event Name	Description
182	QMSS_INTD_2_HIGH_28	Navigator second hi interrupt
183	QMSS_INTD_2_HIGH_29	Navigator second hi interrupt
184	QMSS_INTD_2_HIGH_30	Navigator second hi interrupt
185	QMSS_INTD_2_HIGH_31	Navigator second hi interrupt
186	MPU_12_INT	MPU12 addressing violation interrupt and protection violation interrupt
187	MPU_13_INT	MPU13 addressing violation interrupt and protection violation interrupt
188	MPU_14_INT	MPU14 addressing violation interrupt and protection violation interrupt
189	Reserved	Reserved
190	Reserved	Reserved
191	Reserved	Reserved
192	Reserved	Reserved
193	Reserved	Reserved
194	Reserved	Reserved
195	Reserved	Reserved
196	Reserved	Reserved
197	Reserved	Reserved
198	Reserved	Reserved
199	TRACER_QMSS_QM_CFG2_INT	Tracer sliding time window interrupt for Navigator CFG2 slave port
200	TRACER_EDMACC_0	Tracer sliding time window interrupt foR EDMA3CC0
201	TRACER_EDMACC_123_INT	Tracer sliding time window interrupt for EDMA3CC1, EDMA3CC2 and EDMA3CC3
202	TRACER_CIC_INT	Tracer sliding time window interrupt for interrupt controllers (CIC)
203	MPU_4_INT	MPU4 addressing violation interrupt and protection violation interrupt
204	MPU_5_INT	MPU5 addressing violation interrupt and protection violation interrupt
205	MPU_6_INT	MPU6 addressing violation interrupt and protection violation interrupt
206	MPU_7_INT	MPU7 addressing violation interrupt and protection violation interrupt
207	MPU_8_INT	MPU8 addressing violation interrupt and protection violation interrupt
208	QMSS_INTD_2_PKTDMA_0	Navigator ECC error interrupt
209	QMSS_INTD_2_PKTDMA_1	Navigator ECC error interrupt
210	SR_0_VPSMPSACK	SmartReflex VPVOLTUPDATE asserted and SMPS has acknowledged in a defined time interval
211	DDR3_0_ERR	DDR3A error interrupt
212	HYPERLINK_0_INT	HyperLink 0 interrupt
213	EDMACC_0_ERRINT	EDMA3CC0 error interrupt
214	EDMACC_0_MPINT	EDMA3CC0 memory protection interrupt
215	EDMACC_0_TC_0_ERRINT	EDMA3CC0 TPTC0 error interrupt
216	EDMACC_0_TC_1_ERRINT	EDMA3CC0 TPTC1 error interrupt
217	EDMACC_1_ERRINT	EDMA3CC1 error interrupt
218	EDMACC_1_MPINT	EDMA3CC1 memory protection interrupt
219	EDMACC_1_TC_0_ERRINT	EDMA3CC1 TPTC0 error interrupt
220	EDMACC_1_TC_1_ERRINT	EDMA3CC1 TPTC1 error interrupt
221	EDMACC_1_TC_2_ERRINT	EDMA3CC1 TPTC2 error interrupt
222	EDMACC_1_TC_3_ERRINT	EDMA3CC1 TPTC3 error interrupt
223	EDMACC_2_ERRINT	EDMA3CC2 error interrupt
224	EDMACC_2_MPINT	EDMA3CC2 memory protection interrupt
225	EDMACC_2_TC_0_ERRINT	EDMA3CC2 TPTC0 error interrupt

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Table 4-25 CIC2 Event Inputs (Secondary Events for EDMA3CC0 and HyperLinks) (Part 7 of 12)

Event No.	Event Name	Description
226	EDMACC_2_TC_1_ERRINT	EDMA3CC2 TPTC1 error interrupt
227	EDMACC_2_TC_2_ERRINT	EDMA3CC2 TPTC2 error interrupt
228	EDMACC_2_TC_3_ERRINT	EDMA3CC2 TPTC3 error interrupt
229	EDMACC_3_ERRINT	EDMA3CC3 error interrupt
230	EDMACC_3_MPINT	EDMA3CC3 memory protection interrupt
231	EDMACC_3_TC_0_ERRINT	EDMA3CC3 TPTC0 error interrupt
232	EDMACC_3_TC_1_ERRINT	EDMA3CC3 TPTC1 error interrupt
233	EDMACC_4_ERRINT	EDMA3CC4 error interrupt
234	EDMACC_4_MPINT	EDMA3CC4 memory protection interrupt
235	EDMACC_4_TC_0_ERRINT	EDMA3CC4 TPTC0 error interrupt
236	EDMACC_4_TC_1_ERRINT	EDMA3CC4 TPTC1 error interrupt
237	QMSS_QUE_PEND_652	Navigator transmit queue pending event for indicated queue
238	QMSS_QUE_PEND_653	Navigator transmit queue pending event for indicated queue
239	QMSS_QUE_PEND_654	Navigator transmit queue pending event for indicated queue
240	QMSS_QUE_PEND_655	Navigator transmit queue pending event for indicated queue
241	QMSS_QUE_PEND_656	Navigator transmit queue pending event for indicated queue
242	QMSS_QUE_PEND_657	Navigator transmit queue pending event for indicated queue
243	QMSS_QUE_PEND_658	Navigator transmit queue pending event for indicated queue
244	QMSS_QUE_PEND_659	Navigator transmit queue pending event for indicated queue
245	QMSS_QUE_PEND_660	Navigator transmit queue pending event for indicated queue
246	QMSS_QUE_PEND_661	Navigator transmit queue pending event for indicated queue
247	QMSS_QUE_PEND_662	Navigator transmit queue pending event for indicated queue
248	QMSS_QUE_PEND_663	Navigator transmit queue pending event for indicated queue
249	QMSS_QUE_PEND_664	Navigator transmit queue pending event for indicated queue
250	QMSS_QUE_PEND_665	Navigator transmit queue pending event for indicated queue
251	QMSS_QUE_PEND_666	Navigator transmit queue pending event for indicated queue
252	QMSS_QUE_PEND_667	Navigator transmit queue pending event for indicated queue
253	QMSS_QUE_PEND_668	Navigator transmit queue pending event for indicated queue
254	QMSS_QUE_PEND_669	Navigator transmit queue pending event for indicated queue
255	QMSS_QUE_PEND_670	Navigator transmit queue pending event for indicated queue
256	QMSS_QUE_PEND_671	Navigator transmit queue pending event for indicated queue
257	QMSS_QUE_PEND_8844	Navigator transmit queue pending event for indicated queue
258	QMSS_QUE_PEND_8845	Navigator transmit queue pending event for indicated queue
259	QMSS_QUE_PEND_8846	Navigator transmit queue pending event for indicated queue
260	QMSS_QUE_PEND_8847	Navigator transmit queue pending event for indicated queue
261	QMSS_QUE_PEND_8848	Navigator transmit queue pending event for indicated queue
262	QMSS_QUE_PEND_8849	Navigator transmit queue pending event for indicated queue
263	QMSS_QUE_PEND_8850	Navigator transmit queue pending event for indicated queue
264	QMSS_QUE_PEND_8851	Navigator transmit queue pending event for indicated queue
265	QMSS_QUE_PEND_8852	Navigator transmit queue pending event for indicated queue
266	QMSS_QUE_PEND_8853	Navigator transmit queue pending event for indicated queue
267	QMSS_QUE_PEND_8854	Navigator transmit queue pending event for indicated queue
268	QMSS_QUE_PEND_8855	Navigator transmit queue pending event for indicated queue
269	QMSS_QUE_PEND_8856	Navigator transmit queue pending event for indicated queue

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Table 4-25 CIC2 Event Inputs (Secondary Events for EDMA3CC0 and HyperLinks) (Part 8 of 12)

Event No.	Event Name	Description
270	QMSS_QUE_PEND_8857	Navigator transmit queue pending event for indicated queue
271	QMSS_QUE_PEND_8858	Navigator transmit queue pending event for indicated queue
272	QMSS_QUE_PEND_8859	Navigator transmit queue pending event for indicated queue
273	QMSS_QUE_PEND_8860	Navigator transmit queue pending event for indicated queue
274	QMSS_QUE_PEND_8861	Navigator transmit queue pending event for indicated queue
275	QMSS_QUE_PEND_8862	Navigator transmit queue pending event for indicated queue
276	QMSS_QUE_PEND_8863	Navigator transmit queue pending event for indicated queue
277	10GbE_LINK_INT0	10 Gigabit Ethernet subsystem MDIO interrupt
278	10GbE_LINK_INT1	10 Gigabit Ethernet subsystem MDIO interrupt
279	10GbE_USER_INT0	10 Gigabit Ethernet subsystem MDIO interrupt
280	10GbE_USER_INT1	10 Gigabit Ethernet subsystem MDIO interrupt
281	10GbE_MISC_INT	10 Gigabit Ethernet subsystem MDIO interrupt
282	10GbE_INT_PKTDMA_0	10 Gigabit Ethernet Packet DMA starvation interrupt
283	SEM_INT0	Semaphore interrupt
284	SEM_INT1	Semaphore interrupt
285	SEM_INT2	Semaphore interrupt
286	SEM_INT3	Semaphore interrupt
287	SEM_INT4	Semaphore interrupt
288	SEM_INT5	Semaphore interrupt
289	SEM_INT6	Semaphore interrupt
290	SEM_INT7	Semaphore interrupt
291	SEM_INT8	Semaphore interrupt
292	SEM_INT9	Semaphore interrupt
293	SEM_INT10	Semaphore interrupt
294	SEM_INT11	Semaphore interrupt
295	SEM_INT12	Semaphore interrupt
296	SEM_INT13	Semaphore interrupt
297	SEM_INT14	Semaphore interrupt
298	SEM_INT15	Semaphore interrupt
299	SEM_ERR8	Semaphore error interrupt
300	SEM_ERR9	Semaphore error interrupt
301	SEM_ERR10	Semaphore error interrupt
302	SEM_ERR11	Semaphore error interrupt
303	SEM_ERR12	Semaphore error interrupt
304	SEM_ERR13	Semaphore error interrupt
305	SEM_ERR14	Semaphore error interrupt
306	SEM_ERR15	Semaphore error interrupt
307	DDR3_1_ERR	DDR3B error interrupt
308	HYPERLINK_1_INT	HyperLink 1 interrupt
309	FFTC_0_INT0	FFTC interrupt
310	FFTC_0_INT1	FFTC interrupt
311	FFTC_0_INT2	FFTC interrupt
312	FFTC_0_INT3	FFTC interrupt
313	FFTC_1_INT0	FFTC interrupt

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Table 4-25 CIC2 Event Inputs (Secondary Events for EDMA3CC0 and HyperLinks) (Part 9 of 12)

Event No.	Event Name	Description
314	FFTC_1_INT1	FFTC interrupt
315	FFTC_1_INT2	FFTC interrupt
316	FFTC_1_INT3	FFTC interrupt
317	FFTC_2_INT0	FFTC interrupt
318	FFTC_2_INT1	FFTC interrupt
319	FFTC_2_INT2	FFTC interrupt
320	FFTC_2_INT3	FFTC interrupt
321	FFTC_3_INT0	FFTC interrupt
322	FFTC_3_INT1	FFTC interrupt
323	FFTC_3_INT2	FFTC interrupt
324	FFTC_3_INT3	FFTC interrupt
325	FFTC_4_INT0	FFTC interrupt
326	FFTC_4_INT1	FFTC interrupt
327	FFTC_4_INT2	FFTC interrupt
328	FFTC_4_INT3	FFTC interrupt
329	FFTC_5_INT0	FFTC interrupt
330	FFTC_5_INT1	FFTC interrupt
331	FFTC_5_INT2	FFTC interrupt
332	FFTC_5_INT3	FFTC interrupt
333	AIF_INT	AIF interrupt
334	AIF_ATEVT0	AIF timer event
335	AIF_ATEVT1	AIF timer event
336	AIF_ATEVT2	AIF timer event
337	AIF_ATEVT3	AIF timer event
338	AIF_ATEVT4	AIF timer event
339	AIF_ATEVT5	AIF timer event
340	AIF_ATEVT6	AIF timer event
341	AIF_ATEVT7	AIF timer event
342	AIF_ATEVT8	AIF timer event
343	AIF_ATEVT9	AIF timer event
344	AIF_ATEVT10	AIF timer event
345	AIF_ATEVT11	AIF timer event
346	AIF_ATEVT12	AIF timer event
347	AIF_ATEVT13	AIF timer event
348	AIF_ATEVT14	AIF timer event
349	AIF_ATEVT15	AIF timer event
350	Reserved	Reserved
351	Reserved	Reserved
352	Reserved	Reserved
353	Reserved	Reserved
354	TCP3D_0_INT	TCP3d interrupt
355	TCP3D_1_INT	TCP3d interrupt
356	TCP3D_2_INT	TCP3d interrupt
357	TCP3D_3_INT	TCP3d interrupt

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Table 4-25 CIC2 Event Inputs (Secondary Events for EDMA3CC0 and HyperLinks) (Part 10 of 12)

Event No.	Event Name	Description
358	BCP_INT0	BCP interrupt
359	BCP_INT1	BCP interrupt
360	BCP_INT2	BCP interrupt
361	BCP_INT3	BCP interrupt
362	PSC_ALLINT	PSC interrupt
363	Reserved	Reserved
364	RAC_0_TRACE_GCCP0	RAC trace
365	RAC_0_TRACE_GCCP1	RAC trace
366	RAC_1_TRACE_GCCP0	RAC trace
367	RAC_1_TRACE_GCCP1	RAC trace
368	RAC_2_TRACE_GCCP0	RAC trace
369	RAC_2_TRACE_GCCP1	RAC trace
370	RAC_3_TRACE_GCCP0	RAC trace
371	RAC_3_TRACE_GCCP1	RAC trace
372	MPU_9_INT	MPU9 addressing violation interrupt and protection violation interrupt
373	MPU_10_INT	MPU10 addressing violation interrupt and protection violation interrupt
374	MPU_11_INT	MPU11 addressing violation interrupt and protection violation interrupt
375	TRACER_MSMC_4_INT	Tracer sliding time window interrupt for MSMC SRAM Bank 4
376	TRACER_MSMC_5_INT	Tracer sliding time window interrupt for MSMC SRAM Bank 4
377	TRACER_MSMC_6_INT	Tracer sliding time window interrupt for MSMC SRAM Bank 4
378	TRACER_MSMC_7_INT	Tracer sliding time window interrupt for MSMC SRAM Bank 4
379	TRACER_DDR_1_INT	Tracer sliding time window interrupt for DDR3B
380	TRACER_BCR_INT	Tracer sliding time window interrupt for BCR
381	TRACER_RAC_1_INT	Tracer sliding time window interrupt for RAC
382	TRACER_RAC_2_INT	Tracer sliding time window interrupt for RAC
383	TRACER_RAC_FE_INT	Tracer sliding time window interrupt for RAC
384	TRACER_SPI_ROM_EMIF_INT	Tracer sliding time window interrupt for SPI/ROM/EMIF16 modules
385	TRACER_TAC_BE_INT	Tracer sliding time window interrupt for TAC
386	Reserved	Reserved
387	TIMER_8_INTL	Timer interrupt low
388	TIMER_8_INTH	Timer interrupt high
389	TIMER_9_INTL	Timer interrupt low
390	TIMER_9_INTH	Timer interrupt high
391	TIMER_10_INTL	Timer interrupt low
392	TIMER_10_INTH	Timer interrupt high
393	TIMER_11_INTL	Timer interrupt low
394	TIMER_11_INTH	Timer interrupt high
395	TIMER_14_INTL	Timer interrupt low
396	TIMER_14_INTH	Timer interrupt high
397	TIMER_15_INTL	Timer interrupt low
398	TIMER_15_INTH	Timer interrupt high
399	USB_INT00	USB interrupt
400	USB_INT04	USB interrupt
401	USB_INT05	USB interrupt

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Table 4-25 CIC2 Event Inputs (Secondary Events for EDMA3CC0 and HyperLinks) (Part 11 of 12)

Event No.	Event Name	Description
402	USB_INT06	USB interrupt
403	USB_INT07	USB interrupt
404	USB_INT08	USB interrupt
405	USB_INT09	USB interrupt
406	USB_INT10	USB interrupt
407	USB_INT11	USB interrupt
408	USB_MISCINT	USB miscellaneous interrupt
409	USB_OABSINT	USB OABS interrupt
410	TCP3D_0_REVT0	TCP3d interrupt
411	TCP3D_0_REVT1	TCP3d interrupt
412	TCP3D_1_REVT0	TCP3d interrupt
413	TCP3D_1_REVT1	TCP3d interrupt
414	TCP3D_2_REVT0	TCP3d interrupt
415	TCP3D_2_REVT1	TCP3d interrupt
416	TCP3D_3_REVT0	TCP3d interrupt
417	TCP3D_3_REVT1	TCP3d interrupt
418	VCP_0_INT0	VCP interrupt
419	VCP_0_INT1	VCP interrupt
420	VCP_0_INT2	VCP interrupt
421	VCP_0_INT3	VCP interrupt
422	VCP_1_INT0	VCP interrupt
423	VCP_1_INT1	VCP interrupt
424	VCP_1_INT2	VCP interrupt
425	VCP_1_INT3	VCP interrupt
426	VCP_0_REVT0	VCP interrupt
427	VCP_0_XEVT0	VCP interrupt
428	VCP_0_REVT1	VCP interrupt
429	VCP_0_XEVT1	VCP interrupt
430	VCP_0_REVT2	VCP interrupt
431	VCP_0_XEVT2	VCP interrupt
432	VCP_0_REVT3	VCP interrupt
433	VCP_0_XEVT3	VCP interrupt
434	VCP_1_REVT0	VCP interrupt
435	VCP_1_XEVT0	VCP interrupt
436	VCP_1_REVT1	VCP interrupt
437	VCP_1_XEVT1	VCP interrupt
438	VCP_1_REVT2	VCP interrupt
439	VCP_1_XEVT2	VCP interrupt
440	VCP_1_REVT3	VCP interrupt
441	VCP_1_XEVT3	VCP interrupt
442	TETB_OVFLINT0	ETB0 overflow (emulation trace buffer)
443	TETB_UNFLINT0	ETB0 underflow
444	TETB_OVFLINT1	ETB1 overflow (emulation trace buffer)
445	TETB_UNFLINT1	ETB1 underflow

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Table 4-25 CIC2 Event Inputs (Secondary Events for EDMA3CC0 and HyperLinks) (Part 12 of 12)

Event No.	Event Name	Description
446	TETB_OVFLINT2	ETB2 overflow (emulation trace buffer)
447	TETB_UNFLINT2	ETB2 underflow
448	TETB_OVFLINT3	ETB3 overflow (emulation trace buffer)
449	TETB_UNFLINT3	ETB3 underflow
450	TETB_OVFLINT4	ETB4 overflow (emulation trace buffer)
451	TETB_UNFLINT4	ETB4 underflow
452	TETB_OVFLINT5	ETB5 overflow (emulation trace buffer)
453	TETB_UNFLINT5	ETB5 underflow
454	TETB_OVFLINT6	ETB6 overflow (emulation trace buffer)
455	TETB_UNFLINT6	ETB6 underflow
456	TETB_OVFLINT7	ETB7 overflow (emulation trace buffer)
457	TETB_UNFLINT7	ETB7 underflow
458	Reserved	Reserved
459	RAC_0_INT	RAC interrupt
460	RAC_1_INT	RAC interrupt
461	RAC_2_INT	RAC interrupt
462	RAC_3_INT	RAC interrupt
463	GPIO_INT0	GPIO interrupt
464	GPIO_INT1	GPIO interrupt
465	GPIO_INT2	GPIO interrupt
466	GPIO_INT3	GPIO interrupt
467	GPIO_INT4	GPIO interrupt
468	GPIO_INT5	GPIO interrupt
469	GPIO_INT6	GPIO interrupt
470	GPIO_INT7	GPIO interrupt
471	IPC_GR0	IPC interrupt generation
472	IPC_GR1	IPC interrupt generation
473	IPC_GR2	IPC interrupt generation
474	IPC_GR3	IPC interrupt generation
475	IPC_GR4	IPC interrupt generation
476	IPC_GR5	IPC interrupt generation
477	IPC_GR6	IPC interrupt generation
478	IPC_GR7	IPC interrupt generation
End of Table 4-25		

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4.3.2 CIC Registers

This section includes the CIC memory map information and registers.

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4.3.2.1 CIC0 Register Map

Table 4-26 CIC0 Registers (Part 1 of 3)

Address Offset	Register Mnemonic	Register Name
0x0	REVISION_REG	Revision Register
0x4	CONTROL_REG	Control Register
0xc	HOST_CONTROL_REG	Host Control Register
0x10	GLOBAL_ENABLE_HINT_REG	Global Host Int Enable Register
0x20	STATUS_SET_INDEX_REG	Status Set Index Register
0x24	STATUS_CLR_INDEX_REG	Status Clear Index Register
0x28	ENABLE_SET_INDEX_REG	Enable Set Index Register
0x2c	ENABLE_CLR_INDEX_REG	Enable Clear Index Register
0x34	HINT_ENABLE_SET_INDEX_REG	Host Int Enable Set Index Register
0x38	HINT_ENABLE_CLR_INDEX_REG	Host Int Enable Clear Index Register
0x200	RAW_STATUS_REG0	Raw Status Register 0
0x204	RAW_STATUS_REG1	Raw Status Register 1
0x208	RAW_STATUS_REG2	Raw Status Register 2
0x20c	RAW_STATUS_REG3	Raw Status Register 3
0x210	RAW_STATUS_REG4	Raw Status Register 4
0x214	RAW_STATUS_REG5	Raw Status Register 5
0x218	RAW_STATUS_REG6	Raw Status Register 6
0x280	ENA_STATUS_REG0	Enabled Status Register 0
0x284	ENA_STATUS_REG1	Enabled Status Register 1
0x288	ENA_STATUS_REG2	Enabled Status Register 2
0x28c	ENA_STATUS_REG3	Enabled Status Register 3
0x290	ENA_STATUS_REG4	Enabled Status Register 4
0x294	ENA_STATUS_REG5	Enabled Status Register 5
0x298	ENA_STATUS_REG6	Enabled Status Register 6
0x300	ENABLE_REG0	Enable Register 0
0x304	ENABLE_REG1	Enable Register 1
0x308	ENABLE_REG2	Enable Register 2
0x30c	ENABLE_REG3	Enable Register 3
0x310	ENABLE_REG4	Enable Register 4
0x314	ENABLE_REG5	Enable Register 5
0x318	ENABLE_REG6	Enable Register 6
0x380	ENABLE_CLR_REG0	Enable Clear Register 0
0x384	ENABLE_CLR_REG1	Enable Clear Register 1
0x388	ENABLE_CLR_REG2	Enable Clear Register 2
0x38c	ENABLE_CLR_REG3	Enable Clear Register 3
0x390	ENABLE_CLR_REG4	Enable Clear Register 4
0x394	ENABLE_CLR_REG5	Enable Clear Register 5
0x398	ENABLE_CLR_REG6	Enable Clear Register 6
0x400	CH_MAP_REG0	Interrupt Channel Map Register for 0 to 0+3
0x404	CH_MAP_REG1	Interrupt Channel Map Register for 4 to 4+3
0x408	CH_MAP_REG2	Interrupt Channel Map Register for 8 to 8+3
0x40c	CH_MAP_REG3	Interrupt Channel Map Register for 12 to 12+3

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Table 4-26 CIC0 Registers (Part 2 of 3)

Address Offset	Register Mnemonic	Register Name
0x410	CH_MAP_REG4	Interrupt Channel Map Register for 16 to 16+3
0x414	CH_MAP_REG5	Interrupt Channel Map Register for 20 to 20+3
0x418	CH_MAP_REG6	Interrupt Channel Map Register for 24 to 24+3
0x41c	CH_MAP_REG7	Interrupt Channel Map Register for 28 to 28+3
0x420	CH_MAP_REG8	Interrupt Channel Map Register for 32 to 32+3
0x424	CH_MAP_REG9	Interrupt Channel Map Register for 36 to 36+3
0x428	CH_MAP_REG10	Interrupt Channel Map Register for 40 to 40+3
0x42c	CH_MAP_REG11	Interrupt Channel Map Register for 44 to 44+3
0x430	CH_MAP_REG12	Interrupt Channel Map Register for 48 to 48+3
0x434	CH_MAP_REG13	Interrupt Channel Map Register for 52 to 52+3
0x438	CH_MAP_REG14	Interrupt Channel Map Register for 56 to 56+3
0x43c	CH_MAP_REG15	Interrupt Channel Map Register for 60 to 60+3
0x440	CH_MAP_REG16	Interrupt Channel Map Register for 64 to 64+3
0x444	CH_MAP_REG17	Interrupt Channel Map Register for 68 to 68+3
0x448	CH_MAP_REG18	Interrupt Channel Map Register for 72 to 72+3
0x44c	CH_MAP_REG19	Interrupt Channel Map Register for 76 to 76+3
0x450	CH_MAP_REG20	Interrupt Channel Map Register for 80 to 80+3
0x454	CH_MAP_REG21	Interrupt Channel Map Register for 84 to 84+3
0x458	CH_MAP_REG22	Interrupt Channel Map Register for 88 to 88+3
0x45c	CH_MAP_REG23	Interrupt Channel Map Register for 92 to 92+3
0x460	CH_MAP_REG24	Interrupt Channel Map Register for 96 to 96+3
0x464	CH_MAP_REG25	Interrupt Channel Map Register for 100 to 100+3
0x468	CH_MAP_REG26	Interrupt Channel Map Register for 104 to 104+3
0x46c	CH_MAP_REG27	Interrupt Channel Map Register for 108 to 108+3
0x470	CH_MAP_REG28	Interrupt Channel Map Register for 112 to 112+3
0x474	CH_MAP_REG29	Interrupt Channel Map Register for 116 to 116+3
0x478	CH_MAP_REG30	Interrupt Channel Map Register for 120 to 120+3
0x47c	CH_MAP_REG31	Interrupt Channel Map Register for 124 to 124+3
0x480	CH_MAP_REG32	Interrupt Channel Map Register for 128 to 128+3
0x484	CH_MAP_REG33	Interrupt Channel Map Register for 132 to 132+3
0x488	CH_MAP_REG34	Interrupt Channel Map Register for 136 to 136+3
0x48c	CH_MAP_REG35	Interrupt Channel Map Register for 140 to 140+3
0x490	CH_MAP_REG36	Interrupt Channel Map Register for 144 to 144+3
0x494	CH_MAP_REG37	Interrupt Channel Map Register for 148 to 148+3
0x498	CH_MAP_REG38	Interrupt Channel Map Register for 152 to 152+3
0x49c	CH_MAP_REG39	Interrupt Channel Map Register for 156 to 156+3
0x4a0	CH_MAP_REG40	Interrupt Channel Map Register for 160 to 160+3
0x4a4	CH_MAP_REG41	Interrupt Channel Map Register for 164 to 164+3
0x4a8	CH_MAP_REG42	Interrupt Channel Map Register for 168 to 168+3
0x4ac	CH_MAP_REG43	Interrupt Channel Map Register for 172 to 172+3
0x4b0	CH_MAP_REG44	Interrupt Channel Map Register for 176 to 176+3
0x4b4	CH_MAP_REG45	Interrupt Channel Map Register for 180 to 180+3
0x4b8	CH_MAP_REG46	Interrupt Channel Map Register for 184 to 184+3
0x4bc	CH_MAP_REG47	Interrupt Channel Map Register for 188 to 188+3

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Table 4-26 CIC0 Registers (Part 3 of 3)

Address Offset	Register Mnemonic	Register Name
0x4c0	CH_MAP_REG48	Interrupt Channel Map Register for 192 to 192+3
0x4c4	CH_MAP_REG49	Interrupt Channel Map Register for 196 to 196+3
0x4c8	CH_MAP_REG50	Interrupt Channel Map Register for 200 to 200+3
0x4cc	CH_MAP_REG51	Interrupt Channel Map Register for 204 to 204+3
0x800	HINT_MAP_REG0	Host Interrupt Map Register for 0 to 0+3
0x804	HINT_MAP_REG1	Host Interrupt Map Register for 4 to 4+3
0x808	HINT_MAP_REG2	Host Interrupt Map Register for 8 to 8+3
0x80c	HINT_MAP_REG3	Host Interrupt Map Register for 12 to 12+3
0x810	HINT_MAP_REG4	Host Interrupt Map Register for 16 to 16+3
0x814	HINT_MAP_REG5	Host Interrupt Map Register for 20 to 20+3
0x818	HINT_MAP_REG6	Host Interrupt Map Register for 24 to 24+3
0x81c	HINT_MAP_REG7	Host Interrupt Map Register for 28 to 28+3
0x820	HINT_MAP_REG8	Host Interrupt Map Register for 32 to 32+3
0x824	HINT_MAP_REG9	Host Interrupt Map Register for 36 to 36+3
0x828	HINT_MAP_REG10	Host Interrupt Map Register for 40 to 40+3
0x82c	HINT_MAP_REG11	Host Interrupt Map Register for 44 to 44+3
0x830	HINT_MAP_REG12	Host Interrupt Map Register for 48 to 48+3
0x834	HINT_MAP_REG13	Host Interrupt Map Register for 52 to 52+3
0x838	HINT_MAP_REG14	Host Interrupt Map Register for 56 to 56+3
0x83c	HINT_MAP_REG15	Host Interrupt Map Register for 60 to 60+3
0x840	HINT_MAP_REG16	Host Interrupt Map Register for 64 to 64+3
0x844	HINT_MAP_REG17	Host Interrupt Map Register for 68 to 68+3
0x848	HINT_MAP_REG18	Host Interrupt Map Register for 72 to 72+3
0x84c	HINT_MAP_REG19	Host Interrupt Map Register for 76 to 76+3
0x1500	ENABLE_HINT_REG0	Host Interrupt Enable Register 0
0x1504	ENABLE_HINT_REG1	Host Interrupt Enable Register 1
0x1508	ENABLE_HINT_REG2	Host Interrupt Enable Register 2
End of Table 4-26		

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4.3.2.2 CIC1 Register Map

Table 4-27 CIC1 Registers (Part 1 of 3)

Address Offset	Register Mnemonic	Register Name
0x0	REVISION_REG	Revision Register
0x10	GLOBAL_ENABLE_HINT_REG	Global Host Interrupt Enable Register
0x20	STATUS_SET_INDEX_REG	Status Set Index Register
0x24	STATUS_CLR_INDEX_REG	Status Clear Index Register
0x28	ENABLE_SET_INDEX_REG	Enable Set Index Register
0x2c	ENABLE_CLR_INDEX_REG	Enable Clear Index Register
0x34	HINT_ENABLE_SET_INDEX_REG	Host Interrupt Enable Set Index Register
0x38	HINT_ENABLE_CLR_INDEX_REG	Host Interrupt Enable Clear Index Register
0x200	RAW_STATUS_REG0	Raw Status Register 0
0x204	RAW_STATUS_REG1	Raw Status Register 1
0x208	RAW_STATUS_REG2	Raw Status Register 2

Table 4-27 CIC1 Registers (Part 2 of 3)

Address Offset	Register Mnemonic	Register Name
0x20c	RAW_STATUS_REG3	Raw Status Register 3
0x210	RAW_STATUS_REG4	Raw Status Register 4
0x280	ENA_STATUS_REG0	Enabled Status Register 0
0x284	ENA_STATUS_REG1	Enabled Status Register 1
0x288	ENA_STATUS_REG2	Enabled Status Register 2
0x28c	ENA_STATUS_REG3	Enabled Status Register 3
0x290	ENA_STATUS_REG4	Enabled Status Register 4
0x300	ENABLE_REG0	Enable Register 0
0x304	ENABLE_REG1	Enable Register 1
0x308	ENABLE_REG2	Enable Register 2
0x30c	ENABLE_REG3	Enable Register 3
0x310	ENABLE_REG4	Enable Register 4
0x380	ENABLE_CLR_REG0	Enable Clear Register 0
0x384	ENABLE_CLR_REG1	Enable Clear Register 1
0x388	ENABLE_CLR_REG2	Enable Clear Register 2
0x38c	ENABLE_CLR_REG3	Enable Clear Register 3
0x390	ENABLE_CLR_REG4	Enable Clear Register 4
0x400	CH_MAP_REG0	Interrupt Channel Map Register for 0 to 0+3
0x404	CH_MAP_REG1	Interrupt Channel Map Register for 4 to 4+3
0x408	CH_MAP_REG2	Interrupt Channel Map Register for 8 to 8+3
0x40c	CH_MAP_REG3	Interrupt Channel Map Register for 12 to 12+3
0x410	CH_MAP_REG4	Interrupt Channel Map Register for 16 to 16+3
0x414	CH_MAP_REG5	Interrupt Channel Map Register for 20 to 20+3
0x418	CH_MAP_REG6	Interrupt Channel Map Register for 24 to 24+3
0x41c	CH_MAP_REG7	Interrupt Channel Map Register for 28 to 28+3
0x420	CH_MAP_REG8	Interrupt Channel Map Register for 32 to 32+3
0x424	CH_MAP_REG9	Interrupt Channel Map Register for 36 to 36+3
0x428	CH_MAP_REG10	Interrupt Channel Map Register for 40 to 40+3
0x42c	CH_MAP_REG11	Interrupt Channel Map Register for 44 to 44+3
0x430	CH_MAP_REG12	Interrupt Channel Map Register for 48 to 48+3
0x434	CH_MAP_REG13	Interrupt Channel Map Register for 52 to 52+3
0x438	CH_MAP_REG14	Interrupt Channel Map Register for 56 to 56+3
0x43c	CH_MAP_REG15	Interrupt Channel Map Register for 60 to 60+3
0x440	CH_MAP_REG16	Interrupt Channel Map Register for 64 to 64+3
0x444	CH_MAP_REG17	Interrupt Channel Map Register for 68 to 68+3
0x448	CH_MAP_REG18	Interrupt Channel Map Register for 72 to 72+3
0x44c	CH_MAP_REG19	Interrupt Channel Map Register for 76 to 76+3
0x450	CH_MAP_REG20	Interrupt Channel Map Register for 80 to 80+3
0x454	CH_MAP_REG21	Interrupt Channel Map Register for 84 to 84+3
0x458	CH_MAP_REG22	Interrupt Channel Map Register for 88 to 88+3
0x45c	CH_MAP_REG23	Interrupt Channel Map Register for 92 to 92+3
0x460	CH_MAP_REG24	Interrupt Channel Map Register for 96 to 96+3
0x464	CH_MAP_REG25	Interrupt Channel Map Register for 100 to 100+3
0x468	CH_MAP_REG26	Interrupt Channel Map Register for 104 to 104+3

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Table 4-27 CIC1 Registers (Part 3 of 3)

Address Offset	Register Mnemonic	Register Name
0x46c	CH_MAP_REG27	Interrupt Channel Map Register for 108 to 108+3
0x470	CH_MAP_REG28	Interrupt Channel Map Register for 112 to 112+3
0x474	CH_MAP_REG29	Interrupt Channel Map Register for 116 to 116+3
0x478	CH_MAP_REG30	Interrupt Channel Map Register for 120 to 120+3
0x47c	CH_MAP_REG31	Interrupt Channel Map Register for 124 to 124+3
0x480	CH_MAP_REG32	Interrupt Channel Map Register for 128 to 128+3
0x484	CH_MAP_REG33	Interrupt Channel Map Register for 132 to 132+3
0x488	CH_MAP_REG34	Interrupt Channel Map Register for 136 to 136+3
0x48c	CH_MAP_REG35	Interrupt Channel Map Register for 140 to 140+3
0x490	CH_MAP_REG36	Interrupt Channel Map Register for 144 to 144+3
0x494	CH_MAP_REG37	Interrupt Channel Map Register for 148 to 148+3
0x498	CH_MAP_REG38	Interrupt Channel Map Register for 152 to 152+3
0x49c	CH_MAP_REG39	Interrupt Channel Map Register for 156 to 156+3
0x800	HINT_MAP_REG0	Host Interrupt Map Register for 0 to 0+3
0x804	HINT_MAP_REG1	Host Interrupt Map Register for 4 to 4+3
0x808	HINT_MAP_REG2	Host Interrupt Map Register for 8 to 8+3
0x80c	HINT_MAP_REG3	Host Interrupt Map Register for 12 to 12+3
0x810	HINT_MAP_REG4	Host Interrupt Map Register for 16 to 16+3
0x814	HINT_MAP_REG5	Host Interrupt Map Register for 20 to 20+3
0x818	HINT_MAP_REG6	Host Interrupt Map Register for 24 to 24+3
0x81c	HINT_MAP_REG7	Host Interrupt Map Register for 28 to 28+3
0x820	HINT_MAP_REG8	Host Interrupt Map Register for 32 to 32+3
0x824	HINT_MAP_REG9	Host Interrupt Map Register for 36 to 36+3
0x828	HINT_MAP_REG10	Host Interrupt Map Register for 40 to 40+3
0x82c	HINT_MAP_REG11	Host Interrupt Map Register for 44 to 44+3
0x830	HINT_MAP_REG12	Host Interrupt Map Register for 48 to 48+3
0x834	HINT_MAP_REG13	Host Interrupt Map Register for 52 to 52+3
0x1500	ENABLE_HINT_REG0	Host Interrupt Enable Register 0
0x1504	ENABLE_HINT_REG1	Host Interrupt Enable Register 1
End of Table 4-27		

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4.3.2.3 CIC2 Register Map

Table 4-28 CIC2 Registers (Part 1 of 2)

Address Offset	Register Mnemonic	Register Name
0x0	REVISION_REG	Revision Register
0x10	GLOBAL_ENABLE_HINT_REG	Global Host Interrupt Enable Register
0x20	STATUS_SET_INDEX_REG	Status Set Index Register
0x24	STATUS_CLR_INDEX_REG	Status Clear Index Register
0x28	ENABLE_SET_INDEX_REG	Enable Set Index Register
0x2c	ENABLE_CLR_INDEX_REG	Enable Clear Index Register
0x34	HINT_ENABLE_SET_INDEX_REG	Host Interrupt Enable Set Index Register
0x38	HINT_ENABLE_CLR_INDEX_REG	Host Interrupt Enable Clear Index Register
0x200	RAW_STATUS_REG0	Raw Status Register 0

Table 4-28 CIC2 Registers (Part 2 of 2)

Address Offset	Register Mnemonic	Register Name
0x204	RAW_STATUS_REG1	Raw Status Register 1
0x280	ENA_STATUS_REG0	Enabled Status Register 0
0x284	ENA_STATUS_REG1	Enabled Status Register 1
0x300	ENABLE_REG0	Enable Register 0
0x304	ENABLE_REG1	Enable Register 1
0x380	ENABLE_CLR_REG0	Enable Clear Register 0
0x384	ENABLE_CLR_REG1	Enable Clear Register 1
0x400	CH_MAP_REG0	Interrupt Channel Map Register for 0 to 0+3
0x404	CH_MAP_REG1	Interrupt Channel Map Register for 4 to 4+3
0x408	CH_MAP_REG2	Interrupt Channel Map Register for 8 to 8+3
0x40c	CH_MAP_REG3	Interrupt Channel Map Register for 12 to 12+3
0x410	CH_MAP_REG4	Interrupt Channel Map Register for 16 to 16+3
0x414	CH_MAP_REG5	Interrupt Channel Map Register for 20 to 20+3
0x418	CH_MAP_REG6	Interrupt Channel Map Register for 24 to 24+3
0x41c	CH_MAP_REG7	Interrupt Channel Map Register for 28 to 28+3
0x420	CH_MAP_REG8	Interrupt Channel Map Register for 32 to 32+3
0x424	CH_MAP_REG9	Interrupt Channel Map Register for 36 to 36+3
0x428	CH_MAP_REG10	Interrupt Channel Map Register for 40 to 40+3
0x42c	CH_MAP_REG11	Interrupt Channel Map Register for 44 to 44+3
0x430	CH_MAP_REG12	Interrupt Channel Map Register for 48 to 48+3
0x434	CH_MAP_REG13	Interrupt Channel Map Register for 52 to 52+3
0x438	CH_MAP_REG14	Interrupt Channel Map Register for 56 to 56+3
0x43c	CH_MAP_REG15	Interrupt Channel Map Register for 60 to 60+3
0x800	HINT_MAP_REG0	Host Interrupt Map Register for 0 to 0+3
0x804	HINT_MAP_REG1	Host Interrupt Map Register for 4 to 4+3
0x808	HINT_MAP_REG2	Host Interrupt Map Register for 8 to 8+3
0x80c	HINT_MAP_REG3	Host Interrupt Map Register for 12 to 12+3
0x810	HINT_MAP_REG4	Host Interrupt Map Register for 16 to 16+3
0x814	HINT_MAP_REG5	Host Interrupt Map Register for 20 to 20+3
0x818	HINT_MAP_REG6	Host Interrupt Map Register for 24 to 24+3
0x81c	HINT_MAP_REG7	Host Interrupt Map Register for 28 to 28+3
0x820	HINT_MAP_REG8	Host Interrupt Map Register for 32 to 32+3
0x824	HINT_MAP_REG9	Host Interrupt Map Register for 36 to 36+3
0x828	HINT_MAP_REG10	Host Interrupt Map Register for 40 to 40+3
0x1500	ENABLE_HINT_REG0	Host Interrupt Enable Register 0
0x1504	ENABLE_HINT_REG1	Host Interrupt Enable Register 1
End of Table 4-28		

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4.3.3 Inter-Processor Register Map

Table 4-29 IPC Generation Registers (IPCGRx)

Address Start	Address End	Size	Register Name	Description
0x02620200	0x02620203	4B	NMIGR0	NMI Event Generation Register for C66x CorePac0
0x02620204	0x02620207	4B	NMIGR1	NMI Event Generation Register for C66x CorePac1
0x02620208	0x0262020B	4B	NMIGR2	NMI Event Generation Register for C66x CorePac2
0x0262020C	0x0262020F	4B	NMIGR3	NMI Event Generation Register for C66x CorePac3
0x02620210	0x02620213	4B	NMIGR4	NMI Event Generation Register for C66x CorePac4
0x02620214	0x02620217	4B	NMIGR5	NMI Event Generation Register for C66x CorePac5
0x02620218	0x0262021B	4B	NMIGR6	NMI Event Generation Register for C66x CorePac6
0x0262021C	0x0262021F	4B	NMIGR7	NMI Event Generation Register for C66x CorePac7
0x02620220	0x0262023F	32B	Reserved	Reserved
0x02620240	0x02620243	4B	IPCGR0	IPC Generation Register for C66x CorePac0
0x02620244	0x02620247	4B	IPCGR1	IPC Generation Register for C66x CorePac1
0x02620248	0x0262024B	4B	IPCGR2	IPC Generation Register for C66x CorePac2
0x0262024C	0x0262024F	4B	IPCGR3	IPC Generation Register for C66x CorePac3
0x02620250	0x02620253	4B	IPCGR4	IPC Generation Register for C66x CorePac4
0x02620254	0x02620257	4B	IPCGR5	IPC Generation Register for C66x CorePac5
0x02620258	0x0262025B	4B	IPCGR6	IPC Generation Register for C66x CorePac6
0x0262025C	0x0262025F	4B	IPCGR7	IPC Generation Register for C66x CorePac7
0x02620260	0x02620263	4B	IPCGR8	Reserved
0x02620264	0x02620267	4B	IPCGR9	Reserved
0x02620268	0x0262026B	4B	IPCGR10	Reserved
0x0262026C	0x0262026F	4B	IPCGR11	Reserved
0x02620270	0x0262027B	12B	Reserved	Reserved
0x0262027C	0x0262027F	4B	IPCGRH	IPC Generation Register for Host
0x02620280	0x02620283	4B	IPCAR0	IPC Acknowledgement Register for C66x CorePac0
0x02620284	0x02620287	4B	IPCAR1	IPC Acknowledgement Register for C66x CorePac1
0x02620288	0x0262028B	4B	IPCAR2	IPC Acknowledgement Register for C66x CorePac2
0x0262028C	0x0262028F	4B	IPCAR3	IPC Acknowledgement Register for C66x CorePac3
0x02620290	0x02620293	4B	IPCAR4	IPC Acknowledgement Register for C66x CorePac4
0x02620294	0x02620297	4B	IPCAR5	IPC Acknowledgement Register for C66x CorePac5
0x02620298	0x0262029B	4B	IPCAR6	IPC Acknowledgement Register for C66x CorePac6
0x0262029C	0x0262029F	4B	IPCAR7	IPC Acknowledgement Register for C66x CorePac7
0x026202A0	0x026202A3	4B	IPCAR8	Reserved
0x026202A4	0x026202A7	4B	IPCAR9	Reserved
0x026202A8	0x026202AB	4B	IPCAR10	Reserved
0x026202AC	0x026202AF	4B	IPCAR11	Reserved
0x026202B0	0x026202BB	12B	Reserved	Reserved
0x026202A0	0x026202BB	28B	Reserved	Reserved
0x026202BC	0x026202BF	4B	IPCARH	IPC Acknowledgement Register for host
End of Table 4-29				

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4.3.4 NMI and LRESET

The Non-Maskable Interrupts (NMI) can be generated by chip-level registers and the LRESET can be generated by software writing into LPSC registers. LRESET and NMI can also be asserted by device pins or watchdog timers. One NMI pin and one LRESET pin are shared by all eight C66x CorePacs on the device. The CORESEL[3:0] pins can be configured to select between the eight C66x CorePacs available as shown in Table 4-30.

Table 4-30 LRESET and NMI Decoding

CORESEL[3:0] Pin Input	LRESET Pin Input	NMI Pin Input	LRESETNMIEN Pin Input	Reset Mux Block Output
XXXX	X	X	1	No local reset or NMI assertion
0000	0	X	0	Assert local reset to C66x CorePac0
0001	0	X	0	Assert local reset to C66x CorePac1
0010	0	X	0	Assert local reset to C66x CorePac2
0011	0	X	0	Assert local reset to C66x CorePac3
0100	0	X	0	Assert local reset to C66x CorePac4
0101	0	X	0	Assert local reset to C66x CorePac5
0110	0	X	0	Assert local reset to C66x CorePac6
0111	0	X	0	Assert local reset to C66x CorePac7
1XXX	0	X	0	Assert local reset to all C66x CorePacs
0000	1	1	0	De-assert local reset & NMI to C66x CorePac0
0001	1	1	0	De-assert local reset & NMI to C66x CorePac1
0010	1	1	0	De-assert local reset & NMI to C66x CorePac2
0011	1	1	0	De-assert local reset & NMI to C66x CorePac3
0100	1	1	0	De-assert local reset & NMI to C66x CorePac4
0101	1	1	0	De-assert local reset & NMI to C66x CorePac5
0110	1	1	0	De-assert local reset & NMI to C66x CorePac6
0111	1	1	0	De-assert local reset & NMI to C66x CorePac7
1XXX	1	1	0	De-assert local reset & NMI to all C66x CorePacs
0000	1	0	0	Assert NMI to C66x CorePac0
0001	1	0	0	Assert NMI to C66x CorePac1
0010	1	0	0	Assert NMI to C66x CorePac2
0011	1	0	0	Assert NMI to C66x CorePac3
0100	1	0	0	Assert NMI to C66x CorePac4
0101	1	0	0	Assert NMI to C66x CorePac5
0110	1	0	0	Assert NMI to C66x CorePac6
0111	1	0	0	Assert NMI to C66x CorePac7
1XXX	1	0	0	Assert NMI to all C66x CorePacs
End of Table 4-30				

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4.4 Enhanced Direct Memory Access (EDMA3) Controller for TCI6634K2K

The primary purpose of the EDMA3 is to service user-programmed data transfers between two memory-mapped slave endpoints on the device. The EDMA3 services software-driven paging transfers (e.g., data movement between external memory and internal memory), performs sorting or subframe extraction of various data structures, services event driven peripherals, and offloads data transfers from the device C66x DSP CorePac.

There are 5 EDMA channel controllers on the device:

- EDMA3CC0 has two transfer controllers: TPTC0 and TPTC1.
- EDMA3CC1 has four transfer controllers: TPTC0, TPTC1, TPTC2, and TPTC3.
- EDMA3CC2 has four transfer controllers: TPTC0, TPTC1, TPTC2, and TPTC3.
- EDMA3CC3 has two transfer controllers: TPTC0 and TPTC1.
- EDMA3CC4 has two transfer controllers: TPTC0 and TPTC1.

In the context of this document, TPTCx is associated with EDMA3CCy, and is referred to as EDMA3CCy TPTCx. Each of the transfer controllers has a direct connection to the switch fabric. Section 6.2 "Switch Fabric Connections Matrix" on page 180 lists the peripherals that can be accessed by the transfer controllers.

EDMA3CC0 is optimized to be used for transfers to/from/within the MSMC and DDR3A/DDR3B subsytems. The others are used for the remaining traffic.

Each EDMA3 channel controller includes the following features:

- Fully orthogonal transfer description
  - 3 transfer dimensions:
    - Array (multiple bytes)
    - Frame (multiple arrays)
    - Block (multiple frames)
  - Single event can trigger transfer of array, frame, or entire block
  - Independent indexes on source and destination
- Flexible transfer definition:
  - Increment or FIFO transfer addressing modes
  - Linking mechanism allows for ping-pong buffering, circular buffering, and repetitive/continuous transfers, all with no CPU intervention
  - Chaining allows multiple transfers to execute with one event
- 512 PaRAM entries for all EDMA3CC
  - Used to define transfer context for channels
  - Each PaRAM entry can be used as a DMA entry, QDMA entry, or link entry
- 64 DMA channels for all EDMA3CC
  - Manually triggered (CPU writes to channel controller register)
  - External event triggered
  - Chain triggered (completion of one transfer triggers another)
- 8 Quick DMA (QDMA) channels per EDMA3CCx
  - Used for software-driven transfers
  - Triggered upon writing to a single PaRAM set entry
- Two transfer controllers and two event queues with programmable system-level priority for EDMA3CC0, EDMA3CC3 and EDMA3CC4, four transfer controllers and four event queues with programmable system-level priority for each of EDMA3CC1 and EDMA3CC2

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- Interrupt generation for transfer completion and error conditions
- Debug visibility
  - Queue watermarking/threshold allows detection of maximum usage of event queues
  - Error and status recording to facilitate debug

4.4.1 EDMA3 Device-Specific Information

The EDMA supports two addressing modes: constant addressing and increment addressing mode. Constant addressing mode is applicable to a very limited set of use cases. For most applications, increment mode can be used. On the TCI6634K2K SoC, the EDMA can use constant addressing mode only with the enhanced Viterbi decoder coprocessor (VCP) and the enhanced turbo decoder coprocessor (TCP). Constant addressing mode is not supported by any other peripheral or internal memory in the DSP. Note that increment mode is supported by all peripherals, including VCP and TCP. For more information on these two addressing modes, see the *Enhanced Direct Memory Access 3 (EDMA3) for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

For the range of memory addresses that includes EDMA3 channel controller (EDMA3CC) control registers and EDMA3 transfer controller (TPTC) control registers see Section 4.1 "Memory Map Summary for TCI6634K2K" on page 80. For memory offsets and other details on EDMA3CC and TPTC Control Register entries, see the *Enhanced Direct Memory Access 3 (EDMA3) for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

4.4.2 EDMA3 Channel Controller Configuration

Table 4-31 shows the configuration for each of the EDMA3 channel controllers present on the device.

Table 4-31 EDMA3 Channel Controller Configuration

Description	EDMA3 CC0	EDMA3 CC1	EDMA3 CC2	EDMA3 CC3	EDMA3 CC4
Number of DMA channels in channel controller	64	64	64	64	64
Number of QDMA channels	8	8	8	8	8
Number of interrupt channels	64	64	64	64	64
Number of PaRAM set entries	512	512	512	512	512
Number of event queues	2	4	4	2	2
Number of transfer controllers	2	4	4	2	2
Memory protection existence	Yes	Yes	Yes	Yes	Yes
Number of memory protection and shadow regions	8	8	8	8	8
End of Table 4-31					

4.4.3 EDMA3 Transfer Controller Configuration

Each transfer controller on the device is designed differently based on considerations like performance requirements, system topology (like main TeraNet bus width, external memory bus width), etc. The parameters that determine the transfer controller configurations are:

- **FIFOSIZE:** Determines the size in bytes for the data FIFO that is the temporary buffer for the in-flight data. The data FIFO is where the read return data read by the TC read controller from the source endpoint is stored and subsequently written out to the destination endpoint by the TC write controller.
- **BUSWIDTH:** The width of the read and write data buses in bytes, for the TC read and write controller, respectively. This is typically equal to the bus width of the main TeraNet interface.
- **Default Burst Size (DBS):** The DBS is the maximum number of bytes per read/write command issued by a transfer controller.

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- **DSTREGDEPTH:** This determines the number of destination FIFO register sets. The number of destination FIFO register sets for a transfer controller determines the maximum number of outstanding transfer requests.

All four parameters listed above are fixed by the design of the device.

Table 4-32 shows the configuration of each of the EDMA3 transfer controllers present on the device.

Table 4-32 EDMA3 Transfer Controller Configuration

Parameter	EDMA3 CC0/CC4		EDMA3 CC1				EDMA3 CC2				EDMA3CC3	
	TC0	TC1	TC0	TC1	TC2	TC3	TC0	TC1	TC2	TC3	TC0	TC1
FIFOSIZE	1024 bytes	1024 bytes	1024 bytes	1024 bytes	1024 bytes	1024 bytes	1024 bytes	1024 bytes	1024 bytes	1024 bytes	1024 bytes	1024 bytes
BUSWIDTH	32 bytes	32 bytes	16 bytes	16 bytes	16 bytes	16 bytes	16 bytes	16 bytes	16 bytes	16 bytes	16 bytes	16 bytes
DSTREGDEPTH	4 entries	4 entries	4 entries	4 entries	4 entries	4 entries	4 entries	4 entries	4 entries	4 entries	4 entries	4 entries
DBS	128 bytes	128 bytes	128 bytes	128 bytes	128 bytes	128 bytes	128 bytes	128 bytes	128 bytes	128 bytes	128 bytes	128 bytes
End of Table 4-32												

4.4.4 EDMA3 Channel Synchronization Events

The EDMA3 supports up to 64 DMA channels for all EDMA3CC that can be used to service system peripherals and to move data between system memories. DMA channels can be triggered by synchronization events generated by system peripherals. The following tables list the source of the synchronization event associated with each of the EDMA EDMA3CC DMA channels. On the TCI6634K2K, the association of each synchronization event and DMA channel is fixed and cannot be reprogrammed.

For more detailed information on the EDMA3 module and how EDMA3 events are enabled, captured, processed, prioritized, linked, chained, and cleared, etc., see the *Enhanced Direct Memory Access 3 (EDMA3) for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

Table 4-33 EDMA3CC0 Events for TCI6634 (Part 1 of 3)

Event No.	Event Name	Description
0	TIMER_8_INTL	Timer interrupt low
1	TIMER_8_INTH	Timer interrupt high
2	TIMER_9_INTL	Timer interrupt low
3	TIMER_9_INTH	Timer interrupt high
4	TIMER_10_INTL	Timer interrupt low
5	TIMER_10_INTH	Timer interrupt high
6	TIMER_11_INTL	Timer interrupt low
7	TIMER_11_INTH	Timer interrupt high
8	CIC_2_OUT66	CIC2 Interrupt Controller output
9	CIC_2_OUT67	CIC2 Interrupt Controller output
10	CIC_2_OUT68	CIC2 Interrupt Controller output
11	CIC_2_OUT69	CIC2 Interrupt Controller output
12	CIC_2_OUT70	CIC2 Interrupt Controller output
13	CIC_2_OUT71	CIC2 Interrupt Controller output
14	CIC_2_OUT72	CIC2 Interrupt Controller output
15	CIC_2_OUT73	CIC2 Interrupt Controller output
16	GPIO_INT8	GPIO interrupt
17	GPIO_INT9	GPIO interrupt

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Table 4-33 EDMA3CC0 Events for TCI6634 (Part 2 of 3)

Event No.	Event Name	Description
18	GPIO_INT10	GPIO interrupt
19	GPIO_INT11	GPIO interrupt
20	GPIO_INT12	GPIO interrupt
21	GPIO_INT13	GPIO interrupt
22	GPIO_INT14	GPIO interrupt
23	GPIO_INT15	GPIO interrupt
24	TIMER_4_INTL	Timer interrupt low
25	TIMER_4_INTH	Timer interrupt high
26	TIMER_5_INTL	Timer interrupt low
27	TIMER_5_INTH	Timer interrupt high
28	TIMER_6_INTL	Timer interrupt low
29	TIMER_6_INTH	Timer interrupt high
30	TIMER_7_INTL	Timer interrupt low
31	TIMER_7_INTH	Timer interrupt high
32	GPIO_INT0	GPIO interrupt
33	GPIO_INT1	GPIO interrupt
34	GPIO_INT2	GPIO interrupt
35	GPIO_INT3	GPIO interrupt
36	GPIO_INT4	GPIO interrupt
37	GPIO_INT5	GPIO interrupt
38	GPIO_INT6	GPIO interrupt
39	GPIO_INT7	GPIO interrupt
40	TIMER_0_INTL	Timer interrupt low
41	TIMER_0_INTH	Timer interrupt high
42	TIMER_1_INTL	Timer interrupt low
43	TIMER_1_INTH	Timer interrupt high
44	TIMER_2_INTL	Timer interrupt low
45	TIMER_2_INTH	Timer interrupt high
46	TIMER_3_INTL	Timer interrupt low
47	TIMER_3_INTH	Timer interrupt high
48	SRIO_INTDST0	SRIO interrupt
49	SRIO_INTDST1	SRIO interrupt
50	SRIO_INTDST2	SRIO interrupt
51	SRIO_INTDST3	SRIO interrupt
52	SRIO_INTDST4	SRIO interrupt
53	SRIO_INTDST5	SRIO interrupt
54	SRIO_INTDST6	SRIO interrupt
55	SRIO_INTDST7	SRIO interrupt
56	AIF_ATEVT0	AIF timer
57	AIF_ATEVT1	AIF timer
58	AIF_ATEVT2	AIF timer
59	AIF_ATEVT3	AIF timer
60	AIF_ATEVT4	AIF timer
61	AIF_ATEVT5	AIF timer

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Table 4-33 EDMA3CC0 Events for TCI6634 (Part 3 of 3)

Event No.	Event Name	Description
62	AIF_ATEVT6	AIF timer
63	AIF_ATEVT7	AIF timer
End of Table 4-33		

Table 4-34 EDMA3CC1 Events for TCI6634 (Part 1 of 2)

Event No.	Event Name	Description
0	SPI_0_INT0	SPI0 interrupt
1	SPI_0_INT1	SPI0 interrupt
2	SPI_0_XEVT	SPI0 transmit event
3	SPI_0_REVT	SPI0 receive event
4	SEM_INT8	Semaphore interrupt
5	SEM_INT9	Semaphore interrupt
6	GPIO_INT0	GPIO interrupt
7	GPIO_INT1	GPIO interrupt
8	GPIO_INT2	GPIO interrupt
9	GPIO_INT3	GPIO interrupt
10	AIF_ATEVT0	AIF Timer event
11	AIF_ATEVT1	AIF Timer event
12	AIF_ATEVT2	AIF Timer event
13	AIF_ATEVT3	AIF Timer event
14	SEM_INT0	Semaphore interrupt
15	SEM_INT1	Semaphore interrupt
16	SEM_INT2	Semaphore interrupt
17	SEM_INT3	Semaphore interrupt
18	SEM_INT4	Semaphore interrupt
19	SEM_INT5	Semaphore interrupt
20	SEM_INT6	Semaphore interrupt
21	SEM_INT7	Semaphore interrupt
22	TIMER_8_INTL	Timer interrupt low
23	TIMER_8_INTH	Timer interrupt high
24	TIMER_9_INTL	Timer interrupt low
25	TIMER_9_INTH	Timer interrupt high
26	TIMER_10_INTL	Timer interrupt low
27	TIMER_10_INTH	Timer interrupt high
28	TIMER_11_INTL	Timer interrupt low
29	TIMER_11_INTH	Timer interrupt high
30	TIMER_12_INTL	Timer interrupt low
31	TIMER_12_INTH	Timer interrupt high
32	TIMER_13_INTL	Timer interrupt low
33	TIMER_13_INTH	Timer interrupt high
34	TIMER_14_INTL	Timer interrupt low
35	TIMER_14_INTH	Timer interrupt high
36	TIMER_15_INTL	Timer interrupt low
37	TIMER_15_INTH	Timer interrupt high

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Table 4-34 EDMA3CC1 Events for TCI6634 (Part 2 of 2)

Event No.	Event Name	Description
38	SEM_INT10	Semaphore interrupt
39	SEM_INT11	Semaphore interrupt
40	SEM_INT12	Semaphore interrupt
41	SEM_INT13	Semaphore interrupt
42	CIC_2_OUT0	CIC2 Interrupt Controller output
43	CIC_2_OUT1	CIC2 Interrupt Controller output
44	CIC_2_OUT2	CIC2 Interrupt Controller output
45	CIC_2_OUT3	CIC2 Interrupt Controller output
46	CIC_2_OUT4	CIC2 Interrupt Controller output
47	CIC_2_OUT5	CIC2 Interrupt Controller output
48	CIC_2_OUT6	CIC2 Interrupt Controller output
49	CIC_2_OUT7	CIC2 Interrupt Controller output
50	CIC_2_OUT8	CIC2 Interrupt Controller output
51	AIF_ATEVT4	AIF Timer event
52	AIF_ATEVT5	AIF Timer event
53	I2C_0_REVT	I2C0 receive
54	I2C_0_XEVT	I2C0 transmit
55	CIC_2_OUT13	CIC2 Interrupt Controller output
56	CIC_2_OUT14	CIC2 Interrupt Controller output
57	CIC_2_OUT15	CIC2 Interrupt Controller output
58	CIC_2_OUT16	CIC2 Interrupt Controller output
59	CIC_2_OUT17	CIC2 Interrupt Controller output
60	CIC_2_OUT18	CIC2 Interrupt Controller output
61	CIC_2_OUT19	CIC2 Interrupt Controller output
62	Reserved	Reserved
63	Reserved	Reserved
End of Table 4-34		

Table 4-35 EDMA3CC2 Events for TCI6634 (Part 1 of 3)

Event No.	Event Name	Description
0	TAC_DEVT2	TAC debug
1	TAC_DEVT3	TAC debug
2	TAC_DEVT4	TAC debug
3	TAC_DEVT5	TAC debug
4	AIF_ATEVT4	AIF timer
5	AIF_ATEVT5	AIF timer
6	TETB_FULLINT4	TETB4 is full
7	TETB_HFULLINT4	TETB4 is half full
8	TETB_FULLINT5	TETB5 is full
9	TETB_HFULLINT5	TETB5 is half full
10	TETB_FULLINT6	TETB6 is full
11	TETB_HFULLINT6	TETB6 is half full
12	TETB_FULLINT7	TETB7 is full
13	TETB_HFULLINT7	TETB7 is half full

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Table 4-35 EDMA3CC2 Events for TCI6634 (Part 2 of 3)

Event No.	Event Name	Description
14	SRIO_INTDST0	SRIO interrupt
15	SRIO_INTDST1	SRIO interrupt
16	SRIO_INTDST2	SRIO interrupt
17	SRIO_INTDST3	SRIO interrupt
18	SRIO_INTDST4	SRIO interrupt
19	SRIO_INTDST5	SRIO interrupt
20	SRIO_INTDST6	SRIO interrupt
21	SRIO_INTDST7	SRIO interrupt
22	AIF_ATEVT6	AIF timer
23	AIF_ATEVT7	AIF timer
24	TAC_DEVT0	TAC debug
25	TAC_DEVT1	TAC debug
26	GPIO_INT0	GPIO interrupt
27	GPIO_INT1	GPIO interrupt
28	GPIO_INT2	GPIO interrupt
29	GPIO_INT3	GPIO interrupt
30	GPIO_INT4	GPIO interrupt
31	GPIO_INT5	GPIO interrupt
32	GPIO_INT6	GPIO interrupt
33	GPIO_INT7	GPIO interrupt
34	TCP3D_0_REVT0	TCP3d event
35	TCP3D_0_REVT1	TCP3d event
36	TCP3D_1_REVT0	TCP3d event
37	TCP3D_1_REVT1	TCP3d event
38	CIC_2_OUT48	CIC2 Interrupt Controller output
39	TAC_INT	TAC interrupt
40	UART_0_URXEVT	UART0 receive event
41	UART_0_UTXEVT	UART0 transmit event
42	CIC_2_OUT22	CIC2 Interrupt Controller output
43	CIC_2_OUT23	CIC2 Interrupt Controller output
44	CIC_2_OUT24	CIC2 Interrupt Controller output
45	CIC_2_OUT25	CIC2 Interrupt Controller output
46	CIC_2_OUT26	CIC2 Interrupt Controller output
47	CIC_2_OUT27	CIC2 Interrupt Controller output
48	CIC_2_OUT28	CIC2 Interrupt Controller output
49	SPI_0_XEVT	SPI0 transmit event
50	SPI_0_REVT	SPI0 receive event
51	VCP_0_REVT0	VCP receive event
52	VCP_0_XEVT0	VCP transmit event
53	VCP_0_REVT1	VCP receive event
54	VCP_0_XEVT1	VCP transmit event
55	VCP_0_REVT2	VCP receive event
56	VCP_0_XEVT2	VCP transmit event
57	VCP_0_REVT3	VCP receive event

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Table 4-35 EDMA3CC2 Events for TCI6634 (Part 3 of 3)

Event No.	Event Name	Description
58	VCP_0_XEVT3	VCP transmit event
59	RAC_0_INT	RAC interrupt
60	RAC_1_INT	RAC interrupt
61	RAC_2_INT	RAC interrupt
62	RAC_3_INT	RAC interrupt
63	BCP_INT0	BCP interrupt
End of Table 4-35		

Table 4-36 EDMA3CC3 Events for TCI6634 (Part 1 of 2)

Event No.	Event Name	Description
0	SPI_2_INT0	SPI2 interrupt
1	SPI_2_INT1	SPI2 interrupt
2	SPI_2_XEVT	SPI2 transmit event
3	SPI_2_REVT	SPI2 receive event
4	I2C_2_REVT	I2C2 receive
5	I2C_2_XEVT	I2C2 transmit
6	UART_1_URXEVT	UART1 receive event
7	UART_1_UTXEVT	UART1 transmit event
8	SPI_1_INT0	SPI1 interrupt
9	SPI_1_INT1	SPI1 interrupt
10	SPI_1_XEVT	SPI1 transmit event
11	SPI_1_REVT	SPI1 receive event
12	I2C_0_REVT	I2C0 receive
13	I2C_0_XEVT	I2C0 transmit
14	I2C_1_REVT	I2C1 receive
15	I2C_1_XEVT	I2C1 transmit
16	SRIO_INTDST0	SRIO interrupt
17	SRIO_INTDST1	SRIO interrupt
18	SRIO_INTDST2	SRIO interrupt
19	SRIO_INTDST3	SRIO interrupt
20	SRIO_INTDST4	SRIO interrupt
21	SRIO_INTDST5	SRIO interrupt
22	SRIO_INTDST6	SRIO interrupt
23	SRIO_INTDST7	SRIO interrupt
24	TCP3D_0_REVT0	TCP3d event
25	TCP3D_0_REVT1	TCP3d event
26	TCP3D_1_REVT0	TCP3d event
27	TCP3D_1_REVT1	TCP3d event
28	TCP3D_2_REVT0	TCP3d event
29	TCP3D_2_REVT1	TCP3d event
30	TCP3D_3_REVT0	TCP3d event
31	TCP3D_3_REVT1	TCP3d event
32	TETB_FULLINT0	TETB0 is full
33	TETB_HFULLINT0	TETB0 is half full

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Table 4-36 EDMA3CC3 Events for TCI6634 (Part 2 of 2)

Event No.	Event Name	Description
34	TETB_FULLINT1	TETB1 is full
35	TETB_HFULLINT1	TETB1 is half full
36	TETB_FULLINT2	TETB2 is full
37	TETB_HFULLINT2	TETB2 is half full
38	TETB_FULLINT3	TETB3 is full
39	TETB_HFULLINT3	TETB3 is half full
40	VCP_0_REVT0	VCP event
41	VCP_0_XEVT0	VCP event
42	VCP_0_REVT1	VCP event
43	VCP_0_XEVT1	VCP event
44	VCP_0_REVT2	VCP event
45	VCP_0_XEVT2	VCP event
46	VCP_0_REVT3	VCP event
47	VCP_0_XEVT3	VCP event
48	VCP_1_REVT0	VCP event
49	VCP_1_XEVT0	VCP event
50	VCP_1_REVT1	VCP event
51	VCP_1_XEVT1	VCP event
52	VCP_1_REVT2	VCP event
53	VCP_1_XEVT2	VCP event
54	VCP_1_REVT3	VCP event
55	VCP_1_XEVT3	VCP event
56	CIC_2_OUT57	CIC2 Interrupt Controller output
57	CIC_2_OUT50	CIC2 Interrupt Controller output
58	CIC_2_OUT51	CIC2 Interrupt Controller output
59	CIC_2_OUT52	CIC2 Interrupt Controller output
60	CIC_2_OUT53	CIC2 Interrupt Controller output
61	CIC_2_OUT54	CIC2 Interrupt Controller output
62	CIC_2_OUT55	CIC2 Interrupt Controller output
63	CIC_2_OUT56	CIC2 Interrupt Controller output
End of Table 4-36		

Table 4-37 EDMA3CC4 Events for TCI6634 (Part 1 of 3)

Event No.	Event Name	Description
0	GPIO_INT16	GPIO interrupt
1	GPIO_INT17	GPIO interrupt
2	GPIO_INT18	GPIO interrupt
3	GPIO_INT19	GPIO interrupt
4	GPIO_INT20	GPIO interrupt
5	GPIO_INT21	GPIO interrupt
6	GPIO_INT22	GPIO interrupt
7	GPIO_INT23	GPIO interrupt
8	AIF_ATEVT0	AIF timer
9	AIF_ATEVT1	AIF timer

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Table 4-37 EDMA3CC4 Events for TCI6634 (Part 2 of 3)

Event No.	Event Name	Description
10	AIF_ATEVT2	AIF timer
11	AIF_ATEVT3	AIF timer
12	AIF_ATEVT4	AIF timer
13	AIF_ATEVT5	AIF timer
14	AIF_ATEVT6	AIF timer
15	AIF_ATEVT7	AIF timer
16	AIF_ATEVT16	AIF timer
17	AIF_ATEVT17	AIF timer
18	AIF_ATEVT18	AIF timer
19	AIF_ATEVT19	AIF timer
20	AIF_ATEVT20	AIF timer
21	AIF_ATEVT21	AIF timer
22	AIF_ATEVT22	AIF timer
23	AIF_ATEVT23	AIF timer
24	TIMER_8_INTL	Timer interrupt low
25	TIMER_8_INTH	Timer interrupt high
26	TIMER_14_INTL	Timer interrupt low
27	TIMER_14_INTH	Timer interrupt high
28	TIMER_15_INTL	Timer interrupt low
29	TIMER_15_INTH	Timer interrupt high
30	DBGTBR_DMAINT	Debug trace buffer (TBR) DMA event
31	Reserved	Reserved
32	QMSS_QUE_PEND_658	Navigator transmit queue pending event for indicated queue
33	QMSS_QUE_PEND_659	Navigator transmit queue pending event for indicated queue
34	QMSS_QUE_PEND_660	Navigator transmit queue pending event for indicated queue
35	QMSS_QUE_PEND_661	Navigator transmit queue pending event for indicated queue
36	QMSS_QUE_PEND_662	Navigator transmit queue pending event for indicated queue
37	QMSS_QUE_PEND_663	Navigator transmit queue pending event for indicated queue
38	QMSS_QUE_PEND_664	Navigator transmit queue pending event for indicated queue
39	QMSS_QUE_PEND_665	Navigator transmit queue pending event for indicated queue
40	QMSS_QUE_PEND_8736	Navigator transmit queue pending event for indicated queue
41	QMSS_QUE_PEND_8737	Navigator transmit queue pending event for indicated queue
42	QMSS_QUE_PEND_8738	Navigator transmit queue pending event for indicated queue
43	QMSS_QUE_PEND_8739	Navigator transmit queue pending event for indicated queue
44	QMSS_QUE_PEND_8740	Navigator transmit queue pending event for indicated queue
45	QMSS_QUE_PEND_8741	Navigator transmit queue pending event for indicated queue
46	QMSS_QUE_PEND_8742	Navigator transmit queue pending event for indicated queue
47	QMSS_QUE_PEND_8743	Navigator transmit queue pending event for indicated queue
48	Reserved	Reserved
49	Reserved	Reserved
50	Reserved	Reserved
51	Reserved	Reserved
52	Reserved	Reserved
53	Reserved	Reserved

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Table 4-37 EDMA3CC4 Events for TCI6634 (Part 3 of 3)

Event No.	Event Name	Description
54	Reserved	Reserved
55	Reserved	Reserved
56	CIC_2_OUT82	CIC2 Interrupt Controller output
57	CIC_2_OUT83	CIC2 Interrupt Controller output
58	CIC_2_OUT84	CIC2 Interrupt Controller output
59	CIC_2_OUT85	CIC2 Interrupt Controller output
60	CIC_2_OUT86	CIC2 Interrupt Controller output
61	CIC_2_OUT87	CIC2 Interrupt Controller output
62	CIC_2_OUT88	CIC2 Interrupt Controller output
63	CIC_2_OUT89	CIC2 Interrupt Controller output
End of Table 4-37		

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5 System Interconnect

On the KeyStone II devices, the C66x CorePac, the EDMA3 transfer controllers, and the system peripherals are interconnected through the TeraNets, which are non-blocking switch fabrics enabling fast and contention-free internal data movement. The TeraNets provide low-latency, concurrent data transfers between master peripherals and slave peripherals. The TeraNets also allow for seamless arbitration between the system masters when accessing system slaves.

5.1 Internal Buses and Switch Fabrics

Two types of buses exist in the device:

- **Configuration** buses are mainly used to access the register space of a peripheral
- **Data** buses are used mainly for data transfers

Some peripherals have both a data bus and a configuration bus interface, while others only have one type of interface. Furthermore, the bus interface width and speed varies from peripheral to peripheral.

The C66x CorePacs, the EDMA3 traffic controllers, and the various system peripherals can be classified into two categories: masters and slaves.

- Masters are capable of initiating read and write transfers in the system and do not rely on the EDMA3 for their data transfers.
- Slaves on the other hand rely on the masters to perform transfers to and from them.

Examples of masters include the EDMA3 traffic controllers, SRIO, and network coprocessor packet DMA.

Examples of slaves include the SPI, UART, and I^2C.

The masters and slaves in the device communicate through the TeraNet (switch fabric). The device contains two types of switch fabric:

- **Data** TeraNet is a high-throughput interconnect mainly used to move data across the system
- **Configuration** TeraNet is mainly used to access peripheral registers

Note that the data TeraNet also connects to the configuration TeraNet. For more details see 5.2 "Switch Fabric Connections Matrix" on page 165.

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5.2 Switch Fabric Connections Matrix

The following tables list the master and slave end point connections. Intersecting cells may contain one of the following:

- **Y** — There is a connection between this master and that slave.
- **-** — There is NO connection between this master and that slave.
- ***n*** — A numeric value indicates that the path between this master and that slave goes through bridge *n*.

Table 5-1 TCI6634K2K System Interconnect 2, Section 1 (Part 1 of 2)

Masters	Slaves																					
	EDMA0_CC_CFG	EDMA1_CC_CFG	EDMA2_CC_CFG	EDMA3_CC_CFG	EDMA4_CC_CFG	EDMA0_TC(0-1)_CFG	EDMA1_TC(0-3)_CFG	EDMA2_TC(0-3)_CFG	EDMA3_TC(0-1)_CFG	EDMA4_TC(0-1)_CFG	SM_CFG	QM_CFG1	QM_CFG2	CPT_MSMC(0-7)_CFG	CPT_QM_M_CFG	CPT_DDR3A_CFG	CPT_SM_CFG	CPT_QM_CFG1_CFG	CPT_CFG_CFG	CPT_L2_(0-7)_CFG	CPT_RAC_FEI_CFG	CPT_RAC_2FG1_CFG
HyperLink0_Master	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
HyperLink1_Master	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA0_TC0_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-	-	-	-
EDMA0_TC0_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-	-	-	-
EDMA0_TC1_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-	-	-	-
EDMA0_TC1_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-	-	-	-
EDMA1_TC0_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA1_TC0_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA1_TC1_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-	-	-	-
EDMA1_TC1_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-	-	-	-
EDMA1_TC2_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-	-	-	-
EDMA1_TC2_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-	-	-	-
EDMA1_TC3_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA1_TC3_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA2_TC0_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA2_TC0_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA2_TC1_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-	-	-	-
EDMA2_TC1_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-	-	-	-
EDMA2_TC2_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA2_TC2_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA2_TC3_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-	-	-	-
EDMA2_TC3_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-	-	-	-
EDMA3_TC0_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA3_TC0_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA3_TC1_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-	-	-	-
EDMA3_TC1_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-	-	-	-
EDMA4_TC0_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-	-	-	-
EDMA4_TC0_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-	-	-	-
EDMA4_TC1_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-	-	-	-

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Table 5-1 TCI6634K2K System Interconnect 2, Section 1 (Part 2 of 2)

Masters	Slaves																					
	EDMA0_CC_CFG	EDMA1_CC_CFG	EDMA2_CC_CFG	EDMA3_CC_CFG	EDMA4_CC_CFG	EDMA0_TC(0-1)_CFG	EDMA1_TC(0-3)_CFG	EDMA2_TC(0-3)_CFG	EDMA3_TC(0-1)_CFG	EDMA4_TC(0-1)_CFG	SM_CFG	QM_CFG1	QM_CFG2	CPT_MSMC(0-7)_CFG	CPT_QM_M_CFG	CPT_DDR3A_CFG	CPT_SM_CFG	CPT_QM_CFG1_CFG	CPT_CFG_CFG	CPT_L2_(0-7)_CFG	CPT_RAC_FEI_CFG	CPT_RAC_2FG1_CFG
EDMA4_TC1_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-	-	-	-
SRIO Packet DMA	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SRIO	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
PCIE	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
NETCP	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
10GbE	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
MSMC_SYS	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
QM_Master1	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
QM_Master2	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
QM_SEC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
DBG_DAP	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
FFTC_(0-2)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
FFTC_(3-5)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
RAC_(0-3)_BE0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
RAC_(0-3)_BE1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
AIF2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
TAC_FEI(0-2)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
BCP_DIO(0-1)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
BCP Packet DMA	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
USB	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA0_CC_TR	-	-	-	-	-	Y	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA1_CC_TR	-	-	-	-	-	-	Y	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA2_CC_TR	-	-	-	-	-	-	-	Y	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA3_CC_TR	-	-	-	-	-	-	-	-	Y	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA4_CC_TR	-	-	-	-	-	-	-	-	-	Y	-	-	-	-	-	-	-	-	-	-	-	-
CorePac0_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
CorePac1_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
CorePac2_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
CorePac3_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
CorePac4_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
CorePac5_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
CorePac6_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
CorePac7_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y

End of Table 5-1

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Table 5-2 TCI6634K2K System Interconnect 2, Section 2 (Part 1 of 2)

Masters	Slave																
	CPT_TAC_BE_CFG	CPT_QM_CFG2_CFG	CPT_RAC_2FG2_CFG	CPT_DDR3B_CFG	CPT_TPCC0_4_CFG	CPT_TPCC1_2_3_CFG	CPT_INTC_CFG	CPT_SPI_ROM_EMIF16_CFG	CPT_BCR_CFG_CFG	GIC_CFG	NETCP_CFG	10GbE_CFG	USB_MMR_CFG	SRIO_CFG	ADTF(0-7)_CFG	TIMER(0-19)_CFG	GPIO_CFG
HyperLink0_Master	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y
HyperLink1_Master	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y
EDMA0_TC0_RD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA0_TC0_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA0_TC1_RD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA0_TC1_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA1_TC0_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA1_TC0_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA1_TC1_RD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA1_TC1_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA1_TC2_RD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA1_TC2_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA1_TC3_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA1_TC3_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA2_TC0_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA2_TC0_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA2_TC1_RD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA2_TC1_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA2_TC2_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA2_TC2_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA2_TC3_RD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA2_TC3_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA3_TC0_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA3_TC0_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA3_TC1_RD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA3_TC1_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA4_TC0_RD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA4_TC0_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA4_TC1_RD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA4_TC1_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SRIO Packet DMA	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SRIO	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y
PCIE	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y
NETCP	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

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Table 5-2 TCI6634K2K System Interconnect 2, Section 2 (Part 2 of 2)

Masters	Slave																
	CPT_TAC_BE_CFG	CPT_QM_CFG2_CFG	CPT_RAC_2FG2_CFG	CPT_DDR3B_CFG	CPT_TPCC0_4_CFG	CPT_TPCC1_2_3_CFG	CPT_INTC_CFG	CPT_SPI_ROM_EMIF16_CFG	CPT_BCR_CFG_CFG	GIC_CFG	NETCP_CFG	10GbE_CFG	USB_MMR_CFG	SRIO_CFG	ADTF(0-7)_CFG	TIMER(0-19)_CFG	GPIO_CFG
10GbE	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
MSMC_SYS	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
QM_Master1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
QM_Master2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
QM_SEC	-	-	-	-	-	-	-	-	-	-	Y	Y	Y	-	-	-	-
DBG_DAP	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
FFTC_(0-2)	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y
FFTC_(3-5)	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y
RAC_(0-3)_BE0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
RAC_(0-3)_BE1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
AIF2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
TAC_FEI(0-2)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
BCP_DIO(0-1)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
BCP Packet DMA	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y
USB	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA0_CC_TR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA1_CC_TR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA2_CC_TR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA3_CC_TR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA4_CC_TR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CorePac0_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y
CorePac1_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y
CorePac2_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y
CorePac3_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y
CorePac4_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y
CorePac5_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y
CorePac6_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y
CorePac7_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y

End of Table 5-2

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Table 5-3 TCI6634K2K System Interconnect 2, Section 3 (Part 1 of 2)

Masters	Slaves																				
	I2C(0-2)_CFG	SEC_MGR_CFG	BOOTCFG_CFG	PSC_CFG	PLL_CTL_CFG	CP_INTC(0-2)_CFG	MPU(0-14)_CFG	DBG_CFG	SR_CFG(0-1)	OTP_CFG	UART(0-1)_CFG	PCIE_SERDES_CFG	HYPERLINK0_SERDES_CFG	HYPERLINK1_SERDES_CFG	SRIO_SERDES_CFG	DDR3A_PHY_CFG	NETCP_SERDES_CFG	10GbE_SERDES_CFG	USB_PHY_CFG	RAC_(0-3)_CFG	FFTC_(0-7)_CFG
HyperLink0_Master	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
HyperLink1_Master	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA0_TC0_RD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA0_TC0_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA0_TC1_RD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA0_TC1_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA1_TC0_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA1_TC0_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA1_TC1_RD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA1_TC1_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA1_TC2_RD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA1_TC2_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA1_TC3_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA1_TC3_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA2_TC0_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA2_TC0_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA2_TC1_RD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA2_TC1_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA2_TC2_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA2_TC2_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA2_TC3_RD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA2_TC3_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA3_TC0_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA3_TC0_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA3_TC1_RD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA3_TC1_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA4_TC0_RD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA4_TC0_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA4_TC1_RD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA4_TC1_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SRIO Packet DMA	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SRIO	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
PCIE	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
NETCP	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

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Table 5-3 TCI6634K2K System Interconnect 2, Section 3 (Part 2 of 2)

Masters	Slaves																				
	I2C(0-2)_CFG	SEC_MGR_CFG	BOOTCFG_CFG	PSC_CFG	PLL_CTL_CFG	CP_INTC(0-2)_CFG	MPU(0-14)_CFG	DBG_CFG	SR_CFG(0-1)	OTP_CFG	UART(0-1)_CFG	PCIE_SERDES_CFG	HYPERLINK0_SERDES_CFG	HYPERLINK1_SERDES_CFG	SRIO_SERDES_CFG	DDR3A_PHY_CFG	NETCP_SERDES_CFG	10GbE_SERDES_CFG	USB_PHY_CFG	RAC_(0-3)_CFG	FFTC_(0-7)_CFG
10GbE	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
MSMC_SYS	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
QM_Master1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
QM_Master2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
QM_SEC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
DBG_DAP	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
FFTC_(0-2)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
FFTC_(3-5)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
RAC_(0-3)_BE0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
RAC_(0-3)_BE1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
AIF2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
TAC_FEI(0-2)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
BCP_DIO(0-1)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
BCP Packet DMA	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
USB	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA0_CC_TR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA1_CC_TR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA2_CC_TR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA3_CC_TR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA4_CC_TR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CorePac0_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
CorePac1_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
CorePac2_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
CorePac3_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
CorePac4_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
CorePac5_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
CorePac6_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
CorePac7_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y

End of Table 5-3

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Table 5-4 TCI6634K2K System Interconnect 2, Section 4 (Part 1 of 2)

Masters	Slaves																	
	TAC_CFG	TCP3D_(0-3)_CFG	VCP2_(0-7)_CFG	AIF2_CFG	AIF2_SERDES_B8_CFG	AIF2_SERDES_B4_CFG	DDR3B_PHY_CFG	BCP_CFG	BCR_CFG	DBG_TBR_SYS	TETB0_CFG	TETB1_CFG	TETB2_CFG	TETB3_CFG	TETB4_CFG	TETB5_CFG	TETB6_CFG	TETB7_CFG
HyperLink0_Master	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-
HyperLink1_Master	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-
EDMA0_TC0_RD	-	-	-	-	-	-	-	-	-	Y	-	-	-	-	Y	Y	-	-
EDMA0_TC0_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA0_TC1_RD	-	-	-	-	-	-	-	-	-	Y	-	-	-	-	Y	Y	-	-
EDMA0_TC1_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA1_TC0_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	Y	Y	-	-
EDMA1_TC0_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-
EDMA1_TC1_RD	-	-	-	-	-	-	-	-	-	-	Y	Y	-	-	-	-	Y	-
EDMA1_TC1_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA1_TC2_RD	-	-	-	-	-	-	-	-	-	-	-	-	Y	Y	-	-	-	Y
EDMA1_TC2_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA1_TC3_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	Y	Y	-	-
EDMA1_TC3_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-
EDMA2_TC0_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	Y	Y	-	-
EDMA2_TC0_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-
EDMA2_TC1_RD	-	-	-	-	-	-	-	-	-	-	Y	Y	-	-	-	-	Y	-
EDMA2_TC1_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA2_TC2_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	Y	Y	-	-
EDMA2_TC2_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-
EDMA2_TC3_RD	-	-	-	-	-	-	-	-	-	-	-	-	Y	Y	-	-	-	Y
EDMA2_TC3_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA3_TC0_RD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA3_TC0_WR	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-	-	-	-	-	-	-
EDMA3_TC1_RD	-	-	-	-	-	-	-	-	-	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA3_TC1_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA4_TC0_RD	-	-	-	-	-	-	-	-	-	Y	-	-	-	-	Y	Y	-	-
EDMA4_TC0_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA4_TC1_RD	-	-	-	-	-	-	-	-	-	Y	-	-	-	-	Y	Y	-	-
EDMA4_TC1_WR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SRIO Packet DMA	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SRIO	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
PCIE	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
NETCP	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
10GbE	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

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Table 5-4 TCI6634K2K System Interconnect 2, Section 4 (Part 2 of 2)

Masters	Slaves																	
	TAC_CFG	TCP3D_(0-3)_CFG	VCP2_(0-7)_CFG	AIF2_CFG	AIF2_SERDES_B8_CFG	AIF2_SERDES_B4_CFG	DDR3B_PHY_CFG	BCP_CFG	BCR_CFG	DBG_TBR_SYS	TETB0_CFG	TETB1_CFG	TETB2_CFG	TETB3_CFG	TETB4_CFG	TETB5_CFG	TETB6_CFG	TETB7_CFG
MSMC_SYS	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
QM_Master1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
QM_Master2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
QM_SEC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
DBG_DAP	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
FFTC_(0-2)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
FFTC_(3-5)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
RAC_(0-3)_BE0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
RAC_(0-3)_BE1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
AIF2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
TAC_FEI(0-2)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
BCP_DIO(0-1)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
BCP Packet DMA	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
USB	-	-	-	-	-	-	-	-	-	Y	Y	Y	Y	Y	Y	Y	Y	Y
EDMA0_CC_TR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA1_CC_TR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA2_CC_TR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA3_CC_TR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EDMA4_CC_TR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CorePac0_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
CorePac1_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
CorePac2_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
CorePac3_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
CorePac4_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
CorePac5_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
CorePac6_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
CorePac7_CFG	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
End of Table 5-4																		

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5.3 Bus Priorities

The priority level of all master peripheral traffic is defined at the TeraNet boundary. User-programmable priority registers allow software configuration of the data traffic through the TeraNet. Note that a lower number means higher priority — PRI = 000b = urgent, PRI = 111b = low.

All other masters provide their priority directly and do not need a default priority setting. Examples include the C66x CorePacs, whose priorities are set through software in the UMC control registers. All the Packet DMA-based peripherals also have internal registers to define the priority level of their initiated transactions.

The Packet DMA secondary port is one master port that does not have priority allocation register inside the Multicore Navigator. The priority level for transaction from this master port is described by the PKTDMA_PRI_ALLOC register shown in Figure 5-1 and Table 5-5.

Figure 5-1 Packed DMA Priority Allocation Register (PKTDMA_PRI_ALLOC)

31	3	2	0
Reserved		PKTDMA_PRI	
R/W-00000000000000000000001000011		RW-000	

Legend: R= Read only; R/W = Read/Write; -*n* = value after reset

Table 5-5 Packed DMA Priority Allocation Register Field Descriptions

Bit	Field	Description
31-3	Reserved	Reserved.
2-0	PKDTDMA_PRI	Controls the priority level for the transactions from the packet DMA master port, which accesses the external linking RAM.
End of Table 5-5		

For all other modules, see the respective User Guides in 1.9 "Related Documentation from Texas Instruments" on page 22 for programmable priority registers.

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6 Device Boot and Configuration

6.1 Device Boot

6.1.1 Boot Sequence

The boot sequence is a process by which the internal memory is loaded with program and data sections. The boot sequence is started automatically after each power-on reset or warm reset.

The TCI6634 supports several boot processes that begins execution at the ROM base address, which contains the bootloader code necessary to support various device boot modes. The boot processes are software-driven and use the BOOTMODE[15:0] device configuration inputs to determine the software configuration that must be completed. For more details on boot sequence see the Bootloader User Guide in 1.9 "Related Documentation from Texas Instruments" on page 22.

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6.1.2 Boot Modes Supported

The device supports two possible boot modes:

- **Public ROM Boot** — C66x CorePac0 is released from reset and begins executing from the L3 ROM base address. The C66x CorePac0 BootROM reads the bootmode register inside the boot CFG module to determine the boot mode, then performs the boot process and the other C66x CorePacs execute an IDLE instruction. After the boot process is completed, the C66x CorePac0 begins to execute the code downloaded during the boot process. If the downloaded code included code for the other C66x cores, the downloaded code may contain logic to write the code execution addresses to the boot address register for the core that is to execute it. C66x CorePac0 can then generate an interrupt to the core causing it to execute the code. When they receive the IPC interrupt, the rest of the C66x CorePacs complete boot management operations and begin executing from the predefined location in memory.
- **Secure ROM Boot** — The C66x CorePac0 is released from reset and begins executing from secure ROM. The C66x CorePac0 performs the boot process including any authentication and decryption required on the bootloaded image for the C66x CorePacs prior to beginning execution.

The boot process performed by the C66x CorePacs in public ROM boot and secure ROM boot is determined by the BOOTMODE[16:1] value in the DEVSTAT register. The C66x CorePac0 reads this value, and then executes the associated boot process in software. Figure 6-1 shows the bits associated with . Note that the figure does not include bit 0 of the DEVSTAT contents. Bit 0 is used to select system Endianess that is independent of the boot mode.

The boot ROM will continue attempting to boot in this mode until successful or an unrecoverable error occurs.

The PLL settings are shown at the end of this section, and the PLL set-up details can be found in Section 8.5 "Main PLL, DDR3A PLL, DDR3B PLL, PASS PLL and the PLL Controllers" on page 235.

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Figure 6-1 DEVSTAT Boot Mode Pins ROM Mapping

DEVSTAT Boot Mode Pins ROM Mapping																
16	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**Mode**
X	X	0	0	SYSEN	X	X	X		SYS PLL CONFIG			Min	0	0	0	SLEEP
Slave Addr		1	Port		X	X	X						0	0	0	I^2C SLAVE
X	X	X	Bus Addr		Param Idx				X	Port			0	0	1	I^2C MASTER
Width	Csel		Mode						Npin				0	1	0	SPI
0	Base Addr		Wait	Width	X	Chip Sel			SYS PLL CONFIG			0	0	1	1	Reserved
1	First Block			Clear		Chip Sel		1				Min				Reserved
X	Ref Clock		Data Rate		Lane Setup								1	0	0	SRIO
PA clk	Ref clk		Ext Con		Rsvd	Lane Setup							1	0	1	Ethernet
Ref clk	Bar Config				SerDes Cfg							0	1	1	0	PCIe
Port	Ref clk		Data Rate									1	1	1	0	Hyperlink
X	X	X	X	Port	X	X	X					Min	1	1	1	UART

6.1.2.1 Boot Device Field

The Boot Device field BOOTMODE[16-14-4-3-2-1] defines the boot device that is chosen. Table 6-1 shows the supported boot modes.

Table 6-1 Boot Mode Pins: Boot Device Values

Bit	Field	Description
16, 14, 4, 3, 2, 1	Boot Device	Device boot mode » Sleep = X0[Min]000b » I^2C Slave = [Slave Addr1]1[Min]000 b » I^2C Master = X1[Min]001b » SPI = [Width][Csel0][Min]010b » Serial Rapid I/O = [Lane][Ref Clock0][Min]100b » Ethernet (SGMII) = [Pa clk][Ref Clk0][Min]101b » PCI = [Ref clk][Bar Config2]0110b » Hyperlink = [Port][Ref Clk0]1110b » UART = XX[Min]111b
End of Table 6-1		

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6.1.2.2 Device Configuration Field

The device configuration fields BOOTMODE[16:1] are used to configure the boot peripheral and, therefore, the bit definitions depend on the boot mode.

6.1.2.2.1 Sleep Boot Mode Configuration

Figure 6-2 Sleep Boot Mode Configuration Field Description

DEVSTAT Boot Mode Pins ROM Mapping																
16	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
X	X	0	0	SYSEN	X	X	X	1	Sys PLL Config			Min	000			Lendian

Table 6-2 Sleep Boot Configuration Field Descriptions

Bit	Field	Description
16-15	Reserved	Reserved
14	Boot Devices	Boot Device- used in conjunction with Boot Devices [Used in conjunction with bits 3-1] 0 = Sleep (default) Others = Other boot modes
13	Reserved	This pin must be pulled down to GND
12	SYSEN	Enable the System PLL 0 = PLL disabled (default) 1 = PLL enabled
11-9	Reserved	Reserved
8	Boot Master	This pin must be pulled up to DVDD18
7-5	SYS PLL Setting	The PLL default settings are determined by the [7:5] bits. This will set the PLL to the maximum clock setting for the device. Table 6-12 shows settings for various input clock frequencies.
4	Min	Minimum boot configuration select bit. 0 = Minimum boot pin select disabled 1 = Minimum boot pin select enabled. When Min = 1, a predetermined set of values is configured (see the Device Configuration Field Descriptions table for configuration bits with a "(default)" tag added in the description column). When Min = 0, all fields must be independently configured.
3-1	Boot Devices	Boot Devices[3:1] used in conjunction with Boot Device [14] 000 = Sleep Others = Other boot modes
0	Lendian	Endianess (device) 0 = Big endian 1 = Little endian
End of Table 6-2		

6.1.2.2.2 I^2C Boot Device Configuration

I^2C Passive Mode

In passive mode, the device does not drive the clock, but simply acks data received on the specified address.

Figure 6-3 I^2C Passive Mode Device Configuration Fields

DEVSTAT Boot Mode Pins ROM Mapping																
16	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Slave Addr		1	Port		X	X	X	1	Sys PLL Config			Min	000			Lendian

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Table 6-3 I²C Passive Mode Device Configuration Field Descriptions

Bit	Field	Description
16-15	Slave Addr	I²C Slave boot bus address 0 = I²C slave boot bus address is 0x00 1 = I²C slave boot bus address is 0x10 (default) 2 = I²C slave boot bus address is 0x20 3 = I²C slave boot bus address is 0x30
14	Boot Devices	Boot Device[14] used in conjunction with Boot Devices [Use din conjunction with bits 3-1] 0 = Other boot modes 1= I²C Slave boot mode
13-12	Port	I²C port number 0 = I²C0 1 = I²C1 2 = I²C2 3 = Reserved
11-9	Reserved	Reserved
8	Boot Master	This pin must be pulled up to DVDD18
7-5	SYS PLL Setting	The PLL default settings are determined by the [7:5] bits. This will set the PLL to the maximum clock setting for the device. Table 6-12 shows settings for various input clock frequencies.
4	Min	Minimum boot configuration select bit. 0 = Minimum boot pin select disabled 1 = Minimum boot pin select enabled. When Min = 1, a predetermined set of values is configured (see the Device Configuration Field Descriptions table for configuration bits with a "(default)" tag added in the description column). When Min = 0, all fields must be independently configured.
3-1	Boot Devices	Boot Devices[3:1] used in conjunction with Boot Device [14] 000 = I²C Slave Others = Other boot modes
0	Lendian	Endianess 0 = Big endian 1 = Little endian
End of Table 6-3		

I²C Master Mode

In master mode, the I²C device configuration uses ten bits of device configuration instead of seven as used in other boot modes. In this mode, the device makes the initial read of the I²C EEPROM while the PLL is in bypass mode. The initial read contains the desired clock multiplier, which must be set up prior to any subsequent reads.

Figure 6-4 I²C *Master* Mode Device Configuration Fields

DEVSTAT Boot Mode Pins ROM Mapping																
16	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved			Bus Addr		Param Idx			1	Reserved	Port		Min	001			Lendian

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Table 6-4 I²C *Master* Mode Device Configuration Field Descriptions

Bit	Field	Description
16-14	Reserved	Reserved
13-12	Bus Addr	I²C bus address slave device 0 = I²C slave boot bus address is 0x50 (default) 1 = I²C slave boot bus address is 0x51 2 = I²C slave boot bus address is 0x52 3 = I²C slave boot bus address is 0x53
11-9	Param Idx	Parameter Table Index 0-7 = This value specifies the parameter table index (default = 0)
8	Boot Master	This pin must be pulled up to DVDD18
7	Reserved	Reserved
6-5	Port	I²C port number 0 = I²C0 (default) 1 = I²C1 2 = I²C2 3 = Reserved
4	Min	Minimum boot configuration select bit. 0 = Minimum boot pin select disabled 1 = Minimum boot pin select enabled. When Min = 1, a predetermined set of values is configured (see the Device Configuration Field Descriptions table for configuration bits with a "(default)" tag added in the description column). When Min = 0, all fields must be independently configured.
3-1	Boot Devices	Boot Devices[3:1] 001 = I²C Master Others = Other boot modes
0	Lendian	Endianess 0 = Big endian 1 = Little endian
End of Table 6-4		

6.1.2.2.3 SPI Boot Device Configuration

Figure 6-5 SPI Device Configuration Fields

DEVSTAT Boot Mode Pins ROM Mapping																
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Width	Csel		Mode		Param Idx			1	Npin	Port		Min	010			Lendian

Table 6-5 SPI Device Configuration Field Descriptions (Part 1 of 2)

Bit	Field	Description
16	Width	SPI address width configuration 0 = 16-bit address values are used 1 = 24-bit address values are used (default)
15-14	Csel	The chip select field value 0-3(default = 0)
13-12	Mode	Clk Polarity/ Phase 0 = Data is output on the rising edge of SPICLK. Input data is latched on the falling edge. 1 = Data is output one half-cycle before the first rising edge of SPICLK and on subsequent falling edges. Input data is latched on the rising edge of SPICLK. 2 = Data is output on the falling edge of SPICLK. Input data is latched on the rising edge (default). 3 = Data is output one half-cycle before the first falling edge of SPICLK and on subsequent rising edges. Input data is latched on the falling edge of SPICLK.
11-9	Param Idx	Parameter Table Index 0-7 = This value specifies the parameter table index (default = 0)

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Table 6-5 SPI Device Configuration Field Descriptions (Part 2 of 2)

Bit	Field	Description
8	Boot Master	This pin must be pulled up to DVDD18
7	Npin	Selected Chip Select driven 0 = CS0 to the selected chip select is driven 1 = CS0-CS4 to the selected chip select are driven (default)
6-5	Port	Specify SPI port 0 = SPI0 used (default) 1 = SPI1 used 2 = SPI2 used 3 = Reserved
4	Min	Minimum boot configuration select bit. 0 = Minimum boot pin select disabled 1 = Minimum boot pin select enabled. When Min = 1, a predetermined set of values is configured (see the Device Configuration Field Descriptions table for configuration bits with a "(default)" tag added in the description column). When Min = 0, all fields must be independently configured.
3-1	Boot Devices	Boot Devices[3:1] 010 = SPI boot mode Others = Other boot modes
0	Lendian	Endianess 0 = Big endian 1 = Little endian
End of Table 6-5		

6.1.2.2.4 Serial Rapid I/O Boot Device Configuration

The device ID is always set to 0xff (8-bit node IDs) or 0xffff (16 bit node IDs) at power-on reset.

Figure 6-6 Serial Rapid I/O Boot Device Configuration Fields

DEVSTAT Boot Mode Pins ROM Mapping																
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	Ref Clock		Data Rate		Lane Setup			1	Sys PLL Cfg			Min	100			Lendian

Table 6-6 Serial Rapid I/O Boot Device Configuration Field Descriptions (Part 1 of 2)

Bit	Field	Description
16	Reserved	Reserved
15-14	Ref Clock	SRIO Reference clock frequency 0 = 125MHz 1 = 156.25MHz (default) 2 = Reserved 3 = Reserved
13-12	Data Rate	SRIO Data Rate 0 = 1.25 GBs 1 = 2.5 GBs 2 = 3.125 GBs 3 = 5 GBs (default)
11-9	Lane Setup	Lane Set up. 0 = 4 ports, each 1 lane wide (default) 1 = 3 ports, lanes 0, 1 form a 2 lane port, lane 2,3 are single ports 2 = 3 ports, lanes 0, 1 are single lane ports, lanes 2,3 form a 2 lane port 3 = 2 ports, lane 0, 1 are one port, lane 2, 3 are a second port 4 = 1 port, 4 lanes wide 5 - 7 = 4 ports, each 1 lane wide

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Table 6-6 Serial Rapid I/O Boot Device Configuration Field Descriptions (Part 2 of 2)

Bit	Field	Description
8	Boot Master	This pin must be pulled up to DVDD18
7-5	SYS PLL Setting	The PLL default settings are determined by the [7:5] bits. This will set the PLL to the maximum clock setting for the device. Default system reference clock is 156.25 MHz. Table 6-12 shows settings for various input clock frequencies. (default = 4)
4	Min	Minimum boot configuration select bit. 0 = Minimum boot pin select disabled 1 = Minimum boot pin select enabled. When Min = 1, a predetermined set of values is configured (see the Device Configuration Field Descriptions table for configuration bits with a "(default)" tag added in the description column). When Min = 0, all fields must be independently configured.
3-1	Boot Devices	Boot Devices 100 = SRIO boot mode Others = Other boot modes
0	Lendian	Endianess 0 = Big endian 1 = Little endian
End of Table 6-6		

In SRIO boot mode, both the message mode and DirectIO mode will be enabled by default. If use of the memory reserved for received messages is required and reception of messages cannot be prevented, the master can disable the message mode by writing to the boot table and generating a boot restart.

6.1.2.3 Ethernet (SGMII) Boot Device Configuration

Figure 6-7 Ethernet (SGMII) Boot Device Configuration Fields

DEVSTAT Boot Mode Pins ROM Mapping																
16	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Pa clk	Ref Clock		Ext Con		Lane Setup			1	Sys PLL Cfg			Min	101			Lendian

Table 6-7 Ethernet (SGMII) Boot Device Configuration Field Descriptions (Part 1 of 2)

Bit	Field	Description
16	Pa clk	PA clock reference 0 = PA clocked at the same reference as the core reference 1 = PA clocked at the same reference as the SerDes reference (default)
15-14	Ref Clock	SRIO Reference clock frequency 0 = 125MHz 1 = 156.25MHz (default) 2 = Reserved 3 = Reserved
13-12	Ext Con	External connection mode 0 = MAC to MAC connection, master with auto negotiation 1 = MAC to MAC connection, slave with auto negotiation (default) 2 = MAC to MAC, forced link, maximum speed 3 = MAC to fiber connection
11-9	Lane Setup	Lane Setup. 0 = All SGMII ports enabled (default) 1 = Only SGMII port 0 enabled 2 = SGMII port 0 and 1 enabled 3 = SGMII port 0, 1 and 2 enabled 4-5 = Reserved
8	Boot Master	This pin must be pulled up to DVDD18

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Table 6-7 Ethernet (SGMII) Boot Device Configuration Field Descriptions (Part 2 of 2)

Bit	Field	Description
7-5	SYS PLL Setting	The PLL default settings are determined by the [7:5] bits. This will set the PLL to the maximum clock setting for the device. Default system reference clock is 156.25 MHz. Table 6-12 shows settings for various input clock frequencies. (default = 4)
4	Min	Minimum boot configuration select bit. 0 = Minimum boot pin select disabled 1 = Minimum boot pin select enabled. When Min = 1, a predetermined set of values is configured (see the Device Configuration Field Descriptions table for configuration bits with a "(default)" tag added in the description column). When Min = 0, all fields must be independently configured.
3-1	Boot Devices	Boot Devices 101 = Ethernet boot mode Others = Other boot modes
0	Lendian	Endianess 0 = Big endian 1 = Little endian
End of Table 6-7		

6.1.2.3.1 PCIe Boot Device Configuration

Figure 6-8 PCIe Boot Device Configuration Fields

DEVSTAT Boot Mode Pins ROM Mapping																
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ref clk	Bar Config				SERDES Cfg			1	Sys PLL Cfg			0110				Lendian

Table 6-8 PCIe Boot Device Configuration Field Descriptions

Bit	Field	Description
16	Ref clk	PCIe Reference clock frequency 0 = 100MHz 1 = 156.25MHz
15-12	Bar Config	PCIe BAR registers configuration This value can range from 0 to 0xf. See Table 6-9.
11-9	SERDES Cfg	Extra SERDES configuration 0-7 = TBD
8	Boot Master	This pin must be pulled up to DVDD18
7-5	SYS PLL Setting	The PLL default settings are determined by the [7:5] bits.This will set the PLL to the maximum clock setting for the device. Default system reference clock is 156.25 MHz. Table 6-12 shows settings for various input clock frequencies.
4-1	Boot Devices	Boot Devices[4:1] 0110 = PCIe boot mode Others = Other boot modes
0	Lendian	Endianess 0 = Big endian 1 = Little endian
End of Table 6-8		

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Table 6-9 BAR Config / PCIe Window Sizes

BAR cfg	BAR0	32-Bit Address Translation					64-Bit Address Translation	
		BAR1	BAR2	BAR3	BAR4	BAR5	BAR2/3	BAR4/5
0b0000	PCIe MMRs	32	32	32	32	Clone of BAR4		
0b0001		16	16	32	64			
0b0010		16	32	32	64			
0b0011		32	32	32	64			
0b0100		16	16	64	64			
0b0101		16	32	64	64			
0b0110		32	32	64	64			
0b0111		32	32	64	128			
0b1000		64	64	128	256			
0b1001		4	128	128	128			
0b1010		4	128	128	256			
0b1011		4	128	256	256			
0b1100							256	256
0b1101							512	512
0b1110							1024	1024
0b1111							2048	2048

6.1.2.3.2 HyperLink Boot Device Configuration

Figure 6-9 Hyperlink Boot Device Configuration Fields

DEVSTAT Boot Mode Pins ROM Mapping																
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Port	RefClk		Data Rate		SERDES Cfg			1	Sys PLL Cfg			1110				Lendian

Table 6-10 HyperLink Boot Device Configuration Field Descriptions (Part 1 of 2)

Bit	Field	Description
16	Port	HyperLink port 0 = HyperLink0 1 = HyperLink1
15-14	Ref Clocks	HyperLink reference clock configuration 0 = 125 MHz 1 = 156.25 MHz 2-3 = Reserved
13-12	Data Rate	HyperLink data rate configuration 0 = 1.25 GBs 1 = 3.125 GBs 2 = 6.25 GBs 3 = 12.5GBs
11-9	SERDES Cfg	Extra SERDES configuration 0-7 = TBD
8	Boot Master	This pin must be pulled up to DVDD18
7-5	SYS PLL Setting	The PLL default settings are determined by the [7:5] bits. This will set the PLL to the maximum clock setting for the device. Default system reference clock is 156.25 MHz. Table 6-12 shows settings for various input clock frequencies.

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Table 6-10 HyperLink Boot Device Configuration Field Descriptions (Part 2 of 2)

Bit	Field	Description
4-1	Boot Devices	Boot Devices[4:1] 1110 = HyperLink boot mode Others = Other boot modes
0	Lendian	Endianess 0 = Big endian 1 = Little endian
End of Table 6-10		

6.1.2.3.3 UART Boot Device Configuration

Figure 6-10 UART Boot Mode Configuration Field Description

DEVSTAT Boot Mode Pins ROM Mapping																
16	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
X	X	X	X	Port	X	X	X	1	Sys PLL Config			Min	111			Lendian

Table 6-11 UART Boot Configuration Field Descriptions

Bit	Field	Description
16-13	Reserved	Not Used
12	Port	UART Port number 0 = UART0 1 = UART1
11-9	Reserved	Not Used
8	Boot Master	This pin must be pulled up to DVDD18
7-5	SYS PLL Setting	The PLL default settings are determined by the [7:5] bits. This will set the PLL to the maximum clock setting for the device. Table 6-12 shows settings for various input clock frequencies. (default = 4)
4	Min	Minimum boot configuration select bit. 0 = Minimum boot pin select disabled 1 = Minimum boot pin select enabled. When Min = 1, a predetermined set of values is configured (see the Device Configuration Field Descriptions table for configuration bits with a "(default)" tag added in the description column). When Min = 0, all fields must be independently configured.
3-1	Boot Devices	Boot Devices[3:1] 111 = UART boot mode Others = Other boot modes
0	Lendian	Endianess 0 = Big endian 1 = Little endian
End of Table 6-11		

6.1.2.4 Second-Level Bootloaders

Any of the boot modes can be used to download a second-level bootloader. A second-level bootloader allows for:

- Any level of customization to current boot methods
- Definition of a completely customized boot

6.1.3 SoC Security

The TCI6634K2K contains security architecture that allows both the C66x CorePac to perform secure accesses within the device. This security architecture is designed to provide the following:

- Customer software authentication and protection through secure boot and runtime security

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- Network interface security and network security protocol support

The TCI6634K2K supports the following security features for SECURE devices:

- Customer programmable EFUSE security keys
  - Keys to perform secure boot schemes for C66x CorePac
    - One 128-bit private customer encryption key (CEK) + 32 bits of redundancy used for symmetric encryption
    - One 256-bit public manufacturer public key (MPK) + 64 bits of redundancy
  - Additional 4K bits of one-time programmable (OTP) information to allow for enhanced customization
    - Divided into thirty-two 128-bit keys accessed through two key managers
    - Includes both customer usable and redundancy (error detection /correction) bits
- Ability to secure portions of memory / peripherals
- CorePac run-time security and memory protection
- Ability to disable JTAG access
- Hardware encryption accelerators for communication security

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6.1.3.1 System PLL Settings

The PLL default settings are determined by the BOOTMODE[7:5] bits. Table 6-12 shows the settings for various input clock frequencies. This will set the PLL to the maximum clock setting for the device.

CLK = CLKIN × (PLLM+1) ÷ (2 × (PLLD+1))

The configuration for the PASS PLL is also shown. The PASS PLL is configured with these values only if the Ethernet boot mode is selected with the input clock set to match the main PLL clock (not the SGMII SerDes clock). See Table 6-7 for details on configuring Ethernet boot mode. The output from the PASS PLL goes through an on-chip divider to reduce the frequency before reaching the NETCP. The PASS PLL generates 1050 MHz, and after the chip divider (/3), applies 350 MHz to the NETCP.

The Main PLL is controlled using a PLL controller and a chip-level MMR. The DDR3A PLL, DDR3B PLL and PASS PLL are controlled by chip level MMRs. For details on how to set up the PLL see Section 8.5 "Main PLL, DDR3A PLL, DDR3B PLL, PASS PLL and the PLL Controllers" on page 235.For details on the operation of the PLL controller module, see the *Phase Locked Loop (PLL) Controller for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

Table 6-12 System PLL Configuration

BOOTMODE [7:5]	Input Clock Freq (MHz)	800 MHz Device			1000 MHz Device			1200 MHz Device			PA = 350 MHz (1)		
		PLLD	PLLM	DSP ƒ	PLLD	PLLM	DSP ƒ	PLLD	PLLM	DSP ƒ	PLLD	PLLM	DSP ƒ (2)
0b000	50.00	0	31	800	0	39	1000	0	47	1200	0	41	1050
0b001	66.67	0	23	800.04	0	29	1000.05	0	35	1200.06	1	62	1050.053
0b010	80.00	0	19	800	0	24	1000	0	29	1200	3	104	1050
0b011	100.00	0	15	800	0	19	1000	0	23	1200	0	20	1050
0b100	156.25	0	40	800.78	4	63	1000	24	45	1197.92	24	335	1050
0b101	250.00	4	31	800	0	7	1000	4	47	1200	4	41	1050
0b110	312.50	7	40	800.78	4	31	1000	2	22	1197.92	24	167	1050
0b111	122.88	0	12	798.72	3	64	999.989	0	19	1200.80	11	204	1049.6
End of Table 6-12													

1 The PASS PLL generates 1050 MHz and is internally divided by 3 to feed 350 MHz to the packet accelerator.
2 ƒ represents frequency in MHz.

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6.2 Device Configuration

Certain device configurations like boot mode and endianess are selected at device power-on reset. The status of the peripherals (enabled/disabled) is determined after device power-on reset. By default, the peripherals on the device are disabled and need to be enabled by software before being used.

6.2.1 Device Configuration at Device Reset

The logic level present on each device configuration pin is latched at power-on reset to determine the device configuration. The logic level on the device configuration pins can be set by using external pullup/pulldown resistors or by using some control device (e.g., FPGA/CPLD) to intelligently drive these pins. When using a control device, care should be taken to ensure there is no contention on the lines when the device is out of reset. The device configuration pins are sampled during power-on reset and are driven after the reset is removed. To avoid contention, the control device must stop driving the device configuration pins of the DSP. Table 6-13 describes the device configuration pins.

Note—If a configuration pin must be routed out from the device and it is not driven (Hi-Z state), the internal pullup/pulldown (IPU/IPD) resistor should not be relied upon. TI recommends the use of an external pullup/pulldown resistor. For more detailed information on pullup/pulldown resistors and situations in which external pullup/pulldown resistors are required, see the **Pullup/PullDown Resistors** section of the **Terminals** chapter.

Table 6-13 Device Configuration Pins

Configuration Pin	Pin No.	IPD/IPU (1)	Functional Description
LENDIAN(1) (2)	F29	IPU	Device endian mode (LENDIAN) 0 = Device operates in big endian mode 1 = Device operates in little endian mode
BOOTMODE[15:0] (1) (2)	B31, E32, A31, F30, E30, F31, G30, A30, C30, D30, E29, B29, A35, D29, B30, F29	IPD	Method of boot See "Boot Modes Supported" on page 174 for more details. See the Bootloader for the C66x DSP User Guide in 1.9 "Related Documentation from Texas Instruments" on page 22for detailed information on boot configuration.
AVSIFSEL[1:0] (1) (2)	M1, M2	IPD	AVS interface selection 00 = AVS 4-pin Dual Phase VCNTL[5:2] and I^2C 01 = AVS 4-pin Single Phase VCNTL[5:2] and I^2C 1x = AVS 6-pin Single Phase VCNTL[5:0]
End of Table 6-13			

1 Internal 100-µA pulldown or pullup is provided for this terminal. In most systems, a 1-kΩ resistor can be used to oppose the IPD/IPU. For more detailed information on pulldown/pullup resistors and situations in which external pulldown/pullup resistors are required, see the **Pullup/Pulldown Resistors** section of the **Terminals** chapter.

2 These signal names are the secondary functions of these pins.

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6.2.2 Peripheral Selection After Device Reset

Several of the peripherals on the TCI6634K2K are controlled by the Power Sleep Controller (PSC). By default, the PCIe, SRIO, HyperLink, RAC, TAC, FFTC, AIF2, TCP3d, TCP3e, and VCP are held in reset and clock-gated. The memories in these modules are also in a low-leakage sleep mode. Software is required to turn these memories on. Then, the software enables the modules (turns on clocks and de-asserts reset) before these modules can be used.

If one of the above modules is used in the selected ROM boot mode, the ROM code automatically enables the module.

All other modules come up enabled by default and there is no special software sequence to enable. For more detailed information on the PSC usage, see the *Power Sleep Controller (PSC) for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

6.2.3 Device State Control Registers

The TCI6634K2K device has a set of registers that are used to control the status of its peripherals. These registers are shown in Table 6-14.

Table 6-14 Device State Control Registers (Part 1 of 4)

Address Start	Address End	Size	Acronym	Description
0x02620000	0x02620007	8B	Reserved	
0x02620008	0x02620017	16B	Reserved	
0x02620018	0x0262001B	4B	JTAGID	See section 6.2.3.3
0x0262001C	0x0262001F	4B	Reserved	
0x02620020	0x02620023	4B	DEVSTAT	See section 6.2.3.1
0x02620024	0x02620037	20B	Reserved	
0x02620038	0x0262003B	4B	KICK0	See section 6.2.3.4
0x0262003C	0x0262003F	4B	KICK1	
0x02620040	0x02620043	4B	DSP_BOOT_ADDR0	The boot address for C66x CorePac0
0x02620044	0x02620047	4B	DSP_BOOT_ADDR1	The boot address for C66x CorePac1
0x02620048	0x0262004B	4B	DSP_BOOT_ADDR2	The boot address for C66x CorePac2
0x0262004C	0x0262004F	4B	DSP_BOOT_ADDR3	The boot address for C66x CorePac3
0x02620050	0x02620053	4B	DSP_BOOT_ADDR4	The boot address for C66x CorePac4
0x02620054	0x02620057	4B	DSP_BOOT_ADDR5	The boot address for C66x CorePac5
0x02620058	0x0262005B	4B	DSP_BOOT_ADDR6	The boot address for C66x CorePac6
0x0262005C	0x0262005F	4B	DSP_BOOT_ADDR7	The boot address for C66x CorePac7
0x02620060	0x026200DF	128B	Reserved	
0x026200E0	0x0262010F	48B	Reserved	
0x02620110	0x02620117	8B	MACID	See section 8.17 "Network Coprocessor Gigabit Ethernet (GbE) Switch Subsystem" on page 267
0x02620118	0x0262012F	24B	Reserved	
0x02620130	0x02620133	4B	LRSTNMIPINSTAT_CLR	See section 6.2.3.6
0x02620134	0x02620137	4B	RESET_STAT_CLR	See section 6.2.3.8
0x02620138	0x0262013B	4B	Reserved	
0x0262013C	0x0262013F	4B	BOOTCOMPLETE	See section 6.2.3.9
0x02620140	0x02620143	4B	Reserved	
0x02620144	0x02620147	4B	RESET_STAT	See section 6.2.3.7
0x02620148	0x0262014B	4B	LRSTNMIPINSTAT	See section 6.2.3.5
0x0262014C	0x0262014F	4B	DEVCFG	See section 6.2.3.2

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Table 6-14 Device State Control Registers (Part 2 of 4)

Address Start	Address End	Size	Acronym	Description
0x02620150	0x02620153	4B	PWRSTATECTL	See section 6.2.3.10
0x02620154	0x02620157	4B	Reserved	
0x02620158	0x0262015B	4B	Reserved	
0x0262015C	0x0262015F	4B	Reserved	
0x02620160	0x02620160	4B	Reserved	
0x02620164	0x02620167	4B	Reserved	
0x02620168	0x0262016B	4B	Reserved	
0x0262016C	0x0262017F	20B	Reserved	
0x02620180	0x02620183	4B	SmartReflex Class0	TBD
0x02620184	0x0262018F	12B	Reserved	
0x02620190	0x02620193	4B	Reserved	
0x02620194	0x02620197	4B	Reserved	
0x02620198	0x0262019B	4B	Reserved	
0x0262019C	0x0262019F	4B	Reserved	
0x026201A0	0x026201A3	4B	Reserved	
0x026201A4	0x026201A7	4B	Reserved	
0x026201A8	0x026201AB	4B	Reserved	
0x026201AC	0x026201AF	4B	Reserved	
0x026201B0	0x026201B3	4B	Reserved	
0x026201B4	0x026201B7	4B	Reserved	
0x026201B8	0x026201BB	4B	Reserved	
0x026201BC	0x026201BF	4B	Reserved	
0x026201C0	0x026201C3	4B	Reserved	
0x026201C4	0x026201C7	4B	Reserved	
0x026201C8	0x026201CB	4B	Reserved	
0x026201CC	0x026201CF	4B	Reserved	
0x026201D0	0x026201FF	48B	Reserved	
0x02620200	0x02620203	4B	NMIGR0	See section 6.2.3.11
0x02620204	0x02620207	4B	NMIGR1	
0x02620208	0x0262020B	4B	NMIGR2	
0x0262020C	0x0262020F	4B	NMIGR3	
0x02620210	0x02620213	4B	NMIGR4	
0x02620214	0x02620217	4B	NMIGR5	
0x02620218	0x0262021B	4B	NMIGR6	
0x0262021C	0x0262021F	4B	NMIGR7	
0x02620220	0x0262023F	32B	Reserved	

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Table 6-14 Device State Control Registers (Part 3 of 4)

Address Start	Address End	Size	Acronym	Description
0x02620240	0x02620243	4B	IPCGR0	See section 6.2.3.12
0x02620244	0x02620247	4B	IPCGR1	
0x02620248	0x0262024B	4B	IPCGR2	
0x0262024C	0x0262024F	4B	IPCGR3	
0x02620250	0x02620253	4B	IPCGR4	
0x02620254	0x02620257	4B	IPCGR5	
0x02620258	0x0262025B	4B	IPCGR6	
0x0262025C	0x0262025F	4B	IPCGR7	
0x02620260	0x02620263	4B	IPCGR8	
0x02620264	0x02620267	4B	IPCGR9	
0x02620268	0x0262026B	4B	IPCGR10	
0x0262026C	0x0262026F	4B	IPCGR11	
0x02620270	0x0262027B	12B	Reserved	
0x0262027C	0x0262027F	4B	IPCGRH	See section 6.2.3.14
0x02620280	0x02620283	4B	IPCAR0	See section 6.2.3.13
0x02620284	0x02620287	4B	IPCAR1	
0x02620288	0x0262028B	4B	IPCAR2	
0x0262028C	0x0262028F	4B	IPCAR3	
0x02620290	0x02620293	4B	IPCAR4	
0x02620294	0x02620297	4B	IPCAR5	
0x02620298	0x0262029B	4B	IPCAR6	
0x0262029C	0x0262029F	4B	IPCAR7	
0x026202A0	0x026202A3	4B	IPCAR8	
0x026202A4	0x026202A7	4B	IPCAR9	
0x026202A8	0x026202AB	4B	IPCAR10	
0x026202AC	0x026202AF	4B	IPCAR11	
0x026202B0	0x026202BB	12B	Reserved	
0x026202BC	0x026202BF	4B	IPCARH	See section 6.2.3.15
0x026202C0	0x026202FF	64B	Reserved	
0x02620300	0x02620303	4B	TINPSEL	See section 6.2.3.16
0x02620304	0x02620307	4B	TOUTPSEL	See section 6.2.3.17
0x02620308	0x0262030B	4B	RSTMUX0	See section 6.2.3.18
0x0262030C	0x0262030F	4B	RSTMUX1	
0x02620310	0x02620313	4B	RSTMUX2	
0x02620314	0x02620317	4B	RSTMUX3	
0x02620318	0x0262031B	4B	RSTMUX4	
0x0262031C	0x0262031F	4B	RSTMUX5	
0x02620320	0x02620323	4B	RSTMUX6	
0x02620324	0x02620327	4B	RSTMUX7	
0x02620328	0x0262032B	4B	RSTMUX8	
0x0262032C	0x0262032F	4B	RSTMUX9	
0x02620330	0x02620333	4B	RSTMUX10	
0x02620334	0x02620337	4B	RSTMUX11	
0x02620338	0x0262034F	4B	Reserved	

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Table 6-14 Device State Control Registers (Part 4 of 4)

Address Start	Address End	Size	Acronym	Description
0x02620350	0x02620353	4B	MAINPLLCTL0	See section 8.5 "Main PLL, DDR3A PLL, DDR3B PLL, PASS PLL and the PLL Controllers" on page 235
0x02620354	0x02620357	4B	MAINPLLCTL1	
0x02620358	0x0262035B	4B	PASSPLLCTL0	See section 8.7 "PASS PLL" on page 251
0x0262035C	0x0262035F	4B	PASSPLLCTL1	
0x02620360	0x02620363	4B	DDR3APLLCTL0	See section 8.6 "DDR3A PLL and DDR3B PLL" on page 249
0x02620364	0x02620367	4B	DDR3APLLCTL1	
0x02620368	0x0262036B	4B	DDR3BPLLCTL0	See section 8.6 "DDR3A PLL and DDR3B PLL" on page 249
0x0262036C	0x0262036F	4B	DDR3BPLLCTL1	
0x02620370	0x02620373	4B	Reserved	
0x02620374	0x02620377	4B	Reserved	
0x02620378	0x0262039B	132B	Reserved	
0x0262039C	0x0262039F	4B	Reserved	
0x02620400	0x026205FF	256B	Reserved	
0x02620600	0x026206FF	256B	Reserved	
0x02620700	0x02620703	4B	CHIP_MISC_CTL0	See section "Chip Miscellaneous Control (CHIP_MISC_CTL0) Register" on page 205
0x02620704	0x0262070F	12B	Reserved	
0x02620710	0x02620713	4B	SYSENDSTAT	See section "System Endian Status Register (SYSENDSTAT)" on page 206
0x02620714	0x02620717	4B	PLLLOCK_PINCTL	See section "PLL Lock Pin Control (PLLLOCK_PINCTL) Register" on page 206
0x02620718	0x0262071B	4B	PLLLOCK_STAT	See section "PLL Lock Status (PLLLOCK_STAT) Register" on page 208
0x0262071C	0x0262071F	4B	PLLLOCK_EVAL	See section "PLL Lock Evaluation (PLLLOCK_EVAL) Register" on page 210
0x02620720	0x0262072F	16B	Reserved	
0x02620730	0x02620733	4B	SYNCECLK_PINCTL	See section "SYNECLK_PINCTL Register" on page 210
0x02620734	0x02620737	4B	Reserved	
0x02620738	0x0262074F	24B	Reserved	
0x02620750	0x026207FF	176B	Reserved	
0x02620800	0x02620FFF	2048B	Reserved	
End of Table 6-14				

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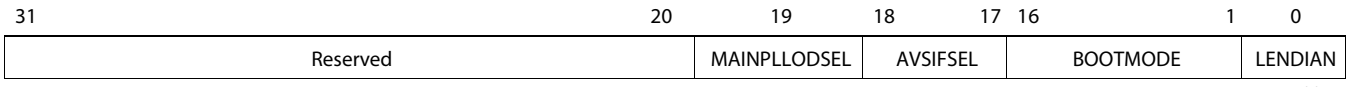
6.2.3.1 Device Status (DEVSTAT) Register

The Device Status Register depicts device configuration selected upon a power-on reset by the $\overline{\text{POR}}$ or $\overline{\text{RESETFULL}}$ pin. Once set, these bits remain set until a power-on reset. The Device Status Register is shown in the figure below.

Figure 6-11 Device Status Register



Legend: R = Read only; RW = Read/Write; -*n* = value after reset

1 x indicates the bootstrap value latched via the external pin

Table 6-15 Device Status Register Field Descriptions

Bit	Field	Description
31-20	Reserved	Reserved
19	MAINPLLODSEL	Main PLL Output divider select 0 = Main PLL output divider needs to be set to 2 by BOOTROM 1 = Main PLL output divider needs to be set to 1 by BOOTROM
18-17	AVSIFSEL	AVS interface selection 00 = AVS 4-bit Dual Phase VCNTL[5:2] and I^2C 01 = AVS 4-bit Single Phase VCNTL[5:2] and I^2C 1x = AVS 6-bit Single Phase VCNTL[5:0]
16-1	BOOTMODE	Determines the bootmode configured for the device. For more information on bootmode, see Section 6.1.2 "Boot Modes Supported" on page 174 and see the *Bootloader for the C66x DSP User Guide* in1.9 "Related Documentation from Texas Instruments" on page 22.
0	LENDIAN	Device endian mode (LENDIAN) — shows the status of whether the system is operating in big endian mode or little endian mode (default). 0 = System is operating in big endian mode 1 = System is operating in little endian mode (default)
End of Table 6-15		

6.2.3.2 Device Configuration Register

The Device Configuration Register is one-time writeable through software. The register is reset on all hard resets and is locked after the first write. The Device Configuration Register is shown in Figure 6-12 and described in Table 6-16.

Figure 6-12 Device Configuration Register (DEVCFG)

31	3	2	1	0
Reserved		PCIESSMODE		SYSCLKOUTEN
R-0		R/W-00		R/W-1

Legend: R = Read only; RW = Read/Write; -n = value after reset

Table 6-16 Device Configuration Register Field Descriptions

Bit	Field	Description
31-3	Reserved	Reserved. Read only, writes have no effect.
2-1	PCIESSMODE	Device Type Input of PCIeSS 00 = Endpoint 01 = Legacy Endpoint 10 = Rootcomplex 11 = Reserved)
0	SYSCLKOUTEN	SYSCLKOUT enable 0 = No clock output 1 = Clock output enabled (default)
End of Table 6-16		

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6.2.3.3 JTAG ID (JTAGID) Register Description

The JTAG ID register is a read-only register that identifies to the customer the JTAG/Device ID. For the device, the JTAG ID register resides at address location 0x02620018. The JTAG ID Register is shown below.

Figure 6-13 JTAG ID (JTAGID) Register

31–28	27–12	11–1	0
VARIANT	PART NUMBER	MANUFACTURER	LSB
R-xxxx	R-1011 1001 1000 0001	R-0000 0010 111	R-1

Legend: RW = Read/Write; R = Read only; -n = value after reset

Table 6-17 JTAG ID Register Field Descriptions

Bit	Field	Value	Description
31-28	VARIANT	xxxx	Variant value
27-12	PART NUMBER	1011 1001 1000 0001	Part Number for boundary scan
11-1	MANUFACTURER	0000 0010 111	Manufacturer
0	LSB	1	This bit is read as a 1 for TCI6634K2K
End of Table 6-17			

Note—The value of the VARIANT and PART NUMBER fields depends on the silicon revision being used. See the Silicon Errata for details.

6.2.3.4 Kicker Mechanism (KICK0 and KICK1) Register

The Bootcfg module contains a kicker mechanism to prevent spurious writes from changing any of the Bootcfg MMR (memory mapped registers) values. When the kicker is locked (which it is initially after power on reset), none of the Bootcfg MMRs are writable (they are only readable). This mechanism requires an MMR write to each of the KICK0 and KICK1 registers with exact data values before the kicker lock mechanism is unlocked. See Table 6-14 "Device State Control Registers" on page 186 for the address location. Once released, all the Bootcfg MMRs having write permissions are writable (the read only MMRs are still read only). The KICK0 data is 0x83e70b13. The KICK1 data is 0x95a4f1e0. Writing any other data value to either of these kick MMRs locks the kicker mechanism and blocks writes to Bootcfg MMRs. To ensure protection to all Bootcfg MMRs, software must always re-lock the kicker mechanism after completing the MMR writes.

6.2.3.5 LRESETNMI PIN Status (LRSTNMIPINSTAT) Register

The LRSTNMIPINSTAT Register latches the status of $\overline{\text{LRESET}}$ and $\overline{\text{NMI}}$ based on the setting of CORESEL[2:0]. The LRESETNMI PIN Status Register is shown in the figure and table below.

Figure 6-14 LRESETNMI PIN Status Register (LRSTNMIPINSTAT)

31–24	23	22	21	20	19	18	17	16	15–8	7	6	5	4	3	2	1	0
Reserved	NMI7	NMI6	NMI5	NMI4	NMI3	NMI2	NMI1	NMI0	Reserved	LR7	LR6	LR5	LR4	LR3	LR2	LR1	LR0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Legend: R = Read only; -*n* = value after reset

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Table 6-18 LRESETNMI PIN Status Register Field Descriptions

Bit	Field	Description
31-24	Reserved	Reserved
23	NMI7	C66x CorePac7 in NMI
22	NMI6	C66x CorePac6 in NMI
21	NMI5	C66x CorePac5 in NMI
20	NM4	C66x CorePac4 in NMI
19	NMI3	C66x CorePac3 in NMI
18	NMI2	C66x CorePac2 in NMI
17	NMI1	C66x CorePac1 in NMI
16	NMI0	C66x CorePac0 in NMI
15-8	Reserved	Reserved
7	LR7	C66x CorePac7 in Local Reset
6	LR6	C66x CorePac6 in Local Reset
5	LR5	C66x CorePac5 in Local Reset
4	LR4	C66x CorePac4 in Local Reset
3	LR3	C66x CorePac3 in Local Reset
2	LR2	C66x CorePac2 in Local Reset
1	LR1	C66x CorePac1 in Local Reset
0	LR0	C66x CorePac0 in Local Reset
End of Table 6-18		

6.2.3.6 LRESETNMI PIN Status Clear (LRSTNMIPINSTAT_CLR) Register

The LRSTNMIPINSTAT_CLR Register clears the status of $\overline{\text{LRESET}}$ and $\overline{\text{NMI}}$ based on CORESEL[2:0]. The LRESETNMI PIN Status Clear Register is shown in the figure and table below.

Figure 6-15 LRESETNMI PIN Status Clear Register (LRSTNMIPINSTAT_CLR)

31 24	23	22	21	20	19	18	17	16	15 8	7	6	5	4	3	2	1	0
Reserved	NMI7	NMI6	NMI5	NMI4	NMI3	NMI2	NMI1	NMI0	Reserved	LR7	LR6	LR5	LR4	LR3	LR2	LR1	LR0
R-0	WC,+0	WC,+0	WC,+0	WC,+0	WC,+0	WC,+0	WC,+0	WC,+0	R-0	WC,+0	WC,+0	WC,+0	WC,+0	WC,+0	WC,+0	WC,+0	WC,+0

Legend: R = Read only; -*n* = value after reset; WC = Write 1 to Clear

Table 6-19 LRESETNMI PIN Status Clear Register Field Descriptions (Part 1 of 2)

Bit	Field	Description
31-24	Reserved	Reserved
23	NMI7	C66x CorePac7 in NMI Clear
22	NM6	C66x CorePac6 in NMI Clear
21	NMI5	C66x CorePac5 in NMI Clear
20	NMI4	C66x CorePac4 in NMI Clear
19	NMI3	C66x CorePac3 in NMI Clear
18	NMI2	C66x CorePac2 in NMI Clear
17	NMI1	C66x CorePac1 in NMI Clear
16	NMI0	C66x CorePac0 in NMI Clear
15-8	Reserved	Reserved

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Table 6-19 LRESETNMI PIN Status Clear Register Field Descriptions (Part 2 of 2)

Bit	Field	Description
7	LR7	C66x CorePac7 in Local Reset Clear
6	LR6	C66x CorePac6 in Local Reset Clear
5	LR5	C66x CorePac5 in Local Reset Clear
4	LR4	C66x CorePac4 in Local Reset Clear
3	LR3	C66x CorePac3 in Local Reset Clear
2	LR2	C66x CorePac2 in Local Reset Clear
1	LR1	C66x CorePac1 in Local Reset Clear
0	LR0	C66x CorePac0 in Local Reset Clear
End of Table 6-19		

6.2.3.7 Reset Status (RESET_STAT) Register

The Reset Status Register (RESET_STAT) captures the status of local reset (LRx) for each of the cores and also the global device reset (GR). Software can use this information to take different device initialization steps.

- **In case of local reset:** The LRx bits are written as 1 and the GR bit is written as 0 only when the C66x CorePac receives a local reset without receiving a global reset.
- **In case of global reset:** The LRx bits are written as 0 and the GR bit is written as 1 only when a global reset is asserted.

The Reset Status Register is shown in the figure and table below.

Figure 6-16 Reset Status Register (RESET_STAT)

31	30 8	7	6	5	4	3	2	1	0
GR	Reserved	LR7	LR6	LR5	LR4	LR3	LR2	LR1	LR0
R, +1	R, + 000 0000 0000 0000 0000 0000	R,+0	R,+0	R,+0	R,+0	R,+0	R,+0	R,+0	R,+0

Legend: R = Read only; -*n* = value after reset

Table 6-20 Reset Status Register Field Descriptions (Part 1 of 2)

Bit	Field	Description
31	GR	Global reset status 0 = Device has not received a global reset. 1 = Device received a global reset.
30-8	Reserved	Reserved.
7	LR7	C66x CorePac7 reset status 0 = C66x CorePac7 has not received a local reset. 1 = C66x CorePac7 received a local reset.
6	LR6	C66x CorePac6 reset status 0 = C66x CorePac6 has not received a local reset. 1 = C66x CorePac6 received a local reset.
5	LR5	C66x CorePac5 reset status 0 = C66x CorePac5 has not received a local reset. 1 = C66x CorePac5 received a local reset.
4	LR4	C66x CorePac4 reset status 0 = C66x CorePac4 has not received a local reset. 1 = C66x CorePac4received a local reset.

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Table 6-20 Reset Status Register Field Descriptions (Part 2 of 2)

Bit	Field	Description
3	LR3	C66x CorePac3 reset status 0 = C66x CorePac3 has not received a local reset. 1 = C66x CorePac3 received a local reset.
2	LR2	C66x CorePac2 reset status 0 = C66x CorePac2 has not received a local reset. 1 = C66x CorePac2 received a local reset.
1	LR1	C66x CorePac1 reset status 0 = C66x CorePac1 has not received a local reset. 1 = C66x CorePac1 received a local reset.
0	LR0	C66x CorePac0 reset status 0 = C66x CorePac0 has not received a local reset. 1 = C66x CorePac0 received a local reset.
End of Table 6-20		

6.2.3.8 Reset Status Clear (RESET_STAT_CLR) Register

The RESET_STAT bits can be cleared by writing 1 to the corresponding bit in the RESET_STAT_CLR register. The Reset Status Clear Register is shown in the figure and table below.

Figure 6-17 Reset Status Clear Register (RESET_STAT_CLR)

31	30 8	7	6	5	4	3	2	1	0
GR	Reserved	LR7	LR6	LR5	LR4	LR3	LR2	LR1	LR0
RW, +0	R, + 000 0000 0000 0000 0000 0000	RW,+0	RW,+0	RW,+0	RW,+0	RW,+0	RW,+0	RW,+0	RW,+0

Legend: R = Read only; RW = Read/Write; -*n* = value after reset

Table 6-21 Reset Status Clear Register Field Descriptions (Part 1 of 2)

Bit	Field	Description
31	GR	Global reset clear bit 0 = Writing a 0 has no effect. 1 = Writing a 1 to the GR bit clears the corresponding bit in the RESET_STAT register.
30-8	Reserved	Reserved.
7	LR7	C66x CorePac7 reset clear bit 0 = Writing a 0 has no effect. 1 = Writing a 1 to the LR7 bit clears the corresponding bit in the RESET_STAT register.
6	LR6	C66x CorePac6 reset clear bit 0 = Writing a 0 has no effect. 1 = Writing a 1 to the LR6 bit clears the corresponding bit in the RESET_STAT register.
5	LR5	C66x CorePac5 reset clear bit 0 = Writing a 0 has no effect. 1 = Writing a 1 to the LR5 bit clears the corresponding bit in the RESET_STAT register.
4	LR4	C66x CorePac4 reset clear bit 0 = Writing a 0 has no effect. 1 = Writing a 1 to the LR4 bit clears the corresponding bit in the RESET_STAT register.
3	LR3	C66x CorePac3 reset clear bit 0 = Writing a 0 has no effect. 1 = Writing a 1 to the LR3 bit clears the corresponding bit in the RESET_STAT register.
2	LR2	C66x CorePac2 reset clear bit 0 = Writing a 0 has no effect. 1 = Writing a 1 to the LR2 bit clears the corresponding bit in the RESET_STAT register.

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Table 6-21 Reset Status Clear Register Field Descriptions (Part 2 of 2)

Bit	Field	Description
1	LR1	C66x CorePac1 reset clear bit 0 = Writing a 0 has no effect. 1 = Writing a 1 to the LR1 bit clears the corresponding bit in the RESET_STAT register.
0	LR0	C66x CorePac0 reset clear bit 0 = Writing a 0 has no effect. 1 = Writing a 1 to the LR0 bit clears the corresponding bit in the RESET_STAT register.
End of Table 6-21		

6.2.3.9 Boot Complete (BOOTCOMPLETE) Register

The BOOTCOMPLETE register controls the BOOTCOMPLETE pin status to indicate the completion of the ROM booting process. The Boot Complete Register is shown in the figure and table below.

Figure 6-18 Boot Complete Register (BOOTCOMPLETE)

31 8	7	6	5	4	3	2	1	0
Reserved	BC7	BC6	BC5	BC4	BC3	BC	BC1	BC0
R, + 0000 0000 0000 0000 0000 0000	RW,+0	RW,+0	RW,+0	RW,+0	RW,+0	RW,+0	RW,+0	RW,+0

Legend: R = Read only; RW = Read/Write; *-n* = value after reset

Table 6-22 Boot Complete Register Field Descriptions

Bit	Field	Description
31-8	Reserved	Reserved.
7	BC7	C66x CorePac7 boot status 0 = C66x CorePac 7 boot NOT complete 1 = C66x CorePac 7 boot complete
6	BC6	C66x CorePac6 boot status 0 = C66x CorePac 6 boot NOT complete 1 = C66x CorePac 6 boot complete
5	BC5	C66x CorePac5 boot status 0 = C66x CorePac 5 boot NOT complete 1 = C66x CorePac 5 boot complete
4	BC4	C66x CorePac4 boot status 0 = C66x CorePac 4 boot NOT complete 1 = C66x CorePac 4 boot complete
3	BC3	C66x CorePac 3 boot status 0 = C66x CorePac 3 boot NOT complete 1 = C66x CorePac 3 boot complete
2	BC2	C66x CorePac2 boot status 0 = C66x CorePac 2 boot NOT complete 1 = C66x CorePac 2 boot complete
1	BC1	C66x CorePac1 boot status 0 = C66x CorePac 1 boot NOT complete 1 = C66x CorePac 1 boot complete
0	BC0	C66x CorePac0 boot status 0 = C66x CorePac 0 boot NOT complete 1 = C66x CorePac 0 boot complete
End of Table 6-22		

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The BCx bit indicates the boot complete status of the corresponding C66x CorePac. All BCx bits are sticky bits — that is, they can be set only once by the software after device reset and they will be cleared to 0 on all device resets (warm reset and power-on reset).

Boot ROM code is implemented such that each C66x CorePac sets its corresponding BCx bit immediately before branching to the predefined location in memory.

6.2.3.10 Power State Control (PWRSTATECTL) Register

The Power State Control Register (PWRSTATECTL) is controlled by the software to indicate the power-saving mode. Under ROM code, the C66x CorePac reads this register to differentiate between the various power saving modes. This register is cleared only by POR and is not changed by any other device reset. See the *Hardware Design Guide for KeyStone Devices* in1.9 "Related Documentation from Texas Instruments" on page 22 for more information. The PWRSTATECTL Register is shown in Figure 6-19 and described in Table 6-23.

Figure 6-19 Power State Control Register (PWRSTATECTL)

31	3	2	1	0
GENERAL_PURPOSE		HIBERNATION_MODE	HIBERNATION	STANDBY
RW, +0000 0000 0000 0000 0000 0000 0000 0		RW,+0	RW,+0	RW,+0

Legend: RW = Read/Write; -*n* = value after reset

Table 6-23 Power State Control Register Field Descriptions

Bit	Field	Description
31-3	GENERAL_PURPOSE	Used to provide a start address for execution out of the hibernation modes. See the *Bootloader for the C66x DSP User Guide* in1.9 "Related Documentation from Texas Instruments" on page 22.
2	HIBERNATION_MODE	Indicates whether the device is in hibernation mode 1 or mode 2. 0 = Hibernation mode 1 1 = Hibernation mode 2
1	HIBERNATION	Indicates whether the device is in hibernation mode or not. 0 = Not in hibernation mode 1 = Hibernation mode
0	STANDBY	Indicates whether the device is in standby mode or not. 0 = Not in standby mode 1 = Standby mode
End of Table 6-23		

6.2.3.11 NMI Event Generation to C66x CorePac (NMIGRx) Register

NMIGRx registers generate NMI events to the corresponding C66x CorePac. The TCI6634 has eight NMIGRx registers (NMIGR0 through NMIGR7). The NMIGR0 register generates an NMI event to C66x CorePac0, the NMIGR1 register generates an NMI event to C66x CorePac1, and so on. Writing a 1 to the NMIG field generates an NMI pulse. Writing a 0 has no effect and Reads return 0 and have no other effect. The NMI event generation to the C66x CorePac is shown in Figure 6-20 and described in Table 6-24.

Figure 6-20 NMI Generation Register (NMIGRx)

31	1	0
Reserved		NMIG
R, +0000 0000 0000 0000 0000 0000 0000 000		RW,+0

Legend: RW = Read/Write; -*n* = value after reset

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Table 6-24 NMI Generation Register Field Descriptions

Bit	Field	Description
31-1	Reserved	Reserved
0	NMIG	Reads return 0 Writes: 0 = No effect 1 = Creates NMI pulse to the corresponding C66x CorePac — C66x CorePac0 for NMIGR0, etc.
End of Table 6-24		

6.2.3.12 IPC Generation (IPCGRx) Registers

The IPCGRx Registers facilitate inter-C66x CorePac interrupts.

The TCI6634K2K has eight IPCGRx registers (IPCGR0 through IPCG7). These registers can be used by external hosts or CorePacs to generate interrupts to other CorePacs. A write of 1 to the IPCG field of the IPCGRx register generates an interrupt pulse to the C66x CorePacx (0 <= x <= 7).

These registers also provide a *Source ID* facility identifying up to 28 different sources of interrupts. Allocation of source bits to source processor and meaning is entirely based on software convention. The register field descriptions are given in the following tables. There can be numerous sources for these registers as this is completely controlled by software. Any master that has access to BOOTCFG module space can write to these registers. The IPC Generation Register is shown in Figure 6-21 and described in Table 6-25.

Figure 6-21 IPC Generation Registers (IPCGRx)

31	30	29	28	27 – 8	7	6	5	4	3 – 1	0
SRCS27	SRCS26	SRCS25	SRCS24	SRCS23 – SRCS4	SRCS3	SRCS2	SRCS1	SRCS0	Reserved	IPCG
RW +0	RW +0	RW +0	RW +0	RW +0 (per bit field)	RW +0	RW +0	RW +0	RW +0	R, +000	RW +0

Legend: R = Read only; RW = Read/Write; *-n* = value after reset

Table 6-25 IPC Generation Registers Field Descriptions

Bit	Field	Description
31-4	SRCSx	Reads return current value of internal register bit. Writes: 0 = No effect 1 = Sets both SRCSx and the corresponding SRCCx.
3-1	Reserved	Reserved
0	IPCG	Reads return 0. Writes: 0 = No effect 1 = Creates an inter-DSP interrupt.
End of Table 6-25		

6.2.3.13 IPC Acknowledgement (IPCARx) Registers

The IPCARx registers facilitate inter-CorePac interrupt acknowledgement.

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The TCI6634K2K has eight IPCARx (IPCAR0 through IPCAR7) registers. These registers also provide a *Source ID* facility by which up to 28 different sources of interrupts can be identified. Allocation of source bits to source processor and meaning is entirely based on software convention. The register field descriptions are given in the following tables. Virtually anything can be a source for these registers as this is completely controlled by software. Any master that has access to BOOTCFG module space can write to these registers. The IPC Acknowledgement Register is shown in the following figure and table.

Figure 6-22 IPC Acknowledgement Registers (IPCARx)

31	30	29	28	27 – 8	7	6	5	4	3 – 0
SRCC27	SRCC26	SRCC25	SRCC24	SRCC23 – SRCC4	SRCC3	SRCC2	SRCC1	SRCC0	Reserved
RW +0	RW +0	RW +0	RW +0	RW +0 (per bit field)	RW +0	RW +0	RW +0	RW +0	R, +0000

Legend: R = Read only; RW = Read/Write; -*n* = value after reset

Table 6-26 IPC Acknowledgement Registers Field Descriptions

Bit	Field	Description
31-4	SRCCx	Reads return current value of internal register bit. Writes: 0 = No effect 1 = Clears both SRCCx and the corresponding SRCSx
3-0	Reserved	Reserved
End of Table 6-26		

6.2.3.14 IPC Generation Host (IPCGRH) Register

The IPCGRH register facilitates interrupts to external hosts. Operation and use of the IPCGRH register is the same as for other IPCGR registers. The interrupt output pulse created by the IPCGRH register appears on device pin HOUT.

The host interrupt output pulse is stretched so that it is asserted for four bootcfg clock cycles (SYSCLK1/6) followed by a deassertion of four bootcfg clock cycles. Generating the pulse results in a pulse-blocking window that is eight SYSCLK1/6-cycles long. Back-to-back writes to the IPCRGH register with the IPCG bit (bit 0) set, generates only one pulse if the back-to-back writes to IPCGRH are less than the eight SYSCLK1/6 cycle window — the pulse blocking window. To generate back-to-back pulses, the back-to-back writes to the IPCGRH register must be written after the eight SYSCLK1/6 cycle pulse-blocking window has elapsed. The IPC Generation Host Register is shown in Figure 6-23 and described in Table 6-27.

Figure 6-23 IPC Generation Registers (IPCGRH)

31	30	29	28	27 – 8	7	6	5	4	3 – 1	0
SRCS27	SRCS26	SRCS25	SRCS24	SRCS23 – SRCS4	SRCS3	SRCS2	SRCS1	SRCS0	Reserved	IPCG
RW +0	RW +0	RW +0	RW +0	RW +0 (per bit field)	RW +0	RW +0	RW +0	RW +0	R, +000	RW +0

Legend: R = Read only; RW = Read/Write; -*n* = value after reset

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Table 6-27 IPC Generation Registers Field Descriptions

Bit	Field	Description
31-4	SRCSx	Reads return current value of internal register bit. Writes: 0 = No effect 1 = Sets both SRCSx and the corresponding SRCCx.
3-1	Reserved	Reserved
0	IPCG	Reads return 0. Writes: 0 = No effect 1 = Creates an interrupt pulse on device pin (host interrupt/event output in HOUT pin)
End of Table 6-27		

6.2.3.15 IPC Acknowledgement Host (IPCARH) Register

The IPCARH register facilitates external host interrupts. Operation and use of the IPCARH register is the same as for other IPCAR registers. The IPC Acknowledgement Host Register is shown in Figure 6-24 and described in Table 6-28.

Figure 6-24 IPC Acknowledgement Register (IPCARH)

31	30	29	28	27 – 8	7	6	5	4	3 – 0
SRCC27	SRCC26	SRCC25	SRCC24	SRCC23 – SRCC4	SRCC3	SRCC2	SRCC1	SRCC0	Reserved
RW +0	RW +0	RW +0	RW +0	RW +0 (per bit field)	RW +0	RW +0	RW +0	RW +0	R, +0000

Legend: R = Read only; RW = Read/Write; *-n* = value after reset

Table 6-28 IPC Acknowledgement Register Field Descriptions

Bit	Field	Description
31-4	SRCCx	Reads the return current value of the internal register bit. Writes: 0 = No effect 1 = Clears both SRCCx and the corresponding SRCSx
3-0	Reserved	Reserved
End of Table 6-28		

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6.2.3.16 Timer Input Selection Register (TINPSEL)

The Timer Input Selection Register selects timer inputs and is shown in Figure 6-25 and described in Table 6-29.

Figure 6-25 Timer Input Selection Register (TINPSEL)

31	30	29	28	27	26	25	24
TINPHSEL15	TINPLSEL15	TINPHSEL14	TINPLSEL14	TINPHSEL13	TINPLSEL13	TINPHSEL12	TINPLSEL12
RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0
23	22	21	20	19	18	17	16
TINPHSEL11	TINPLSEL11	TINPHSEL10	TINPLSEL10	TINPHSEL9	TINPLSEL9	TINPHSEL8	TINPLSEL8
RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0
15	14	13	12	11	10	9	8
TINPHSEL7	TINPLSEL7	TINPHSEL6	TINPLSEL6	TINPHSEL5	TINPLSEL5	TINPHSEL4	TINPLSEL4
RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0
7	6	5	4	3	2	1	0
TINPHSEL3	TINPLSEL3	TINPHSEL2	TINPLSEL2	TINPHSEL1	TINPLSEL1	TINPHSEL0	TINPLSEL0
RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0

Legend: R = Read only; RW = Read/Write; -*n* = value after reset

Table 6-29 Timer Input Selection Field Description (Part 1 of 3)

Bit	Field	Description
31	TINPHSEL15	Input select for TIMER15 high. 0 = TIMI0 1 = TIMI1
30	TINPLSEL15	Input select for TIMER15 low. 0 = TIMI0 1 = TIMI1
29	TINPHSEL14	Input select for TIMER14 high. 0 = TIMI0 1 = TIMI1
28	TINPLSE14	Input select for TIMER14 low. 0 = TIMI0 1 = TIMI1
27	TINPHSEL13	Input select for TIMER13 high. 0 = TIMI0 1 = TIMI1
26	TINPLSEL13	Input select for TIMER13 low. 0 = TIMI0 1 = TIMI1
25	TINPHSEL12	Input select for TIMER12 high. 0 = TIMI0 1 = TIMI1
24	TINPLSEL12	Input select for TIMER12low. 0 = TIMI0 1 = TIMI1
23	TINPHSEL11	Input select for TIMER11 high. 0 = TIMI0 1 = TIMI1

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Table 6-29 Timer Input Selection Field Description (Part 2 of 3)

Bit	Field	Description
22	TINPLSEL11	Input select for TIMER11 low. 0 = TIMI0 1 = TIMI1
21	TINPHSEL10	Input select for TIMER10 high. 0 = TIMI0 1 = TIMI1
20	TINPLSEL10	Input select for TIMER10 low. 0 = TIMI0 1 = TIMI1
19	TINPHSEL9	Input select for TIMER9 high. 0 = TIMI0 1 = TIMI1
18	TINPLSEL9	Input select for TIMER9 low. 0 = TIMI0 1 = TIMI1
17	TINPHSEL8	Input select for TIMER8 high. 0 = TIMI0 1 = TIMI1
16	TINPLSEL8	Input select for TIMER8 low. 0 = TIMI0 1 = TIMI1
15	TINPHSEL7	Input select for TIMER7 high. 0 = TIMI0 1 = TIMI1
14	TINPLSEL7	Input select for TIMER7 low. 0 = TIMI0 1 = TIMI1
13	TINPHSEL6	Input select for TIMER6 high. 0 = TIMI0 1 = TIMI1
12	TINPLSEL6	Input select for TIMER6 low. 0 = TIMI0 1 = TIMI1
11	TINPHSEL5	Input select for TIMER5 high. 0 = TIMI0 1 = TIMI1
10	TINPLSEL5	Input select for TIMER5 low. 0 = TIMI0 1 = TIMI1
9	TINPHSEL4	Input select for TIMER4 high. 0 = TIMI0 1 = TIMI1
8	TINPLSEL4	Input select for TIMER4 low. 0 = TIMI0 1 = TIMI1
7	TINPHSEL3	Input select for TIMER3 high. 0 = TIMI0 1 = TIMI1
6	TINPLSEL3	Input select for TIMER3 low. 0 = TIMI0 1 = TIMI1

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Table 6-29 Timer Input Selection Field Description (Part 3 of 3)

Bit	Field	Description
5	TINPHSEL2	Input select for TIMER2 high. 0 = TIMI0 1 = TIMI1
4	TINPLSEL2	Input select for TIMER2 low. 0 = TIMI0 1 = TIMI1
3	TINPHSEL1	Input select for TIMER1 high. 0 = TIMI0 1 = TIMI1
2	TINPLSEL1	Input select for TIMER1 low. 0 = TIMI0 1 = TIMI1
1	TINPHSEL0	Input select for TIMER0 high. 0 = TIMI0 1 = TIMI1
0	TINPLSEL0	Input select for TIMER0 low. 0 = TIMI0 1 = TIMI1
End of Table 6-29		

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6.2.3.17 Timer Output Selection Register (TOUTPSEL)

The control register TOUTSEL handles the timer output selection and is shown in Figure 6-26 and described in Table 6-30.

Figure 6-26 Timer Output Selection Register (TOUTPSEL)

31	10	9	5	4	0
Reserved		TOUTPSEL1		TOUTPSEL0	
R,+00000000000000000000		RW,+00001		RW,+00000	

Legend: R = Read only; RW = Read/Write; -*n* = value after reset

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Table 6-30 Timer Output Selection Field Description

Bit	Field	Description	
31-10	Reserved	Reserved	
9-5	TOUTPSEL1	Output select for TIMO1	
		00000: TOUTL0	10000: TOUTL8
		00001: TOUTH0	10001: TOUTH8
		00010: TOUTL1	10010: TOUTL9
		00011: TOUTH1	10011: TOUTH9
		00100: TOUTL2	10100: TOUTL10
		00101: TOUTH2	10101: TOUTH10
		00110: TOUTL3	10110: TOUTL11
		00111: TOUTH3	10111: TOUTH11
		01000: TOUTL4	11000: TOUTL12
		01001: TOUTH4	11001: TOUTH12
		01010: TOUTL5	11010: TOUTL13
		01011: TOUTH5	11011: TOUTH13
		01100: TOUTL6	11100: TOUTL14
		01101: TOUTH6	11101: TOUTH14
		01110: TOUTL7	11110: TOUTL15
		01111: TOUTH7	11111: TOUTH15
4-0	TOUTPSEL0	Output select for TIMO0	
		00000: TOUTL0	10000: TOUTL8
		00001: TOUTH0	10001: TOUTH8
		00010: TOUTL1	10010: TOUTL9
		00011: TOUTH1	10011: TOUTH9
		00100: TOUTL2	10100: TOUTL10
		00101: TOUTH2	10101: TOUTH10
		00110: TOUTL3	10110: TOUTL11
		00111: TOUTH3	10111: TOUTH11
		01000: TOUTL4	11000: TOUTL12
		01001: TOUTH4	11001: TOUTH12
		01010: TOUTL5	11010: TOUTL13
		01011: TOUTH5	11011: TOUTH13
		01100: TOUTL6	11100: TOUTL14
		01101: TOUTH6	11101: TOUTH14
		01110: TOUTL7	11110: TOUTL15
		01111: TOUTH7	11111: TOUTH15
End of Table 6-30			

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6.2.3.18 Reset Mux (RSTMUXx) Register

Software controls the Reset Mux block through the reset multiplex registers using RSTMUX0 through RSTMUX7 for each of the C66x CorePacs on the device. These registers are located in Bootcfg memory space. The Reset Mux Register is shown in the figure and table below.

Figure 6-27 Reset Mux Register

31 10	9	8	7 5	4	3 1	0
Reserved	EVTSTATCLR	Reserved	DELAY	EVTSTAT	OMODE	LOCK
R, +0000 0000 0000 0000 0000 00	RC, +0	R, +0	RW, +100	R, +0	RW, +000	RW, +0

Legend: R = Read only; RW = Read/Write; -*n* = value after reset; RC = Read only and write 1 to clear

Table 6-31 Reset Mux Register Field Descriptions

Bit	Field	Description
31-10	Reserved	Reserved
9	EVTSTATCLR	Clear event status 0 = Writing 0 has no effect 1 = Writing 1 to this bit clears the EVTSTAT bit
8	Reserved	Reserved
7-5	DELAY	Delay cycles between NMI & local reset 000b = 256 SYSCLK1/6 cycles delay between NMI & local reset, when OMODE = 100b 001b = 512 SYSCLK1/6 cycles delay between NMI & local reset, when OMODE = 100b 010b = 1024 SYSCLK1/6 cycles delay between NMI & local reset, when OMODE = 100b 011b = 2048 SYSCLK1/6 cycles delay between NMI & local reset, when OMODE = 100b 100b = 4096 SYSCLK1/6 cycles delay between NMI & local reset, when OMODE = 100b (default) 101b = 8192 SYSCLK1/6 cycles delay between NMI & local reset, when OMODE = 100b 110b = 16384 SYSCLK1/6 cycles delay between NMI & local reset, when OMODE = 100b 111b = 32768 SYSCLK1/6 cycles delay between NMI & local reset, when OMODE = 100b
4	EVTSTAT	Event status 0 = No event received (Default) 1 = WD timer event received by Reset Mux block
3-1	OMODE	Timer event operation mode 000b = WD timer event input to the Reset Mux block does not cause any output event (default) 001b = Reserved 010b = WD Timer Event input to the Reset Mux block causes local reset input to C66x CorePac. processor 011b = WD Timer Event input to the Reset Mux block causes NMI input to C66x CorePac. 100b = WD Timer Event input to the Reset Mux block causes NMI input followed by local reset input to C66x CorePac. Delay between NMI and local reset is set in DELAY bit field. 101b = WD timer event input to the Reset Mux block causes device reset to TCI6634. 110b = Reserved 111b = Reserved
0	LOCK	Lock register fields 0 = Register fields are not locked (default) 1 = Register fields are locked until the next timer reset
End of Table 6-31		

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6.2.3.19 Device Speed (DEVSPEED) Register

The Device Speed Register shows the device speed grade and is shown below.

Figure 6-28 Device Speed Register (DEVSPEED)

31 28	27 16	15 12	11 0
Reserved	DEVSPEED	Reserved	Reserved
R-n		R-n	

Legend: R = Read only; -*n* = value after reset

Table 6-32 Device Speed Register Field Descriptions

Bit	Field	Description
31-28	Reserved	Reserved. Read only
27-16	DEVSPEED	Indicates the speed of the device (read only) 0b0000 0000 0000 = 800 MHz 0b0000 0000 0001 = 1000 MHz 0b0000 0000 001x = 1228.8 MHz 0b0000 0000 01xx = 1350.8 MHz 0b0000 0000 01xx = 1413.12 MHz 0b0000 0001 xxxx = 1536 MHz 0b0000 001x xxxx = 1413.12 MHz 0b0000 01xx xxxx = 1350.8 MHz 0b0000 1xxx xxxx = 1228.8 MHz 0b0001 xxxx xxxx= 1000 MHz 0b001x xxxx xxxx = 800 MHz
15-0	Reserved	Reserved. Read only
End of Table 6-32		

6.2.3.20 Chip Miscellaneous Control (CHIP_MISC_CTL0) Register

Figure 6-29 Chip Miscellaneous Control Register (CHIP_MISC_CTL0)

31 18	17	16	15	14	13	12	11 3	2 0
Reserved	AETMUXSEL1	AET_MUXSEL0	Reserved	RAC23_DIS	RAC01_DIS	MSMC_BLOCK_PARITY_RST	Reserved	QM_PRIORITY
R, + 00 0000 0000 0000	RW,+0	RW,+0	RW,+0	RW,+0	RW,+0	RW,+0	RW,+0	RW,+0

Legend: R = Read only; RW = Read/Write; -*n* = value after reset

Table 6-33 Chip Miscellaneous Control Register Field Descriptions (Part 1 of 2)

Bit	Field	Description
31-18	Reserved	Reserved.
17	AETMUXSEL1	Controls the mux that selects whether an AET event from EDMA CC2 or EDMA CC3 is connected to the C66x Interrupt Controller 0 = EDMA CC2 (default) 1 = EDMA CC3
16	AETMUXSEL0	Controls the mux that selects whether an AET event from EDMA CC2 or EDMA CC4 is connected to the C66x Interrupt Controller 0 = EDMA CC2 (default) 1 = EDMA CC4
15	Reserved	Reserved

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Table 6-33 Chip Miscellaneous Control Register Field Descriptions (Part 2 of 2)

Bit	Field	Description
14	RAC23_DIS	Controls RAC broadcaster indicates presence/absence of RAC 2/3 1 = RAC is Disabled 0 = RAC is Enabled
13	RAC01_DIS	Controls RAC broadcaster indicates presence/absence of RAC 0/1 1 = RAC is Disabled 0 = RAC is Enabled
12	MSMC_BLOCK_PARITY_RST	Controls MSMC parity RAM reset. When set to '1' means the MSMC parity RAM will not be reset.
11-3	Reserved	Reserved
2-0	QM_PRIORITY	Control the priority level for the transactions from QM_Master port, which access the external linking RAM.
End of Table 6-33		

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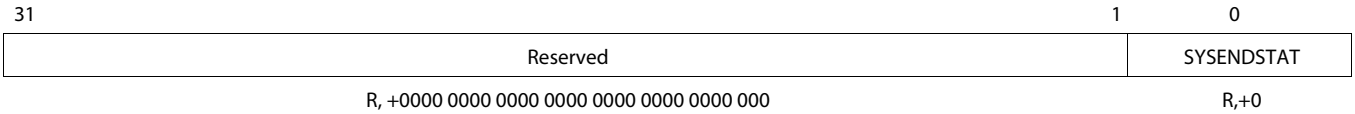
6.2.3.21 System Endian Status Register (SYSENDSTAT)

This register provides a way for reading the system endianness in an endian-neutral way. A zero value indicates big endian and a non-zero value indicates little endian. The SYSENDSTAT register captures the LENDIAN bootmode pin and is used by the BOOTROM to guide the bootflow. The value is latched on the rising edge of $\overline{\text{POR}}$ or $\overline{\text{RESETFULL}}$.

Figure 6-30 System Endian Status Register



Legend: RW = Read/Write; -*n* = value after reset

Table 6-34 System Endian Status Register Descriptions

Bit	Field	Description
31-1	Reserved	Reserved
0	SYSENDSTAT	Reflects the same value as the LENDIAN bit in the DEVSTAT register. 0 - C66x/System is in Big Endian 1 - C66x/System is in Little Endian
End of Table 6-34		

6.2.3.22 PLL Lock Pin Control (PLLLOCK_PINCTL) Register

This register controls the PLLLOCK mux and selects which PLL lock signals are routed to the PLLLOCK device pin.

Note that the select encoding is one hot, meaning that a 1 is written to only one bit in the register.

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Figure 6-31 PLL Lock Pin Control Register (PLLLOCK_PINCTL)

31	30	29	28	27	26	25	24
DDR3B DATA8 PLL	DDR3B DATA7 PLL	DDR3B DATA6 PLL	DDR3B DATA5 PLL	DDR3B DATA4 PLL	DDR3B DATA3 PLL	DDR3B DATA2 PLL	DDR3B DATA1 PLL
RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0
23	22	21	20	19	18	17	16
DDR3B DATA0 PLL	DDR3A DATA8 PLL	DDR3A DATA7 PLL	DDR3A DATA6 PLL	DDR3A DATA5 PLL	DDR3A DATA4 PLL	DDR3A DATA3 PLL	DDR3A DATA2 PLL
RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0
15	14	13	12	11	10	9	8
DDR3A DATA1 PLL	DDR3A DATA0 PLL	AIF2 SERDES A PLL	AIF2 SERDES B PLL	Reserved	XGMII PLL	SGMII PLL	Reserved
RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0
7	6	5	4	3	2	1	0
HyperLink PLL	PCIe PLL	SRIO PLL	Reserved	PA PLL	DDR3B PLL	DDR3A PLL	MAIN PLL
RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0

Legend: R = Read only; RW = Read/Write; -*n* = value after reset

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Table 6-35 TCI6634K2K PLL Lock Pin Control Register Field Description

Bit	Field	Description
31 . . . 0	PLL lock bits	One hot encoding description as below: 0x00000001 : Main PLL Lock 0x00000002 : DDR3A PLL Lock 0x00000004 : DDR3B PLL Lock 0x00000008 : PA PLL Lock 0x00000010 : Reseved 0x00000020 : SRIO PLL Lock 0x00000040 : PCIE PLL Lock 0x00000080 : HyperLink PLL Lock 0x00000100 : Reseved 0x00000200 : SGMII PLL Lock 0x00000400 : XGMII PLL Lock 0x00000800 : Reseved 0x00001000 : AIF2 SERDESA PLL Lock 0x00002000 : AIF2 SERDESB PLL Lock 0x00004000 : DDR3A Data0 Macro PLL Lock 0x00008000 : DDR3A Data1 Macro PLL Lock 0x00010000 : DDR3A Data2 Macro PLL Lock 0x00020000 : DDR3A Data3 Macro PLL Lock 0x00040000 : DDR3A Data4 Macro PLL Lock 0x00080000 : DDR3A Data5 Macro PLL Lock 0x00100000 : DDR3A Data6 Macro PLL Lock 0x00200000 : DDR3A Data7 Macro PLL Lock 0x00400000 : DDR3A Data8 Macro PLL Lock 0x00800000 : DDR3B Data0 Macro PLL Lock 0x01000000 : DDR3B Data1 Macro PLL Lock 0x02000000 : DDR3B Data2 Macro PLL Lock 0x04000000 : DDR3B Data3 Macro PLL Lock 0x08000000 : DDR3B Data4 Macro PLL Lock 0x10000000 : DDR3B Data5 Macro PLL Lock 0x20000000 : DDR3B Data6 Macro PLL Lock 0x40000000 : DDR3B Data7 Macro PLL Lock 0x80000000 : DDR3B Data8 Macro PLL Lock
End of Table 6-35		

6.2.3.23 PLL Lock Status (PLLLOCK_STAT) Register

The PLL Lock Status register holds the current status of the PLL lock bit when the PLLLOCK_EVAL bit is set, and in addition, captures loss of LOCK in a sticky fashion.

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Figure 6-32 TCI6634K2K PLL Lock Status Register (PLLLOCK_STAT)

31	30	29	28	27	26	25	24
DDR3B DATA8 PLL	DDR3B DATA7 PLL	DDR3B DATA6 PLL	DDR3B DATA5 PLL	DDR3B DATA4 PLL	DDR3B DATA3 PLL	DDR3B DATA2 PLL	DDR3B DATA1 PLL
R, +0	R, +0	R, +0	R, +0	R, +0	R, +0	R, +0	R, +0
23	22	21	20	19	18	17	16
DDR3B DATA0 PLL	DDR3A DATA8 PLL	DDR3A DATA7 PLL	DDR3A DATA6 PLL	DDR3A DATA5 PLL	DDR3A DATA4 PLL	DDR3A DATA3 PLL	DDR3A DATA2 PLL
R, +0	R, +0	R, +0	R, +0	R, +0	R, +0	R, +0	R, +0
15	14	13	12	11	10	9	8
DDR3A DATA1 PLL	DDR3A DATA0 PLL	AIF2 SERDES A PLL	AIF2 SERDES B PLL	Reserved	XGMII PLL	SGMII PLL	Reserved
R, +0	R, +0	R, +0	R, +0	R, +0	R, +0	R, +0	R, +0
7	6	5	4	3	2	1	0
HyperLink PLL	PCIe PLL	SRIO PLL	Reserved	PA PLL	DDR3B PLL	DDR3A PLL	MAIN PLL
R, +0	R, +0	R, +0	R, +0	R, +0	R, +0	R, +0	R, +0

Legend: R = Read only; RW = Read/Write; -*n* = value after reset

Table 6-36 PLL Lock Status Register Field Description

Bit	Field	Description
31 . . . 0	PLL lock status	0 - PLL LOCK is deasserted (either initial state or lock was lost) 1 - PLL LOCK is asserted (PLL never lost lock after the last PLLLOCK_EVAL occurred)
End of Table 6-36		

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6.2.3.24 PLL Lock Evaluation (PLLLOCK_EVAL) Register

When the PLLLOCK_EVAL for a particular PLL is set, the value of that particular PLL LOCK signal is reevaluated and captured in the PLLLOCK_STAT register.

Figure 6-33 TCI6634K2K PLL Lock Evaluation Register (PLLLOCK_EVAL)

31	30	29	28	27	26	25	24
DDR3B DATA8 PLL	DDR3B DATA7 PLL	DDR3B DATA6 PLL	DDR3B DATA5 PLL	DDR3B DATA4 PLL	DDR3B DATA3 PLL	DDR3B DATA2 PLL	DDR3B DATA1 PLL
RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0
23	22	21	20	19	18	17	16
DDR3B DATA0 PLL	DDR3A DATA8 PLL	DDR3A DATA7 PLL	DDR3A DATA6 PLL	DDR3A DATA5 PLL	DDR3A DATA4 PLL	DDR3A DATA3 PLL	DDR3A DATA2 PLL
RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0
15	14	13	12	11	10	9	8
DDR3A DATA1 PLL	DDR3A DATA0 PLL	AIF2 SERDES A PLL	AIF2 SERDES B PLL	Reserved	XGMII PLL	SGMII PLL	Reserved
RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0
7	6	5	4	3	2	1	0
HyperLink PLL	PCIe PLL	SRIO PLL	Reserved	PA PLL	DDR3B PLL	DDR3A PLL	MAIN PLL
RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0

Legend: R = Read only; RW = Read/Write; -*n* = value after reset

Table 6-37 PLL Lock Evaluation Register Field Description

Bit	Field	Description
31 . . . 0	PLL lock evaluation	Write 0 = No action Write 1 = PLL Lock for the particular PLL being set will be reevaluated and captured in the PLLLOCK_STAT register for the particular PLL Reads always return 0
End of Table 6-37		

6.2.3.25 SYNECLK_PINCTL Register

This register controls the routing of recovered clock signals from any Ethernet port (SGMII/XGMII of the multiport switches) to the two clock outputs TSRXCLKOUT0/TSRXCLKOUT1.

Figure 6-34 SYNECLK_PINCTL Register

31 7	6 4	3	2 0
Reserved	TSRXCLKOUT1SEL	Reserved	TSRXCLKOUT0SEL
R, +0000 0000 0000 0000 0000 0000 0	RW,+0		RW,+0

Legend: RW = Read/Write; -*n* = value after reset

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Table 6-38 SYNECLK_PINCTL Register Descriptions

Bit	Field	Description
31-7	Reserved	Reserved
6-4	TSRXCLKOUT1SEL	000 - SGMII Lane 0 rxbclk 001 - SGMII Lane 1 rxbclk 010 - SGMII Lane 2 rxbclk 011 - SGMII Lane 3 rxbclk 100 - XGMII Lane 0 rxbclk 101 - XGMII Lane 1 rxbclk 110 - XGMII Lane 2 rxbclk 111 - XGMII Lane 3 rxbclk
3	Reserved	Reserved
2-0	TSRXCLKOUT0SEL	000 - SGMII Lane 0 rxbclk 001 - SGMII Lane 1 rxbclk 010 - SGMII Lane 2 rxbclk 011 - SGMII Lane 3 rxbclk 100 - XGMII Lane 0 rxbclk 101 - XGMII Lane 1 rxbclk 110 - XGMII Lane 2 rxbclk 111 - XGMII Lane 3 rxbclk
End of Table 6-38		

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7 Device Operating Conditions

7.1 Absolute Maximum Ratings

Table 7-1 Absolute Maximum Ratings (1)
Over Operating Case Temperature Range (Unless Otherwise Noted)

Supply voltage range (2):	CVDD	-0.3 V to 1.3 V
	CVDD1	-0.3 V to 1.3 V
	DVDD15	-0.3 V to 2.45 V
	DVDD18	-0.3 V to 2.45 V
	VREFSSTL	0.49 × DVDD15 to 0.51 × DVDD15
	VDDAHV	-0.3 V to 2.45 V
	AVDDA6, AVDDA7 AVDDA8, AVDDA9, AVDDA10 AVDDA11, AVDDA12, AVDDA13 AVDDA14, AVDDA15	-0.3 V to 2.45 V
	AVDDA1, AVDDA2, AVDDA4, AVDDA5	-0.3 V to 2.45 V
	VSS Ground	0 V
Input voltage (V_I) range:	LVCMOS (1.8 V)	-0.3 V to DVDD18+0.3 V
	DDR3A, DDR3B	-0.3 V to 2.45 V
	I^2C	-0.3 V to 2.45 V
	LVDS	-0.3 V to DVDD18+0.3 V
	LJCB	-0.3 V to 1.3 V
	SerDes	-0.3 V to CVDD1+0.3 V
Output voltage (V_O) range:	LVCMOS (1.8 V)	-0.3 V to DVDD18+0.3 V
	DDR3A, DDR3B	-0.3 V to 2.45 V
	I^2C	-0.3 V to 2.45 V
	SerDes	-0.3 V to CVDD1+0.3 V
Operating case temperature range, T_C:	Commercial	0°C to 100°C
	Extended	-40°C to 100°C
ESD stress voltage, V_{ESD} (3)	HBM (human body model) (4)	±1000 V
	CDM (charged device model) (5)	±250 V
Overshoot/undershoot (6)	LVCMOS (1.8 V)	20% overshoot/undershoot for 20% of signal duty cycle
	DDR3A, DDR3B	
	I^2C	
Storage temperature range, T_{stg}:		-65°C to 150°C
End of Table 7-1		

1 Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2 All voltage values are with respect to V_{SS}.

3 Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the device.

4 Level listed above is the passing level per ANSI/ESDA/JEDEC JS-001-2010. JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 500 V HBM is possible if necessary precautions are taken. Pins listed as 1000 V may actually have higher performance.

5 Level listed above is the passing level per EIA-JEDEC JESD22-C101E. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as 250 V may actually have higher performance.

6 Overshoot/Undershoot percentage relative to I/O operating values - for example the maximum overshoot value for 1.8-V LVCMOS signals is DVDD18 + 0.20 × DVDD18 and maximum undershoot value would be V_{SS} - 0.20 × DVDD18

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7.2 Recommended Operating Conditions

Table 7-2 Recommended Operating Conditions (1) (2)

			Min	Nom	Max	Unit
CVDD	SR core supply		SRVnom*0.95 (3)	0.8-1.1	SRVnom*1.05	V
CVDD1	Core supply		0.902	0.95	0.997	V
DVDD18	1.8-V supply I/O voltage		1.71	1.8	1.89	V
DVDD15	1.5-V supply I/O voltage		1.425	1.5	1.575	V
VREFSSTL	DDR3A, DDR3B reference voltage		0.49 × DVDD15	0.5 × DVDD15	0.51 × DVDD15	V
V_{DDRx} (4)	SerDes regulator supply		1.71	1.8	1.89	V
V_{DDAx}	PLL analog supply		1.71	1.8	1.89	V
V_{DDTx}	SerDes termination supply		0.807	0.85	0.892	V
V_{SS}	Ground		0	0	0	V
V_{IH}	High-level input voltage	LVCMOS (1.8 V)	0.65 × DVDD18			V
		I^2C	0.7 × DVDD18			V
		DDR3A, DDR3B EMIF	VREFSSTL + 0.1			V
V_{IL}	Low-level input voltage	LVCMOS (1.8 V)			0.35 × DVDD18	V
		DDR3A, DDR3B EMIF	-0.3		VREFSSTL - 0.1	V
		I^2C			0.3 × DVDD18	V
T_C	Operating case temperature	Commercial	0		100	°C
		Extended	-40		100	°C

End of Table 7-2

1 All differential clock inputs comply with the LVDS Electrical Specification, IEEE 1596.3-1996 and all SerDes I/Os comply with the XAUI Electrical Specification, IEEE 802.3ae-2002.

2 All SerDes I/Os comply with the XAUI Electrical Specification, IEEE 802.3ae-2002.

3 SRVnom refers to the unique SmartReflex core supply voltage between 0.8 V and 1.1 V set from the factory for each individual device.

4 Where x = 1, 2, 3, 4... to indicate all supplies of the same kind.

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7.3 Electrical Characteristics

Table 7-3 Electrical Characteristics
Over Recommended Ranges of Supply Voltage and Operating Case Temperature (Unless Otherwise Noted)

Parameter			Test Conditions (1)	Min	Typ	Max	Unit
V_{OH}	High-level output voltage	LVCMOS (1.8 V)	$I_O = I_{OH}$	DVDD18 - 0.45			V
		DDR3A, DDR3B		DVDD15 - 0.4			
		I^2C (2)					
V_{OL}	Low-level output voltage	LVCMOS (1.8 V)	$I_O = I_{OL}$			0.45	V
		DDR3A, DDR3B				0.4	
		I^2C	I_O = 3 mA, pulled up to 1.8 V			0.4	
I_I (3)	Input current [DC]	LVCMOS (1.8 V)	No IPD/IPU	-5		5	µA
			Internal pullup	50	100	170	
			Internal pulldown	-170	-100	-50	
		I^2C	0.1 × DVDD18 V < V_I < 0.9 × DVDD18 V	-10		10	µA
I_{OH}	High-level output current [DC]	LVCMOS (1.8 V)				-6	mA
		DDR3A, DDR3B				-8	
		I^2C (4)					
I_{OL}	Low-level output current [DC]	LVCMOS (1.8 V)				6	mA
		DDR3A, DDR3B				8	
		I^2C				3	
I_{OZ} (5)	Off-state output current [DC]	LVCMOS (1.8 V)		-2		2	µA
		DDR3A, DDR3B		-2		2	
		I^2C		-2		2	
End of Table 7-3							

1 For test conditions shown as MIN, MAX, or TYP, use the appropriate value specified in the recommended operating conditions table.
2 I^2C uses open collector IOs and does not have a V_{OH} Minimum.
3 I_I applies to input-only pins and bidirectional pins. For input-only pins, I_I indicates the input leakage current. For bidirectional pins, I_I includes input leakage current and off-state (Hi-Z) output leakage current.
4 I^2C uses open collector IOs and does not have a I_{OH} Maximum.
5 I_{OZ} applies to output-only pins, indicating off-state (Hi-Z) output leakage current.

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7.4 Power Supply to Peripheral I/O Mapping

Table 7-4 Power Supply to Peripheral I/O Mapping (1) (2)
Over Recommended Ranges of Supply Voltage and Operating Case Temperature (Unless Otherwise Noted)

Power Supply		I/O Buffer Type	Associated Peripheral
CVDD	Supply core voltage	LJCB	SYSCLK(P|N) PLL input buffer
			ALTCORECLK(P|N) PLL input buffer
			SRIOSGMIICLK(P|N) SerDes PLL input buffer
			DDRCLK(P|N) PLL input buffer
			PCIECLK(P|N) SerDes PLL input buffer
			MCMCLK(P|N) SerDes PLL input buffer
			PASSCLK(P|N) PLL input buffer
DVDD15A, DVDD15B	1.5-V supply I/O voltage	DDR3A, DDR3B (1.5 V)	All DDR3A, DDR3B memory controller peripheral I/O buffer
DVDD18	1.8-V supply I/O voltage	LVCMOS (1.8 V)	All GPIO peripheral I/O buffer
			All JTAG and EMU peripheral I/O buffer
			All TIMER peripheral I/O buffer
			All SPI peripheral I/O buffer
			All AIF peripheral I/O buffer
			All RESETs, NMI, control peripheral I/O buffer
			All SmartReflex peripheral I/O buffer
			All Hyperlink sideband peripheral I/O buffer
			All MDIO peripheral I/O buffer
			All UART peripheral I/O buffer
		Open-drain (1.8 V)	All I^2C peripheral I/O buffer
VDDAHV	Hyperlink/SRIO/SGMII/PCIE SerDes termination and analogue front-end supply	SerDes/CML	SerDes CML IO buffer
End of Table 7-4			

1 Please note that this table does not attempt to describe all functions of all power supply terminals but only those whose purpose it is to power peripheral I/O buffers and clock input buffers.

2 Please see the *Hardware Design Guide for KeyStone Devices* in 1.9 "Related Documentation from Texas Instruments" on page 22for more information about individual peripheral I/O.

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8 TCI6634K2K Peripheral Information and Electrical Specifications

This chapter covers the various peripherals on the TCI6634K2K device. Peripheral-specific information, timing diagrams, electrical specifications, and register memory maps are described in this chapter.

8.1 Recommended Clock and Control Signal Transition Behavior

All clocks and control signals ***must*** transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

8.2 Power Supplies

The following sections describe the proper power-supply sequencing and timing needed to properly power on the TCI6634K2K. The various power supply rails and their primary functions are listed in Table 8-1.

Table 8-1 Power Supply Rails on the TCI6634K2K

Name	Primary Function	Voltage	Notes
CVDD	SmartReflex DSP core supply voltage	0.8 - 1.1 V	DSP variable core supply
CVDDS	SerDes analog power supply voltage	0.85 V	SerDes analog supply
VDDAH	SerDes I/O power supply voltage	1.8 V	SerDes I/O power supply
CVDD1	DSP core fixed supply voltage	0.95 V	DSP Core fixed supply
VDDPLL	DDR3 PHY PLL supply voltage	1.8 V	DDR3 PHY PLL supply
DVDD15A	DDR3A I/O power supply voltage	1.5 V	DDR3A I/O power supply
DVDD15B	DDR3B I/O power supply voltage	1.5 V	DDR3B I/O power supply
DVDD18	1.8-V I/O power supply voltage	1.5 V	1.8-V I/O power supply
VDDA18	PLL supply voltage	1.8 V	PLL supplies
USBDVDD33	USB 3.3-V IO supply	3.3 V	USB high voltage supply
USB085	USB LV PHY power supply voltage	0.85 V	USB LV PHY supply
VSS	Ground	GND	Ground
End of Table 8-1			

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8.2.1 Power-Up Sequencing

This section defines the requirements for a power up sequencing from a power-on reset condition. There are two acceptable power sequences for the device. The first sequence stipulates the core voltages starting before the IO voltages as shown below.

1. CVDD
2. CVDD1
3. CVDDSVDDAH, VDDPLL, DVDD18, VDDA18
4. DVDD15A, DVDD15B

The second sequence provides compatibility with other TI processors with the IO voltage starting before the core voltages as shown below.

1. CVDDS
2. VDDAH, VDDPLL, DVDD18, VDDA18
3. DVDD15A, DVDD15B
4. CVDD
5. CVDD1

The clock input buffers for SYSCLK, ALTCORECLK, DDR3ACLK, DDR3BCLK, PASSCLK, SRIOSGMIICLK, PCIECLK, and HYPCLK use CVDD as a supply voltage. These clock inputs are not failsafe and must be held in a high-impedance state until CVDD is at a valid voltage level. Driving these clock inputs high before CVDD is valid could cause damage to the device. Once CVDD is valid, it is acceptable that the P and N legs of these clocks may be held in a static state (either high and low or low and high) until a valid clock frequency is needed at that input. To avoid internal oscillation, the clock inputs should be removed from the high impedance state shortly after CVDD is present.

If a clock input is not used, it must be held in a static state. To accomplish this, the N leg should be pulled to ground through a 1-kΩ resistor. The P leg should be tied to CVDD to ensure it will not have any voltage present until CVDD is active. Connections to the IO cells powered by DVDD18 and DVDD15 (DVDD15A and DVDD15B) are not failsafe and should not be driven high before these voltages are active. Driving these IO cells high before DVDD18 or DVDD15 are valid could cause damage to the device.

The device initialization is divided into two phases. The first phase consists of the time period from the activation of the first power supply until the point at which all supplies are active and at a valid voltage level. Either of the sequencing scenarios described above can be implemented during this phase. The figures below show both the core-before-IO voltage sequence and the IO-before-core voltage sequence. $\overline{\text{POR}}$ must be held low for the entire power stabilization phase.

This is followed by the device initialization phase. The rising edge of $\overline{\text{POR}}$ followed by the rising edge of $\overline{\text{RESETFULL}}$ triggers the end of the initialization phase, but both must be inactive for the initialization to complete. $\overline{\text{POR}}$ must always go inactive before $\overline{\text{RESETFULL}}$ goes inactive as described below. SYSCLK1 in the following section refers to the clock that is used by the C66x CorePac. See Figure 8-7 for more details.

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8.2.1.1 Core-Before-IO Power Sequencing

Figure 8-1 shows the power sequencing and reset control of the TCI6634K2K for device initialization. $\overline{\text{POR}}$ may be removed after the power has been stable for the required 100 µsec. $\overline{\text{RESETFULL}}$ must be held low for a period (see Time 9 in Figure 8-1) after the rising edge of $\overline{\text{POR}}$, but may be held low for longer periods if necessary. The configuration bits shared with the GPIO pins will be latched on the rising edge of $\overline{\text{RESETFULL}}$ and must meet the setup and hold times specified. SYSCLK1 must always be active before $\overline{\text{POR}}$ can be removed. Core-before-IO power sequencing is defined in Table 8-2.

Note—TI recommends a maximum of 100 ms between one power rail being valid and the next power rail in the sequence starting to ramp.

Figure 8-1 Core Before IO Power Sequencing

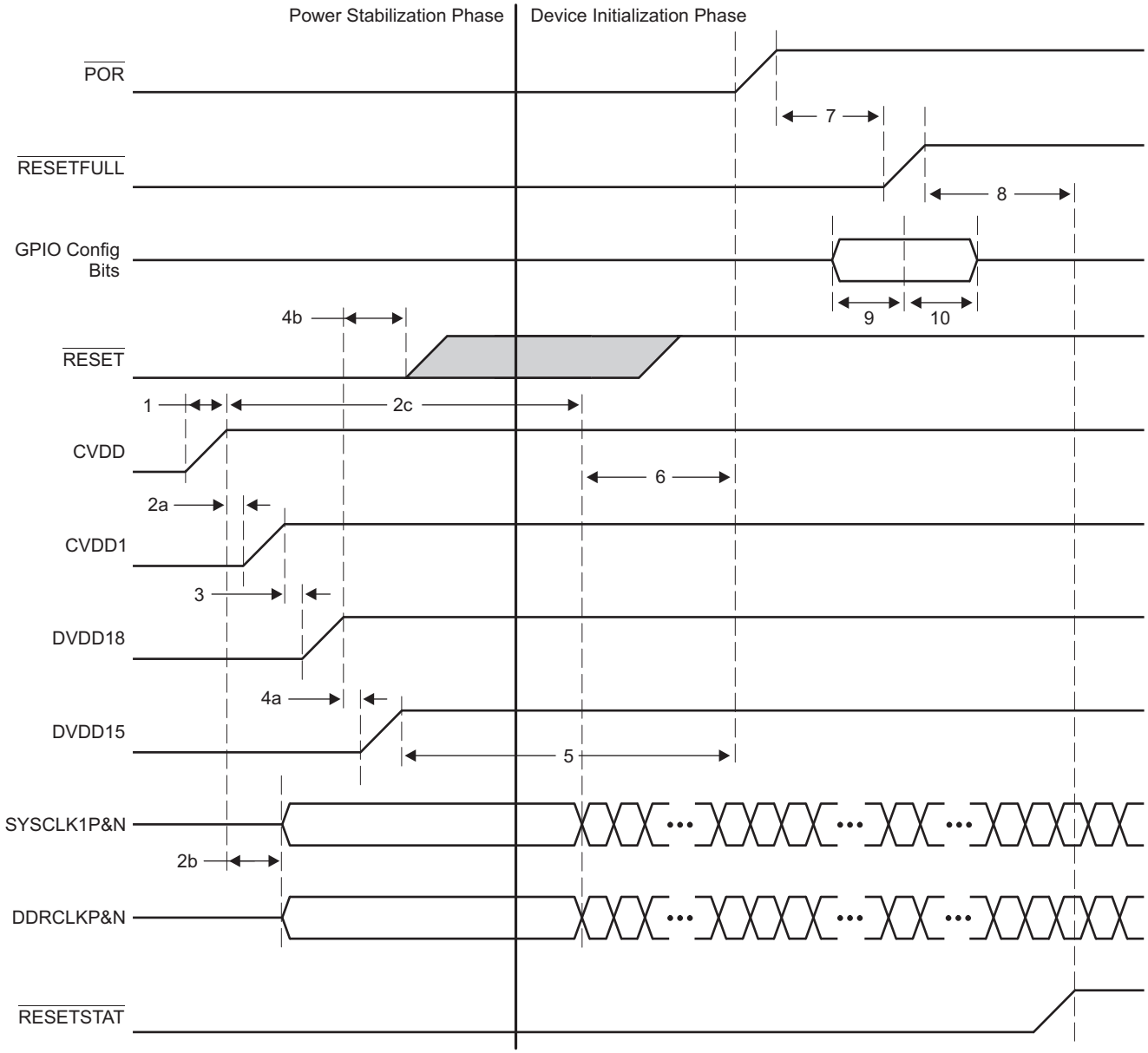

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Table 8-2 Core Before IO Power Sequencing

Time	System State
1	**Begin Power Stabilization Phase** • CVDD (core AVS) ramps up. • $\overline{\text{POR}}$ must be held low through the power stabilization phase. Because $\overline{\text{POR}}$ is low, all the core logic that has async reset (created from $\overline{\text{POR}}$) is put into the reset state.
2a	• CVDD1 (core constant) ramps at the same time or shortly following CVDD. Although ramping CVDD1,and CVDD simultaneously is permitted, the voltage for CVDD1 ***must never exceed*** CVDD until after CVDD has reached a valid voltage. • The purpose of ramping up the core supplies close to each other is to reduce crowbar current. CVDD1 should trail CVDD as this will ensure that the Word Lines (WLs) in the memories are turned off and there is no current through the memory bit cells. If, however, CVDD1 (core constant) ramps up before CVDD (core AVS), then the worst-case current could be on the order of twice the specified draw of CVDD1.
2b	• Once CVDD is valid, the clock drivers can be enabled. Although the clock inputs are not necessary at this time, they should either be driven with a valid clock or be held in a static state with one leg high and one leg low.
2c	• The DDR3ACLK, DDR3BCLK and SYSCLK1 may begin to toggle anytime between when CVDD is at a valid level and the setup time before $\overline{\text{POR}}$ goes high specified by t6.
3	• Filtered versions of 1.8 V can ramp simultaneously with DVDD18. • $\overline{\text{RESETSTAT}}$ is driven low once the DVDD18 supply is available. • All LVCMOS input and bidirectional pins must not be driven or pulled high until DVDD18 is present. Driving an input or bidirectional pin before DVDD18 is valid could cause damage to the device.
4a	• DVDD15 (DVDD15A and DVDD15B, 1.5 V) supplies are ramped up following DVDD18. Although ramping DVDD18 and DVDD15 simultaneously is permitted, the voltage for DVDD15 ***must never exceed*** DVDD18.
4b	• $\overline{\text{RESET}}$ may be driven high any time after DVDD18 is at a valid level. In a $\overline{\text{POR}}$-controlled boot, $\overline{\text{RESET}}$ must be high before $\overline{\text{POR}}$ is driven high.
5	• $\overline{\text{POR}}$ must continue to remain low for at least 100 µs after power has stabilized. **End power stabilization phase**
6	• Device initialization requires 500 SYSCLK1 periods after the Power Stabilization Phase. The maximum clock period is 33.33 nsec, so a delay of an additional 16 µs is required before a rising edge of $\overline{\text{POR}}$. The clock must be active during the entire 16 µs.
7	• $\overline{\text{RESETFULL}}$ must be held low for at least 24 transitions of the SYSCLK1 after $\overline{\text{POR}}$ has stabilized at a high level.
8	• The rising edge of the $\overline{\text{RESETFULL}}$ will remove the reset to the efuse farm allowing the scan to begin. • Once device initialization and the efuse farm scan are complete, the $\overline{\text{RESETSTAT}}$ signal is driven high. This delay will be 10000 to 50000 clock cycles. **End device initialization phase**
9	• GPIO configuration bits must be valid for at least 12 transitions of the SYSCLK1 before the rising edge of $\overline{\text{RESETFULL}}$.
10	• GPIO configuration bits must be held valid for at least 12 transitions of the SYSCLK1 after the rising edge of $\overline{\text{RESETFULL}}$.
End of Table 8-2	

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8.2.1.2 IO-Before-Core Power Sequencing

The timing diagram for IO-before-core power sequencing is shown in Figure 8-2 and defined in Table 8-3.

Note—TI recommends a maximum of 100 ms between one power rail being valid, and the next power rail in the sequence starting to ramp.

Figure 8-2 IO-Before-Core Power Sequencing

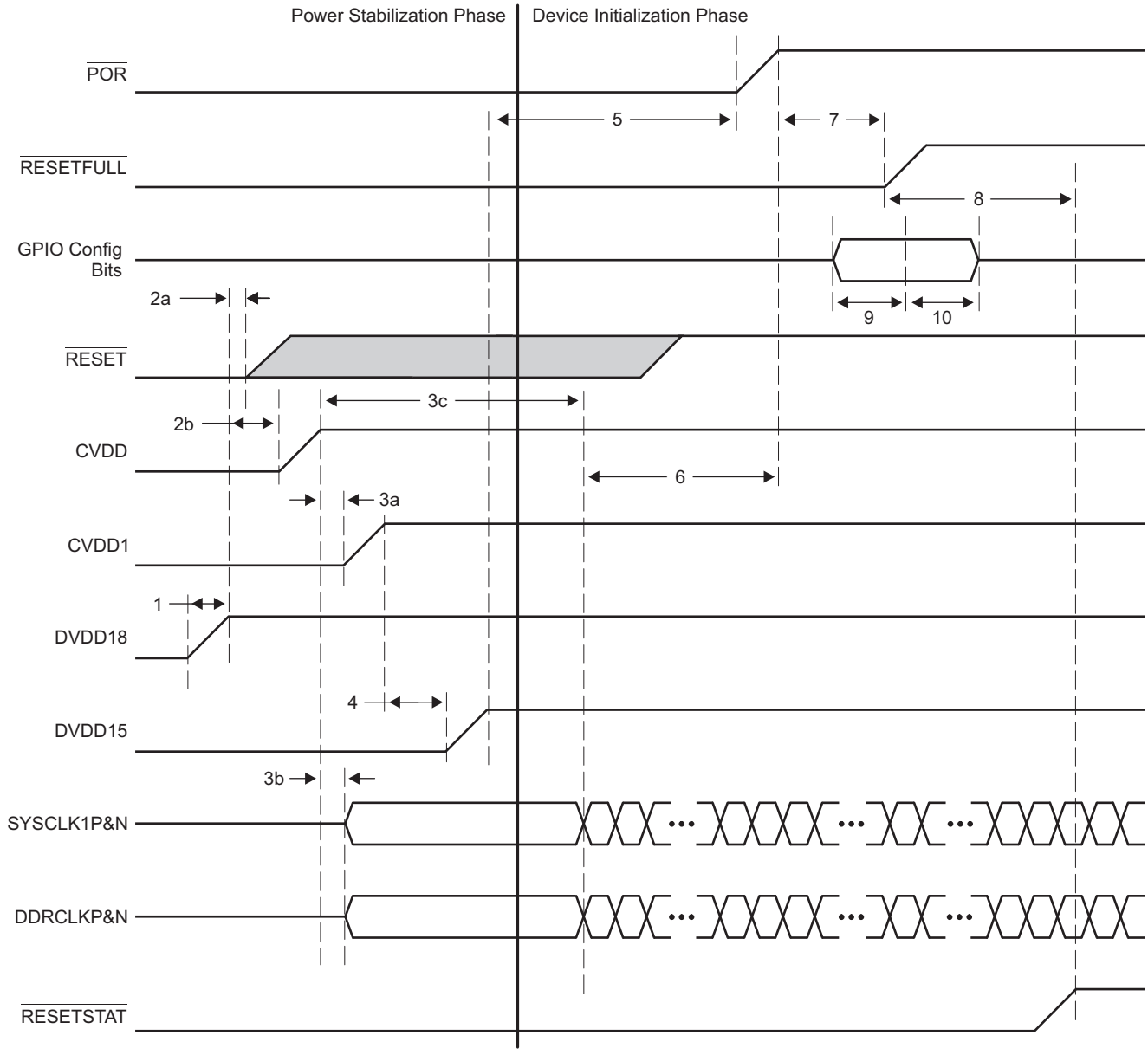

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Table 8-3 IO-Before-Core Power Sequencing

Time	System State
1	**Begin Power Stabilization Phase** • Because $\overline{\text{POR}}$ is low, all the core logic having async reset (created from POR) are put into the reset state once the core supply ramps up. $\overline{\text{POR}}$ must remain low through the power stabilization phase. • Filtered versions of 1.8 V can ramp simultaneously with DVDD18. • $\overline{\text{RESETSTAT}}$ is driven low once the DVDD18 supply is available. • All input and bidirectional pins must not be driven or pulled high until DVDD18 is present. Driving an input or bidirectional pin before DVDD18 is stable could cause damage to the device.
2	• DVDD15 (1.5 V) supply is ramped up following DVDD18.
2a	• $\overline{\text{RESET}}$ may be driven high any time after DVDD18 is at a valid level.
2b	• CVDD (core AVS) ramps up.
3a	• CVDD1 (core constant) ramps at the same time or following CVDD . Although ramping CVDD1 and CVDD simultaneously is permitted, the voltage for CVDD1 ***must never exceed*** CVDD until after CVDD has reached a valid voltage. • The purpose of ramping up the core supplies close to each other is to reduce crowbar current. CVDD1 should trail CVDD as this will ensure that the WLs in the memories are turned off and there is no current through the memory bit cells. If, however, CVDD1(core constant) ramps up before CVDD (core AVS), then the worst case current could be on the order of twice the specified draw of CVDD1.
3b	• Once CVDD is valid, the clock drivers should be enabled. Although the clock inputs are not necessary at this time, they should be driven either with a valid clock or held in a static state with one leg high and one leg low.
3c	• The DDR3ACLK, DDR3BCLK and SYSCLK1 may begin to toggle anytime between when CVDD is at a valid level and the setup time before $\overline{\text{POR}}$ goes high specified by t6.
4	• DVDD15 is ramping up following CVDD1.
5	• $\overline{\text{POR}}$ must continue to remain low for at least 100 µs after power has stabilized. **End power stabilization phase**
6	**Begin Device Initialization** • Device initialization requires 500 SYSCLK1 periods after the power stabilization phase. The maximum clock period is 33.33 nsec so a delay of an additional 16 µs is required before a rising edge of $\overline{\text{POR}}$. The clock must be active during the entire 16 µs. • $\overline{\text{POR}}$ must remain low.
7	• $\overline{\text{RESETFULL}}$ is held low for at least 24 transitions of the SYSCLK1 after $\overline{\text{POR}}$ has stabilized at a high level. • The rising edge of the $\overline{\text{RESETFULL}}$ will remove the reset to the efuse farm allowing the scan to begin.
8	• Once device initialization and the efuse farm scan are complete, the $\overline{\text{RESETSTAT}}$ signal is driven high. This delay is 10000 to 50000 clock cycles. **End device initialization phase**
9	• GPIO configuration bits must be valid for at least 12 transitions of the SYSCLK1 before the rising edge of $\overline{\text{RESETFULL}}$.
10	• GPIO configuration bits must be held valid for at least 12 transitions of the SYSCLK1 after the rising edge of $\overline{\text{RESETFULL}}$.
End of Table 8-3	

8.2.1.3 Prolonged Resets

Holding the device in $\overline{\text{POR}}$, $\overline{\text{RESETFULL}}$, or $\overline{\text{RESET}}$ for long periods of time may affect the long-term reliability of the part (due to an elevated voltage condition that can stress the part). The device should not be held in a reset for times exceeding one hour at a time and no more than 5% of the total lifetime for which the device is powered-up. Exceeding these limits will cause a gradual reduction in the reliability of the part. This can be avoided by allowing the device to boot and then configuring it to enter a hibernation state soon after power is applied. This will satisfy the reset requirement while limiting the power consumption of the device.

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8.2.1.4 Clocking During Power Sequencing

Some of the clock inputs are required to be present for the device to initialize correctly, but behavior of many of the clocks is contingent on the state of the boot configuration pins. Table 8-4 describes the clock sequencing and the conditions that affect clock operation. Note that all clock drivers should be in a high-impedance state until CVDD is at a valid level and that all clock inputs be either active or in a static state with one leg pulled to ground and the other connected to CVDD.

Table 8-4 Clock Sequencing

Clock	Condition	Sequencing
DDR3ACLK	None	Must be present 16 µsec before $\overline{\text{POR}}$ transitions high.
DDR3BCLK	None	Must be present 16 µsec before $\overline{\text{POR}}$ transitions high.
SYSCLK	CORECLKSEL = 0	SYSCLK is used to clock the core PLL. It must be present 16 µsec before $\overline{\text{POR}}$ transitions high.
	CORECLKSEL = 1	SYSCLK is used only for AIF2. Clock must be present before the reset to the AIF2 is removed. Reserved.
ALTCORECLK	CORECLKSEL = 0	ALTCORECLK is not used and should be tied to a static state.
	CORECLKSEL = 1	ALTCORECLK is used to clock the core PLL. It must be present 16 µsec before $\overline{\text{POR}}$ transitions high.
PASSCLK	PASSCLKSEL = 0	PASSCLK is not used and should be tied to a static state.
	PASSCLKSEL = 1	PASSCLK is used as a source for the PASS PLL. It must be present before the PASS PLL is removed from reset and programmed.
SRIOSGMIICLK	An SGMII port will be used.	SRIOSGMIICLK must be present 16 µsec before $\overline{\text{POR}}$ transitions high.
	SGMII will not be used. SRIO will be used as a boot device.	SRIOSGMIICLK must be present 16 µsec before $\overline{\text{POR}}$ transitions high.
	SGMII will not be used. SRIO will be used after boot.	SRIOSGMIICLK is used as a source to the SRIO SerDes PLL. It must be present before the SRIO is removed from reset and programmed.
	SGMII will not be used. SRIO will not be used.	SRIOSGMIICLK is not used and should be tied to a static state.
PCIECLK	PCIE will be used as a boot device.	PCIECLK must be present 16 µsec before $\overline{\text{POR}}$ transitions high.
	PCIE will be used after boot.	PCIECLK is used as a source to the PCIE SerDes PLL. It must be present before the PCIe is removed from reset and programmed.
	PCIE will not be used.	PCIECLK is not used and should be tied to a static state.
HYPCLK	HyperLink will be used as a boot device.	HYPCLK must be present 16 µsec before $\overline{\text{POR}}$ transitions high.
	HyperLink will be used after boot.	HYPCLK is used as a source to the HyperLink SerDes PLL. It must be present before the HyperLink is removed from reset and programmed.
	HyperLink will not be used.	HYPCLK is not used and should be tied to a static state.
End of Table 8-4		

8.2.2 Power-Down Sequence

The power down sequence is the exact reverse of the power-up sequence described above. The goal is to prevent an excessive amount of static current and to prevent overstress of the device. A power-good circuit that monitors all the supplies for the device should be used in all designs. If a catastrophic power supply failure occurs on any voltage rail, $\overline{\text{POR}}$ should transition to low to prevent over-current conditions that could possibly impact device reliability.

A system power monitoring solution is needed to shut down power to the board if a power supply fails. Long-term exposure to an environment in which one of the power supply voltages is no longer present will affect the reliability of the device. Holding the device in reset is not an acceptable solution because prolonged periods of time with an active reset can affect long term reliability.

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8.2.3 Power Supply Decoupling and Bulk Capacitors

To properly decouple the supply planes on the PCB from system noise, decoupling and bulk capacitors are required. Bulk capacitors are used to minimize the effects of low-frequency current transients and decoupling or bypass capacitors are used to minimize higher frequency noise. For recommendations on selection of power supply decoupling and bulk capacitors see the *Hardware Design Guide for KeyStone II Devices* (currently in development).

8.2.4 SmartReflex

Increasing the device complexity increases its power consumption. With higher clock rates and increased performance comes an inevitable penalty: increasing leakage currents. Leakage currents are present in any powered circuit, independent of clock rates and usage scenarios. This static power consumption is mainly determined by transistor type and process technology. Higher clock rates also increase dynamic power, which is the power used when transistors switch. The dynamic power depends mainly on a specific usage scenario, clock rates, and I/O activity.

Texas Instruments SmartReflex technology is used to decrease both static and dynamic power consumption while maintaining the device performance. SmartReflex in the TCI6634K2K device is a feature that allows the core voltage to be optimized based on the process corner of the device. This requires a voltage regulator for each TCI6634K2K device.

To help maximize performance and minimize power consumption of the device, SmartReflex is required to be implemented. The voltage selection can be accomplished using 4 VCNTL pins or 6 VCNTL pins (depending on power supply device being used), which are used to select the output voltage of the core voltage regulator.

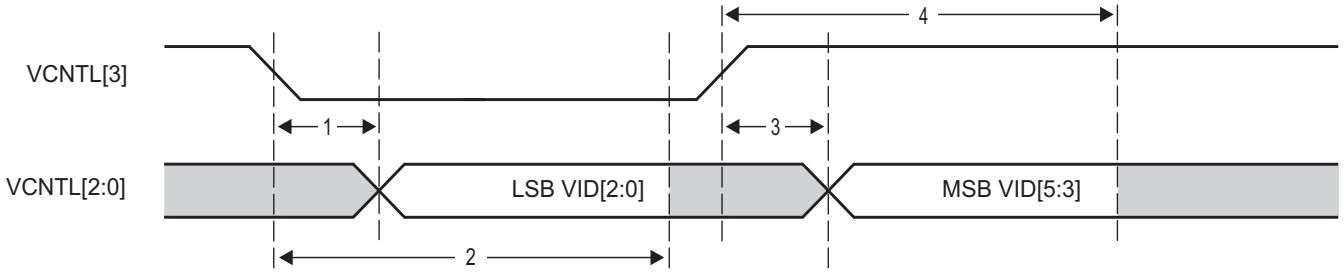
For information on implementation of SmartReflex see the *DSP Power Consumption Summary for KeyStone Devices Application Report* and the *Hardware Design Guide for KeyStone II Devices* (in development).

Table 8-5 SmartReflex 4-Pin 6-bit VID Interface Switching Characteristics
(see Figure 8-3)

No.	Parameter		Min	Max	Unit
1	td(VCNTL[2:0]-VCNTL[3])	Delay time - VCNTL[2:0] valid after VCNTL[3] low		300.00	ns
2	toh(VCNTL[3]-VCNTL[2:0])	Output hold time - VCNTL[2:0] valid after VCNTL[3]	0.07	172020C (1)	ms
3	td(VCNTL[2:0]-VCNTL[3])	Delay time - VCNTL[2:0] valid after VCNTL[3] high		300.00	ns
4	toh(VCNTL[3]-VCNTL[2:0)	Output hold time - VCNTL[2:0] valid after VCNTL[3] high	0.07	172020C	ms
End of Table 8-5					

1 C = 1/SYSCLK1 frequency (See Figure 8-9)in ms

Figure 8-3 SmartReflex 4-Pin 6-bit VID Interface Timing



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8.3 Power Sleep Controller (PSC)

The Power Sleep Controller (PSC) includes a Global Power Sleep Controller (GPSC) and a number of Local Power Sleep Controllers (LPSC) that control overall device power by turning off unused power domains and gating off clocks to individual peripherals and modules. The PSC provides the user with an interface to control several important power and clock operations.

For information on the Power Sleep Controller, see the *Power Sleep Controller (PSC) for KeyStone Devices* User Guide in 1.9 "Related Documentation from Texas Instruments" on page 22.

8.3.1 Power Domains

The device has several power domains that can be turned on for operation or off to minimize power dissipation. The Global Power Sleep Controller (GPSC) is used to control the power gating of various power domains.

The following table shows the TCI6634K2K power domains.

Table 8-6 Power Domains (Part 1 of 2)

Domain	Block(s)	Note	Power Connection
0	Most peripheral logic	Cannot be disabled	Always on
1	Per-core TETB and system TETB	RAMs can be powered down	Software control
2	Network Coprocessor	Logic can be powered down	Software control
3	PCIe	Logic can be powered down	Software control
4	SRIO	Logic can be powered down	Software control
5	HyperLink0	Logic can be powered down	Software control
6	Reserved	Reserved	Reserved
7	MSMC RAM	MSMC RAM can be powered down	Software control
8	C66x Core 0, L1/L2 RAMs	L2 RAMs can sleep	Software control via C66x CorePac. For details, see the C66x CorePac Reference Guide.
9	C66x Core 1, L1/L2 RAMs	L2 RAMs can sleep	
10	C66x Core 2, L1/L2 RAMs	L2 RAMs can sleep	
11	C66x Core 3, L1/L2 RAMs	L2 RAMs can sleep	
12	C66x Core 4, L1/L2 RAMs	L2 RAMs can sleep	
13	C66x Core 5, L1/L2 RAMs	L2 RAMs can sleep	
14	C66x Core 6, L1/L2 RAMs	L2 RAMs can sleep	
15	C66x Core 7, L1/L2 RAMs	L2 RAMs can sleep	
16	EMIF(DDR3A, DDR3B)	Logic can be powered down	Software control
17	RAC_0, RAC_1, and TAC	Logic can be powered down	Software control
18	RAC_2, RAC_3	Logic can be powered down	Software control
19	FFTC_0 and FFTC_1	Logic can be powered down	Software control
20	FFTC_2, FFTC_3, FFTC_4, FFTC_5	Logic can be powered down	Software control
21	AIF2	RAMs can be powered down	Software control
22	TCP3d_0, TCP3d_1	RAMs can be powered down	Software control
23	TCP3d_2, TCP3d_3	RAMs can be powered down	Software control
24	VCP2_0, VCP2_1, VCP2_2, and VCP2_3	RAMs can be powered down	Software control
25	VCP2_4, VCP2_5, VCP2_6 and VCP2_7	RAMs can be powered down	Software control
26	BCP	Logic can be powered down	Software control
27	Reserved	Reserved	Reserved
28	HyperLink1	Logic can be powered down	Software control
29	10GbE	Logic can be powered down	Software control

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Table 8-6 Power Domains (Part 2 of 2)

Domain	Block(s)	Note	Power Connection
30	Reserved	Reserved	Reserved
31	Reserved	Reserved	Reserved
End of Table 8-6			

8.3.2 Clock Domains

Clock gating to each logic block is managed by the Local Power Sleep Controllers (LPSCs) of each module. For modules with a dedicated clock or multiple clocks, the LPSC communicates with the PLL controller to enable and disable that module's clock(s) at the source. For modules that share a clock with other modules, the LPSC controls the clock gating logic for each module.

Table 8-7 shows the TCI6634K2K clock domains.

Table 8-7 Clock Domains (Part 1 of 2)

LPSC Number	Module(s)	Notes
0	Shared LPSC for all peripherals other than those listed in this table	Always on
1	Reserved	Reserved
2	Reserved	Reserved
3	TCP3e	Software control
4	VCP2_0	Software control
5	Debug subsystem and tracers	Software control
6	Per-core TETB and system TETB	Software control
7	Packet Accelerator	Software control
8	Ethernet SGMIIs	Software control
9	Security Accelerator	Software control
10	PCIe	Software control
11	SRIO	Software control
12	HyperLink0	Software control
13	SmartReflex	Always on
14	MSMC RAM	Software control
15	C66x CorePac0	Always on
16	C66x CorePac1	Always on
17	C66x CorePac2	Always on
18	C66x CorePac3	Always on
19	C66x CorePac4	Always on
20	C66x CorePac5	Always on
21	C66x CorePac6	Always on
22	C66x CorePac7	Always on
23	DDR3A EMIF	Always on
24	DDR3B EMIF	Always on
25	TAC	Software control
26	RAC_0 and RAC_1	Software control
27	RAC_2 and RAC_3	Software control
28	FFTC_0	Software control
29	FFTC_1	Software control

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Table 8-7 Clock Domains (Part 2 of 2)

LPSC Number	Module(s)	Notes
30	FFTC_2	Software control
31	FFTC_3	Software control
32	FFTC_4	Software control
33	FFTC_5	Software control
34	AIF2	Software control
35	TCP3d_0	Software control
36	TCP3d_1	Software control
37	TCP3d_2	Software control
38	TCP3d_3	Software control
39	VCP2_0	Software control
40	VCP2_1	Software control
41	VCP2_2	Software control
42	VCP2_3	Software control
43	VCP2_4	Software control
44	VCP2_5	Software control
45	VCP2_6	Software control
46	VCP2_7	Software control
47	BCP	Software control
48	Reserved	Reserved
49	HyperLink1	Software control
50	10GbE	Software control
51	Reserved	Reserved
52	Reserved	Reserved
No LPSC	Bootcfg, PSC, and PLL Controller	These modules do not use LPSC
End of Table 8-7		

8.3.3 PSC Register Memory Map

Table 8-8 shows the PSC Register memory map.

Table 8-8 PSC Register Memory Map (Part 1 of 5)

Offset	Register	Description
0x000	PID	Peripheral Identification Register
0x004 - 0x010	Reserved	Reserved
0x014	VCNTLID	Voltage Control Identification Register
0x018 - 0x11C	Reserved	Reserved
0x120	PTCMD	Power Domain Transition Command Register
0x124	Reserved	Reserved
0x128	PTSTAT	Power Domain Transition Status Register
0x12C - 0x1FC	Reserved	Reserved
0x200	PDSTAT0	Power Domain Status Register 0
0x204	PDSTAT1	Power Domain Status Register 1
0x208	PDSTAT2	Power Domain Status Register 2
0x20C	PDSTAT3	Power Domain Status Register 3
0x210	PDSTAT4	Power Domain Status Register 4

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Table 8-8 PSC Register Memory Map (Part 2 of 5)

Offset	Register	Description
0x214	PDSTAT5	Power Domain Status Register 5
0x218	PDSTAT6	Power Domain Status Register 6
0x21C	PDSTAT7	Power Domain Status Register 7
0x220	PDSTAT8	Power Domain Status Register 8
0x224	PDSTAT9	Power Domain Status Register 9
0x228	PDSTAT10	Power Domain Status Register 10
0x22C	PDSTAT11	Power Domain Status Register 11
0x230	PDSTAT12	Power Domain Status Register 12
0x234	PDSTAT13	Power Domain Status Register 13
0x238	PDSTAT14	Power Domain Status Register 14
0x23C	PDSTAT15	Power Domain Status Register 15
0x240	PDSTAT16	Power Domain Status Register 16
0x244	PDSTAT17	Power Domain Status Register 17
0x248	PDSTAT18	Power Domain Status Register 18
0x24C	PDSTAT19	Power Domain Status Register 19
0x250	PDSTAT20	Power Domain Status Register 20
0x254	PDSTAT21	Power Domain Status Register 21
0x258	PDSTAT22	Power Domain Status Register 22
0x25C	PDSTAT23	Power Domain Status Register 23
0x260	PDSTAT24	Power Domain Status Register 24
0x264	PDSTAT25	Power Domain Status Register 25
0x268	PDSTAT26	Power Domain Status Register 26
0x26C	PDSTAT27	Power Domain Status Register 27
0x270	PDSTAT28	Power Domain Status Register 28
0x274	PDSTAT29	Power Domain Status Register 29
0x278	PDSTAT30	Power Domain Status Register 30
0x27C	PDSTAT31	Power Domain Status Register 31
0x27C - 0x2FC	Reserved	Reserved
0x300	PDCTL0	Power Domain Control Register 0
0x304	PDCTL1	Power Domain Control Register 1
0x308	PDCTL2	Power Domain Control Register 2
0x30C	PDCTL3	Power Domain Control Register 3
0x310	PDCTL4	Power Domain Control Register 4
0x314	PDCTL5	Power Domain Control Register 5
0x318	PDCTL6	Power Domain Control Register 6
0x31C	PDCTL7	Power Domain Control Register 7
0x320	PDCTL8	Power Domain Control Register 8
0x324	PDCTL9	Power Domain Control Register 9
0x328	PDCTL10	Power Domain Control Register 10
0x32C	PDCTL11	Power Domain Control Register 11
0x330	PDCTL12	Power Domain Control Register 12
0x334	PDCTL13	Power Domain Control Register 13
0x338	PDCTL14	Power Domain Control Register 14
0x33C	PDCTL15	Power Domain Control Register 15

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Table 8-8 PSC Register Memory Map (Part 3 of 5)

Offset	Register	Description
0x340	PDCTL16	Power Domain Control Register 16
0x344	PDCTL17	Power Domain Control Register 17
0x348	PDCTL18	Power Domain Control Register 18
0x34C	PDCTL19	Power Domain Control Register 19
0x350	PDCTL20	Power Domain Control Register 20
0x354	PDCTL21	Power Domain Control Register 21
0x358	PDCTL22	Power Domain Control Register 22
0x35c	PDCTL23	Power Domain Control Register 23
0x360	PDCTL24	Power Domain Control Register 24
0x364	PDCTL25	Power Domain Control Register 25
0x368	PDCTL26	Power Domain Control Register 26
0x36C	PDCTL27	Power Domain Control Register 27
0x370	PDCTL28	Power Domain Control Register 28
0x374	PDCTL29	Power Domain Control Register 29
0x378	PDCTL30	Power Domain Control Register 30
0x37C	PDCTL31	Power Domain Control Register 31
0x380 - 0x7FC	Reserved	Reserved
0x800	MDSTAT0	Module Status Register 0 (never gated)
0x804	MDSTAT1	Module Status Register 1
0x808	MDSTAT2	Module Status Register 2
0x80C	MDSTAT3	Module Status Register 3
0x810	MDSTAT4	Module Status Register 4
0x814	MDSTAT5	Module Status Register 5
0x818	MDSTAT6	Module Status Register 6
0x81C	MDSTAT7	Module Status Register 7
0x820	MDSTAT8	Module Status Register 8
0x824	MDSTAT9	Module Status Register 9
0x828	MDSTAT10	Module Status Register 10
0x82C	MDSTAT11	Module Status Register 11
0x830	MDSTAT12	Module Status Register 12
0x834	MDSTAT13	Module Status Register 13
0x838	MDSTAT14	Module Status Register 14
0x83C	MDSTAT15	Module Status Register 15
0x840	MDSTAT16	Module Status Register 16
0x844	MDSTAT17	Module Status Register 17
0x848	MDSTAT18	Module Status Register 18
0x84C	MDSTAT19	Module Status Register 19
0x850	MDSTAT20	Module Status Register 20
0x854	MDSTAT21	Module Status Register 21
0x858	MDSTAT22	Module Status Register 22
0x85C	MDSTAT23	Module Status Register 23
0x860	MDSTAT24	Module Status Register 24
0x864	MDSTAT25	Module Status Register 25
0x868	MDSTAT26	Module Status Register 26

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Table 8-8 PSC Register Memory Map (Part 4 of 5)

Offset	Register	Description
0x86C	MDSTAT27	Module Status Register 27
0x870	MDSTAT28	Module Status Register 28
0x874	MDSTAT29	Module Status Register 29
0x878	MDSTAT30	Module Status Register 30
0x87C	MDSTAT31	Module Status Register31
0x880	MDSTAT32	Module Status Register 32
0x884	MDSTAT33	Module Status Register 33
0x888	MDSTAT34	Module Status Register 34
0x88C	MDSTAT35	Module Status Register 35
0x890	MDSTAT36	Module Status Register 36
0x894	MDSTAT37	Module Status Register 37
0x898	MDSTAT38	Module Status Register 38
0x89C	MDSTAT39	Module Status Register 39
0x8A0	MDSTAT40	Module Status Register 40
0x8A4	MDSTAT41	Module Status Register 41
0x8A8	MDSTAT42	Module Status Register 42
0x8AC	MDSTAT43	Module Status Register 43
0x8B0	MDSTAT44	Module Status Register 44
0x8B4	MDSTAT45	Module Status Register 45
0x8B8	MDSTAT46	Module Status Register 46
0x8BC	MDSTAT47	Module Status Register 47
0x8C0	MDSTAT48	Module Status Register 48
0x8C4	MDSTAT49	Module Status Register 49
0x8C8	MDSTAT50	Module Status Register 50
0x8CC	MDSTAT51	Module Status Register 51
0x8D0	MDSTAT52	Module Status Register 52
0x8D4 - 0x9FC	Reserved	Reserved
0xA00	MDCTL0	Module Control Register 0 (never gated)
0xA04	MDCTL1	Module Control Register 1
0xA08	MDCTL2	Module Control Register 2
0xA0C	MDCTL3	Module Control Register 3
0xA10	MDCTL4	Module Control Register 4
0xA14	MDCTL5	Module Control Register 5
0xA18	MDCTL6	Module Control Register 6
0xA1C	MDCTL7	Module Control Register 7
0xA20	MDCTL8	Module Control Register 8
0xA24	MDCTL9	Module Control Register 9
0xA28	MDCTL10	Module Control Register 10
0xA2C	MDCTL11	Module Control Register 11
0xA30	MDCTL12	Module Control Register 12
0xA34	MDCTL13	Module Control Register 13
0xA38	MDCTL14	Module Control Register 14
0xA3C	MDCTL15	Module Control Register 15
0xA40	MDCTL16	Module Control Register 16

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Table 8-8 PSC Register Memory Map (Part 5 of 5)

Offset	Register	Description
0xA44	MDCTL17	Module Control Register 17
0xA48	MDCTL18	Module Control Register 18
0xA4C	MDCTL19	Module Control Register 19
0xA50	MDCTL20	Module Control Register 20
0xA54	MDCTL21	Module Control Register 21
0xA58	MDCTL22	Module Control Register 22
0xA5C	MDCTL23	Module Control Register 23
0xA60	MDCTL24	Module Control Register 24
0xA64	MDCTL25	Module Control Register 25
0xA68	MDCTL26	Module Control Register 26
0xA6C	MDCTL27	Module Control Register 27
0xA70	MDCTL28	Module Control Register 28
0xA74	MDCTL29	Module Control Register 29
0xA78	MDCTL30	Module Control Register 30
0xA7C	MDCTL31	Module Control Register31
0xA80	MDCTL32	Module Control Register 32
0xA84	MDCTL33	Module Control Register 33
0xA88	MDCTL34	Module Control Register 34
0xA8C	MDCTL35	Module Control Register 35
0xA90	MDCTL36	Module Control Register 36
0xA94	MDCTL37	Module Control Register 37
0xA98	MDCTL38	Module Control Register 38
0xA9C	MDCTL39	Module Control Register 39
0xAA0	MDCTL40	Module Control Register 40
0xAA4	MDCTL41	Module Control Register 41
0xAA8	MDCTL42	Module Control Register 42
0xAAC	MDCTL43	Module Control Register 43
0xAB0	MDCTL44	Module Control Register 44
0xAB4	MDCTL45	Module Control Register 45
0xAB8	MDCTL46	Module Control Register 46
0xABC	MDCTL47	Module Control Register 47
0xAC0	MDCTL48	Module Control Register 48
0xAC4	MDCTL49	Module Control Register 49
0xAC8	MDCTL50	Module Control Register 50
0xACC	MDCTL51	Module Control Register 51
0xAD0	MDCTL52	Module Control Register 52
0xAD4 - 0xFFC	Reserved	Reserved
End of Table 8-8		

8.4 Reset Controller

The reset controller detects the different type of resets supported on the TCI6634K2K device and manages the distribution of those resets throughout the device. The device has the following types of resets:

- Power-on reset

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- Hard reset
- Soft reset
- Local reset

Table 8-9 explains further the types of reset, the reset initiator, and the effects of each reset on the device. For more information on the effects of each reset on the PLL controllers and their clocks, see Section 8.4.7 "Reset Electrical Data/Timing" on page 234.

Table 8-9 Reset Types

Type	Initiator	Effect(s)
Power-on reset	$\overline{\text{POR}}$ pin $\overline{\text{RESETFULL}}$ pin	Resets the entire chip including the test and emulation logic. The device configuration pins are latched only during power-on reset.
Hard reset	$\overline{\text{RESET}}$ pin PLLCTL [1] Register (RSCTRL) Watchdog timers Emulation	Hard reset resets everything except for test, emulation logic, and reset isolation modules. This reset is different from power-on reset in that the PLL Controller assumes power and clocks are stable when a hard reset is asserted. The device configurations pins are not relatched. Emulation-initiated reset is always a hard reset. By default, these initiators are configured as hard reset, but can be configured (except emulation) as a soft reset in the RSCFG Register of the PLL Controller. Contents of the DDR3 SDRAM memory can be retained during a hard reset if the SDRAM is placed in self-refresh mode.
Soft reset	$\overline{\text{RESET}}$ pin PLLCTL Register (RSCTRL) Watchdog timers	Soft reset behaves like hard reset except that PCIe MMRs (memory-mapped registers) and DDR3 EMIF MMRs contents are retained. By default, these initiators are configured as hard reset, but can be configured as soft reset in the RSCFG Register of the PLL Controller. Contents of the DDR3 SDRAM memory can be retained during a soft reset if the SDRAM is placed in self-refresh mode.
Local reset	$\overline{\text{LRESET}}$ pin Watchdog timer timeout LPSC MMRs	Resets the C66x CorePac, without disturbing clock alignment or memory contents. The device configuration pins are not relatched.
End of Table 8-9		

1 All masters in the device have access to the PLL Control Registers.

8.4.1 Power-on Reset

Power-on reset is used to reset the entire device, including the test and emulation logic.

Power-on reset is initiated by the following:

1. $\overline{\text{POR}}$ pin
2. $\overline{\text{RESETFULL}}$ pin

During power-up, the $\overline{\text{POR}}$ pin must be asserted (driven low) until the power supplies have reached their normal operating conditions. Also a $\overline{\text{RESETFULL}}$ pin is provided to allow reset of the entire device, including the reset-isolated logic, when the device is already powered up. For this reason, the $\overline{\text{RESETFULL}}$ pin, unlike $\overline{\text{POR}}$, should be driven by the on-board host control other than the power good circuitry. For power-on reset, the Main PLL Controller comes up in bypass mode and the PLL is not enabled. Other resets do not affect the state of the PLL or the dividers in the PLL Controller.

The following sequence must be followed during a power-on reset:

1. Wait for all power supplies to reach normal operating conditions while keeping the $\overline{\text{POR}}$ pin asserted (driven low). While $\overline{\text{POR}}$ is asserted, all pins except $\overline{\text{RESETSTAT}}$ will be set to high-impedance. After the $\overline{\text{POR}}$ pin is deasserted (driven high), all Z group pins, low group pins, and high group pins are set to their reset state and remain in their reset state until otherwise configured by their respective peripheral. All peripherals that are power-managed are disabled after a power-on reset and must be enabled through the Device State Control Registers (for more details, see 6.2.3 "Device State Control Registers" on page 186).

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2. Clocks are reset, and they are propagated throughout the chip to reset any logic that was using reset synchronously. All logic is now reset and RESETSTAT is driven low, indicating that the device is in reset.
3. POR must be held active until all supplies on the board are stable, and then for at least an additional period of time (as specified in Section 8.2.1 "Power-Up Sequencing" on page 217) for the chip-level PLLs to lock.
4. The POR pin can now be de-asserted. Reset-sampled pin values are latched at this point. Then, all chip-level PLLs are taken out of reset, locking sequences begin, and all power-on device initialization processes begin.
5. After device initialization is complete, the RESETSTAT pin is de-asserted (driven high). By this time, the DDR3A PLL and DDR3B PLL have already completed their locking sequences and are supplying a valid clock. The system clocks of the PLL controllers are allowed to finish their current cycles and then are paused for 10 cycles of their respective system reference clocks. After the pause, the system clocks are restarted at their default divide-by settings.
6. The device is now out of reset and code execution begins as dictated by the selected boot mode.

Note—To most of the device, reset is de-asserted only when the POR and RESET pins are both de-asserted (driven high). Therefore, in the sequence described above, if the RESET pin is held low past the low period of the POR pin, most of the device will remain in reset. The RESET pin should not be tied to the POR pin.

8.4.2 Hard Reset

A hard reset will reset everything on the device except the PLLs, test logic, emulation logic, and reset-isolated modules. POR should also remain de-asserted during this time.

Hard reset is initiated by the following:

- RESET pin
- RSCTRL Register in the PLL Controller
- Watchdog timer
- Emulation

By default, all the initiators listed above are configured to generate a hard reset. Except for emulation, all of the other three initiators can be configured in the RSCFG Register in the PLL Controller to generate soft resets.

The following sequence must be followed during a hard reset:

1. The RESET pin is asserted (driven low) for a minimum of 24 CLKIN1 cycles. During this time the RESET signal propagates to all modules (except those specifically mentioned above). To prevent off-chip contention during the warm reset, all I/O must be Hi-Z for modules affected by RESET.
2. Once all logic is reset, RESETSTAT is asserted (driven low) to denote that the device is in reset.
3. The RESET pin can now be released. A minimal device initialization begins to occur. Note that configuration pins are not re-latched and clocking is unaffected within the device.
4. After device initialization is complete, the RESETSTAT pin is de-asserted (driven high).

Note—The POR pin should be held inactive (high) throughout the warm reset sequence. Otherwise, if POR is activated (brought low), the minimum POR pulse width must be met. The RESET pin should not be tied to the POR pin.

8.4.3 Soft Reset

A soft reset behaves like a hard reset except that the PCIe MMRs (memory-mapped registers), DDR3A and DDR3B EMIF MMRs content is retained. POR should also remain de-asserted during this time.

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Soft reset is initiated by the following:

- $\overline{\text{RESET}}$ pin
- RSCTRL Register in the PLL Controller
- Watchdog timer

In the case of a soft reset, the clock logic and the power control logic of the peripherals are not affected, and, therefore, the enabled/disabled state of the peripherals is not affected. On a soft reset, the DDR3A and DDR3B memory controller registers are ***not*** reset. If the user places the DDR3A and DDR3B SDRAM in self-refresh mode before invoking the soft reset, the DDR3A and DDR3B SDRAM memory content is retained.

During a soft reset, the following occurs:

1. The $\overline{\text{RESETSTAT}}$ pin goes low to indicate an internal reset is being generated. The reset propagates through the system. Internal system clocks are not affected. PLLs remain locked.
2. After device initialization is complete, the $\overline{\text{RESETSTAT}}$ pin is deasserted (driven high). In addition, the PLL Controller pauses system clocks for approximately 8 cycles.

   At this point:

   - The peripherals remain in the state they were in before the soft reset.
   - The states of the Boot Mode configuration pins are preserved as controlled by the DEVSTAT Register.
   - The DDR3A and DDR3B MMRs and PCIe MMRs retain their previous values. Only the DDR3A and DDR3B memory controller and PCIe state machines are reset by the soft reset.
   - The PLL Controller remains in the mode it was in prior to the soft reset.
   - System clocks are unaffected.

The boot sequence is started after the system clocks are restarted. Because the Boot Mode configuration pins are not latched with a soft reset, the previous values (as shown in the DEVSTAT Register), are used to select the boot mode.

8.4.4 Local Reset

The local reset can be used to reset a particular C66x CorePac without resetting any other device components.

Local reset is initiated by the following:

- $\overline{\text{LRESET}}$ pin
- Watchdog timer should cause one of the below based on the setting of the CORESEL[2:0] and RSTCFG registers in the PLL Controller. (See "Reset Configuration Register (RSTCFG)" on page 244 and 5.3.2 "CIC Registers" on page 158.)
  - Local reset
  - NMI
  - NMI followed by a time delay and then a local reset for the C66x CorePac selected
  - Hard reset by requesting reset via the PLL Controller
- LPSC MMRs (memory-mapped registers)

For more details see the *Phase Locked Loop (PLL) Controller for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22)

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8.4.5 Reset Priority

If any of the above reset sources occur simultaneously, the PLL Controller processes only the highest priority reset request. The reset request priorities are as follows (high to low):

- Power-on reset
- Hard/soft reset

8.4.6 Reset Controller Register

The reset controller registers are part of the PLL Controller MMRs. All TCI6634 device-specific MMRs are covered in Section 8.5.2 "PLL Controller Memory Map" on page 239. For more details on these registers and how to program them, see the *Phase Locked Loop (PLL) Controller for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

8.4.7 Reset Electrical Data/Timing

Table 8-10 Reset Timing Requirements (1)
(see Figure 8-4 and Figure 8-5)

No.			Min	Max	Unit
		RESETFULL Pin Reset			
1	tw(RESETFULL)	Pulse width - pulse width RESETFULL low	500C		ns
		Soft/Hard-Reset			
2	tw(RESET)	Pulse width - pulse width RESET low	500C		ns
End of Table 8-10					

1 C = 1/SYSCLK1 clock frequency in ns

Table 8-11 Reset Switching Characteristics (1)
(see Figure 8-4 and Figure 8-5)

No.	Parameter		Min	Max	Unit
		RESETFULL Pin Reset			
3	td(RESETFULLH-RESETSTATH)	Delay time - RESETSTAT high after RESETFULL high		50000C	ns
		Soft/Hard Reset			
4	td(RESETH-RESETSTATH)	Delay time - RESETSTAT high after RESET high		50000C	ns
End of Table 8-11					

1 C = 1/SYSCLK1 clock frequency in ns

Figure 8-4 RESETFULL Reset Timing

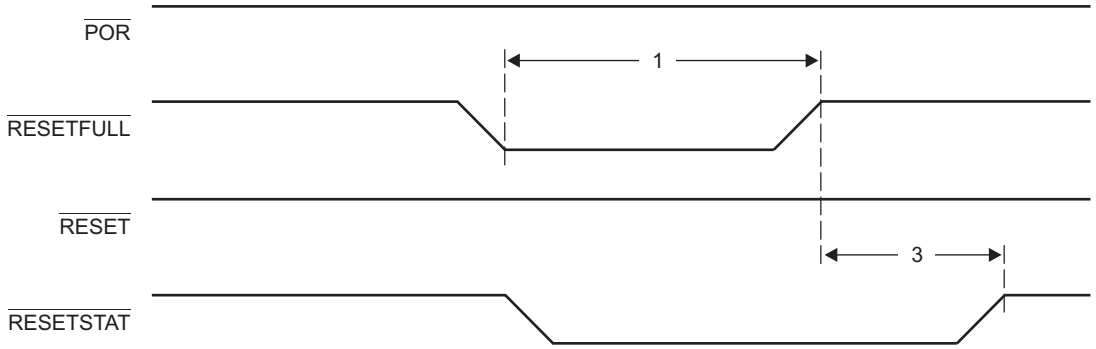

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Figure 8-5 Soft/Hard Reset Timing

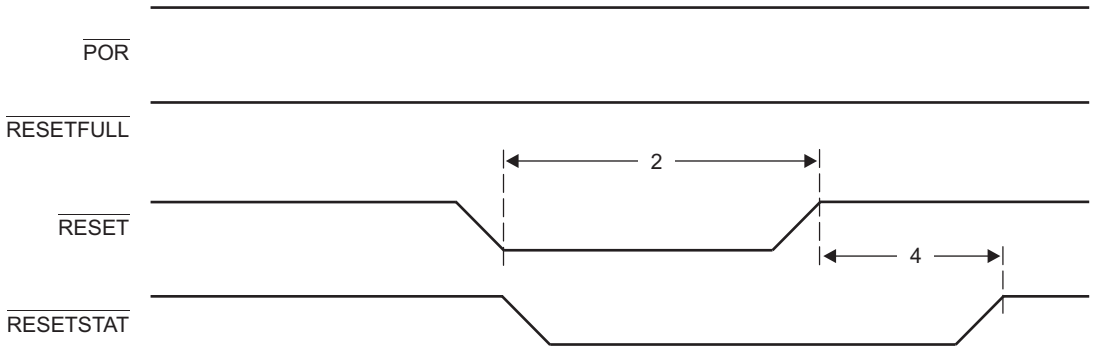
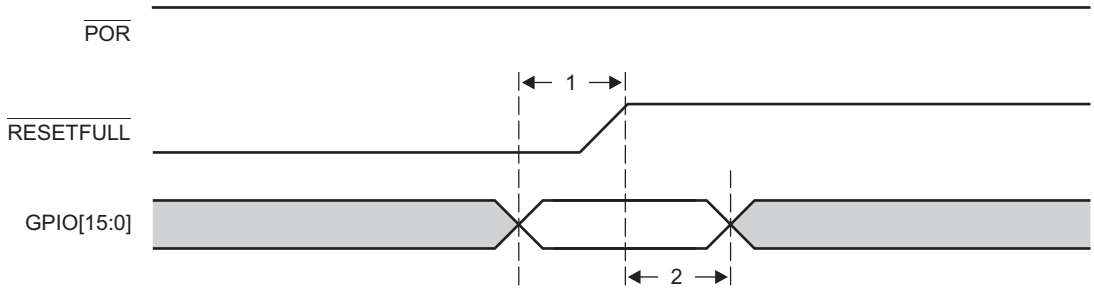


Table 8-12 Boot Configuration Timing Requirements (1)
See Figure 8-6)

No.			Min	Max	Unit
1	tsu(GPIOn-RESETFULL)	Setup time - GPIO valid before RESETFULL asserted	12C		ns
2	th(RESETFULL-GPIOn)	Hold time - GPIO valid after RESETFULL asserted	12C		ns
End of Table 8-12					

1 C = 1/SYSCLK1 clock frequency in ns.

Figure 8-6 Boot Configuration Timing



8.5 Main PLL, DDR3A PLL, DDR3B PLL, PASS PLL and the PLL Controllers

This section provides a description of the Main PLL, DDR3A PLL, DDR3B PLL, PASS PLL, and the PLL Controller. For details on the operation of the PLL Controller module, see the *Phase Locked Loop (PLL) Controller for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

The Main PLL is controlled by the standard PLL Controller. The PLL Controller manages the clock ratios, alignment, and gating for the system clocks to the device. By default, the device powers up with the main PLL bypassed. Figure 8-7 shows a block diagram of the Main PLL and the PLL Controller.

The DDR3A PLL, DDR3B PLL, and PASS PLL are used to provide dedicated clock to the DDR3A, DDR3B, and PASS respectively. These chip level PLLs support a wide range of multiplier and divider values, which can be programmed through the chip level registers located in the Device Control Register block. The Boot ROM will program the multiplier values for main PLL, and PASS PLL based on boot mode. (See "Device Boot and Configuration" on page 174 for more details.)

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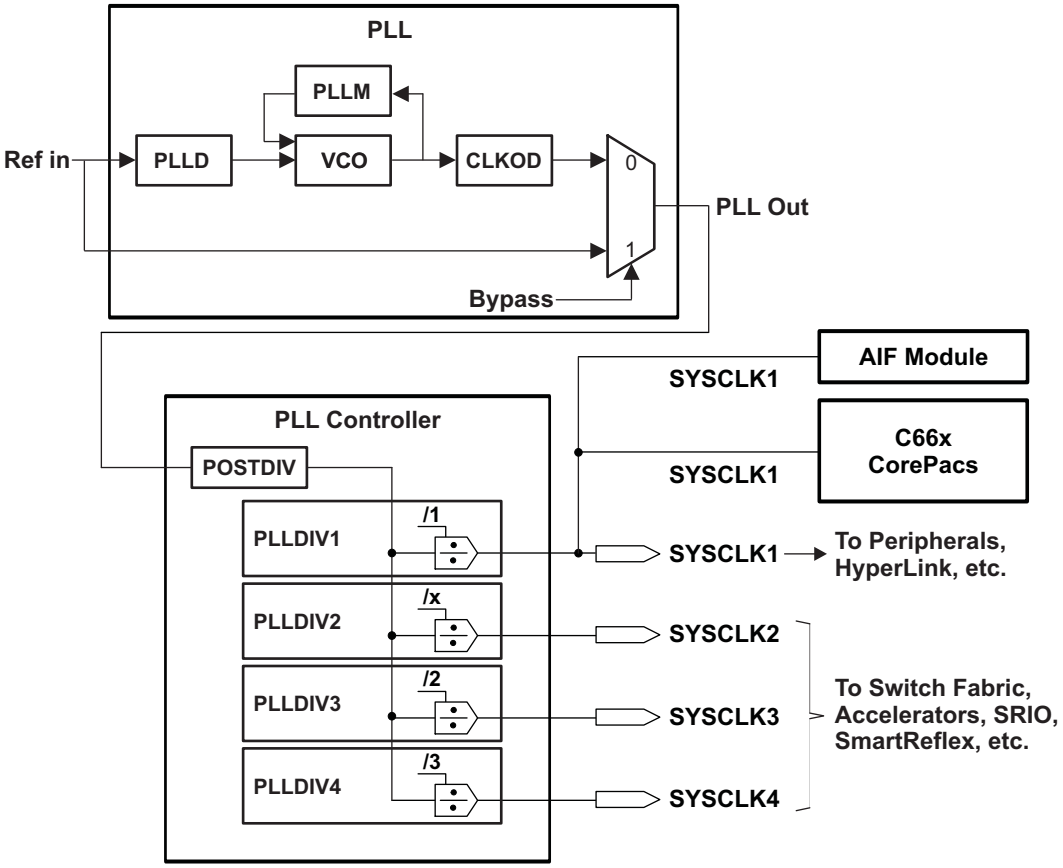
The DDR3A PLL and DDR3B PLL are used to supply clocks to DDR3A and DDR3B EMIF logic. These PLLs can also be used without programming the PLL Controller. Instead, they can be controlled using the chip-level registers (DDR3APLLCTL0, DDR3APLLCTL1,DDR3BPLLCTL0, DDR3BPLLCTL1) located in the Device Control Register block. To write to these registers, software must go through an unlocking sequence using the KICK0/KICK1 registers.

The multiplier values for all chip-level PLLs can be reprogrammed later based on the input parameter table. This feature provides flexibility in that these PLLs may be able to reuse other clock sources instead of having its own clock source.

Figure 8-7 Main PLL and PLL Controller



Note that the Main PLL Controller registers can be accessed by any master in the device. The PLLM[5:0] bits of the multiplier are controlled by the PLLM Register inside the PLL Controller and the PLLM[12:6] bits are controlled by the chip-level MAINPLLCTL0 Register. The output divide and bypass logic of the PLL are controlled by fields in the SECCTL Register in the PLL Controller. Only PLLDIV3, and PLLDIV4 are programmable on the device. See the *Phase Locked Loop (PLL) Controller for KeyStone Devices User Guide* in section 1.9 "Related Documentation from Texas Instruments" on page 22for more details on how to program the PLL controller.

The multiplication and division ratios within the PLL and the post-division for each of the chip-level clocks are determined by a combination of this PLL and the Main PLL Controller. The Main PLL Controller also controls reset propagation through the chip, clock alignment, and test points. The Main PLL Controller monitors the PLL status and provides an output signal indicating when the PLL is locked.

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Main PLL power is supplied externally via the Main PLL power-supply pin (AVDDA1). An external EMI filter circuit must be added to all PLL supplies. See the *Hardware Design Guide for KeyStone Devices* in section 1.9 "Related Documentation from Texas Instruments" on page 22 for detailed recommendations. For the best performance, TI recommends that all the PLL external components be on a single side of the board without jumpers, switches, or components other than those shown. For reduced PLL jitter, maximize the spacing between switching signal traces and the PLL external components (C1, C2, and the EMI Filter).

The minimum SYSCLK rise and fall times should also be observed. For the input clock timing requirements, see Section 8.5.4 "Main PLL Controller/SRIO/HyperLink/PCIe Clock Input Electrical Data/Timing".

It should be assumed that any registers not included in these sections are not supported by the device. Furthermore, only the bits within the registers described here are supported. Avoid writing to any reserved memory location or changing the value of reserved bits.

The PLL Controller module as described in the *Phase Locked Loop (PLL) Controller for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22 includes a superset of features, some of which are not supported on the TCI6634K2K device. The following sections describe the registers that are supported.

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8.5.1 Main PLL Controller Device-Specific Information

8.5.1.1 Internal Clocks and Maximum Operating Frequencies

The Main PLL, used to drive theC66x CorePacs, the switch fabric, and a majority of the peripheral clocks (all but the DDR3 and the PASS modules) requires a PLL Controller to manage the various clock divisions, gating, and synchronization. The Main PLL Controller has four SYSCLK outputs that are listed below, along with the clock descriptions. Each SYSCLK has a corresponding divider that divides down the output clock of the PLL. Note that dividers are not programmable unless explicitly mentioned in the description below.

- **SYSCLK1:** Full-rate clock for all C66x CorePacs. Using local dividers, SYSCLK1 is used to derive clocks required for the majority of peripherals that do not need reset isolation.

  The system peripherals and modules driven by SYSCLK1 are as follows; however, not all peripherals are supported in every part. See the Features chapter for the complete list of peripherals supported in your part.

  AIF2, BCP, FFTC, RAC, TAC, TCP3d, VCP2, EMIF16, USB 3.0, XGMII, HyperLink, PCIe, SGMII, SRIO, GPIO, Timer64, I^2C, SPI, TeraNet, UART, ROM, CIC, Security Manager, BootCFG, PSC, Queue Manager, Semaphore, MPUs, EDMA, MSMC, DDR3, EMIF.
- **SYSCLK2:** Full-rate, reset-isolated clock used to generate various other clocks required by peripherals that need reset isolation: e.g., SmartReflex and SRIO.
- **SYSCLK3:** 1/x-rate clock used to clock the C66x CorePac emulation. The default rate for this clock is 1/3. This clock is programmable from /1 to /32, where this clock does not violate the maximum of 350 MHz. SYSCLK3 can be turned off by software.
- **SYSCLK4:** 1/z-rate clock for the system trace module only. The default rate for this clock is 1/5. This clock is configurable: the maximum configurable clock is 210 MHz and the minimum configuration clock is 32 MHz. SYSCLK4 can be turned off by software.

Only SYSCLK3 and SYSCLK4 are programmable.

8.5.1.2 Local Clock Dividers

The clock signals from the Main PLL Controller are routed to various modules and peripherals on the device. Some modules and peripherals have one or more internal clock dividers. Other modules and peripherals have no internal clock dividers, but are grouped together and receive clock signals from a shared local clock divider. Internal and shared local clock dividers have fixed division ratios. See table Table 8-13.

Table 8-13 Main PLL Controller Module Clock Domains Internal and Shared Local Clock Dividers

Clock	Module	Internal Clock Divider(s)	Shared Local Clock Divider
SYSCLK1 Internal Clock Dividers			
SYSCLK1	10 Gigabit Media Independent Interface (XGMII)	/3, /6	--
	Antenna Interface Subsystem 2 (AIF2)	/3, /6	--
	Bit Rate Coprocessor (BCP)	/3	--
	C66x DSP CorePacs	/1, /2, /3, /4	--
	Chip Interrupt Controllers (CICx)	/6	--
	DDR3 Memory Controller A (also receives clocks from the DDR3A_PLL)	/2	--
	DDR3 Memory Controller B (also receives clocks from the DDR3B_PLL)	/3	--
	EMIF16	/6	--
	Enhanced Viterbi-Decoder Coprocessor (VCP)	/3	--
	Fast Fourier Transform Coprocessor (FFTC)	/3	--
	HyperLink	/2, /3, /6	--
	Multicore Navigator Queue Manager	/3	--
	MultiCore Shared Memory Controller (MSMC)	/1	--
	PCI express (PCIe)	/2, /3, /4, /6	--
	Receive Accelerator Coprocessor (RAC)	/3, /4	--
	ROM	/6	--
	Serial Gigabit Media Independent Interface (SGMII)	/2, /3, /6, /8	--
	Transmit Accelerator Coprocessor (TAC)	/3	--
	Turbo Decoder Coprocessor (TCP3d)	/2, /3	--
	Universal Asynchronous Receiver/Transmitter (UART)	/6	--
	Universal Serial Bus 3.0 (USB 3.0)	/3, /6	--
SYSCLK1 Shared Local Clock Dividers			
SYSCLK1	Power/Sleep Controller (PSC)	--	/12, /24
	EDMA	--	/3
	Memory Protection Units (MPUx)		
	Semaphore		
	TeraNet (CPU/3 domain)		
SYSCLK1	Boot Config	--	/6
	General-Purpose Input/Output (GPIO)		
	I^2C		
	Security Manager		
	Serial Peripheral Interconnect (SPI)		
	TeraNet (CPU /6 domain)		
	Timers		
SYSCLK2 Internal Clock Dividers			
SYSCLK2	Serial RapidIO (SRIO)	/3, /4, /6	--
	SmartReflex C66x CorePacs	/12, /128	--
End of Table 8-13			

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8.5.1.3 Module Clock Input

Table 8-7 lists various clock domains in the device and their distribution in each peripheral. The table also shows the distributed clock division in modules and their mapping with source clocks of the device PLLs.

8.5.1.4 Main PLL Controller Operating Modes

The Main PLL Controller has two modes of operation: bypass mode and PLL mode. The mode of operation is determined by the BYPASS bit of the PLL Secondary Control Register (SECCTL).

- In bypass mode, PLL input is fed directly out as SYSCLK1.
- In PLL mode, SYSCLK1 is generated from the PLL output using the values set in the PLLM and PLLD fields in the MAINPLLCTL0 Register.

External hosts must avoid access attempts to the DSP while the frequency of its internal clocks is changing. User software must implement a mechanism that causes the DSP to notify the host when the PLL configuration has completed.

8.5.1.5 Main PLL Stabilization, Lock, and Reset Times

The PLL stabilization time is the amount of time that must be allotted for the internal PLL regulators to become stable after device power-up. The device should not be taken out of reset until this stabilization time has elapsed.

The PLL reset time is the amount of wait time needed when resetting the PLL (writing PLLRST = 1), in order for the PLL to properly reset, before bringing the PLL out of reset (writing PLLRST = 0). For the Main PLL reset time value, see Table 8-14.

The PLL lock time is the amount of time needed from when the PLL is taken out of reset to when the PLL Controller can be switched to PLL mode. The Main PLL lock time is given in Table 8-14.

Table 8-14 Main PLL Stabilization, Lock, and Reset Times

Parameter	Min	Typ	Max	Unit
PLL stabilization time	100			µs
PLL lock time			2000 × C (1)	
PLL reset time	1000			ns
End of Table 8-14				

1 C = SYSCLK1(N|P) cycle time in ns.

8.5.2 PLL Controller Memory Map

The memory map of the Main PLL Controller is shown in Table 8-15. TCI6634K2K-specific Main PLL Controller Register definitions can be found in the sections following Table 8-15. For other registers in the table, see the *Phase Locked Loop (PLL) Controller for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

It is recommended to use read-modify-write sequence to make any changes to the valid bits in the Main PLL Controller registers.

Note that only registers documented here are accessible on the TCI6634K2K. Other addresses in the Main PLL Controller memory map including the Reserved registers must not be modified. Furthermore, only the bits within the registers described here are supported.

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Table 8-15 PLL Controller Registers (Including Reset Controller)

Hex Address Range	Acronym	Register Name
00 0231 0000 - 00 0231 00E3	-	Reserved
00 0231 00E4	RSTYPE	Reset Type Status Register (Reset Main PLL Controller)
00 0231 00E8	RSTCTRL	Software Reset Control Register (Reset Main PLL Controller)
00 0231 00EC	RSTCFG	Reset Configuration Register (Reset Main PLL Controller)
00 0231 00F0	RSISO	Reset Isolation Register (Reset Main PLL Controller)
00 0231 00F0 - 00 0231 00FF	-	Reserved
00 0231 0100	PLLCTL	PLL Control Register
00 0231 0104	-	Reserved
00 0231 0108	SECCTL	PLL Secondary Control Register
00 0231 010C	-	Reserved
00 0231 0110	PLLM	PLL Multiplier Control Register
00 0231 0114	-	Reserved
00 0231 0118	PLLDIV1	PLL Controller Divider 1Register
00 0231 011C	PLLDIV2	PLL Controller Divider 2 Register
00 0231 0120	PLLDIV3	PLL Controller Divider 3Register
00 0231 0124	-	Reserved
00 0231 0128	POSTDIV	PLL Controller Post-Divide Register
00 0231 012C - 00 0231 0134	-	Reserved
00 0231 0138	PLLCMD	PLL Controller Command Register
00 0231 013C	PLLSTAT	PLL Controller Status Register
00 0231 0140	ALNCTL	PLL Controller Clock Align Control Register
00 0231 0144	DCHANGE	PLLDIV Ratio Change Status Register
00 0231 0148	CKEN	Reserved
00 0231 014C	CKSTAT	Reserved
00 0231 0150	SYSTAT	SYSCLK Status Register
00 0231 0154 - 00 0231 015C	-	Reserved
00 0231 0160	PLLDIV4	PLL Controller Divider 4Register
00 0231 0164	PLLDIV5	Reserved
00 0231 0168	PLLDIV6	Reserved
00 0231 016C	PLLDIV7	Reserved
00 0231 0170	PLLDIV8	Reserved
00 0231 0174 - 00 0231 0193	PLLDIV9 - PLLDIV16	Reserved
00 0231 0194 - 00 0231 01FF	-	Reserved
End of Table 8-15		

8.5.2.1 PLL Secondary Control Register (SECCTL)

The PLL Secondary Control Register contains extra fields to control the Main PLL and is shown in Figure 8-8 and described in Table 8-16.

Figure 8-8 PLL Secondary Control Register (SECCTL)

31 24	23	22 19	18 0
Reserved	BYPASS	OUTPUT DIVIDE	Reserved
R-0000 0000	RW-1	RW-0001	RW-001 0000 0000 0000 0000

Legend: R/W = Read/Write; R = Read only; -*n* = value after reset

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Table 8-16 PLL Secondary Control Register Field Descriptions

Bit	Field	Description
31-24	Reserved	Reserved
23	BYPASS	Main PLL bypass enable 0 = Main PLL bypass disabled 1 = Main PLL bypass enabled
22-19	OUTPUT DIVIDE	Output divider ratio bits 0h = ÷1. Divide frequency by 1 1h = ÷2. Divide frequency by 2 2h = ÷3. Divide frequency by 3 3h = ÷4. Divide frequency by 4 4h - Fh = ÷5 to ÷16. Divide frequency range: divide frequency by 5 to divide frequency by 80.
18-0	Reserved	Reserved
End of Table 8-16		

8.5.2.2 PLL Controller Divider Register (PLLDIV3, and PLLDIV4)

The PLL Controller Divider Registers (PLLDIV3 and PLLDIV4) are shown in Figure 8-9 and described in Table 8-17. The default values of the RATIO field on a reset for PLLDIV3, and PLLDIV4 are different as mentioned in the footnote of Figure 8-9.

Figure 8-9 PLL Controller Divider Register (PLLDIVn)

31 16	15	14 8	7 0
Reserved	Dn (1) EN	Reserved	RATIO
R-0	R/W-1	R-0	R/W-n (2)

Legend: R/W = Read/Write; R = Read only; -*n* = value after reset

1 D2EN for PLLDIV2; D5EN for PLLDIV5; D8EN for PLLDIV8

2 n=02h for PLLDIV2; n=04h for PLLDIV5; n=3Fh for PLLDIV8

Table 8-17 PLL Controller Divider Register Field Descriptions

Bit	Field	Description
31-16	Reserved	Reserved
15	D*n*EN	Divider D*n* enable bit (See footnote of Figure 8-9) 0 = Divider *n* is disabled 1 = No clock output. Divider *n* is enabled.
14-8	Reserved	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
7-0	RATIO	Divider ratio bits (See footnote of Figure 8-9) 0h = ÷1. Divide frequency by 1 1h = ÷2. Divide frequency by 2 2h = ÷3. Divide frequency by 3 3h = ÷4. Divide frequency by 4 4h - 4Fh = ÷5 to ÷80. Divide frequency range: divide frequency by 5 to divide frequency by 80.
End of Table 8-17		

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8.5.2.3 PLL Controller Clock Align Control Register (ALNCTL)

The PLL Controller Clock Align Control Register (ALNCTL) is shown in Figure 8-10 and described in Table 8-18.

Figure 8-10 PLL Controller Clock Align Control Register (ALNCTL)

31	5	4	3	2	0
Reserved		ALN4	ALN3	Reserved	
R-0		R/W-1	R/W-1	R-0	

Legend: R/W = Read/Write; R = Read only; -*n* = value after reset, for reset value

Table 8-18 PLL Controller Clock Align Control Register Field Descriptions

Bit	Field	Description
31-5 2-0	Reserved	Reserved. This location is always read as 0. A value written to this field has no effect.
4 3	ALN4 ALN3	SYSCLK*n* alignment. Do not change the default values of these fields. 0 = Do not align SYSCLK*n* to other SYSCLKs during GO operation. If SYS*n* in DCHANGE is set, SYSCLK*n* switches to the new ratio immediately after the GOSET bit in PLLCMD is set. 1 = Align SYSCLK*n* to other SYSCLKs selected in ALNCTL when the GOSET bit in PLLCMD is set and SYS*n* in DCHANGE is 1. The SYSCLK*n* rate is set to the ratio programmed in the RATIO bit in PLLDIV*n*.
End of Table 8-18		

8.5.2.4 PLLDIV Divider Ratio Change Status Register (DCHANGE)

Whenever a different ratio is written to the PLLDIV*n* registers, the PLL CTL flags the change in the DCHANGE Status Register. During the GO operation, the PLL controller changes only the divide ratio of the SYSCLKs with the bit set in DCHANGE. Note that the ALNCTL Register determines if that clock also needs to be aligned to other clocks. The PLLDIV Divider Ratio Change Status Register is shown in Figure 8-11 and described in Table 8-19.

Figure 8-11 PLLDIV Divider Ratio Change Status Register (DCHANGE)

31	5	4	3	2	0
Reserved		SYS4	SYS3	Reserved	
R-0		R/W-1	R/W-1	R-0	

Legend: R/W = Read/Write; R = Read only; -*n* = value after reset, for reset value

Table 8-19 PLLDIV Divider Ratio Change Status Register Field Descriptions

Bit	Field	Description
31-5 2-0	Reserved	Reserved. This bit location is always read as 0. A value written to this field has no effect.
4 3	SYS4 SYS3	Identifies when the SYSCLK*n* divide ratio has been modified. 0 = SYSCLK*n* ratio has not been modified. When GOSET is set, SYSCLK*n* will not be affected. 1 = SYSCLK*n* ratio has been modified. When GOSET is set, SYSCLK*n* will change to the new ratio.
End of Table 8-19		

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8.5.2.5 SYSCLK Status Register (SYSTAT)

The SYSCLK Status Register (SYSTAT) shows the status of SYSCLK[4:1]. SYSTAT is shown in Figure 8-12 and described in Table 8-20.

Figure 8-12 SYSCLK Status Register (SYSTAT)

31	4	3	2	1	0
Reserved		SYS4ON	SYS3ON	SYS2ON	SYS1ON
R-n		R-1	R-1	R-1	R-1

Legend: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 8-20 SYSCLK Status Register Field Descriptions

Bit	Field	Description
31-4	Reserved	Reserved. This location is always read as 0. A value written to this field has no effect.
3-0	SYS[N (1)]ON	SYSCLK[N] on status 0 = SYSCLK[N] is gated 1 = SYSCLK[N] is on
End of Table 8-20		

1 Where N = 1, 2, 3, or 4

8.5.2.6 Reset Type Status Register (RSTYPE)

The Reset Type Status (RSTYPE) Register latches the cause of the last reset. If multiple reset sources occur simultaneously, this register latches the highest priority reset source. The Reset Type Status Register is shown in Figure 8-13 and described in Table 8-21.

Figure 8-13 Reset Type Status Register (RSTYPE)

31 29	28	27 12	11 8	7 3	2	1	0
Reserved	EMU-RST	Reserved	WDRST[N]	Reserved	PLLCTRLRST	$\overline{\text{RESET}}$	POR
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Legend: R = Read only; -*n* = value after reset

Table 8-21 Reset Type Status Register Field Descriptions (Part 1 of 2)

Bit	Field	Description
31-29	Reserved	Reserved. Always reads as 0. Writes have no effect.
28	EMU-RST	Reset initiated by emulation 0 = Not the last reset to occur 1 = The last reset to occur
27-12	Reserved	Reserved. Always reads as 0. Writes have no effect.
11 10 9 8	WDRST3 WDRST2 WDRST1 WDRST0	Reset initiated by Watchdog Timer[N] 0 = Not the last reset to occur 1 = The last reset to occur
7-3	Reserved	Reserved. Always reads as 0. Writes have no effect.
2	PLLCTLRST	Reset initiated by PLLCTL 0 = Not the last reset to occur 1 = The last reset to occur

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Table 8-21 Reset Type Status Register Field Descriptions (Part 2 of 2)

Bit	Field	Description
1	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ reset 0 = $\overline{\text{RESET}}$ was not the last reset to occur 1 = $\overline{\text{RESET}}$ was the last reset to occur
0	POR	Power-on reset 0 = Power-on reset was not the last reset to occur 1 = Power-on reset was the last reset to occur
End of Table 8-21		

8.5.2.7 Reset Control Register (RSTCTRL)

This register contains a key that enables writes to the MSB of this register and the RSTCFG register. The key value is 0x5A69. A valid key will be stored as 0x000C. Any other key value is invalid. When the RSTCTRL or the RSTCFG is written, the key is invalidated. Every write must be set up with a valid key. The Software Reset Control Register (RSTCTRL) is shown in Figure 8-14 and described in Table 8-22.

Figure 8-14 Reset Control Register (RSTCTRL)

31 17	16	15 0
Reserved	SWRST	KEY
R-0x0000	R/W-0x (1)	R/W-0x0003

Legend: R = Read only; -*n* = value after reset;

1 Writes are conditional based on valid key.

Table 8-22 Reset Control Register Field Descriptions

Bit	Field	Description
31-17	Reserved	Reserved
16	SWRST	Software reset 0 = Reset 1 = Not reset
15-0	KEY	Key used to enable writes to RSTCTRL and RSTCFG.
End of Table 8-22		

8.5.2.8 Reset Configuration Register (RSTCFG)

This register is used to configure the type of reset (a hard reset or a soft reset) initiated by $\overline{\text{RESET}}$, the watchdog timer, and the Main PLL Controller's RSTCTRL Register. By default, these resets are hard resets. The Reset Configuration Register (RSTCFG) is shown in Figure 8-15 and described in Table 8-23.

Figure 8-15 Reset Configuration Register (RSTCFG)

31 16	15 14	13	12	11 4	3 0
Reserved	Reserved	PLLCTLRSTTYPE	$\overline{\text{RESET}}$TYPE	Reserved	WDTYPE[N (1)]
R-0x0000	R-00	R/W-0 (2)	R/W-0[2]	R-0x0	R/W-0x00[2]

Legend: R = Read only; R/W = Read/Write; -*n* = value after reset

1 Where N = 1, 2, 3,....N (Not all these outputs may be used on a specific device.)
2 Writes are conditional based on valid key. For details, see Section 8.5.2.7 "Reset Control Register (RSTCTRL)".

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Table 8-23 Reset Configuration Register Field Descriptions

Bit	Field	Description
31-14	Reserved	Reserved
13	PLLCTLRSTTYPE	PLL controller initiates a software-driven reset of type: 0 = Hard reset (default) 1 = Soft reset
12	$\overline{\text{RESET}}$TYPE	$\overline{\text{RESET}}$ initiates a reset of type: 0 = Hard reset (default) 1 = Soft reset
11-4	Reserved	Reserved
3 2 1 0	WDTYPE3 WDTYPE2 WDTYPE1 WDTYPE0	Watchdog timer [N] initiates a reset of type: 0 = Hard reset (default) 1 = Soft reset
End of Table 8-23		

8.5.2.9 Reset Isolation Register (RSISO)

This register is used to select the module clocks that must maintain their clocking without pausing through non-power-on reset. Setting any of these bits effectively blocks reset to all Main PLL Control Registers in order to maintain current values of PLL multiplier, divide ratios, and other settings. Along with setting the module-specific bit in RSISO, the corresponding MDCTLx[12] bit also needs to be set in the PSC to reset-isolate a particular module. For more information on the MDCTLx Register, see the *Power Sleep Controller (PSC) for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22. The Reset Isolation Register (RSISO) is shown in Figure 8-16 and described in Table 8-24.

Figure 8-16 Reset Isolation Register (RSISO)

31 16	15 10	9	8	7 4	3	2 0
Reserved	Reserved	SRIOISO	SRISO	Reserved	AIF2ISO Reserved	Reserved
R-0x0000	R-0x00	R/W-0	R/W-0	R-0x0	R/W-0	R-000

Legend: R = Read only; R/W = Read/Write; -*n* = value after reset

Table 8-24 Reset Isolation Register Field Descriptions

Bit	Field	Description
31-10	Reserved	Reserved.
9	SRIOISO	Isolate SRIO module control 0 = Not reset isolated 1 = Reset isolated
8	SRISO	Isolate SmartReflex control 0 = Not reset isolated 1 = Reset isolated
7-4	Reserved	Reserved
3	AIF2ISO	Isolate AIF2 module control 0 = Not reset isolated 1 = Reset isolated
3	Reserved	Reserved
2-0	Reserved	Reserved
End of Table 8-24		

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8.5.3 Main PLL Control Registers

The Main PLL uses two chip-level registers (MAINPLLCTL0 and MAINPLLCTL1) along with the Main PLL Controller for its configuration. These MMRs (memory-mapped registers) exist inside the Bootcfg space. To write to these registers, software should go through an unlocking sequence using the KICK0 and KICK1 registers. These registers reset only on a $\overline{\text{POR}}$ reset.

For valid configurable values of the MAINPLLCTL registers, see Section 6.1.3.1 "System PLL Settings" on page 184. See Section 6.2.3.4 "Kicker Mechanism (KICK0 and KICK1) Register" on page 191 for the address location of the KICK registers and their locking and unlocking sequences.

See Figure 8-17 and Table 8-25 for MAINPLLCTL0 details and Figure 8-18 and Table 8-26 for MAINPLLCTL1 details.

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Figure 8-17 Main PLL Control Register 0 (MAINPLLCTL0)

31–24	23–19	18–12	11–6	5–0
BWADJ[7:0]	Reserved	PLLM[12:6]	Reserved	PLLD
RW,+0000 0101	RW - 0000 0	RW,+0000000	RW, +000000	RW,+000000

Legend: RW = Read/Write; -*n* = value after reset

Table 8-25 Main PLL Control Register 0 (MAINPLLCTL0) Field Descriptions

Bit	Field	Description
31-24	BWADJ[7:0]	BWADJ[11:8] and BWADJ[7:0] are located in MAINPLLCTL0 and MAINPLLCTL1 registers. BWADJ[11:0] should be programmed to a value equal to half of PLLM[12:0] value (round down if PLLM has an odd value) Example: If PLLM = 15, then BWADJ = 7.
23-19	Reserved	Reserved
18-12	PLLM[12:6]	7-bits of a 13-bit field PLLM that selects the values for the multiplication factor. PLLM field is loaded with the multiply factor minus 1. The PLLM[5:0] bits of the multiplier are controlled by the PLLM register inside the PLL Controller and the PLLM[12:6] bits are controlled by the above chip-level register. MAINPLLCTL0 register PLLM[12:6] bits should be written just before writing to PLLM register PLLM[5:0] bits in the controller to have the complete 13 bit value latched when the GO operation is initiated in the PLL controller. See the *Phase Locked Loop (PLL) Controller for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22for the recommended programming sequence. Output Divide ratio and Bypass enable/disable of the Main PLL is also controlled by the SECCTL register in the PLL Controller. See the "PLL Secondary Control Register (SECCTL)" on page 240 for more details.
11-6	Reserved	Reserved
5-0	PLLD	A 6-bit field that selects the values for the reference divider. PLLD field is loaded with reference divide value minus 1.
End of Table 8-25		

Figure 8-18 Main PLL Control Register 1 (MAINPLLCTL1)

31–4	3–0
Reserved	BWADJ[11:8]
RW - 00000000000000000000000000000	RW- 0000

Legend: RW = Read/Write; -*n* = value after reset

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Table 8-26 Main PLL Control Register 1 (MAINPLLCTL1) Field Descriptions

Bit	Field	Description
31-4	Reserved	Reserved
3-0	BWADJ[11:8]	BWADJ[11:8] and BWADJ[7:0] are located in MAINPLLCTL0 and MAINPLLCTL1 registers. BWADJ[11:0] should be programmed to a value equal to half of PLLM[12:0] value (round down if PLLM has an odd value) Example: If PLLM = 15, then BWADJ = 7
End of Table 8-26		

8.5.4 Main PLL Controller/SRIO/HyperLink/PCIe Clock Input Electrical Data/Timing

Table 8-27 Main PLL Controller/SRIO/HyperLink/PCIe Clock Input Timing Requirements (1) (Part 1 of 2)
(see Figure 8-19 and Figure 8-20)

No.			Min	Max	Unit
		SYSCLK[P:N]			
1	tc(SYSCLKN)	Cycle time SYSCLKN cycle time	3.25 or 6.51 or 8.138 (2)		ns
1	tc(SYSCLKP)	Cycle time SYSCLKP cycle time	3.25 or 6.51 or 8.138		ns
3	tw(SYSCLKN)	Pulse width SYSCLKN high	0.45*tc	0.55*tc	ns
2	tw(SYSCLKN)	Pulse width SYSCLKN low	0.45*tc	0.55*tc	ns
2	tw(SYSCLKP)	Pulse width SYSCLKP high	0.45*tc	0.55*tc	ns
3	tw(SYSCLKP)	Pulse width SYSCLKP low	0.45*tc	0.55*tc	ns
4	tr(SYSCLKN_250 mv)	Transition time SYSCLKN rise time (250 mV)	50	350	ps
4	tf(SYSCLKN_250 mv)	Transition time SYSCLKN fall time (250 mV)	50	350	ps
4	tr(SYSCLKP_250 mv)	Transition time SYSCLKP rise time (250 mV)	50	350	ps
4	tf(SYSCLKP_250 mv)	Transition time SYSCLKP fall time (250 mV)	50	350	ps
5	tj(SYSCLKN)	Jitter, peak_to_peak _ periodic SYSCLKN		100 (4 (3))	ps
5	tj(SYSCLKP)	Jitter, peak_to_peak _ periodic SYSCLKP		100 (4)	ps
		ALTCORECLK[P:N]			
1	tc(ALTCORCLKN)	Cycle time ALTCORECLKN cycle time	3.2	25	ns
1	tc(ALTCORECLKP)	Cycle time ALTCORECLKP cycle time	3.2	25	ns
3	tw(ALTCORECLKN)	Pulse width ALTCORECLKN high	0.45*tc(ALTCORECLKN)	0.55*tc(ALTCORECLKN)	ns
2	tw(ALTCORECLKN)	Pulse width ALTCORECLKN low	0.45*tc(ALTCORECLKN)	0.55*tc(ALTCORECLKN)	ns
2	tw(ALTCORECLKP)	Pulse width ALTCORECLKP high	0.45*tc(ALTCORECLKP)	0.55*tc(ALTCORECLKP)	ns
3	tw(ALTCORECLKP)	Pulse width ALTCORECLKP low	0.45*tc(ALTCORECLKP)	0.55*tc(ALTCORECLKP)	ns
4	tr(ALTCORECLKN_250 mv)	Transition time ALTCORECLKN rise time (250 mV)	50	350	ps
4	tf(ALTCORECLKN_250 mv)	Transition time ALTCORECLKN fall time (250 mV)	50	350	ps
4	tr(ALTCORECLKP_250 mv)	Transition time ALTCORECLKP rise time (250 mV)	50	350	ps
4	tf(ALTCORECLKP_250 mv)	Transition time ALTCORECLKP fall time (250 mV)	50	350	ps
5	tj(ALTCORECLKN)	Jitter, peak_to_peak _ periodic ALTCORECLKN		100	ps
5	tj(ALTCORECLKP)	Jitter, peak_to_peak _ periodic ALTCORECLKP		100	ps
		SRIOSGMIICLK[P:N]			
1	tc(SRIOSMGMIICLKN)	Cycle time SRIOSMGMIICLKN cycle time	TBD		ns
1	tc(SRIOSMGMIICLKP)	Cycle time SRIOSMGMIICLKP cycle time	TBD		ns
3	tw(SRIOSMGMIICLKN)	Pulse width SRIOSMGMIICLKN high	TBD	TBD	ns
2	tw(SRIOSMGMIICLKN)	Pulse width SRIOSMGMIICLKN low	TBD	TBD	ns
2	tw(SRIOSMGMIICLKP)	Pulse width SRIOSMGMIICLKP high	TBD	TBD	ns
3	tw(SRIOSMGMIICLKP)	Pulse width SRIOSMGMIICLKP low	TBD	TBD	ns

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Table 8-27 Main PLL Controller/SRIO/HyperLink/PCIe Clock Input Timing Requirements [1] (Part 2 of 2)
(see Figure 8-19 and Figure 8-20)

No.			Min	Max	Unit
4	tr(SRIOSMGMIICLKN_250mv)	Transition time SRIOSMGMIICLKN rise time (250 mV)	TBD	TBD	ps
4	tf(SRIOSMGMIICLKN_250mv)	Transition time SRIOSMGMIICLKN fall time (250 mV)	TBD	TBD	ps
4	tr(SRIOSMGMIICLKP_250mv)	Transition time SRIOSMGMIICLKP rise time (250 mV)	TBD	TBD	ps
4	tf(SRIOSMGMIICLKP_250mv)	Transition time SRIOSMGMIICLKP fall time (250 mV)	TBD	TBD	ps
5	tj(SRIOSMGMIICLKN)	Jitter, RMS SRIOSMGMIICLKN		TBD	ps, RMS
5	tj(SRIOSMGMIICLKP)	Jitter, RMS SRIOSMGMIICLKP		TBD	ps, RMS
5	tj(SRIOSMGMIICLKN)	Jitter, RMS SRIOSMGMIICLKN (SRIO not used)		TBD	ps, RMS
5	tj(SRIOSMGMIICLKP)	Jitter, RMS SRIOSMGMIICLKP (SRIO not used)		TBD	ps, RMS
HyperLink CLK[P:N]					
1	tc(HYPCLKN)	Cycle time HYPCLKN cycle time	3.2 or 4 or 6.4		ns
1	tc(HYPCLKP)	Cycle time HYPCLKP cycle time	3.2 or 4 or 6.4		ns
3	tw(HYPCLKN)	Pulse width HYPCLKN high	0.45*tc(HYPCLKN)	0.55*tc(HYPCLKN)	ns
2	tw(HYPCLKN)	Pulse width HYPCLKN low	0.45*tc(HYPCLKN)	0.55*tc(HYPCLKN)	ns
2	tw(HYPCLKP)	Pulse width HYPCLKP high	0.45*tc(HYPCLKP)	0.55*tc(HYPCLKP)	ns
3	tw(HYPCLKP)	Pulse width HYPCLKP low	0.45*tc(HYPCLKP)	0.55*tc(HYPCLKP)	ns
4	tr(HYPCLKN_250mv)	Transition time HYPCLKN rise time (250 mV)	50	350	ps
4	tf(HYPCLKN_250mv)	Transition time HYPCLKN fall time (250 mV)	50	350	ps
4	tr(HYPCLKP_250mv)	Transition time HYPCLKP rise time (250 mV)	50	350	ps
4	tf(HYPCLKP_250mv)	Transition time HYPCLKP fall time (250 mV)	50	350	ps
5	tj(HYPCLKN)	Jitter, RMS HYPCLKN		4	ps, RMS
5	tj(HYPCLKP)	Jitter, RMS HYPCLKP		4	ps, RMS
PCIECLK[P:N]					
1	tc(PCIECLKN)	Cycle time PCIECLKN cycle time	3.2 or 4 or 6.4 or 10		ns
1	tc(PCIECLKP)	Cycle time PCIECLKP cycle time	3.2 or 4 or 6.4 or 10		ns
3	tw(PCIECLKN)	Pulse width PCIECLKN high	0.45*tc(PCIECLKN)	0.55*tc(PCIECLKN)	ns
2	tw(PCIECLKN)	Pulse width PCIECLKN low	0.45*tc(PCIECLKN)	0.55*tc(PCIECLKN)	ns
2	tw(PCIECLKP)	Pulse width PCIECLKP high	0.45*tc(PCIECLKP)	0.55*tc(PCIECLKP)	ns
3	tw(PCIECLKP)	Pulse width PCIECLKP low	0.45*tc(PCIECLKP)	0.55*tc(PCIECLKP)	ns
4	tr(PCIECLKN_250mv)	Transition time PCIECLKN rise time (250 mV)	50	350	ps
4	tf(PCIECLKN_250mv)	Transition time PCIECLKN fall time (250 mV)	50	350	ps
4	tr(PCIECLKP_250mv)	Transition time PCIECLKP rise time (250 mV)	50	350	ps
4	tf(PCIECLKP_250mv)	Transition time PCIECLKP fall time (250 mV)	50	350	ps
5	tj(PCIECLKN)	Jitter, RMS PCIECLKN		4	ps, RMS
5	tj(PCIECLKP)	Jitter, RMS PCIECLKP		4	ps, RMS
End of Table 8-27					

1 See the Hardware Design Guide for KeyStone Devices in 1.9 "Related Documentation from Texas Instruments" on page 22for detailed recommendations.
2 If AIF2 is being used then SYSCLK(N|P) can be programmed only to fixed values, if AIF2 is not being used then any value in the range between the min and max values can be used.
3 If AIF2 is used then the Max allowed jitter on SYSCLK(N|P) is 4ps RMS

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Figure 8-19 Main PLL Controller/SRIO/HyperLink/PCIe Clock Input Timing

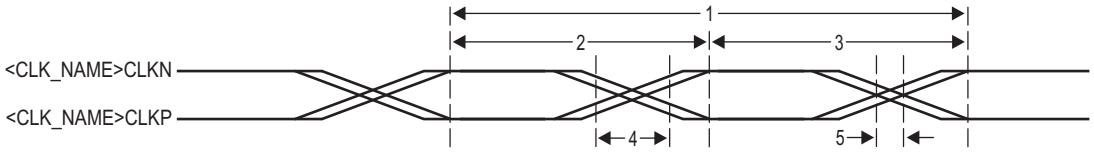
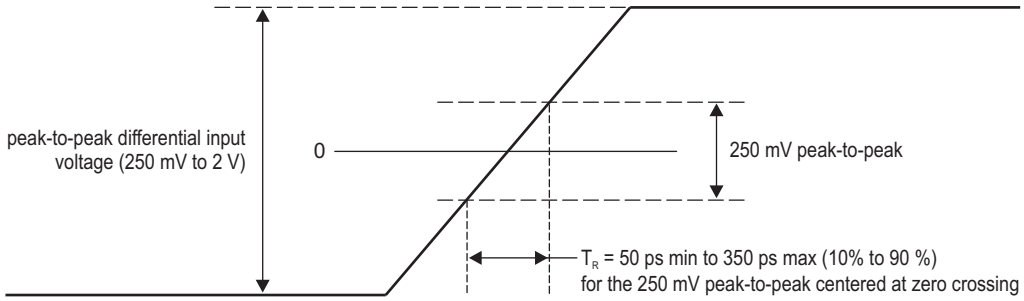


Figure 8-20 Main PLL Transition Time

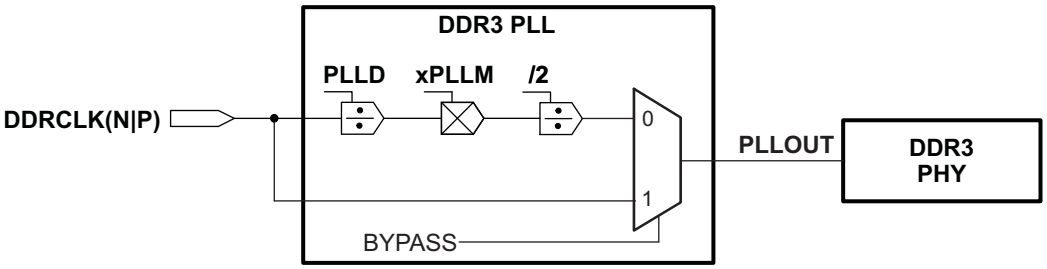


8.6 DDR3A PLL and DDR3B PLL

The DDR3A PLL and DDR3B PLL generate interface clocks for the DDR3A and DDR3B memory controllers. When coming out of power-on reset, DDR3A PLL and DDR3B PLL are programmed to a valid frequency during the boot configuration process before being enabled and used.

DDR3A PLL and DDR3B PLL power is supplied via the DDR3 PLL power-supply pin (AVDDA2). An external EMI filter circuit must be added to all PLL supplies. See the *Hardware Design Guide for KeyStone Devices* in 1.9 "Related Documentation from Texas Instruments" on page 22for detailed recommendations.

Figure 8-21 DDR3A PLL and DDR3B PLL Block Diagram



8.6.1 DDR3A PLL and DDR3B PLL Control Registers

The DDR3A PLL and DDR3B PLL, which are used to drive the DDR3A PHY and DDR3B PHY for the EMIF, do not use a PLL controller. DDR3A PLL and DDR3B PLL can be controlled using the DDR3APLLCTL0/DDR3BPLLCTL0 and DDR3APLLCTL1/DDR3BPLLCTL1 registers located in the Bootcfg module. These MMRs (memory-mapped registers) exist inside the Bootcfg space. To write to these registers, software must go through an unlocking sequence using the KICK0 and KICK1 registers. For suggested configurable values, see 6.1.3.1 "System PLL Settings" on page 184. See 6.2.3.4 "Kicker Mechanism (KICK0 and KICK1)

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Register" on page 191 for the address location of the registers and locking and unlocking sequences for accessing the registers. These registers are reset on POR only.

Figure 8-22 DDR3A PLL and DDR3B PLL Control Register 0 (DDR3APLLCTL0/DDR3BPLLCTL0)

31–24	23	22–19	18–6	5–0
BWADJ[7:0]	BYPASS	CLKOD	PLLM	PLLD
RW,+0000 1001	RW,+0	RW,+0001	RW,+0000000010011	RW,+000000

Legend: RW = Read/Write; -*n* = value after reset

Table 8-28 DDR3A PLL and DDR3B PLL Control Register 0 Field Descriptions

Bit	Field	Description
31-24	BWADJ[7:0]	BWADJ[11:8] and BWADJ[7:0] are located in DDR3PLLCTL0 and DDR3PLLCTL1 registers. BWADJ[11:0] should be programmed to a value equal to half of PLLM[12:0] value (round down if PLLM has an odd value) Example: If PLLM = 15, then BWADJ = 7
23	BYPASS	Enable bypass mode 0 = Bypass disabled 1 = Bypass enabled
22-19	CLKOD	A 4-bit field that selects the values for the PLL post divider. Valid post divider values are 1 and even values from 2 to 16. CLKOD field is loaded with output divide value minus 1
18-6	PLLM	A 13-bit field that selects the values for the PLL multiplication factor. PLLM field is loaded with the multiply factor minus 1
5-0	PLLD	A 6-bit field that selects the values for the reference (input) divider. PLLD field is loaded with reference divide value minus 1
End of Table 8-28		

Figure 8-23 DDR3A PLL and DDR3B PLL Control Register 1 (DDR3APLLCTL0/DDR3BPLLCTL1)

31–15	14	13–4	3–0
Reserved	PLLRESET	Reserved	BWADJ[11:8]
RW - 00000000000000000	RW,+0	RW-00000000000	RW- 0000

Legend: RW = Read/Write; -*n* = value after reset

Table 8-29 DDR3A PLL and DDR3B PLL Control Register 1 Field Descriptions

Bit	Field	Description
31-15	Reserved	Reserved
14	PLLRESET	PLL RESET 0 = Reset deasserted to PLL 1 = Reset asserted to PLL
13-4	Reserved	Reserved
3-0	BWADJ[11:8]	BWADJ[11:8] and BWADJ[7:0] are located in MAINPLLCTL0 and MAINPLLCTL1 registers. BWADJ[11:0] should be programmed to a value equal to half of PLLM[12:0] value (round down if PLLM has an odd value) Example: If PLLM = 15, then BWADJ = 7
End of Table 8-29		

8.6.2 DDR3A PLL and DDR3B PLL Device-Specific Information

As shown in Figure 8-21, the output of DDR3A PLL and DDR3B PLL (PLLOUT) is divided by 2 and directly fed to the DDR3A and DDR3B memory controller. During power-on resets, the internal clocks of the DDR3 PLL are affected as described in Section 8.4 "Reset Controller" on page 230. The DDR3 PLL is unlocked only during the power-up sequence and is locked by the time the RESETSTAT pin goes high. It does not lose lock during any of the other resets.

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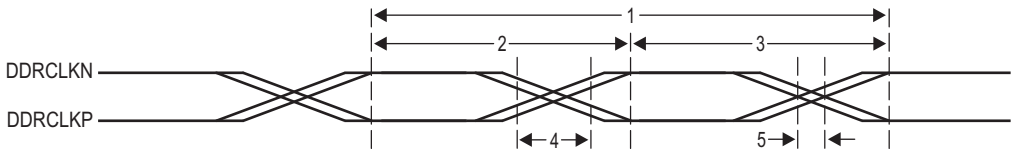
8.6.3 DDR3 PLL Input Clock Electrical Data/Timing

Table 8-30 applies to both DDR3A and DDR3B memory interfaces.

Table 8-30 DDR3 PLL DDRCLK(N|P) Timing Requirements
(see Figure 8-24 and Figure 8-20)

No.			Min	Max	Unit
		DDRCLK[P:N]			
1	tc(DDRCLKN)	Cycle time _ DDRCLKN cycle time	3.2	25	ns
1	tc(DDRCLKP)	Cycle time _ DDRCLKP cycle time	3.2	25	ns
3	tw(DDRCLKN)	Pulse width _ DDRCLKN high	0.45*tc(DDRCLKN)	0.55*tc(DDRCLKN)	ns
2	tw(DDRCLKN)	Pulse width _ DDRCLKN low	0.45*tc(DDRCLKN)	0.55*tc(DDRCLKN)	ns
2	tw(DDRCLKP)	Pulse width _ DDRCLKP high	0.45*tc(DDRCLKP)	0.55*tc(DDRCLKP)	ns
3	tw(DDRCLKP)	Pulse width _ DDRCLKP low	0.45*tc(DDRCLKP)	0.55*tc(DDRCLKP)	ns
4	tr(DDRCLKN_250 mv)	Transition time _ DDRCLKN rise time (250 mV)	50	350	ps
4	tf(DDRCLKN_250 mv)	Transition time _ DDRCLKN fall time (250 mV)	50	350	ps
4	tr(DDRCLKP_250 mv)	Transition time _ DDRCLKP rise time (250 mV)	50	350	ps
4	tf(DDRCLKP_250 mv)	Transition time _ DDRCLKP fall time (250 mV)	50	350	ps
5	tj(DDRCLKN)	Jitter, peak_to_peak _ periodic DDRCLKN		0.02*tc(DDRCLKN)	ps
5	tj(DDRCLKP)	Jitter, peak_to_peak _ periodic DDRCLKP		0.02*tc(DDRCLKP)	ps
End of Table 8-30					

Figure 8-24 DDR3 PLL DDRCLK Timing



8.7 PASS PLL

The PASS PLL generates interface clocks for the Network Coprocessor. Using the PACLKSEL pin the user can select the input source of the PASS PLL as either the output of the Main PLL mux or the PASSCLK clock reference source. When coming out of power-on reset, PASS PLL comes out in a bypass mode and needs to be programmed to a valid frequency before being enabled and used.

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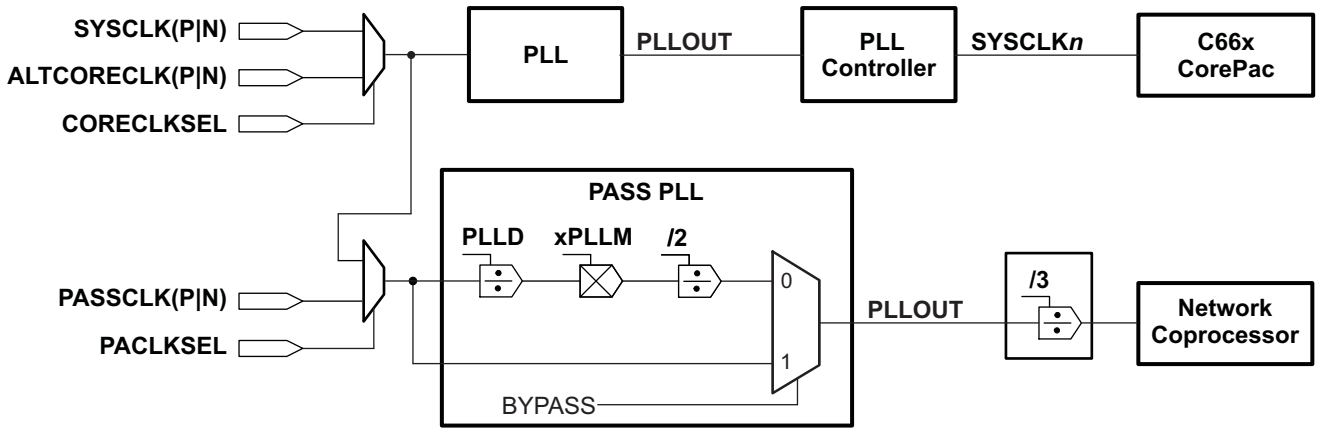
PASS PLL power is supplied via the PASS PLL power-supply pin (AVDDA3). An external EMI filter circuit must be added to all PLL supplies. See the *Hardware Design Guide for KeyStone Devices* in 1.9 "Related Documentation from Texas Instruments" on page 22for detailed recommendations.

Figure 8-25 PASS PLL Block Diagram



8.7.1 PASS PLL Local Clock Dividers

The clock signal from the PASS PLL Controller is routed to the Network Coprocessor. The Net CP module has two internal dividers with fixed division ratios. See table Table 8-31.

Table 8-31 PASS PLL Clock Domain Module Internal Clock Dividers

Clock	Module	Internal Clock Divider(s)
PLLOUT	Network Coprocessor	/13, /16
End of Table 8-31		

8.7.2 PASS PLL Control Registers

The PASS PLL, which is used to drive the Network Coprocessor, does not use a PLL controller. PASS PLL can be controlled using the PAPLLCTL0 and PAPLLCTL1 registers located in the Bootcfg module. These MMRs (memory-mapped registers) exist inside the Bootcfg space. To write to these registers, software must go through an unlocking sequence using the KICK0 and KICK1 registers. For suggested configuration values, see 6.1.3.1 "System PLL Settings" on page 184. See 6.2.3.4 "Kicker Mechanism (KICK0 and KICK1) Register" on page 191 for the address location of the registers and locking and unlocking sequences for accessing these registers. These registers are reset on $\overline{\text{POR}}$ only.

Figure 8-26 PASS PLL Control Register 0 (PASSPLLCTL0)

31–24	23	22–19	18–6	5–0
BWADJ[7:0]	BYPASS	Reserved	PLLM	PLLD
RW,+0000 1001	RW,+0	RW,+0001	RW,+0000000010011	RW,+000000

Legend: RW = Read/Write; -*n* = value after reset

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Table 8-32 PASS PLL Control Register 0 Field Descriptions (PASSPLLCTL0)

Bit	Field	Description
31-24	BWADJ[7:0]	BWADJ[11:8] and BWADJ[7:0] are located in PASSPLLCTL0 and PASSPLLCTL1 registers. BWADJ[11:0] should be programmed to a value equal to half of PLLM[12:0] value (round down if PLLM has an odd value) Example: If PLLM = 15, then BWADJ = 7
23	BYPASS	Enable bypass mode 0 = Bypass disabled 1 = Bypass enabled
22-19	Reserved	Reserved
18-6	PLLM	A 13-bit field that selects the values for the multiplication factor (see note below). PLLM field is loaded with the multiply factor minus 1.
5-0	PLLD	A 6-bit field that selects the values for the reference divider. PLLD field is loaded with reference divide value minus 1.
End of Table 8-32		

Figure 8-27 PASS PLL Control Register 1 (PASSPLLCTL1)

31 — 15	14	13 — 4	3 — 0
Reserved	PLLRESET	Reserved	BWADJ[11:8]
RW - 00000000000000000	RW,+0	RW-00000000000	RW- 0000

Legend: RW = Read/Write; -*n* = value after reset

Table 8-33 PASS PLL Control Register 1 Field Descriptions (PASSPLLCTL1)

Bit	Field	Description
31-15	Reserved	Reserved
14	PLLRESET	PLL RESET 0: Reset deasserted to PLL 1: Reset asserted to PLL
13-4	Reserved	Reserved
3-0	BWADJ[11:8]	BWADJ[11:8] and BWADJ[7:0] are located in MAINPLLCTL0 and MAINPLLCTL1 registers. BWADJ[11:0] should be programmed to a value equal to half of PLLM[12:0] value (round down if PLLM has an odd value) Example: If PLLM = 15, then BWADJ = 7
End of Table 8-33		

8.7.3 PASS PLL Device-Specific Information

As shown in Figure 8-25, the output of PASS PLL (PLLOUT) is divided by 3 and directly fed to the Network Coprocessor. During power-on resets, the internal clocks of the PASS PLL are affected as described in Section 8.4 "Reset Controller" on page 230. The PASS PLL is unlocked only during the power-up sequence and is locked by the time the $\overline{\text{RESETSTAT}}$ pin goes high. It does not lose lock during any other resets.

8.7.4 PASS PLL Input Clock Electrical Data/Timing

Table 8-34 PASS PLL Timing Requirements (Part 1 of 2)
(See Figure 8-28 and Figure 8-20)

No.			Min	Max	Unit
PASSCLK[P:N]					
1	tc(PASSCLKN)	Cycle time _ PASSCLKN cycle time	3.2	6.4	ns
1	tc(PASSCLKP)	Cycle time _ PASSCLKP cycle time	3.2	6.4	ns
3	tw(PASSCLKN)	Pulse width _ PASSCLKN high	0.45*tc(PASSCLKN)	0.55*tc(PASSCLKN)	ns
2	tw(PASSCLKN)	Pulse width _ PASSCLKN low	0.45*tc(PASSCLKN)	0.55*tc(PASSCLKN)	ns

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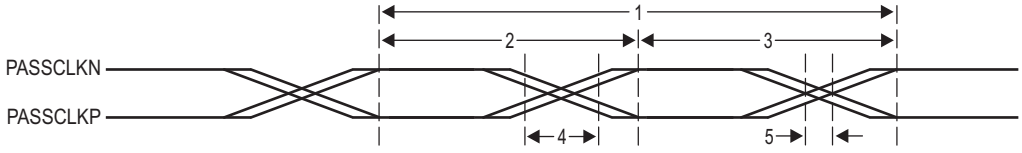
Table 8-34 PASS PLL Timing Requirements (Part 2 of 2)
(See Figure 8-28 and Figure 8-20)

No.			Min	Max	Unit
2	tw(PASSCLKP)	Pulse width _ PASSCLKP high	0.45*tc(PASSCLKP)	0.55*tc(PASSCLKP)	ns
3	tw(PASSCLKP)	Pulse width _ PASSCLKP low	0.45*tc(PASSCLKP)	0.55*tc(PASSCLKP)	ns
4	tr(PASSCLKN_250mv)	Transition time _ PASSCLKN rise time (250 mV)	50	350	ps
4	tf(PASSCLKN_250mv)	Transition time _ PASSCLKN fall time (250 mV)	50	350	ps
4	tr(PASSCLKP_250mv)	Transition time _ PASSCLKP rise time (250 mV)	50	350	ps
4	tf(PASSCLKP_250mv)	Transition time _ PASSCLKP fall time (250 mV)	50	350	ps
5	tj(PASSCLKN)	Jitter, peak_to_peak _ periodic PASSCLKN		100	ps, pk-pk
5	tj(PASSCLKP)	Jitter, peak_to_peak _ periodic PASSCLKP		100	ps, pk-pk
End of Table 8-34					

Figure 8-28 PASS PLL Timing



8.8 External Interrupts

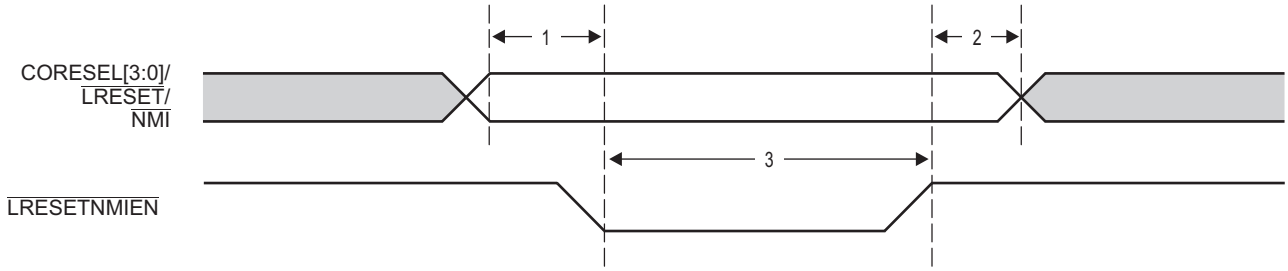
8.8.1 External Interrupts Electrical Data/Timing

Table 8-35 $\overline{\text{NMI}}$ and $\overline{\text{LRESET}}$ Timing Requirements (1)
(see Figure 8-29)

No.			Min	Max	Unit
1	tsu($\overline{\text{LRESET}}$-$\overline{\text{LRESETNMIEN}}$L)	Setup time - $\overline{\text{LRESET}}$ valid before $\overline{\text{LRESETNMIEN}}$ low	12*P		ns
1	tsu($\overline{\text{NMI}}$-$\overline{\text{LRESETNMIEN}}$L)	Setup time - $\overline{\text{NMI}}$ valid before $\overline{\text{LRESETNMIEN}}$ low	12*P		ns
1	tsu(CORESELn-$\overline{\text{LRESETNMIEN}}$L)	Setup time - CORESEL[3:0] valid before $\overline{\text{LRESETNMIEN}}$ low	12*P		ns
2	th($\overline{\text{LRESETNMIEN}}$L-$\overline{\text{LRESET}}$)	Hold time - $\overline{\text{LRESET}}$ valid after $\overline{\text{LRESETNMIEN}}$ high	12*P		ns
2	th($\overline{\text{LRESETNMIEN}}$L-$\overline{\text{NMI}}$)	Hold time - $\overline{\text{NMI}}$ valid after $\overline{\text{LRESETNMIEN}}$ high	12*P		ns
2	th($\overline{\text{LRESETNMIEN}}$L-CORESELn)	Hold time - CORESEL[3:0] valid after $\overline{\text{LRESETNMIEN}}$ high	12*P		ns
3	tw($\overline{\text{LRESETNMIEN}}$)	Pulsewidth - $\overline{\text{LRESETNMIEN}}$ low width	12*P		ns
End of Table 8-35					

1 P = 1/SYSCLK1 clock frequency in ns.

Figure 8-29 $\overline{\text{NMI}}$ and $\overline{\text{LRESET}}$ Timing



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8.9 DDR3A and DDR3B Memory Controllers

The 72-bit DDR3 Memory Controller bus of the TCI6634K2K is used to interface to JEDEC standard-compliant DDR3 SDRAM devices. The DDR3 external bus interfaces only to DDR3 SDRAM devices and does not share the bus with any other type of peripheral.

8.9.1 DDR3 Memory Controller Device-Specific Information

The TCI6634K2K includes one 64-bit wide, 1.5-V DDR3 SDRAM EMIF interface. The DDR3 interface can operate at 800 mega transfers per second (MTS), 1033 MTS, and 1333 MTS.

Due to the complicated nature of the interface, a limited number of topologies are supported to provide a 16-bit, 32-bit, or 64-bit interface.

The DDR3 electrical requirements are fully specified in the DDR Jedec Specification JESD79-3C. Standard DDR3 SDRAMs are available in 8-bit and 16-bit versions allowing for the following bank topologies to be supported by the interface:

- **72-bit:** Five 16-bit SDRAMs (including 8 bits of ECC)
- **72-bit:** Nine 8-bit SDRAMs (including 8 bits of ECC)
- **36-bit:** Three 16-bit SDRAMs (including 4 bits of ECC)
- **36-bit:** Five 8-bit SDRAMs (including 4 bits of ECC)
- **64-bit:** Four 16-bit SDRAMs
- **64-bit:** Eight 8-bit SDRAMs
- **32-bit:** Two 16-bit SDRAMs
- **32-bit:** Four 8-bit SDRAMs
- **16-bit:** One 16-bit SDRAM
- **16-bit:** Two 8-bit SDRAMs

The approach to specifying interface timing for the DDR3 memory bus is different than on other interfaces such as I^2C or SPI. For these other interfaces, the device timing was specified in terms of data manual specifications and I/O buffer information specification (IBIS) models. For the DDR3 memory bus, the approach is to specify compatible DDR3 devices and provide the printed circuit board (PCB) solution and guidelines directly to the user.

A race condition may exist when certain masters write data to the DDR3 memory controller. For example, if master A passes a software message via a buffer in external memory and does not wait for an indication that the write completes before signaling to master B that the message is ready, when master B attempts to read the software message, the master B read may bypass the master A write. Thus, master B may read stale data and receive an incorrect message.

Some master peripherals (e.g., EDMA3 transfer controllers with TCCMOD=0) always wait for the write to complete before signaling an interrupt to the system, thus avoiding this race condition. For masters that do not have a hardware specification of write-read ordering, it may be necessary to specify data ordering in the software.

If master A does not wait for an indication that a write is complete, it must perform the following workaround:

1. Perform the required write to DDR3 memory space.
2. Perform a dummy write to the DDR3 memory controller module ID and revision register.
3. Perform a dummy read to the DDR3 memory controller module ID and revision register.
4. Indicate to master B that the data is ready to be read after completion of the read in step 3. The completion of the read in step 3 ensures that the previous write was done.

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8.9.2 DDR3 Slew Rate Control

The DDR3 slew rate is controlled by use of the PHY registers. See the *KeyStone II DDR3 UserGuide* in 1.9 "Related Documentation from Texas Instruments" on page 22 for details.

8.9.3 DDR3 Memory Controller Electrical Data/Timing

The *DDR3 Implementation Guidelines* Application Report in 1.9 "Related Documentation from Texas Instruments" on page 22 specifies a complete DDR3 interface solution as well as a list of compatible DDR3 devices. The DDR3 electrical requirements are fully specified in the DDR3 Jedec Specification JESD79-3C. TI has performed the simulation and system characterization to ensure all DDR3 interface timings in this solution are met. Therefore, no electrical data/timing information is supplied here for this interface.

Note—TI supports ***only*** designs that follow the board design guidelines outlined in the application report.

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8.10 I²C Peripheral

The Inter-Integrated Circuit (I^2C) module provides an interface between DSP and other devices compliant with Philips Semiconductors (now NXP Semiconductors) Inter-Integrated Circuit bus specification version 2.1. External components attached to this 2-wire serial bus can transmit/receive up to 8-bit data to/from the device through the I^2C module.

8.10.1 I²C Device-Specific Information

The device includes multiple I^2C peripheral modules.

Note—When using the I^2C module, ensure there are external pullup resistors on the SDA and SCL pins.

The I^2C modules on the TCI6634K2K may be used by the DSP to control local peripheral ICs (DACs, ADCs, etc.), communicate with other controllers in a system, or to implement a user interface.

The I^2C port supports:

- Compatibility with Philips I^2C specification revision 2.1 (January 2000)
- Fast mode up to 400 kbps (no fail-safe I/O buffers)
- Noise filter to remove noise of 50 ns or less
- 7-bit and 10-bit device addressing modes
- Multi-master (transmit/receive) and slave (transmit/receive) functionality
- Events: DMA, interrupt, or polling
- Slew-rate limited open-drain output buffers

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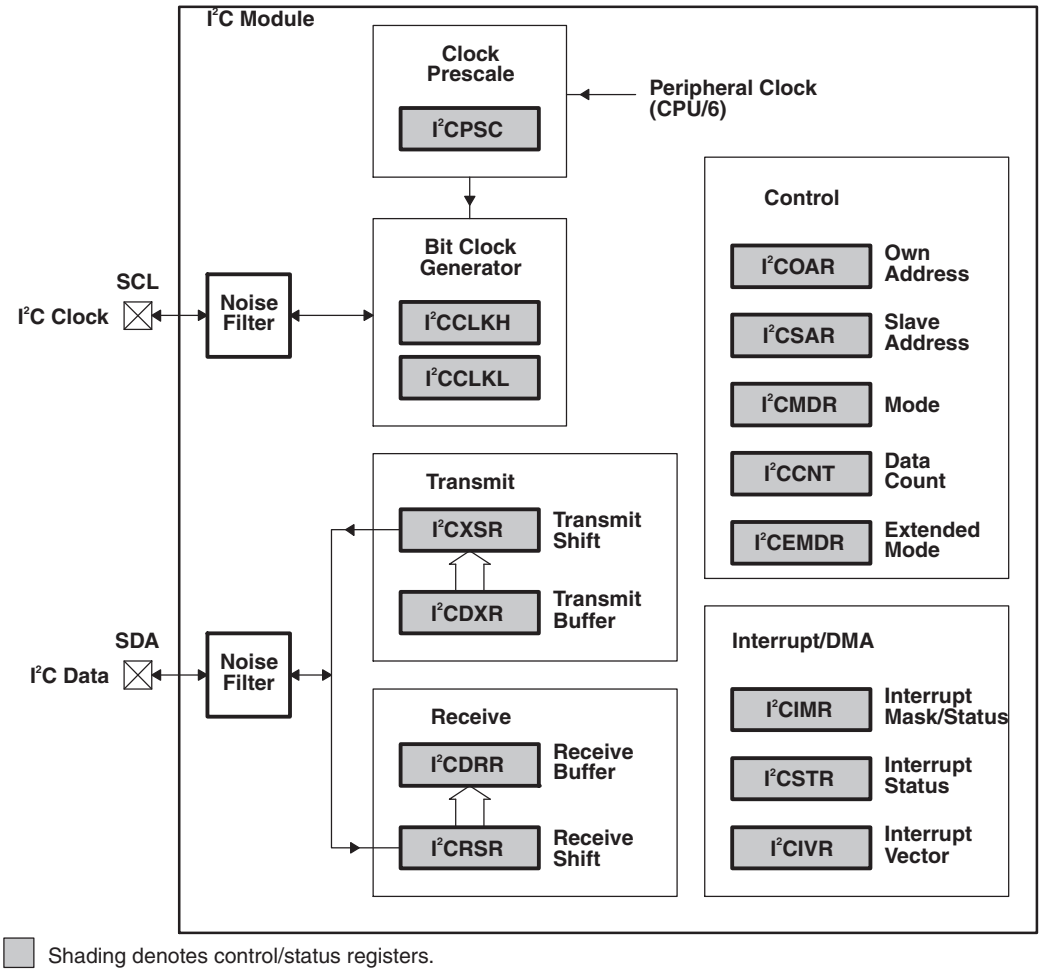
Figure 8-30 shows a block diagram of the I²C module.

Figure 8-30 I²C Module Block Diagram



8.10.2 I²C Peripheral Register Description

Table 8-36 I²C Registers (Part 1 of 2)

Hex Address Offsets	Acronym	Register Name
0x0000	ICOAR	I²C Own Address Register
0x0004	ICIMR	I²C Interrupt Mask/status Register
0x0008	ICSTR	I²C Interrupt Status Register
0x000C	ICCLKL	I²C Clock Low-time Divider Register
0x0010	ICCLKH	I²C Clock High-time Divider Register
0x0014	ICCNT	I²C Data Count Register
0x0018	ICDRR	I²C Data Receive Register
0x001C	ICSAR	I²C Slave Address Register
0x0020	ICDXR	I²C Data Transmit Register
0x0024	ICMDR	I²C Mode Register
0x0028	ICIVR	I²C Interrupt Vector Register
0x002C	ICEMDR	I²C Extended Mode Register
0x0030	ICPSC	I²C Prescaler Register

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Table 8-36 I²C Registers (Part 2 of 2)

Hex Address Offsets	Acronym	Register Name
0x0034	ICPID1	I²C Peripheral Identification Register 1 [value: 0x0000 0105]
0x0038	ICPID2	I²C Peripheral Identification Register 2 [value: 0x0000 0005]
0x003C -0x007F	-	Reserved
End of Table 8-36		

8.10.3 I²C Electrical Data/Timing

8.10.3.1 Inter-Integrated Circuits (I²C) Timing

Table 8-37 I²C Timing Requirements (1)
(see Figure 8-31)

No.			Standard Mode		Fast Mode		Units
			Min	Max	Min	Max	
1	$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
2	$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		µs
3	$t_{h(SDAL-SCLL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		µs
4	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
5	$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
6	$t_{su(SDAV-SCLH)}$	Setup time, SDA valid before SCL high	250		100 (2)		ns
7	$t_{h(SCLL-SDAV)}$	Hold time, SDA valid after SCL low (for I²C bus devices)	0 (3)	3.45	0 (3)	0.9 (4)	µs
8	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
9	$t_{r(SDA)}$	Rise time, SDA		1000	$20 + 0.1C_b$ (5)	300	ns
10	$t_{r(SCL)}$	Rise time, SCL		1000	$20 + 0.1C_b$ (5)	300	ns
11	$t_{f(SDA)}$	Fall time, SDA		300	$20 + 0.1C_b$ (5)	300	ns
12	$t_{f(SCL)}$	Fall time, SCL		300	$20 + 0.1C_b$ (5)	300	ns
13	$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		µs
14	$t_{w(SP)}$	Pulse duration, spike (must be suppressed)			0	50	ns
	C_b (5)	Capacitive load for each bus line		400		400	pF
End of Table 8-37							

1 The I²C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.

2 A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement tsu(SDA-SCLH) ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_r max + $t_{su(SDA-SCLH)}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-Bus Specification) before the SCL line is released.

3 A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

4 The maximum $t_{h(SDA-SCLL)}$ has to be met only if the device does not stretch the low period [$t_{w(SCLL)}$] of the SCL signal.

5 C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

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Figure 8-31 I²C Receive Timings

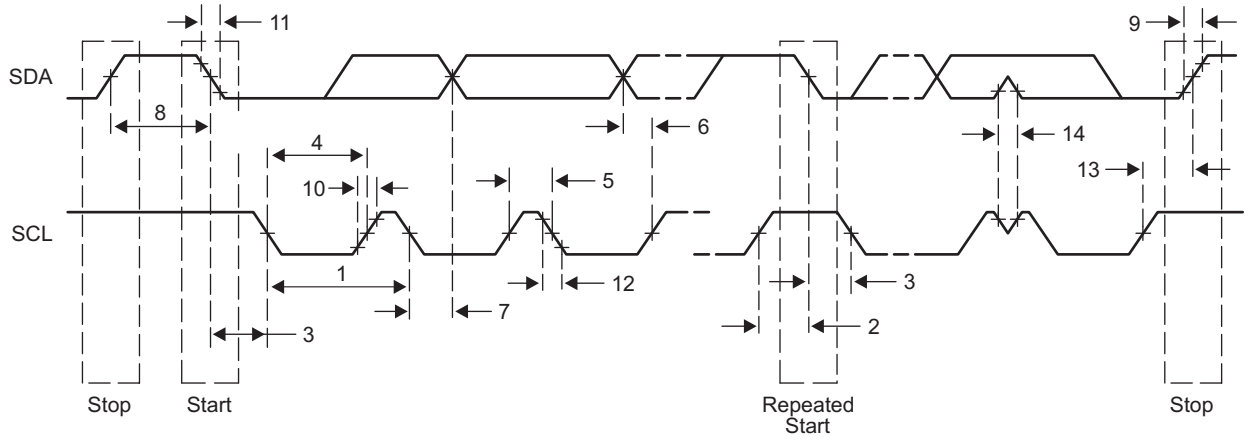

Table 8-38 I²C Switching Characteristics (1)
(see Figure 8-32)

No.	Parameter		Standard Mode Min	Standard Mode Max	Fast Mode Min	Fast Mode Max	Unit
16	$t_{c(SCL)}$	Cycle time, SCL	10		2.5		ms
17	$t_{su(SCLH-SDAL)}$	Setup time, SCL high to SDA low (for a repeated START condition)	4.7		0.6		ms
18	$t_{h(SDAL-SCLL)}$	Hold time, SDA low after SCL low (for a START and a repeated START condition)	4		0.6		ms
19	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		ms
20	$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		ms
21	$t_{d(SDAV-SDLH)}$	Delay time, SDA valid to SCL high	250		100		ns
22	$t_{v(SDLL-SDAV)}$	Valid time, SDA valid after SCL low (for I²C bus devices)	0		0	0.9	ms
23	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		ms
24	$t_{r(SDA)}$	Rise time, SDA		1000	$20 + 0.1C_b$ (1)	300	ns
25	$t_{r(SCL)}$	Rise time, SCL		1000	$20 + 0.1C_b$ (1)	300	ns
26	$t_{f(SDA)}$	Fall time, SDA		300	$20 + 0.1C_b$ (1)	300	ns
27	$t_{f(SCL)}$	Fall time, SCL		300	$20 + 0.1C_b$ (1)	300	ns
28	$t_{d(SCLH-SDAH)}$	Delay time, SCL high to SDA high (for STOP condition)	4		0.6		ms
	C_p	Capacitance for each I²C pin		10		10	pF

End of Table 8-38

1 C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

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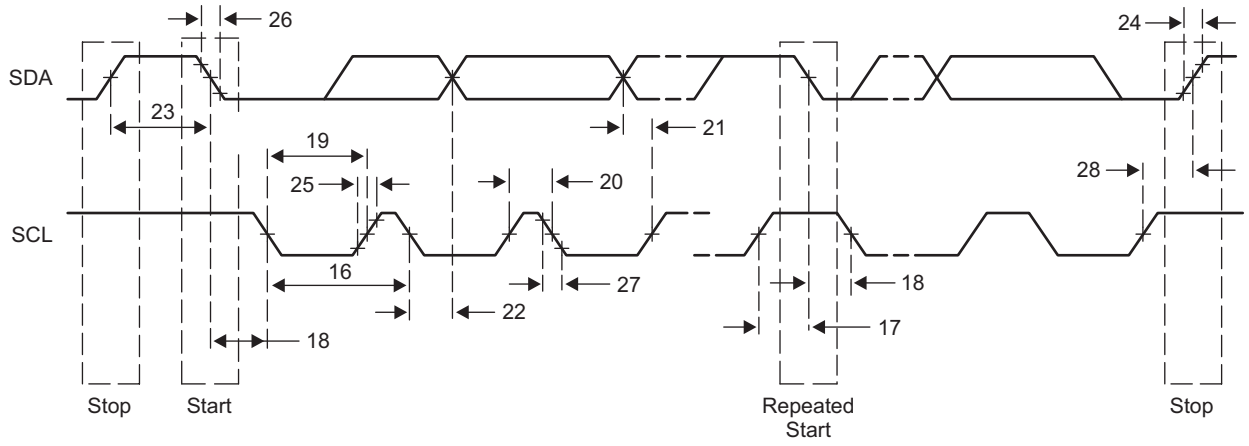
Figure 8-32 I²C Transmit Timings



8.11 SPI Peripheral

The Serial Peripheral Interconnect (SPI) module provides an interface between the DSP and other SPI-compliant devices. The primary intent of this interface is to allow for connection to an SPI ROM for boot. The SPI module on TCI6634K2K is supported only in master mode. Additional chip-level components can also be included, such as temperature sensors or an I/O expander.

8.11.1 SPI Electrical Data/Timing

Table 8-39 SPI Timing Requirements
See Figure 8-33)

No.			Min	Max	Unit
Master Mode Timing Diagrams — Base Timings for 3 Pin Mode					
7	tsu(SPIDIN-SPC)	Input setup time, SPIDIN valid before receive edge of SPICLK. Polarity = 0 Phase = 0	2		ns
7	tsu(SPIDIN-SPC)	Input setup time, SPIDIN valid before receive edge of SPICLK. Polarity = 0 Phase = 1	2		ns
7	tsu(SPIDIN-SPC)	Input setup time, SPIDIN valid before receive edge of SPICLK. Polarity = 1 Phase = 0	2		ns
7	tsu(SPIDIN-SPC)	Input setup time, SPIDIN valid before receive edge of SPICLK. Polarity = 1 Phase = 1	2		ns
8	th(SPC-SPIDIN)	Input hold time, SPIDIN valid after receive edge of SPICLK. Polarity = 0 Phase = 0	5		ns
8	th(SPC-SPIDIN)	Input hold time, SPIDIN valid after receive edge of SPICLK. Polarity = 0 Phase = 1	5		ns
8	th(SPC-SPIDIN)	Input hold time, SPIDIN valid after receive edge of SPICLK. Polarity = 1 Phase = 0	5		ns
8	th(SPC-SPIDIN)	Input hold time, SPIDIN valid after receive edge of SPICLK. Polarity = 1 Phase = 1	5		ns
End of Table 8-39					

Table 8-40 SPI Switching Characteristics (Part 1 of 2)
(See Figure 8-33 and Figure 8-34)

No.	Parameter		Min	Max	Unit
Master Mode Timing Diagrams — Base Timings for 3 Pin Mode					
1	tc(SPC)	Cycle time, SPICLK, all master modes	3*P2 (1)		ns
2	tw(SPCH)	Pulse width high, SPICLK, all master modes	0.5*(3*P2) - 1		ns
3	tw(SPCL)	Pulse width low, SPICLK, all master modes	0.5*(3*P2) - 1		ns
4	td(SPIDOUT-SPC)	Setup (Delay), initial data bit valid on SPIDOUT to initial edge on SPICLK. Polarity = 0, Phase = 0.		5	ns
4	td(SPIDOUT-SPC)	Setup (Delay), initial data bit valid on SPIDOUT to initial edge on SPICLK. Polarity = 0, Phase = 1.		5	ns
4	td(SPIDOUT-SPC)	Setup (Delay), initial data bit valid on SPIDOUT to initial edge on SPICLK Polarity = 1, Phase = 0		5	ns

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Table 8-40 SPI Switching Characteristics (Part 2 of 2)
(See Figure 8-33 and Figure 8-34)

No.	Parameter		Min	Max	Unit
4	td(SPIDOUT-SPC)	Setup (Delay), initial data bit valid on SPIDOUT to initial edge on SPICLK Polarity = 1, Phase = 1		5	ns
5	td(SPC-SPIDOUT)	Setup (Delay), subsequent data bits valid on SPIDOUT to initial edge on SPICLK. Polarity = 0 Phase = 0		2	ns
5	td(SPC-SPIDOUT)	Setup (Delay), subsequent data bits valid on SPIDOUT to initial edge on SPICLK Polarity = 0 Phase = 1		2	ns
5	td(SPC-SPIDOUT)	Setup (Delay), subsequent data bits valid on SPIDOUT to initial edge on SPICLK Polarity = 1 Phase = 0		2	ns
5	td(SPC-SPIDOUT)	Setup (Delay), subsequent data bits valid on SPIDOUT to initial edge on SPICLK Polarity = 1 Phase = 1		2	ns
6	toh(SPC-SPIDOUT)	Output hold time, SPIDOUT valid after receive edge of SPICLK except for final bit. Polarity = 0 Phase = 0	0.5*tc - 2		ns
6	toh(SPC-SPIDOUT)	Output hold time, SPIDOUT valid after receive edge of SPICLK except for final bit. Polarity = 0 Phase = 1	0.5*tc - 2		ns
6	toh(SPC-SPIDOUT)	Output hold time, SPIDOUT valid after receive edge of SPICLK except for final bit. Polarity = 1 Phase = 0	0.5*tc - 2		ns
6	toh(SPC-SPIDOUT)	Output hold time, SPIDOUT valid after receive edge of SPICLK except for final bit. Polarity = 1 Phase = 1	0.5*tc - 2		ns
Additional SPI Master Timings — 4 Pin Mode with Chip Select Option					
19	td(SCS-SPC)	Delay from SPISCSx\ active to first SPICLK. Polarity = 0 Phase = 0	2*P2 - 5	2*P2 + 5	ns
19	td(SCS-SPC)	Delay from SPISCSx\ active to first SPICLK. Polarity = 0 Phase = 1	0.5*tc + (2*P2) - 5	0.5*tc + (2*P2) + 5	ns
19	td(SCS-SPC)	Delay from SPISCSx\ active to first SPICLK. Polarity = 1 Phase = 0	2*P2 - 5	2*P2 + 5	ns
19	td(SCS-SPC)	Delay from SPISCSx\ active to first SPICLK. Polarity = 1 Phase = 1	0.5*tc + (2*P2) - 5	0.5*tc + (2*P2) + 5	ns
20	td(SPC-SCS)	Delay from final SPICLK edge to master deasserting SPISCSx\. Polarity = 0 Phase = 0	1*P2 - 5	1*P2 + 5	ns
20	td(SPC-SCS)	Delay from final SPICLK edge to master deasserting SPISCSx\. Polarity = 0 Phase = 1	0.5*tc + (1*P2) - 5	0.5*tc + (1*P2) + 5	ns
20	td(SPC-SCS)	Delay from final SPICLK edge to master deasserting SPISCSx\. Polarity = 1 Phase = 0	1*P2 - 5	1*P2 + 5	ns
20	td(SPC-SCS)	Delay from final SPICLK edge to master deasserting SPISCSx\. Polarity = 1 Phase = 1	0.5*tc + (1*P2) - 5	0.5*tc + (1*P2) + 5	ns
	tw(SCSH)	Minimum inactive time on SPISCSx\ pin between two transfers when SPISCSx\ is not held using the CSHOLD feature.	2*P2 - 5		ns
End of Table 8-40					

1 P2=1/(SYSCLK1/6)

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Figure 8-33 SPI Master Mode Timing Diagrams — Base Timings for 3-Pin Mode

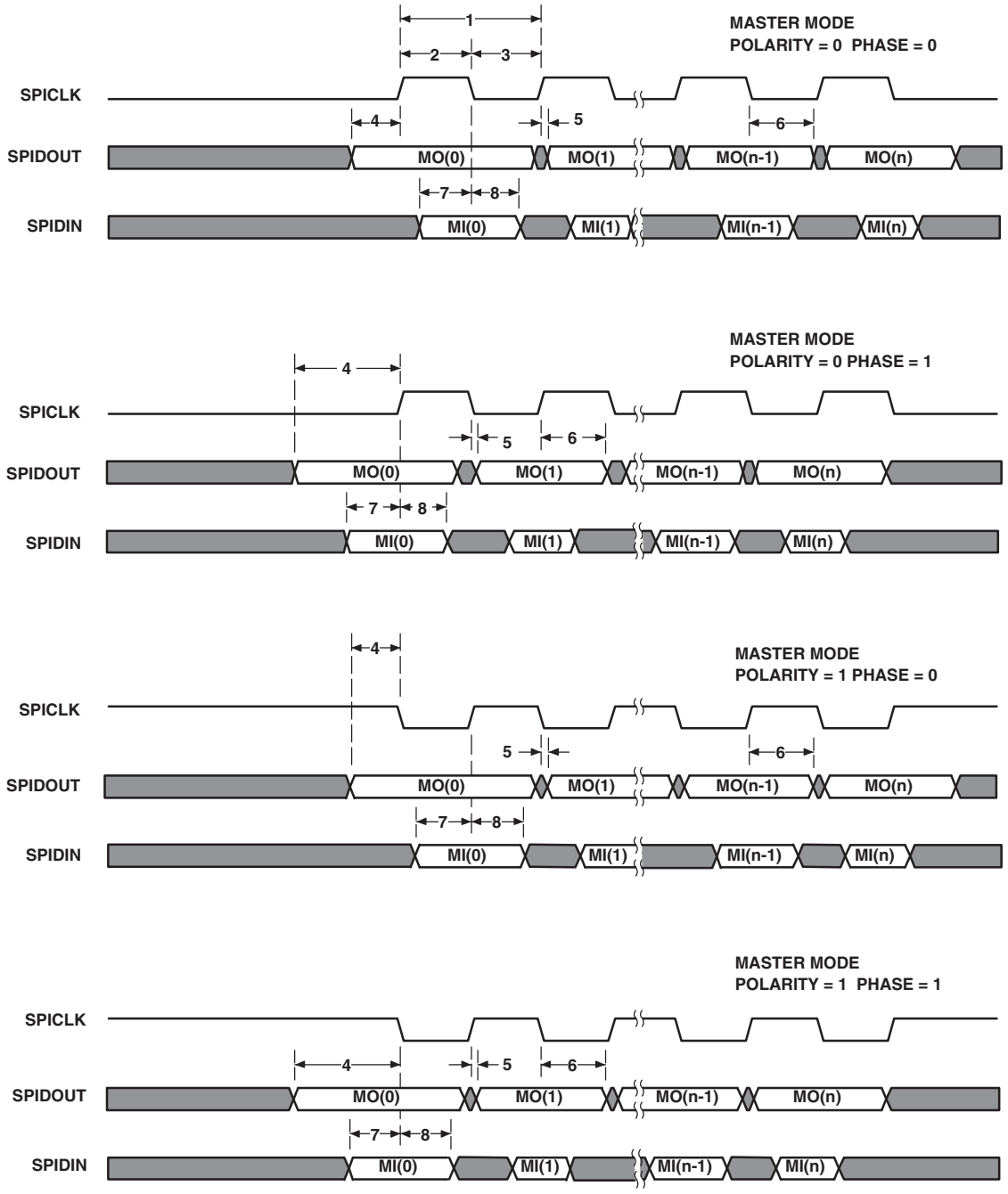
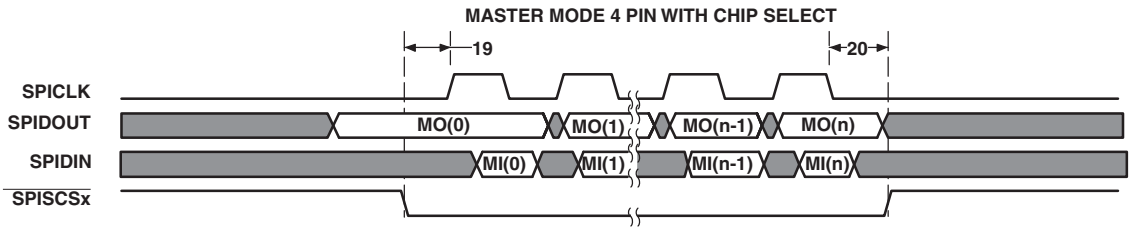


Figure 8-34 SPI Additional Timings for 4-Pin Master Mode with Chip Select Option



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8.12 HyperLink Peripheral

The TCI6634K2K includes HyperLinks for companion device interfaces. This is a four-lane SerDes interface designed to operate at up to 10 Gbps per lane from pin-to-pin. The interface is used to connect with external accelerators that are manufactured using TI libraries. The HyperLink lines must be connected with DC coupling.

The interface includes the serial station management interfaces used to send power management and flow messages between devices. Each HyperLink interface consists of four LVCMOS inputs and four LVCMOS outputs configured as two 2-wire input buses and two 2-wire output buses. Each 2-wire bus includes a data signal and a clock signal.

Table 8-41 HyperLink Peripheral Timing Requirements
(see Figure 8-35, Figure 8-36 and Figure 8-37)

No.			Min	Max	Unit
FL Interface					
1	tc(HYPTXFLCLK)	Clock period - HYPTXFLCLK (C1)	5.75		ns
2	tw(HYPTXFLCLKH)	High pulse width - HYPTXFLCLK	0.4*C1	0.6*C1	ns
3	tw(HYPTXFLCLKL)	Low pulse width - HYPTXFLCLK	0.4*C1	0.6*C1	ns
6	tsu(HYPTXFLDAT-HYPTXFLCLKH)	Setup time - HYPTXFLDAT valid before HYPTXFLCLK high	1		ns
7	th(HYPTXFLCLKH-HYPTXFLDAT)	Hold time - HYPTXFLDAT valid after HYPTXFLCLK high	1		ns
6	tsu(HYPTXFLDAT-HYPTXFLCLKL)	Setup time - HYPTXFLDAT valid before HYPTXFLCLK low	1		ns
7	th(HYPTXFLCLKL-HYPTXFLDAT)	Hold time - HYPTXFLDAT valid after HYPTXFLCLK low	1		ns
PM Interface					
1	tc(HYPRXPMCLK)	Clock period - HYPRXPMCLK (C3)	5.75		ns
2	tw(HYPRXPMCLK)	High pulse width - HYPRXPMCLK	0.4*C3	0.6*C3	ns
3	tw(HYPRXPMCLK)	Low pulse width - HYPRXPMCLK	0.4*C3	0.6*C3	ns
6	tsu(HYPRXPMDAT-HYPRXPMCLKH)	Setup time - HYPRXPMDAT valid before HYPRXPMCLK high	1		ns
7	th(HYPRXPMCLKH-HYPRXPMDAT)	Hold time - HYPRXPMDAT valid after HYPRXPMCLK high	1		ns
6	tsu(HYPRXPMDAT-HYPRXPMCLKL)	Setup time - HYPRXPMDAT valid before HYPRXPMCLK low	1		ns
7	th(HYPRXPMCLKL-HYPRXPMDAT)	Hold time - HYPRXPMDAT valid after HYPRXPMCLK low	1		ns
End of Table 8-41					

Table 8-42 HyperLink Peripheral Switching Characteristics (Part 1 of 2)
(see Figure 8-35, Figure 8-36 and Figure 8-37)

No.	Parameter		Min	Max	Unit
FL Interface					
1	tc(HYPRXFLCLK)	Clock period - HYPRXFLCLK (C2)	6.4		ns
2	tw(HYPRXFLCLKH)	High pulse width - HYPRXFLCLK	0.4*C2	0.6*C2	ns
3	tw(HYPRXFLCLKL)	Low pulse width - HYPRXFLCLK	0.4*C2	0.6*C2	ns
4	tosu(HYPRXFLDAT-HYPRXFLCLKH)	Setup time - HYPRXFLDAT valid before HYPRXFLCLK high	0.25*C2-0.4		ns
5	toh(HYPRXFLCLKH-HYPRXFLDAT)	Hold time - HYPRXFLDAT valid after HYPRXFLCLK high	0.25*C2-0.4		ns
4	tosu(HYPRXFLDAT-HYPRXFLCLKL)	Setup time - HYPRXFLDAT valid before HYPRXFLCLK low	0.25*C2-0.4		ns
5	toh(HYPRXFLCLKL-HYPRXFLDAT)	Hold time - HYPRXFLDAT valid after HYPRXFLCLK low	0.25*C2-0.4		ns
PM Interface					
1	tc(HYPTXPMCLK)	Clock period - HYPTXPMCLK (C4)	6.4		ns
2	tw(HYPTXPMCLK)	High pulse width - HYPTXPMCLK	0.4*C4	0.6*C4	ns
3	tw(HYPTXPMCLK)	Low pulse width - HYPTXPMCLK	0.4*C4	0.6*C4	ns
4	tosu(HYPTXPMDAT-HYPTXPMCLKH)	Setup time - HYPTXPMDAT valid before HYPTXPMCLK high	0.25*C2-0.4		ns
5	toh(HYPTXPMCLKH-HYPTXPMDAT)	Hold time - HYPTXPMDAT valid after HYPTXPMCLK high	0.25*C2-0.4		ns

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Table 8-42 HyperLink Peripheral Switching Characteristics (Part 2 of 2)
(see Figure 8-35, Figure 8-36 and Figure 8-37)

No.	Parameter		Min	Max	Unit
4	tosu(HYPTXPMDAT-HYPTXPMCLKL)	Setup time - HYPTXPMDAT valid before HYPTXPMCLK low	0.25*C2-0.4		ns
5	toh(HYPTXPMCLKL-HYPTXPMDAT)	Hold time - HYPTXPMDAT valid after HYPTXPMCLK low	0.25*C2-0.4		ns
End of Table 8-42					

Figure 8-35 HyperLink Station Management Clock Timing

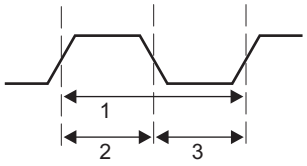
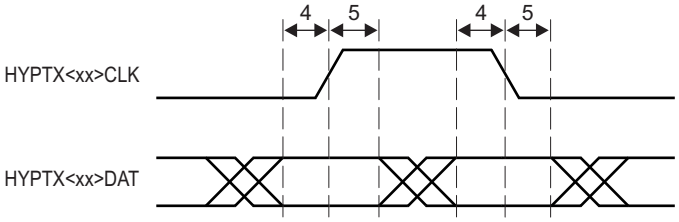
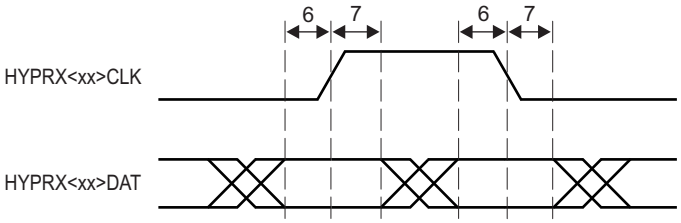


Figure 8-36 HyperLink Station Management Transmit Timing



<xx> represents the interface that is being used: PM or FL

Figure 8-37 HyperLink Station Management Receive Timing



<xx> represents the interface that is being used: PM or FL

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8.13 UART Peripheral

The universal asynchronous receiver/transmitter (UART) module provides an interface between the device and a UART terminal interface or other UART-based peripheral. The UART is based on the industry standard TL16C550 asynchronous communications element which, in turn, is a functional upgrade of the TL16C450. Functionally similar to the TL16C450 on power up (single character or TL16C450 mode), the UART can be placed in an alternate FIFO (TL16C550) mode. This relieves the C66x of excessive software overhead by buffering received and transmitted characters. The receiver and transmitter FIFOs store up to 16 bytes including three additional bits of error status per byte for the receiver FIFO.

The UART performs serial-to-parallel conversions on data received from a peripheral device and parallel-to-serial conversion on data received from the C66x CorePac to be sent to the peripheral device. The C66x CorePac can read the UART status at any time. The UART includes control capability and a processor interrupt system that can be tailored to minimize software management of the communications link. For more information on UART, see the *Universal Asynchronous Receiver/Transmitter (UART) for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

Table 8-43 UART Timing Requirements
(see Figure 8-38 and Figure 8-39)

No.			Min	Max	Unit
Receive Timing					
4	tw(RXSTART)	Pulse width, receive start bit	0.96U [1]	1.05U	ns
5	tw(RXH)	Pulse width, receive data/parity bit high	0.96U	1.05U	ns
5	tw(RXL)	Pulse width, receive data/parity bit low	0.96U	1.05U	ns
6	tw(RXSTOP1)	Pulse width, receive stop bit 1	0.96U	1.05U	ns
6	tw(RXSTOP15)	Pulse width, receive stop bit 1.5	0.96U	1.05U	ns
6	tw(RXSTOP2)	Pulse width, receive stop bit 2	0.96U	1.05U	ns
Autoflow Timing Requirements					
8	td(CTSL-TX)	Delay time, CTS asserted to START bit transmit	P [2]	5P	ns
End of Table 8-43					

1 U = UART baud time = 1/programmed baud rate
2 P = 1/(SYSCLK1/6)

Figure 8-38 UART Receive Timing Waveform

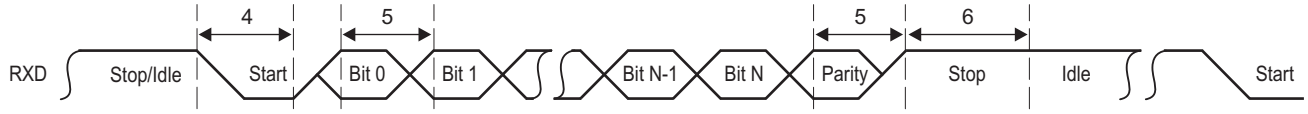

Figure 8-39 UART CTS (Clear-to-Send Input) — Autoflow Timing Waveform

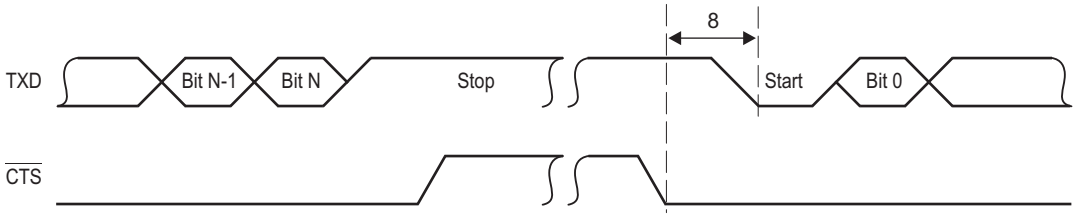

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Table 8-44 UART Switching Characteristics
(See Figure 8-40 and Figure 8-41)

No.	Parameter		Min	Max	Unit
Transmit Timing					
1	tw(TXSTART)	Pulse width, transmit start bit	U (1) - 2	U + 2	ns
2	tw(TXH)	Pulse width, transmit data/parity bit high	U - 2	U + 2	ns
2	tw(TXL)	Pulse width, transmit data/parity bit low	U - 2	U + 2	ns
3	tw(TXSTOP1)	Pulse width, transmit stop bit 1	U - 2	U + 2	ns
3	tw(TXSTOP15)	Pulse width, transmit stop bit 1.5	1.5 * (U - 2)	1.5 * ('U + 2)	ns
3	tw(TXSTOP2)	Pulse width, transmit stop bit 2	2 * (U - 2)	2 * ('U + 2)	ns
Autoflow Timing Requirements					
7	td(RX-RTSH)	Delay time, STOP bit received to RTS deasserted	P (2)	5P	ns
End of Table 8-44					

1 U = UART baud time = 1/programmed baud rate
2 P = 1/(SYSCLK1/6)

Figure 8-40 UART Transmit Timing Waveform

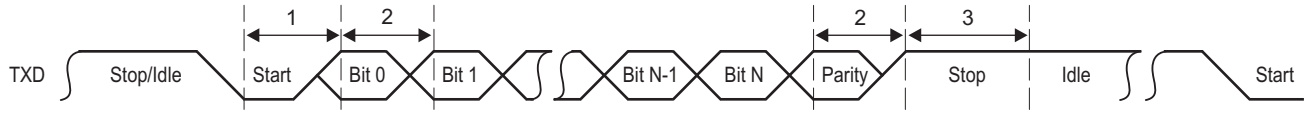
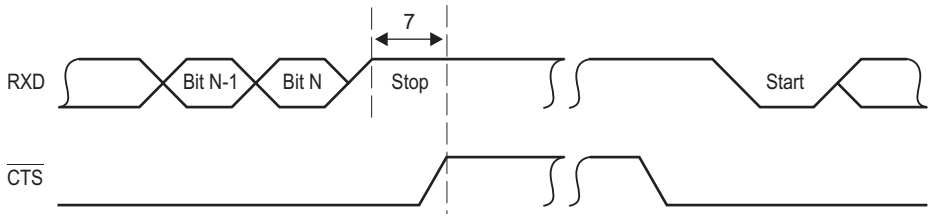


Figure 8-41 UART RTS (Request-to-Send Output) – Autoflow Timing Waveform



8.14 PCIe Peripheral

The two-lane PCI express (PCIe) module on TCI6634K2K provides an interface between the device and other PCIe-compliant devices. The PCIe module provides low pin-count, high-reliability, and high-speed data transfer at rates up to 5.0 Gbps per lane on the serial links. For more information, see the *Peripheral Component Interconnect Express (PCIe) for KeyStone Devices User Guide* in .

8.15 Packet Accelerator

The Packet Accelerator (PA) provides L2 to L4 classification functionalities and supports classification for Ethernet, VLAN, MPLS over Ethernet, IPv4/6, GRE over IP, and other session identification over IP such as TCP and UDP ports. It maintains 8k multiple-in, multiple-out hardware queues and also provides checksum capability as well as some QoS capabilities. The PA enables a single IP address to be used for a multicore device and can process up to 1.5 Mpps. The Packet Accelerator is coupled with the Network Coprocessor. For more information, see the *Packet Accelerator (PA) for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

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8.16 Security Accelerator

The Security Accelerator (SA) provides wire-speed processing on 1 Gbps Ethernet traffic on IPSec, SRTP, and 3GPP Air interface security protocols. It functions on the packet level with the packet and the associated security context being one of the above three types. The Security Accelerator is coupled with the Network Coprocessor, and receives the packet descriptor containing the security context in the buffer descriptor and the data to be encrypted/decrypted in the linked buffer descriptor. For more information, see the Security Accelerator (SA) *for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

8.17 Network Coprocessor Gigabit Ethernet (GbE) Switch Subsystem

The gigabit Ethernet (GbE) switch subsystem provides an efficient interface between the device and the networked community. The Ethernet Media Access Controller (EMAC) supports 10Base-T (10 Mbits/second), and 100BaseTX (100 Mbps), in half- or full-duplex mode, and 1000BaseT (1000 Mbps) in full-duplex mode, with hardware flow control and quality-of-service (QOS) support. The GbE switch subsystem is coupled with the Network Coprocessor. For more information, see the *Gigabit Ethernet (GbE) Switch Subsystem for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

An address range is assigned to the TCI6634K2K. Each individual device has a 48-bit MAC address and consumes only one unique MAC address out of the range. There are two registers to hold these values, MACID1[31:0] (32 bits) and MACID2[15:0] (16 bits) . The bits of these registers are defined as follows:

Figure 8-42 MACID1 Register (MMR Address 0x02620110)

31	0
MACID	
R,+xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx	

Legend: R = Read only; -x, value is indeterminate

Table 8-45 MACID1 Register Field Descriptions

Bit	Field	Description
31-0	MAC ID	MAC ID. Lower 32 bits.

Figure 8-43 MACID2 Register (MMR Address 0x02620114)

31 24	23 18	17	16	15 0
CRC	Reserved	FLOW	BCAST	MACID
R+,cccc cccc	R,+rr rrrr	R,+z	R,+y	R,+xxxx xxxx xxxx xxxx

Legend: R = Read only; -x, value is indeterminate

Table 8-46 MACID2 Register Field Descriptions (Part 1 of 2)

Bit	Field	Description
31-24	Reserved	Variable
23-18	Reserved	000000
17	FLOW	MAC Flow Control 0 = Off 1 = On

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Table 8-46 MACID2 Register Field Descriptions (Part 2 of 2)

Bit	Field	Description
16	BCAST	Default m/b-cast reception 0 = Broadcast 1 = Disabled
15-0	MAC ID	MAC ID. Upper 16 bits.
End of Table 8-46		

There is a central processor time synchronization (CPTS) submodule in the Ethernet switch module that can be used for time synchronization. Programming this register selects the clock source for the CPTS_RCLK. See the *Gigabit Ethernet (GbE) Switch Subsystem for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22for the register address and other details about the time synchronization submodule. The register CPTS_RFTCLK_SEL for reference clock selection of the time synchronization submodule is shown in Figure 8-44.

Figure 8-44 RFTCLK Select Register (CPTS_RFTCLK_SEL)

31	3	2	0
Reserved		CPTS_RFTCLK_SEL	
R - 0		RW - 0	

Legend: R = Read only; -x, value is indeterminate

Table 8-47 RFTCLK Select Register Field Descriptions

Bit	Field	Description
31-3	Reserved	Reserved. Read as 0.
2-0	CPTS_RFTCLK_SEL	Reference clock select. This signal is used to control an external multiplexer that selects one of 8 clocks for time sync reference (RFTCLK). This CPTS_RFTCLK_SEL value can be written only when the CPTS_EN bit is cleared to 0 in the TS_CTL register. 000 = SYSCLK2 001 = SYSCLK3 010 = TIMI0 011 = TIMI1 1xx = Reserved
End of Table 8-47		

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8.18 SGMII/XFI Management Data Input/Output (MDIO)

The management data input/output (MDIO) module implements the 802.3 serial management interface to interrogate and control up to 32 Ethernet PHY(s) connected to the device, using a shared two-wire bus. Application software uses the MDIO module to configure the auto-negotiation parameters of each PHY attached to the EMAC, retrieve the negotiation results, and configure required parameters in the gigabit Ethernet (GbE) and 10-gigabit Ethernet (10GbE) switch subsystems for correct operation. The module allows almost transparent operation of the MDIO interface, with very little attention from the C66x CorePac. For more information, see the *Gigabit Ethernet (GbE) Switch Subsystem for KeyStone Devices User Guide* and the 10-*Gigabit Ethernet (10GbE) Switch Subsystem for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

Table 8-48 MDIO Timing Requirements
(see Figure 8-45)

No.			Min	Max	Unit
1	tc(MDCLK)	Cycle time, MDCLK	400		ns
2	tw(MDCLKH)	Pulse duration, MDCLK high	180		ns
3	tw(MDCLKL)	Pulse duration, MDCLK low	180		ns
4	tsu(MDIO-MDCLKH)	Setup time, MDIO data input valid before MDCLK high	10		ns
5	th(MDCLKH-MDIO)	Hold time, MDIO data input valid after MDCLK high	10		ns
	tt(MDCLK)	Transition time, MDCLK		5	ns
End of Table 8-48					

Figure 8-45 MDIO Input Timing

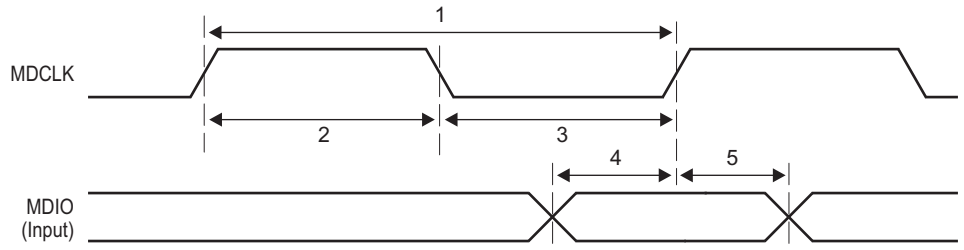
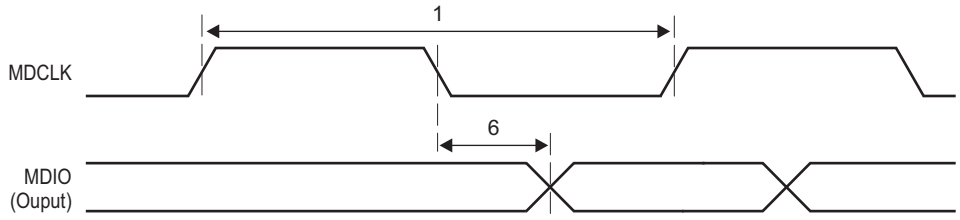


Table 8-49 MDIO Switching Characteristics
(see Figure 8-46)

No.	Parameter		Min	Max	Unit
6	td(MDCLKL-MDIO)	Delay time, MDCLK low to MDIO data output valid		100	ns
End of Table 8-49					

Figure 8-46 MDIO Output Timing



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8.19 Ten-Gigabit Ethernet (10GbE) Switch Subsystem

The 3-port Ten Gigabit Ethernet Switch Subsystem (different from the Network Coprocessor integrated switch) includes a standalone EMAC switch subsystem and a 2-lane SerDes macro. The 2-lane macro enables only 2 external ports. It does not include any packet acceleration or security acceleration engine.

8.19.1 10GbE Supported Features

The key features of the 10GbE module are listed below:

- 10 Gbps EMAC switch subsystem
  - MDIO: Media-dependent input/output module
  - SGMII Interface for 10/100/1000 and 10GBASE-KR for 10G
  - Ethernet switch with wire-rate switching (only two external ports are supported by the SerDes)
  - CPTS module that supports time-stamping for IEEE1588v2 with support for eight hardware push events and generation of compare output pulses
  - Supports XFI electrical interface
- CPDMA

The CPDMA component provides CPPI 4.2 compatible functionality, and provides a 128-bit wide data path to the TeraNet, enabling:

- Support for 8 transmit channel and 16 receive channels
- Support for reset isolation option

For more information, see the Ten *Gigabit Ethernet (10GbE) Switch Subsystem for KeyStone Devices User Guide* (in development).

8.20 Timers

The timers can be used to time events, count events, generate pulses, interrupt the CorePacs, and send synchronization events to the EDMA3 channel controller.

8.20.1 Timers Device-Specific Information

The TCI6634K2K device has twenty 64-bit timers in total, of which Timer0 through Timer7 are dedicated to each of the up to eight C66x CorePacs as watchdog timers and can also be used as general-purpose timers. The remaining timers can be configured as general-purpose timers only, with each timer programmed as a 64-bit timer or as two separate 32-bit timers.

When operating in 64-bit mode, the timer counts either module clock cycles or input (TINPLx) pulses (rising edge) and generates an output pulse/waveform (TOUTLx) plus an internal event (TINTLx) on a software-programmable period. When operating in 32-bit mode, the timer is split into two independent 32-bit timers. Each timer is made up of two 32-bit counters: a high counter and a low counter. The timer pins, TINPLx and TOUTLx are connected to the low counter. The timer pins, TINPHx and TOUTHx are connected to the high counter.

When operating in watchdog mode, the timer counts down to 0 and generates an event. It is a requirement that software writes to the timer before the count expires, after which the count begins again. If the count ever reaches 0, the timer event output is asserted. Reset initiated by a watchdog timer can be set by programming "Reset Type Status Register (RSTYPE)" on page 243 and the type of reset initiated can set by programming "Reset Configuration Register (RSTCFG)" on page 244. For more information, see the *64-bit Timer (Timer 64) for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

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8.20.2 Timers Electrical Timing

The tables and figures below describe the timing requirements and switching characteristics of the timers.

Table 8-50 Timer Input Timing Requirements (1)
(see Figure 8-47)

No.			Min	Max	Unit
1	$t_{w(TINPH)}$	Pulse duration, high	12C		ns
2	$t_{w(TINPL)}$	Pulse duration, low	12C		ns
End of Table 8-50					

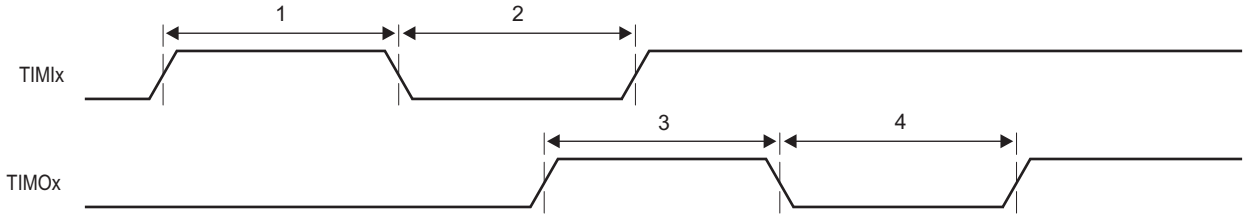
1 C = 1/(SYSCLK1/6) clock frequency in ns

Table 8-51 Timer Output Switching Characteristics (1)
(see Figure 8-47)

No.	Parameter		Min	Max	Unit
3	$t_{w(TOUTH)}$	Pulse duration, high	12C - 3		ns
4	$t_{w(TOUTL)}$	Pulse duration, low	12C - 3		ns
End of Table 8-51					

1 C = 1/(SYSCLK1/6) clock frequency in ns.

Figure 8-47 Timer Timing



8.21 Rake Search Accelerator (RSA)

There are sixteen Rake Search Accelerators (RSAs) on the device. Each C66x CorePac has one set of directly-connected RSA pairs. The RSA is an extension of the C66x CorePac. The C66x CorePac performs send/receive to the RSAs via the .L and .S functional units.

8.22 Enhanced Viterbi-Decoder Coprocessor (VCP2)

The device has eight high-performance embedded Viterbi Decoder Coprocessors (VCP2) that improve channel-decoding operations on-chip. Operating at SYSCLK1 clock divided by 3, each VCP2 can decode more than 762 12.2-Kbps 3G adaptive multi-rate (AMR) [K = 9, R = 1/3] voice channels when running at 333 MHz. The VCP2 supports constraint lengths K = 5, 6, 7, 8, and 9, rates R = 3/4, 1/2, 1/3, 1/4, and 1/5, and flexible polynomials, while generating hard decisions or soft decisions. Communications between the VCP2 and the C66x CorePac are carried out through the EDMA3 controller. The VCP2 supports:

- Unlimited frame sizes
- Code rates 3/4, 1/2, 1/3, 1/4, and 1/5
- Constraint lengths 5, 6, 7, 8, and 9
- Programmable encoder polynomials
- Programmable reliability and convergence lengths
- Hard and soft decoded decisions
- Tail and convergent modes
- Yamamoto logic
- Tail biting logic

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- Various input and output FIFO lengths

For more information, see the *Viterbi Coprocessor (VCP2) for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

8.23 Turbo Decoder Coprocessor (TCP3d)

The TCI6634K2K has four high-performance embedded Turbo-Decoder Coprocessors (TCP3d) that speed up channel-decoding operations on-chip for WCDMA, HSPA, HSPA+, TD-SCDMA, LTE, and WiMAX. Operating at SYSCLK1 divided by 2 or 3, the TCP3d processes data channels at a throughput of > 100 Mbps. For more information, see the *Turbo Decoder Coprocessor 3 (TCP3d) for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

8.24 Turbo Encoder Coprocessor (TCP3e)

The TCI6634K2K has a high-performance Turbo-Encoder Coprocessor (TCP3e) (embedded in the BCP) that speeds up channel-encoding operations on-chip for WCDMA, HSPA, HSPA+, TD-SCDMA, LTE, and WiMAX. Operating at SYSCLK1 divided by 3, the TCP3e is capable of processing data channels at a throughput of > 200 Mbps. For more information, see the *Turbo Encoder Coprocessor 3 (TCP3e) for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

8.25 Bit Rate Coprocessor (BCP)

The BCP is a hardware accelerator for wireless infrastructure and performs most of the uplink and downlink layer 1 bit processing for 3G and 4G wireless standards. BCP supports LTE, LTE-A, FDD WCDMA, TD-SCDMA, and WiMAX 802.16-2009 standards. It supports various downlink processing blocks like CRC attachment, turbo encoding, rate matching, code block concatenation, scrambling, and modulation. BCP supports various uplink processing blocks like soft slicer, de-scrambler, de-concatenation, rate de-matching, and LLR combining. For more information, see the *Bit Coprocessor (BCP) for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

8.26 Serial RapidIO (SRIO) Port

The SRIO port on the device is a high-performance, low pin-count SerDes interconnect. SRIO interconnects in a baseband board design provide connectivity and control among the components. The device supports four 1× Serial RapidIO links or one 4× Serial RapidIO link. The SRIO interface is designed to operate at a data rate of up to 5 Gbps per differential pair. This equals 20 raw GBaud/s for the 4× SRIO port, or approximately 15 Gbps data throughput rate.

The PHY part of the SRIO consists of the physical layer and includes the input and output buffers (each serial link consists of a differential pair), the 8-bit/10-bit encoder/decoder, the PLL clock recovery, and the parallel-to-serial/serial-to-parallel converters.

For more information, see the *Serial RapidIO (SRIO) for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

8.26.1 Serial RapidIO Device-Specific Information

The approach to specifying interface timing for the SRIO Port is different from other interfaces. For these other interfaces, the device timing was specified in terms of data manual specifications and I/O buffer information specification (IBIS) models.

The Serial RapidIO peripheral is a master peripheral in the device. It conforms to the *RapidIO™ Interconnect Specification, Part VI: Physical Layer 1×/4× LP-Serial Specification*, Revision 1.3.

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For the SRIO port, Texas Instruments provides a PCB solution showing two TI SRIO-enabled DSPs connected together via a 4× SRIO link. TI has performed the simulation and system characterization to ensure all SRIO interface timings in this solution are met. The complete SRIO system solution is documented in the *TMS320TCI6484 and TMS320C6457 SerDes Implementation Guidelines* application report (literature number SPRAAY1).

Note—TI supports ***only*** designs that follow the board design guidelines outlined in the application report.

8.27 General-Purpose Input/Output (GPIO)

8.27.1 GPIO Device-Specific Information

The GPIO peripheral pins are used for general purpose input/output for the device. These pins are also used to configure the device at boot time.

For more detailed information on device/peripheral configuration and the TCI6634 device pin muxing, see "Device Configuration" on page 185.

8.27.2 GPIO Peripheral Register Description

Table 8-52 GPIO Registers

Hex Address Offsets	Acronym	Register Name
0x0008	BINTEN	GPIO interrupt per bank enable register
0x000C	-	Reserved
0x0010	DIR	GPIO Direction Register
0x0014	OUT_DATA	GPIO Output Data Register
0x0018	SET_DATA	GPIO Set Data Register
0x001C	CLR_DATA	GPIO Clear Data Register
0x0020	IN_DATA	GPIO Input Data Register
0x0024	SET_RIS_TRIG	GPIO Set Rising Edge Interrupt Register
0x0028	CLR_RIS_TRIG	GPIO Clear Rising Edge Interrupt Register
0x002C	SET_FAL_TRIG	GPIO Set Falling Edge Interrupt Register
0x0030	CLR_FAL_TRIG	GPIO Clear Falling Edge Interrupt Register
0x008C	-	Reserved
0x0090 - 0x03FF	-	Reserved
End of Table 8-52		

8.27.3 GPIO Electrical Data/Timing

Table 8-53 GPIO Input Timing Requirements (1)
(see Figure 8-48)

No.			Min	Max	Unit
1	$t_{w(GPOH)}$	Pulse duration, GPOx high	12C		ns
2	$t_{w(GPOL)}$	Pulse duration, GPOx low	12C		ns
End of Table 8-53					

1 C = 1/SYSCLK1 clock frequency in ns

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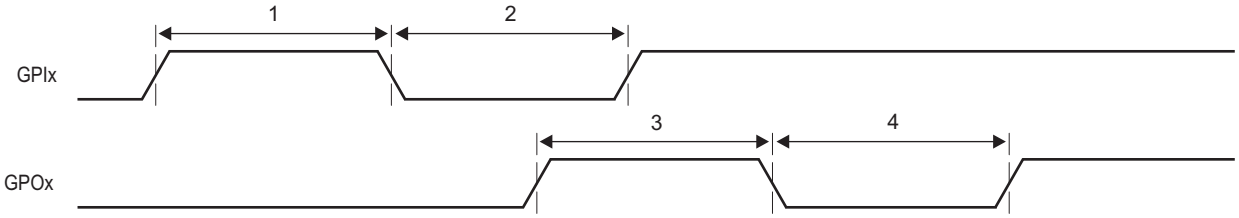
Table 8-54 GPIO Output Switching Characteristics (1)
(see Figure 8-48)

No.	Parameter		Min	Max	Unit
3	$t_{w(GPOH)}$	Pulse duration, GPOx high	36C - 8		ns
4	$t_{w(GPOL)}$	Pulse duration, GPOx low	36C - 8		ns
End of Table 8-54					

1 C = 1/(SYSCLK1/6) clock frequency in ns

Figure 8-48 GPIO Timing



8.28 Semaphore2

The device contains an enhanced Semaphore module for the management of shared resources of the C66x CorePacs. The Semaphore enforces atomic accesses to shared chip-level resources so that the read-modify-write sequence is not broken. The Semaphore module has unique interrupts to each of the C66x CorePacs to identify when that CorePac has acquired the resource.

Semaphore resources within the module are not tied to specific hardware resources. It is a software requirement to allocate semaphore resources to the hardware resource(s) to be arbitrated.

The Semaphore module supports three masters and contains 32 semaphores that can be shared within the system.

There are two methods of accessing a semaphore resource:

- **Direct Access:** A C66x CorePac directly accesses a semaphore resource. If free, the semaphore is granted. If not free, the semaphore is not granted.
- **Indirect Access:** A C66x CorePac indirectly accesses a semaphore resource by writing to it. Once the resource is free, an interrupt notifies the C66x CorePac that the resource is available.

8.29 Antenna Interface Subsystem 2 (AIF2)

The AIF2 transfers data between the external RF units and the C66x CorePacs, RAC, TAC, and the FFTC modules via the TeraNet. The external AIF2 interface connects the AIF2 with either RF units and/or other baseband OBSAI/CPRI devices. The AIF2 has 11 timer synchronization events from the AIF2 Timer (AT) module:

- Timer synchronization events 0-3 are routed as primary events to the EDMA3CC1 and also as secondary events to the C66x CorePacs via CIC2.
- Timer synchronization events 3-7 are routed as primary events to the EDMA3CC2.
- Timer synchronization events 8, 9, and 10 are hard-wired to TAC, RAC_0, and RAC_1 respectively.

Table 8-55 AIF2 Timer Module Timing Requirements (Part 1 of 2)
See Figure 8-47, Figure 8-50, Figure 8-51, and Figure 8-52

No.			Min	Max	Unit
RP1 Clock and Frameburst					
1	tc(RP1CLKN)	Cycle time, RP1CLK(N)	32.55	32.55	ns
1	tc(RP1CLKP)	Cycle time, RP1CLK(P)	32.55	32.55	ns

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Table 8-55 AIF2 Timer Module Timing Requirements (Part 2 of 2)
See Figure 8-47, Figure 8-50, Figure 8-51, and Figure 8-52

No.			Min	Max	Unit
2	tw(RP1CLKNL)	Pulse duration, RP1CLK(N) low	0.4 * C1 (1)	0.6 * C1	ns
3	tw(RP1CLKNH)	Pulse duration, RP1CLK(N) high	0.4 * C1	0.6 * C1	ns
3	tw(RP1CLKPL)	Pulse duration, RP1CLK(P) low	0.4 * C1	0.6 * C1	ns
2	tw(RP1CLKPH)	Pulse duration, RP1CLK(P) high	0.4 * C1	0.6 * C1	ns
4	tr(RP1CLKN)	Rise time - RP1CLKN 10% to 90%		350.00	ps
4	tf(RP1CLKN)	Fall time - RP1CLKN 90% to 10%		350.00	ps
4	tr(RP1CLKP)	Rise time - RP1CLKP 10% to 90%		350.00	ps
4	tf(RP1CLKP)	Fall time - RP1CLKP 90% to 10%		350.00	ps
5	tj(RP1CLKN)	Period jitter (peak-to-peak), RP1CLK(N)		600	ps
5	tj(RP1CLKP)	Period jitter (peak-to-peak), RP1CLK(P)		600	ps
6	tw(RP1FBN)	Bit period, RP1FB(N)	8 * C1	8 * C1	ns
6	tw(RP1FBP)	Bit period, RP1FB(P)	8 * C1	8 * C1	ns
7	tr(RP1CLKN)	Rise time - RP1FBN 10% to 90%		350.00	ps
7	tf(RP1CLKN)	Fall time - RP1FBN 90% to 10%		350.00	ps
7	tr(RP1CLKP)	Rise time - RP1FBP 10% to 90%		350.00	ps
7	tf(RP1CLKP)	Fall time - RP1FBP 90% to 10%		350.00	ps
8	tsu(RP1FBN-RP1CLKP)	Setup time - RP1FBN valid before RP1CLKP high	2		ns
8	tsu(RP1FBN-RP1CLKN)	Setup time - RP1FBN valid before RP1CLKN low	2		ns
8	tsu(RP1FBN-RP1CLKP)	Setup time - RP1FBP valid before RP1CLKP high	2		ns
8	tsu(RP1FBN-RP1CLKN)	Setup time - RP1FBP valid before RP1CLKN low	2		ns
9	th(RP1FBN-RP1CLKP)	Hold time - RP1FBN valid after RP1CLKP high	2		ns
9	th(RP1FBN-RP1CLKN)	Hold time - RP1FBN valid after RP1CLKN low	2		ns
9	th(RP1FBN-RP1CLKP)	Hold time - RP1FBP valid after RP1CLKP high	2		ns
9	th(RP1FBN-RP1CLKN)	Hold time - RP1FBP valid after RP1CLKN low	2		ns
PHY Sync and Radio Sync Pulses					
10	tw(PHYSYNCH)	Pulse duration, PHYSYNC high	6.50		ns
11	tc(PHYSYNC)	Cycle time, PHYSYNC pulse to PHYSYNC pulse	10.00		ms
12	tw(RADSYNCH)	Pulse duration, RADSYNC high	6.50		ns
13	tc(RADSYNC)	Cycle time, RADSYNC pulse to RADSYNC pulse	1.00		ms
End of Table 8-55					

1 C1 = tc(RP1CLKN/P)

Figure 8-49 AIF2 RP1 Frame Synchronization Clock Timing

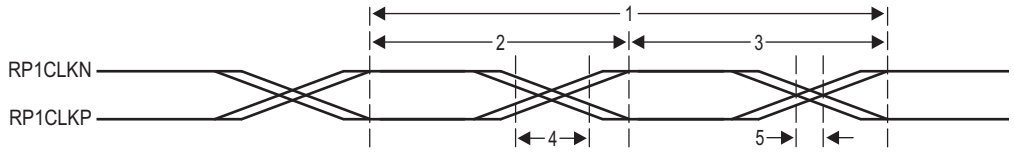

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Figure 8-50 AIF2 RP1 Frame Synchronization Burst Timing

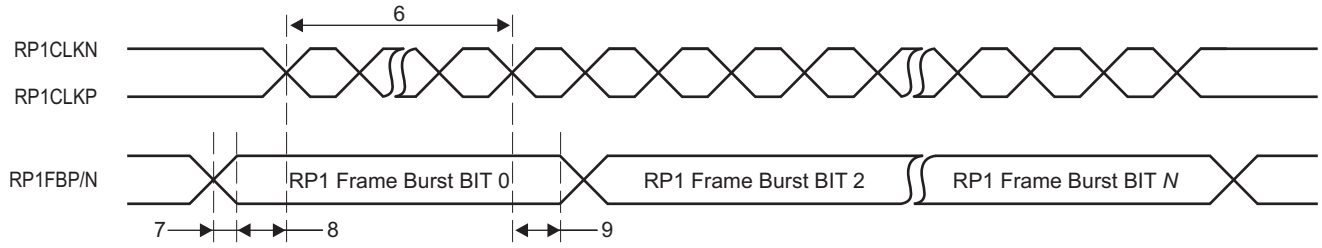


Figure 8-51 AIF2 Physical Layer Synchronization Pulse Timing

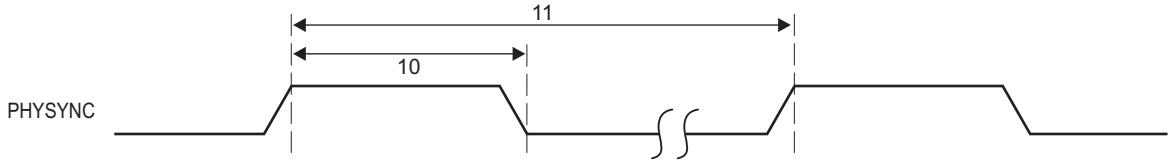


Figure 8-52 AIF2 Radio Synchronization Pulse Timing

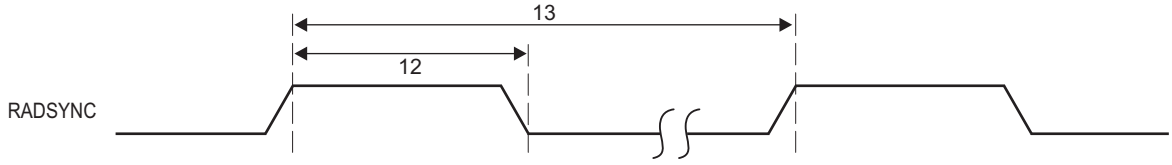
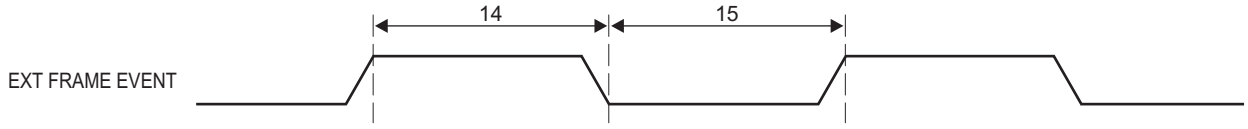


Table 8-56 AIF2 Timer Module Switching Characteristics
(see Figure 8-53)

No.	Parameter		Min	Max	Unit
	External Frame Event				
14	tw(EXTFRAMEEVENTH)	Pulse width, EXTFRAMEEVENT output high	4 * C1 (1)		ns
15	tw(EXTFRAMEEVENTL)	Pulse width, EXTFRAMEEVENT output low	4 * C1		ns
End of Table 8-56					

1 C1 = tc(RP1CLKN/P)

Figure 8-53 AIF2 Timer External Frame Event Timing



8.30 Receive Accelerator Coprocessor (RAC)

The TCI6634K2K has four Receive Accelerator Coprocessor (RAC) subsystems. Each RAC subsystem is a receive chip-rate accelerator based on a generic correlator coprocessor (GCCP). It supports Universal Mobile Telecommunications System (UMTS) operations and assists in transferring data received from the antenna to the receive core and performs receive functions that target the WCDMA macro bits.

The RAC subsystem consists of several components:

- Two GCCP accelerators for finger despread (FD), path monitor (PM), preamble detection (PD), and stream power estimator (SPE)
- Back-end interface (BEI) for management of the RAC configuration and the data output.

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- Front-end interface (FEI) for reception of the antenna data for processing and access to all MMRs (memory-mapped registers) and memories in the RAC components

The RAC has a total of three ports connected to the switch fabric:

- BEI includes two master connections to the switch fabric for output data to device memory. One is 128-bit and the other is 64-bit. Both are clocked at a SYSCLK1 divided by 3 or 4 rate.
- The FEI has a 64-bit slave connection to the switch fabric for input data as well as direct memory access (to facilitate debug)

8.31 Transmit Accelerator Coprocessor (TAC)

The Transmit Accelerator Coprocessor (TAC) subsystem is a transmit chip-rate accelerator for support of UMTS (Universal Mobile Telecommunications System) applications.

8.32 Fast Fourier Transform Coprocessor (FFTC)

There are six Fast Fourier Transform Coprocessors (FFTC) used to accelerate FFT, IFFT, DFT, and IDFT operations. For more information, see the *Fast Fourier Transform Coprocessor (FFTC) for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

8.33 Universal Serial Bus 3.0 (USB 3.0)

The device includes a USB 3.0 controller providing the following capabilities:

- Support of USB 3.0 peripheral (or device) mode at the following speeds:
  - Super Speed (SS) (5 Gbps)
  - High Speed (HS) (480 Mbps)
  - Fast Speed (FS) (12 Mbps)
- Support of USB 3.0 host mode at the following speeds:
  - Super Speed (SS) (5 Gbps)
  - High Speed (HS) (480 Mbps)
  - Fast Speed (FS) (12 Mbps)
  - Low Speed (LS) (1.5 Mbps)
- Support for USB 2.0 OTG 2.0
- Integrated DMA controller with extensible Host Controller Interface (xHCI) support
- Support for 16 transmit and receive endpoints

For more information, see the *Universal Serial Bus (USB) for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

8.34 Universal Subscriber Identity Module (USIM)

The TCI6634K2K is equipped with a Universal Subscriber Identity Module (USIM) for user authentication. The USIM is compatible with ISO, ETSI/GSM, and 3GPP standards.

The USIM is implemented for support of secure devices only. Contact your local technical sales representative for further details.

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8.35 EMIF16 Peripheral

The EMIF16 module provides an interface between the device and external memories such as NAND and NOR flash. For more information, see the *External Memory Interface (EMIF16) for KeyStone Devices User Guide* in 1.9 "Related Documentation from Texas Instruments" on page 22.

8.35.1 EMIF16 Electrical Data/Timing

Table 8-57 EMIF16 Asynchronous Memory Timing Requirements [1] (Part 1 of 2)
(see Figure 8-54 through Figure 8-57)

No.			Min	Max	Unit
General Timing					
2	t_w(WAIT)	Pulse duration, WAIT assertion and deassertion minimum time		2E	ns
28	t_d(WAIT-WEH)	Setup time, WAIT asserted before WE high		4E + 3	ns
14	t_d(WAIT-OEH)	Setup time, WAIT asserted before OE high		4E + 3	ns
Read Timing					
3	t_c(CEL)	EMIF read cycle time when ew = 0, meaning not in extended wait mode	(RS+RST+RH+3) *E-3	(RS+RST+RH+3) *E+3	ns
3	t_c(CEL)	EMIF read cycle time when ew =1, meaning extended wait mode enabled	(RS+RST+RH+3) *E-3	(RS+RST+RH+3) *E+3	ns
4	t_{osu}(CEL-OEL)	Output setup time from CE low to OE low. SS = 0, not in select strobe mode	(RS+1) * E - 3	(RS+1) * E + 3	ns
5	t_{oh}(OEH-CEH)	Output hold time from OE high to CE high. SS = 0, not in select strobe mode	(RH+1) * E - 3	(RH+1) * E + 3	ns
4	t_{osu}(CEL-OEL)	Output setup time from CE low to OE low in select strobe mode, SS = 1	(RS+1) * E - 3	(RS+1) * E + 3	ns
5	t_{oh}(OEH-CEH)	Output hold time from OE high to CE high in select strobe mode, SS = 1	(RH+1) * E - 3	(RH+1) * E + 3	ns
6	t_{osu}(BAV-OEL)	Output setup time from BA valid to OE low	(RS+1) * E - 3	(RS+1) * E + 3	ns
7	t_{oh}(OEH-BAIV)	Output hold time from OE high to BA invalid	(RH+1) * E - 3	(RH+1) * E + 3	ns
8	t_{osu}(AV-OEL)	Output setup time from A valid to OE low	(RS+1) * E - 3	(RS+1) * E + 3	ns
9	t_{oh}(OEH-AIV)	Output hold time from OE high to A invalid	(RH+1) * E - 3	(RH+1) * E + 3	ns
10	t_w(OEL)	OE active time low, when ew = 0. Extended wait mode is disabled.	(RST+1) * E - 3	(RST+1) * E + 3	ns
10	t_w(OEL)	OE active time low, when ew = 1. Extended wait mode is enabled.	(RST+1) * E - 3	(RST+1) * E + 3	ns
11	t_d(WAITH-OEH)	Delay time from WAIT deasserted to OE# high		4E + 3	ns
12	t_{su}(D-OEH)	Input setup time from D valid to OE high	3		ns
13	t_h(OEH-D)	Input hold time from OE high to D invalid	0.5		ns
Write Timing					
15	t_c(CEL)	EMIF write cycle time when ew = 0, meaning not in extended wait mode	(WS+WST+WH+ TA+4)*E-3	(WS+WST+WH+ TA+4)*E+3	ns
15	t_c(CEL)	EMIF write cycle time when ew =1., meaning extended wait mode is enabled	(WS+WST+WH+ TA+4)*E-3	(WS+WST+WH+ TA+4)*E+3	ns
16	t_{osu}CEL-WEL)	Output setup time from CE low to WE low. SS = 0, not in select strobe mode	(WS+1) * E - 3		ns
17	t_{oh}(WEH-CEH)	Output hold time from WE high to CE high. SS = 0, not in select strobe mode	(WH+1) * E - 3		ns
16	t_{osu}CEL-WEL)	Output setup time from CE low to WE low in select strobe mode, SS = 1	(WS+1) * E - 3		ns
17	t_{oh}(WEH-CEH)	Output hold time from WE high to CE high in select strobe mode, SS = 1	(WH+1) * E - 3		ns
18	t_{osu}(RNW-WEL)	Output setup time from RNW valid to WE low	(WS+1) * E - 3		ns
19	t_{oh}(WEH-RNW)	Output hold time from WE high to RNW invalid	(WH+1) * E - 3		ns
20	t_{osu}(BAV-WEL)	Output setup time from BA valid to WE low	(WS+1) * E - 3		ns
21	t_{oh}(WEH-BAIV)	Output hold time from WE high to BA invalid	(WH+1) * E - 3		ns
22	t_{osu}(AV-WEL)	Output setup time from A valid to WE low	(WS+1) * E - 3		ns
23	t_{oh}(WEH-AIV)	Output hold time from WE high to A invalid	(WH+1) * E - 3		ns
24	t_w(WEL)	WE active time low, when ew = 0. Extended wait mode is disabled.	(WST+1) * E - 3		ns

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Table 8-57 EMIF16 Asynchronous Memory Timing Requirements (1) (Part 2 of 2)
(see Figure 8-54 through Figure 8-57)

No.			Min	Max	Unit
24	t_w(WEL)	WE active time low, when ew = 1. Extended wait mode is enabled.	(WST+1) * E - 3		ns
26	t_{osu}(DV-WEL)	Output setup time from D valid to WE low	(WS+1) * E - 3		ns
27	t_{oh}(WEH-DIV)	Output hold time from WE high to D invalid	(WH+1) * E - 3		ns
25	t_d(WAITH-WEH)	Delay time from WAIT deasserted to WE# high		4E + 3	ns
End of Table 8-57					

1 E = 1/(SYSCLK1/6)

Figure 8-54 EMIF16 Asynchronous Memory Read Timing Diagram

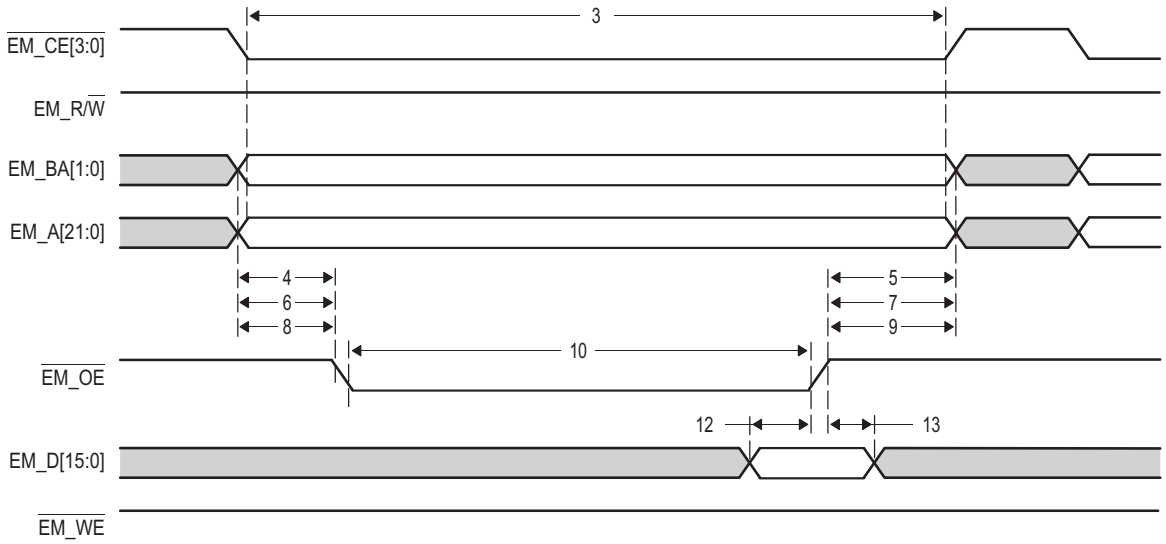

Figure 8-55 EMIF16 Asynchronous Memory Write Timing Diagram

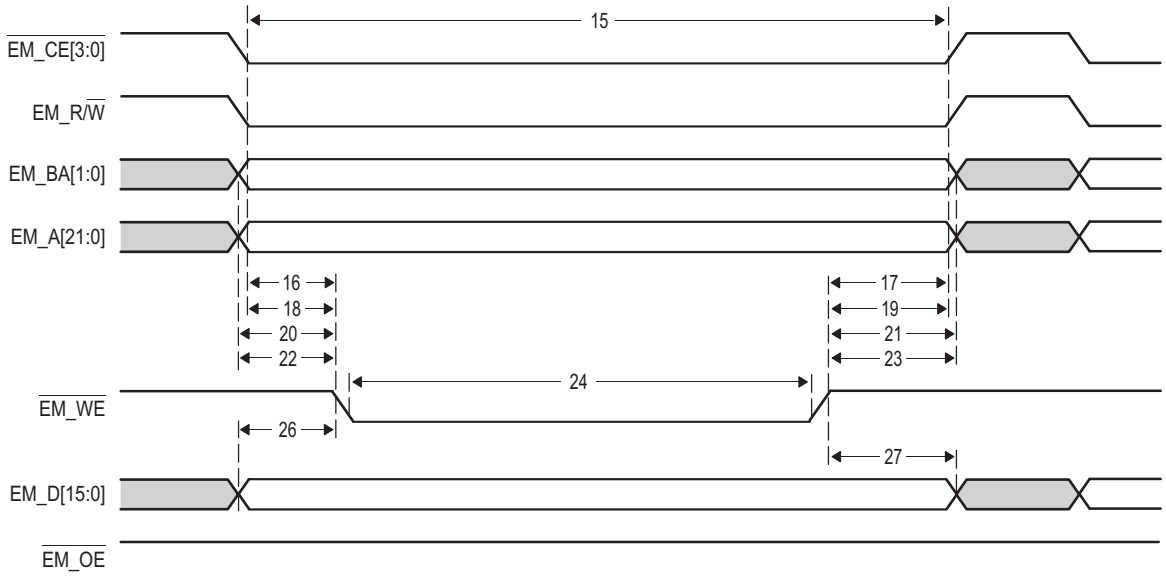

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Figure 8-56 EMIF16 EM_WAIT Read Timing Diagram

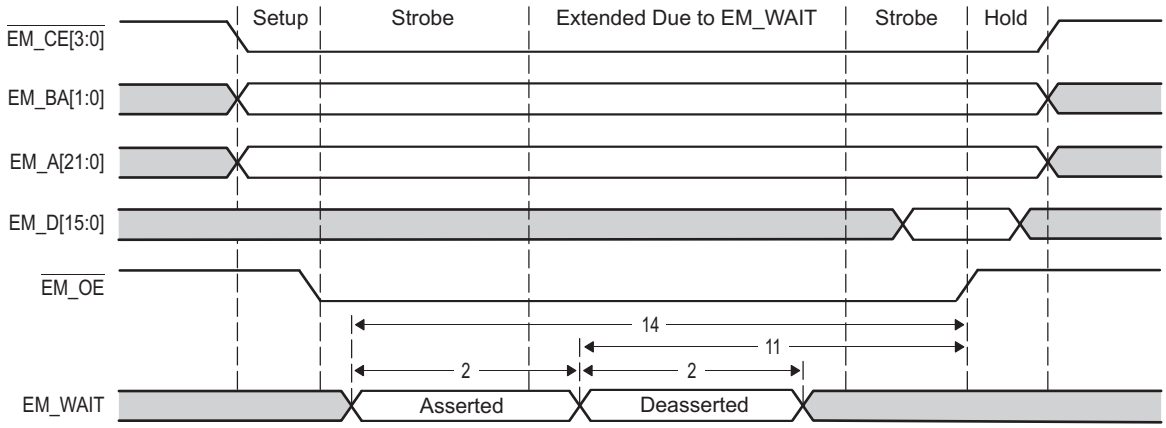
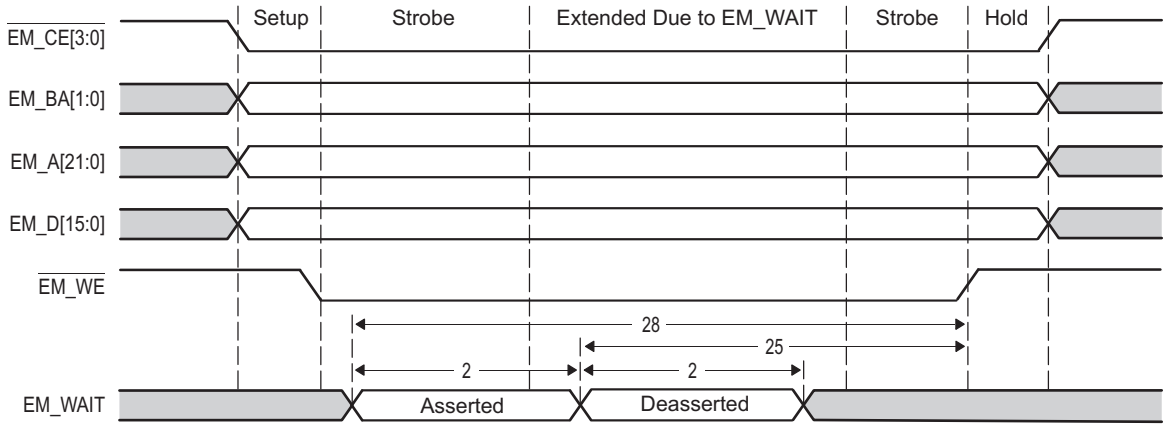


Figure 8-57 EMIF16 EM_WAIT Write Timing Diagram



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8.36 Emulation Features and Capability

8.36.1 Advanced Event Triggering (AET)

The device supports advanced event triggering (AET). This capability can be used to debug complex problems as well as understand performance characteristics of user applications. AET provides the following capabilities:

- **Hardware program breakpoints:** specify addresses or address ranges that can generate events such as halting the processor or triggering the trace capture.
- **Data watchpoints:** specify data variable addresses, address ranges, or data values that can generate events such as halting the processor or triggering the trace capture.
- **Counters:** count the occurrence of an event or cycles for performance monitoring.
- **State sequencing:** allows combinations of hardware program breakpoints and data watchpoints to precisely generate events for complex sequences.

For more information on the AET, see the following documents in 1.9 "Related Documentation from Texas Instruments" on page 22:

- Using Advanced Event Triggering to Find and Fix Intermittent Real-Time Bugs application report
- Using Advanced Event Triggering to Debug Real-Time Problems in High Speed Embedded Microprocessor Systems application report

8.36.2 Trace

The TCI6634K2K device supports trace. Trace is a debug technology that provides a detailed, historical account of application code execution, timing, and data accesses. Trace collects, compresses, and exports debug information for analysis. Trace works in real-time and does not impact the execution of the system.

For more information on board design guidelines for trace advanced emulation, see the *Emulation and Trace Headers Technical Reference* in 1.9 "Related Documentation from Texas Instruments" on page 22.

8.36.2.1 Trace Electrical Data/Timing

Table 8-58 Trace Switching Characteristics
(see Figure 8-58)

No.	Parameter		Min	Max	Unit
1	t_w(DPnH)	Pulse duration, DPn/EMUn high	2.4		ns
1	t_w(DPnH)90%	Pulse duration, DPn/EMUn high detected at 90% Voh	1.5		ns
2	t_w(DPnL)	Pulse duration, DPn/EMUn low	2.4		ns
2	t_w(DPnL)10%	Pulse duration, DPn/EMUn low detected at 10% Voh	1.5		ns
3	t_{sko}(DPn)	Output skew time, time delay difference between DPn/EMUn pins configured as trace	-1	1	ns
	t_{skp}(DPn)	Pulse skew, magnitude of difference between high-to-low (tphl) and low-to-high (tplh) propagation delays.		600	ps
	t_{sldp_o}(DPn)	Output slew rate DPn/EMUn	3.3		V/ns
End of Table 8-58					

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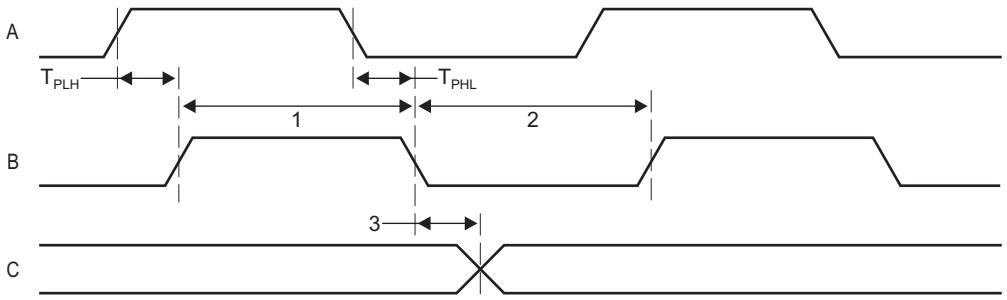
Figure 8-58 Trace Timing



8.36.3 IEEE 1149.1 JTAG

The Joint Test Action Group (JTAG) interface is used to support boundary scan and emulation of the device. The boundary scan supported allows for an asynchronous test reset ($\overline{TRST}$) and only the five baseline JTAG signals (e.g., no EMU[1:0]) required for boundary scan. Most interfaces on the device follow the Boundary Scan Test Specification (IEEE1149.1), while all of the SerDes (SRIO and SGMII) support the AC-coupled net test defined in AC-Coupled Net Test Specification (IEEE1149.6).

It is expected that all compliant devices are connected through the same JTAG interface, in daisy-chain fashion, in accordance with the specification. The JTAG interface uses 1.8-V LVCMOS buffers, compliant with the *Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuit Specification* (EAI/JESD8-5).

8.36.3.1 IEEE 1149.1 JTAG Compatibility Statement

For maximum reliability, the TCI6634K2K device includes an internal pulldown (IPD) on the $\overline{TRST}$ pin to ensure that $\overline{TRST}$ will always be asserted upon power up and the device's internal emulation logic will always be properly initialized when this pin is not routed out. JTAG controllers from Texas Instruments actively drive $\overline{TRST}$ high. However, some third-party JTAG controllers may not drive $\overline{TRST}$ high, but expect the use of an external pullup resistor on $\overline{TRST}$. When using this type of JTAG controller, assert $\overline{TRST}$ to initialize the device after powerup and externally drive $\overline{TRST}$ high before attempting any emulation or boundary scan operations.

8.36.3.2 JTAG Electrical Data/Timing

Table 8-59 JTAG Test Port Timing Requirements
(see Figure 8-59)

No.			Min	Max	Unit
1	$t_{c(TCK)}$	Cycle time, TCK	34		ns
1a	tw(TCKH)	Pulse duration, TCK high (40% of tc)	13.6		ns
1b	tw(TCKL)	Pulse duration, TCK low(40% of tc)	13.6		ns
3	tsu(TDI-TCK)	Input setup time, TDI valid to TCK high	3.4		ns
3	tsu(TMS-TCK)	Input setup time, TMS valid to TCK high	3.4		ns
4	th(TCK-TDI)	Input hold time, TDI valid from TCK high	17		ns
4	th(TCK-TMS)	Input hold time, TMS valid from TCK high	17		ns
End of Table 8-59					

Table 8-60 JTAG Test Port Switching Characteristics
(see Figure 8-59)

No.	Parameter		Min	Max	Unit
2	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid		13.6	ns
End of Table 8-60					

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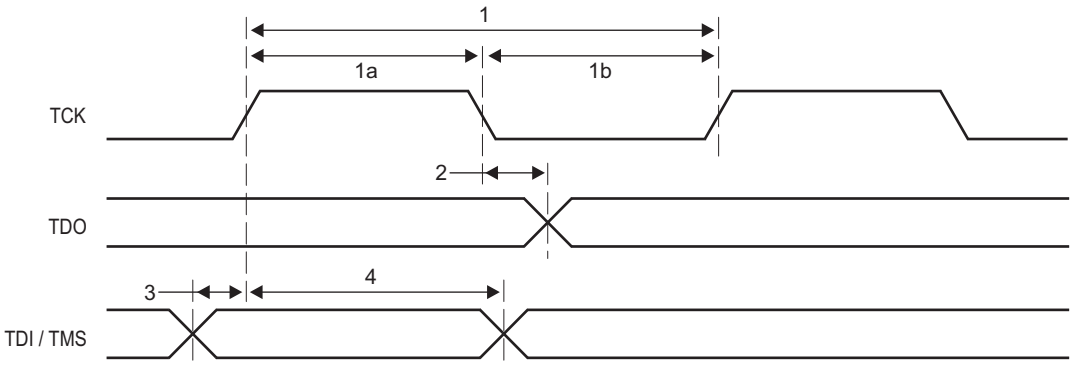
Figure 8-59 JTAG Test-Port Timing



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9 Mechanical Data

9.1 Thermal Data

Table 9-1 shows the thermal resistance characteristics for the PBGA - TBD mechanical package.

Table 9-1 Thermal Resistance Characteristics (PBGA Package) [TBD]

No.			°C/W
1	$R\theta_{JC}$	Junction-to-case	TBD
2	$R\theta_{JB}$	Junction-to-board	TBD
End of Table 9-1			

9.2 Packaging Information

The following packaging information reflects the most current released data available for the designated device(s). This data is subject to change without notice and without revision of this document.

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A Revision History

SPRS833A

- Updated the ALNCTL Register in the Peripheral Information and Electrical Specifications chapter. (Page 242)
- Updated the DCHANGE Register in the Peripheral Information and Electrical Specifications chapter. (Page 242)
- Updated VDDAHV in the Power Supply to Peripheral I/O Mapping table. (Page 215)
- Changed to not support external charge pump for 5V (Page 277)
- Changed 'bit' to 'pin' (Page 185)
- Updated BOOTMODE pins and MIN information (Page 174)
- Added Device Boot and Configuration chapter. (Page 174)
- Added Peripheral Information and Electrical Specifications chapter. (Page 216)
- In the SPI Switching Characteristics table: Changed the incorrect SPIx_Clk signal name to SPICLK. (Page 260)
- In the SPI Switching Characteristics table: Changed the incorrect SPIx_SCS signal name to SPISCSx. (Page 261)
- In the SPI Switching Characteristics table: Corrected signal name from SPIx_SIMO to SPIDOUT. (Page 260)
- In the SPI Timing Requirements table: Changed the incorrect SPIx_Clk signal name to SPICLK. (Page 260)
- In the SPI Timing Requirements table: Corrected signal name SPIx_SOMI to SPIDIN. (Page 260)
- Updated DDRCLKN and DDRCLKP from 0.025 to 0.02. (Page 251)
- Added Security section (Page 183)
- Added thermal values into the Thermal Resistance Characteristics table. (Page 284)
- Voltages for VP and VPH corrected in the Terminal Functions table. (Page 56)

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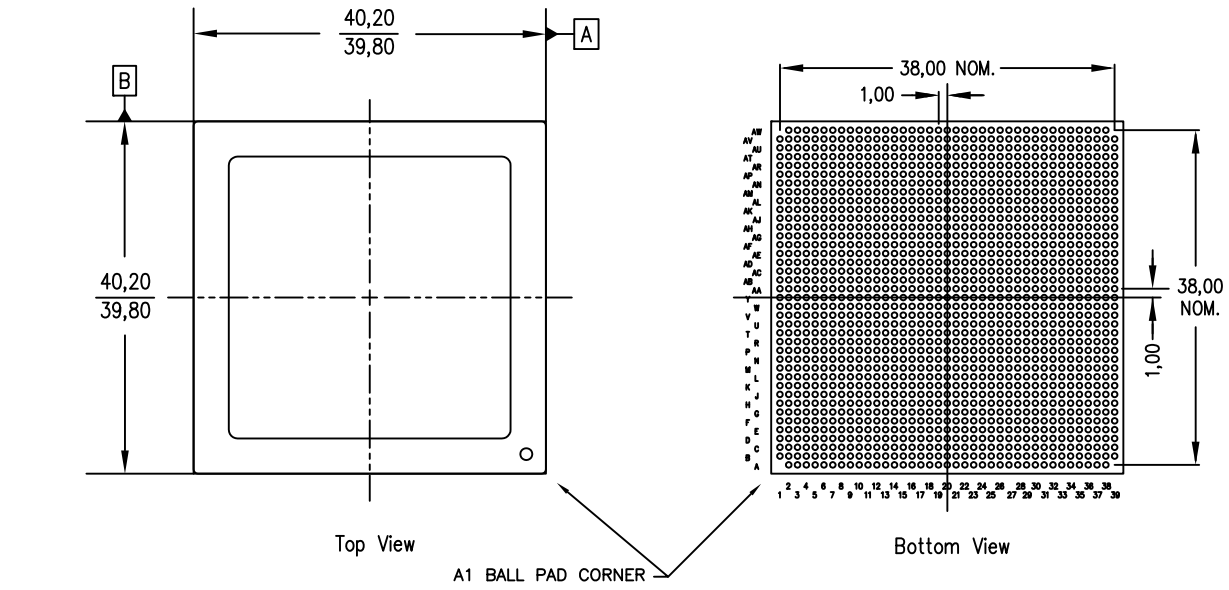
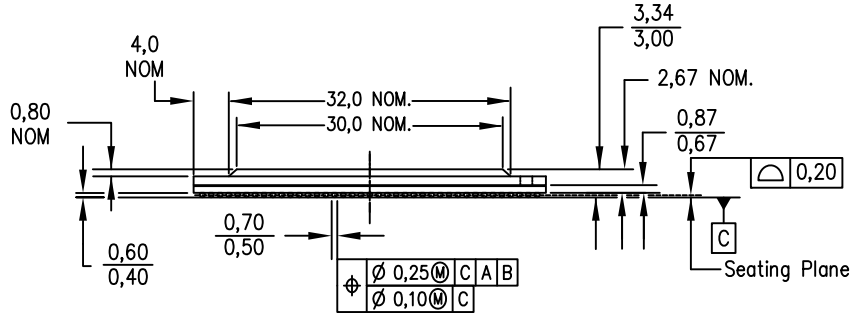
AAW (S–PBGA–N1517) PLASTIC BALL GRID ARRAY

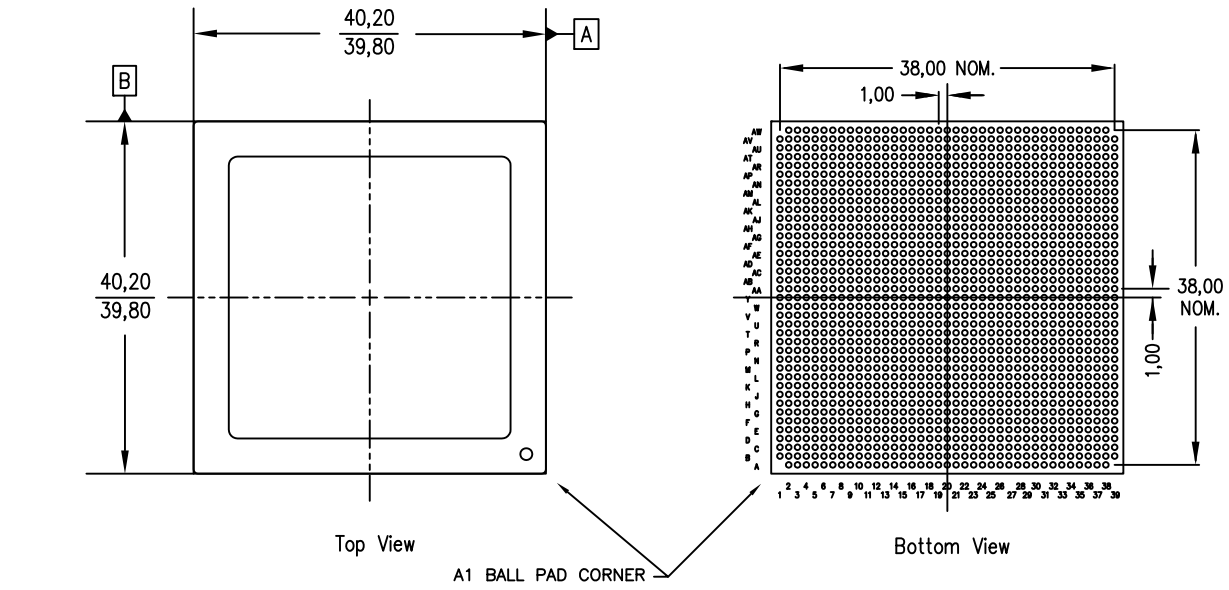


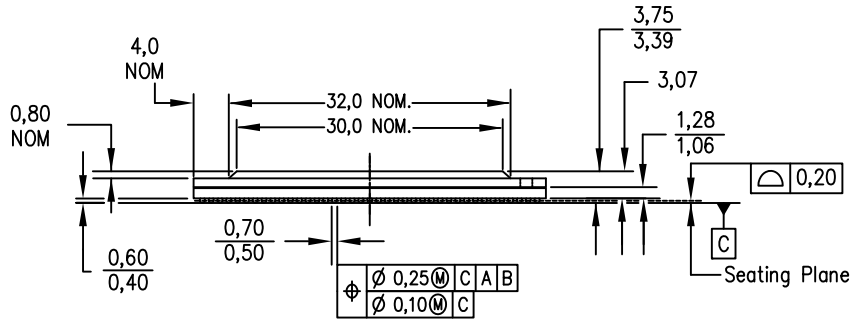


PACKAGE IDENTIFIER: AAW–01 4212578–2/B 10/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Flip chip application only.
D. Pb–free die bump and solder ball.

AAW (S–PBGA–N1517) PLASTIC BALL GRID ARRAY





PACKAGE IDENTIFIER: AAW–02 4212578–3/B 10/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
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