Low Voltage 5-Bit Self-Timed, Single-Wire Output Expander

Check for Samples: TCA5405

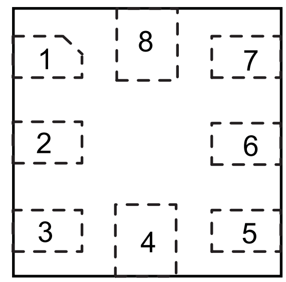
FEATURES

- **Operating Power-Supply Voltage Range of 1.65 V to 3.6 V**
- **Five Independent Push-Pull Outputs**
- **Single Input (DIN) Controls State of All Outputs**
- **High-Current Drive Outputs Maximum Capability for Directly Driving LEDs**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **1000-V Charged-Device Model (C101)**

APPLICATIONS

- **Cell Phones**
- **PDAs**
- **Portable Media Players**
- **MP3 Players**
- **Portable Instrumentation**

RUG PACKAGE (TOP VIEW)



PIN #	NAME	COMMENTS
1	VCC	Supply Voltage
2	DIN	Data Input
3	GND	Ground
4	Q0	GPO
5	Q1	GPO
6	Q2	GPO
7	Q3	GPO
8	Q4	GPO

DESCRIPTION

The TCA5405 is a 5-bit output expander controlled using a single wire input. This device is ideal for portable applications as it has a wide VCC range of 1.65V to 3.6 V. The TCA5405 uses a self-timed serial data protocol with a single data input driven by a master device synchronized to an internal clock of that device. During a Setup phase, the bit period is sampled, then the TCA5405 generates its own internal clock synchronized to that of the Master device to sample the input over a five-bit-period Data Transfer phase and writes the bit states on the parallel outputs after the last bit is sampled. The TCA5405 is available in an 8-pin 1.5mm x 1.5mm RUG uQFN package.

ORDERING INFORMATION

T_A	PACKAGE (1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	uQFN – RUG	Tape and Reel	TCA5405RUGR	6Y

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

APPLICATION DIAGRAM

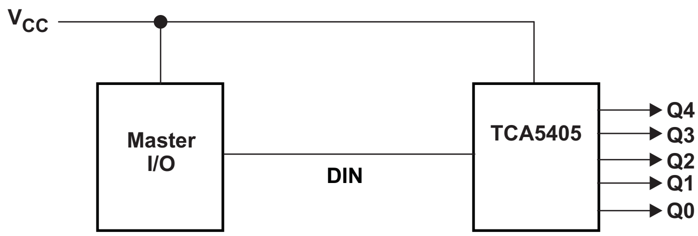


Figure 1. TCA5405 Application Diagram

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.0	V
V_I	Input voltage range(2)		–0.5	4.0	V
V_O	Output voltage range(2)		–0.5	4.0	V
I_{IK}	Input clamp current	$V_I < 0$		±20	mA
I_{OK}	Output clamp current	$V_O < 0$		±20	mA
I_{OL}	Continuous output low current	V_O = 0 to V_{CC}		50	mA
I_{OH}	Continuous output high current	V_O = 0 to V_{CC}		50	mA
I_{CC}	Continuous current through GND			200	mA
	Continuous current through V_{CC}			160	
ΘJA	Package thermal impedance(3)	RUG package		243	°C/W
TSTG	Storage temperature range		–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	3.6	V
V_{IH}	High-level input voltage	DIN	0.7 × V_{CC}	V_{CC} + 0.5	V
V_{IL}	Low-level input voltage	DIN	–0.3	0.3 × V_{CC}	V
I_{OH}	High-level output current	Q0–Q4		20	mA
I_{OL}	Low-level output current	Q0–Q4		20	mA
T_A	Operating free-air temperature		–40	85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 1.65 V to 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18 mA	1.65 V to 3.6 V	–1.2			V
V_{POR}	Power on reset voltage	V_I = V_{CC} or GND, I_O = 0	1.65 V to 3.6 V		1	1.4	V
I_I	DIN	V_I = V_{CC} or GND	1.65 V to 3.6 V			±0.1	μA
I_{CC_STBY}	Standby Supply Current	V_I on DIN = V_{CC} or GND, I_O = 0	1.65 V to 3.6 V		1	2	μA
I_{CC_ACTIVE}	Active current during startup and data transfer					400	μA
C_I	DIN	V_I = V_{CC} or GND	1.65 V to 3.6 V		6	7	pF
V_{OH}	OUT-port high-level output voltage	I_{OH} = –20 mA	1.65 V	1.1			V
			2.3 V	1.7			
			3.6 V	2.5			
V_{OL}	OUT-port low-level output voltage	I_{OL} = 20 mA	1.65 V			0.6	V
			2.3 V			0.3	
			3.6 V			0.25	

TIMING REQUIREMENTS

over recommended operating free-air temperature range, V_{CC} = 1.65 V to 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
t_{PER}	DIN period		1.65 V to 3.6 V	0.001		10	ms
t_{rise}	DIN rise time		1.65 V to 3.6 V			100	ns
t_{fall}	DIN fall time		1.65 V to 3.6 V			100	ns
f_{MIN}	Maximum switching frequency on DIN		1.65 V to 3.6 V	1			MHz
f_{MAX}	Minimum switching frequency on DIN		1.65 V to 3.6 V			10	kHz

PRINCIPLES OF OPERATION

The TCA5405 single-wire bus device has a single-bit Data Line Bus input and has five independent parallel push-pull buffered outputs. A single input is used to control the output state for the writing to these five outputs. This single-wire serial interface is similar to a UART type interface but operates over a wide range of values for the bit period.

The TCA5405 uses a self-timed serial data protocol with a single data input driven by a master device synchronized to an internal clock of that device. During a Setup phase, the bit period is sampled, then the TCA5405 generates its own internal clock synchronized to that of the Master device to sample the input over a five-bit-period Data Transfer phase and writes the bit states on the parallel outputs after the last bit is sampled. The Master output bit must be transmitted via a Totem-pole output structure to ensure proper interpretation of the incoming serial burst.

The single-wire unidirectional interface operation is defined in Figure 2.

INTERFACE TIMING

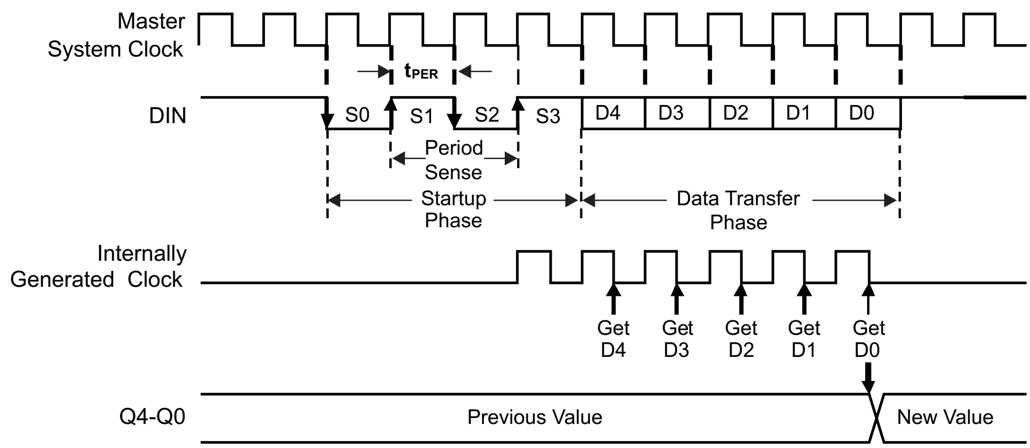


Figure 2. Definition of Single-Wire Interface

To function correctly, the bit period (tPER) of the DIN signal must be constant over the entire data transaction. Therefore, DIN should be driven by a stable periodic signal internal to the Master device (see Figure 2 - Master System Clock). The bit period can be any value between 1μS and 10mS.

The TCA5405 first detects the falling transition on DIN at the beginning of the S0 period to signal the start of an incoming data burst. Next, over the period of S1 and S2, between the two rising edges on DIN, a timer measures the duration of S1/S2 to calculate the bit period of the incoming signal. After that, the TCA5405 uses that value to generate its own internal clock which it uses to sample DIN as near as possible to the center of the subsequent D4-D0 bit periods. After bit D0 is sampled, the five sampled values are sent to the Q4-Q0 outputs. At the end of the D0 bit period, if DIN is not already high, it must be set high to signal the end of the transaction and to prepare for the next one.

TYPICAL CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

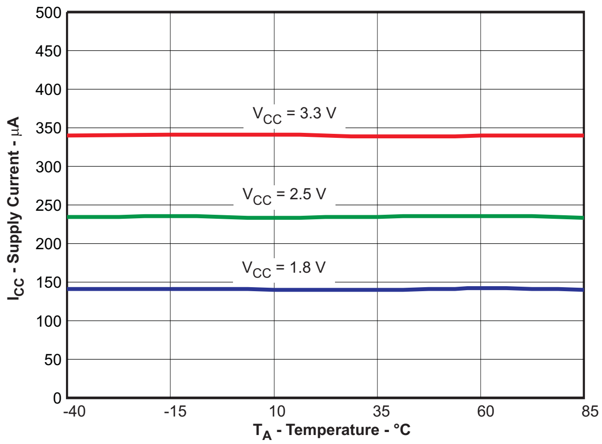


Figure 3. Active Current vs Temperature

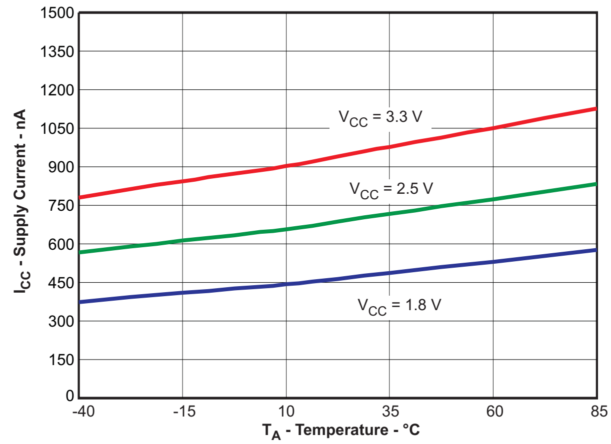


Figure 4. Standby Supply Current vs Temperature

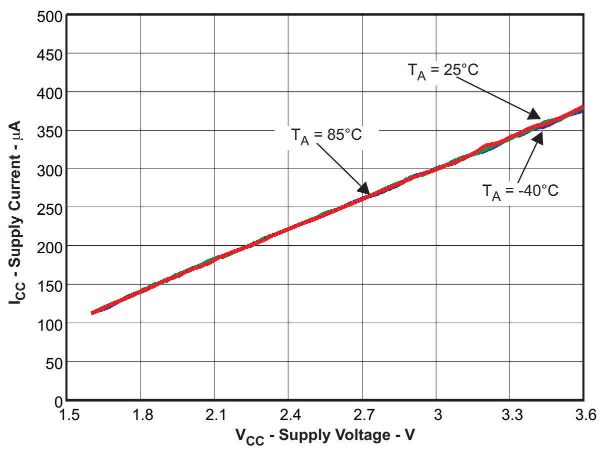


Figure 5. Active Supply Current vs Supply Voltage

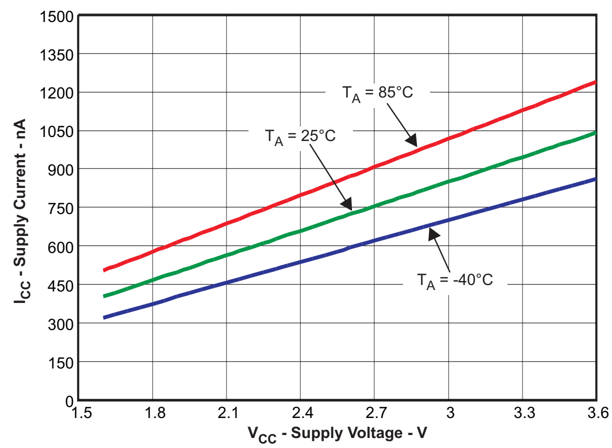


Figure 6. Standby Supply Current vs Supply Voltage

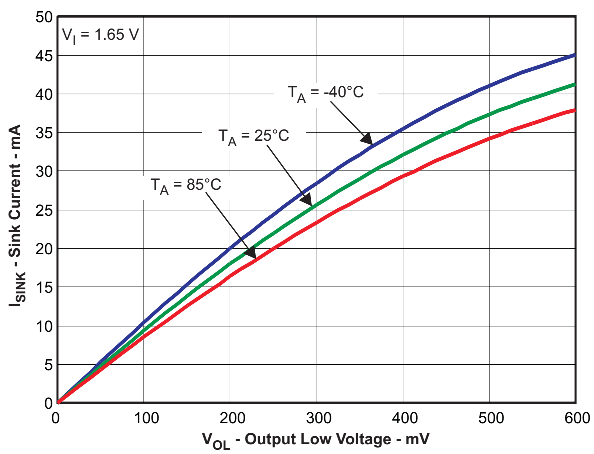


Figure 7. I/O Sink Current vs Output Low Voltage VCC = 1.65V

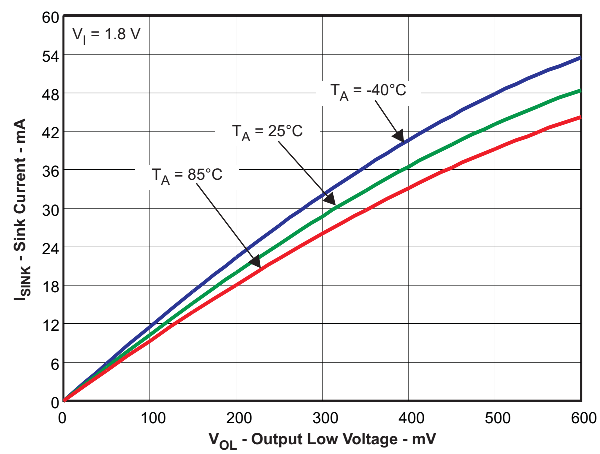


Figure 8. I/O Sink Current vs Output Low Voltage VCC = 1.8 V

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C (unless otherwise noted)

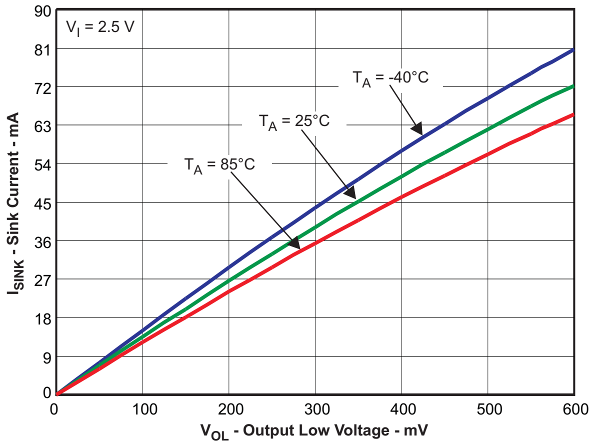


Figure 9. I/O Sink Current vs Output Low Voltage VCC = 2.5V

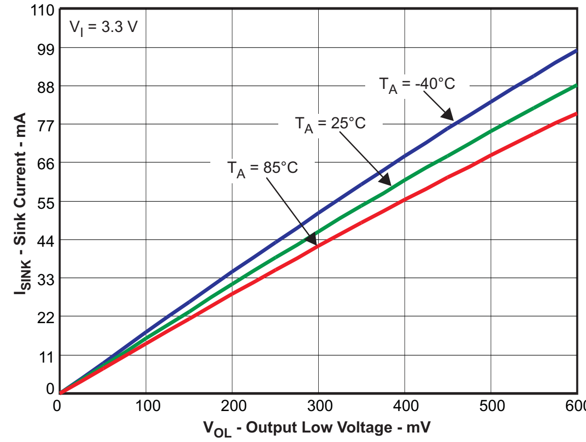


Figure 10. I/O Sink Current vs Output Low Voltage VCC = 3.3V

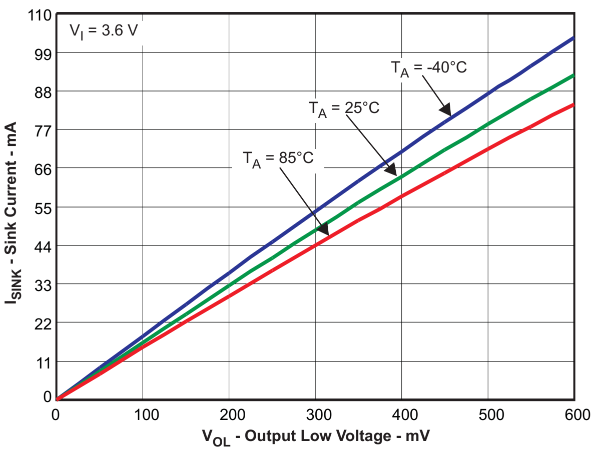


Figure 11. I/O Sink Current vs Output Low Voltage VCC =3.6V

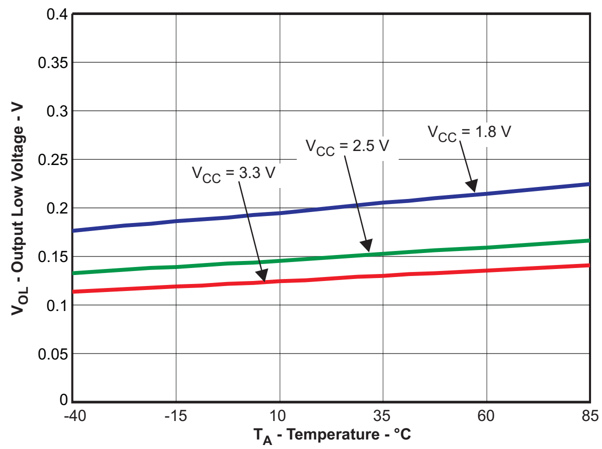


Figure 12. I/O Low Voltage vs Temperature VCC = 3.3V at 20 mA

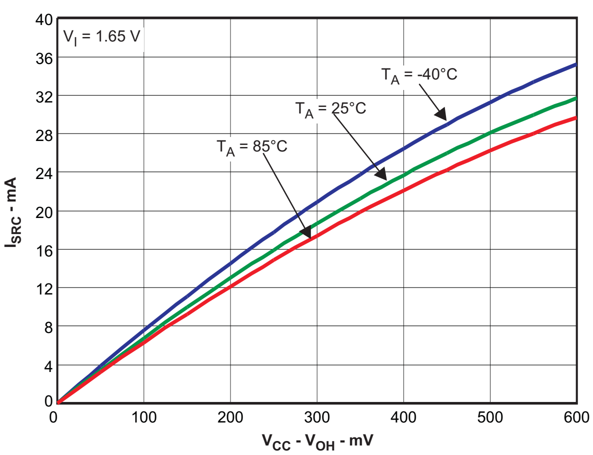


Figure 13. I/O Source Current vs Output High Voltage VCC = 1.65V

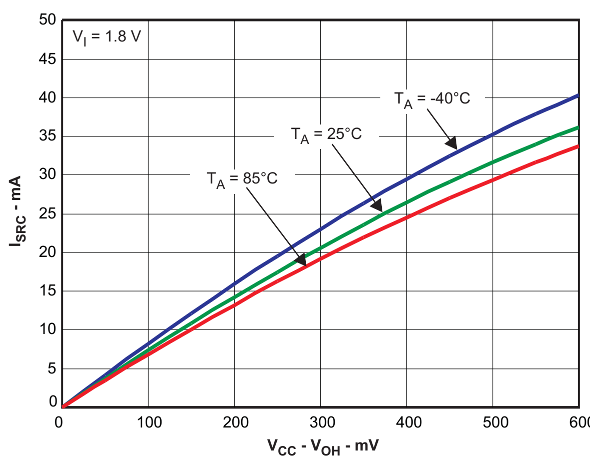


Figure 14. I/O Source Current vs Output High Voltage VCC = 1.8V

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C (unless otherwise noted)

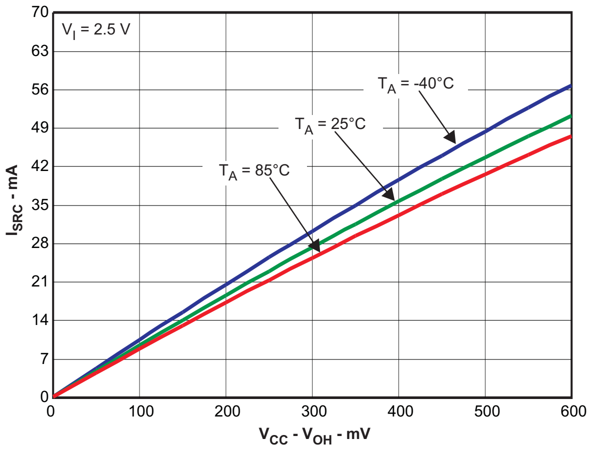


Figure 15. I/O Source Current vs Output High Voltage VCC = 2.5V

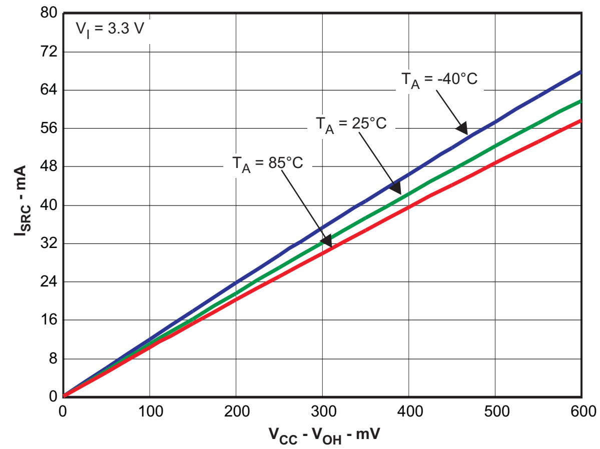


Figure 16. I/O Source Current vs Output High Voltage VCC = 3.3V

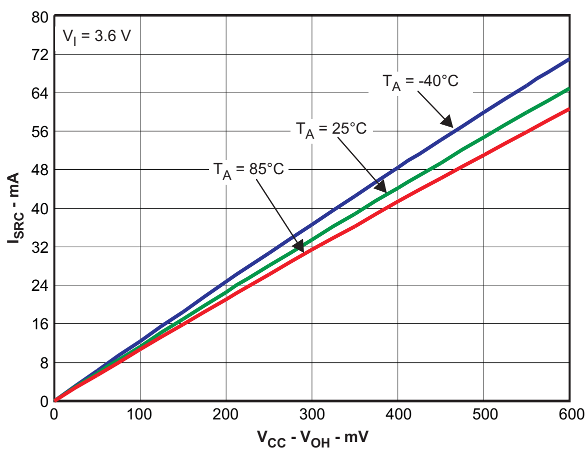


Figure 17. I/O Source Current vs Output High Voltage VCC = 3.6V

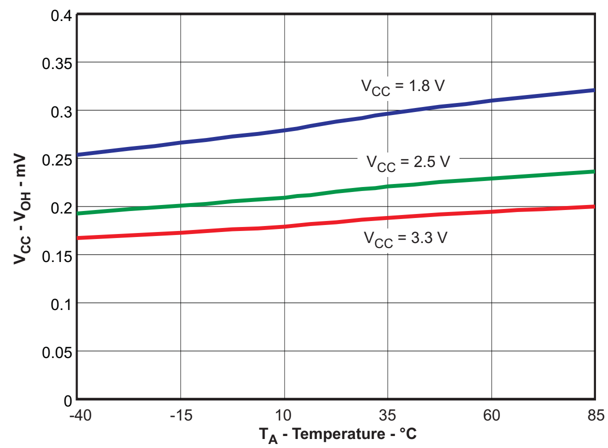


Figure 18. I/O High Voltage vs Temperature VCC = 3.3V at 20 mA

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TCA5405RUGR	ACTIVE	X2QFN	RUG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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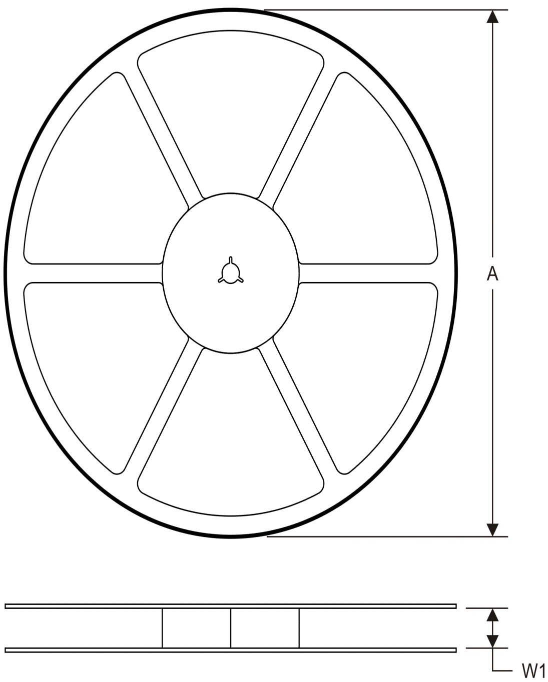
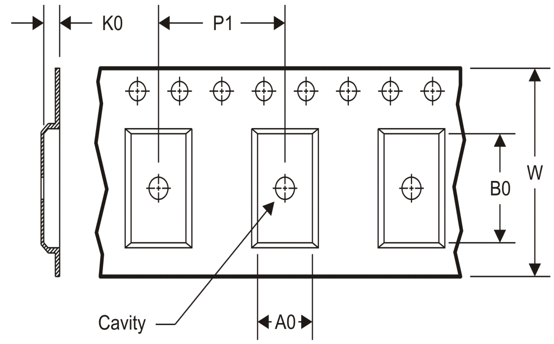
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



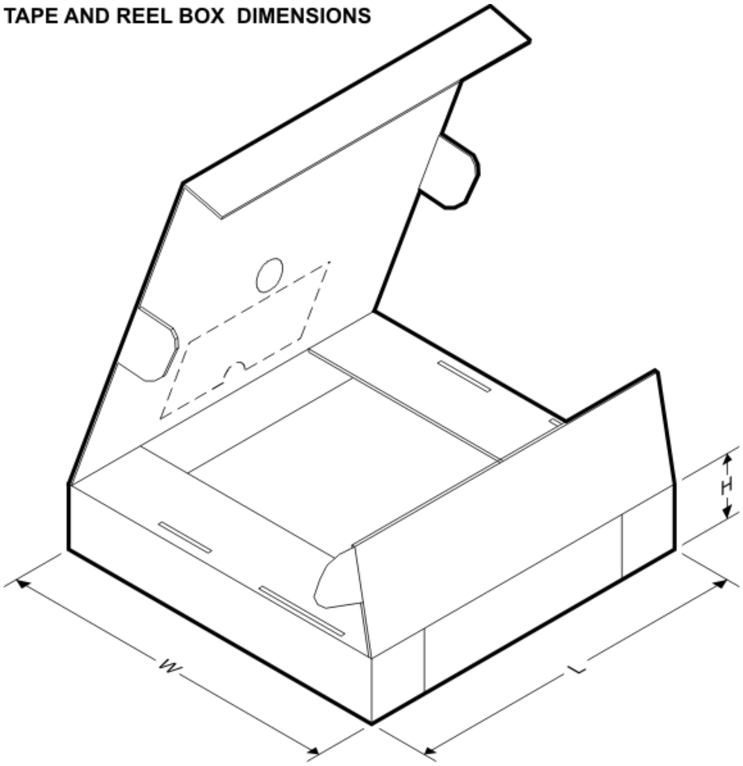
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA5405RUGR	X2QFN	RUG	8	3000	180.0	8.4	1.6	1.6	0.66	4.0	8.0	Q2

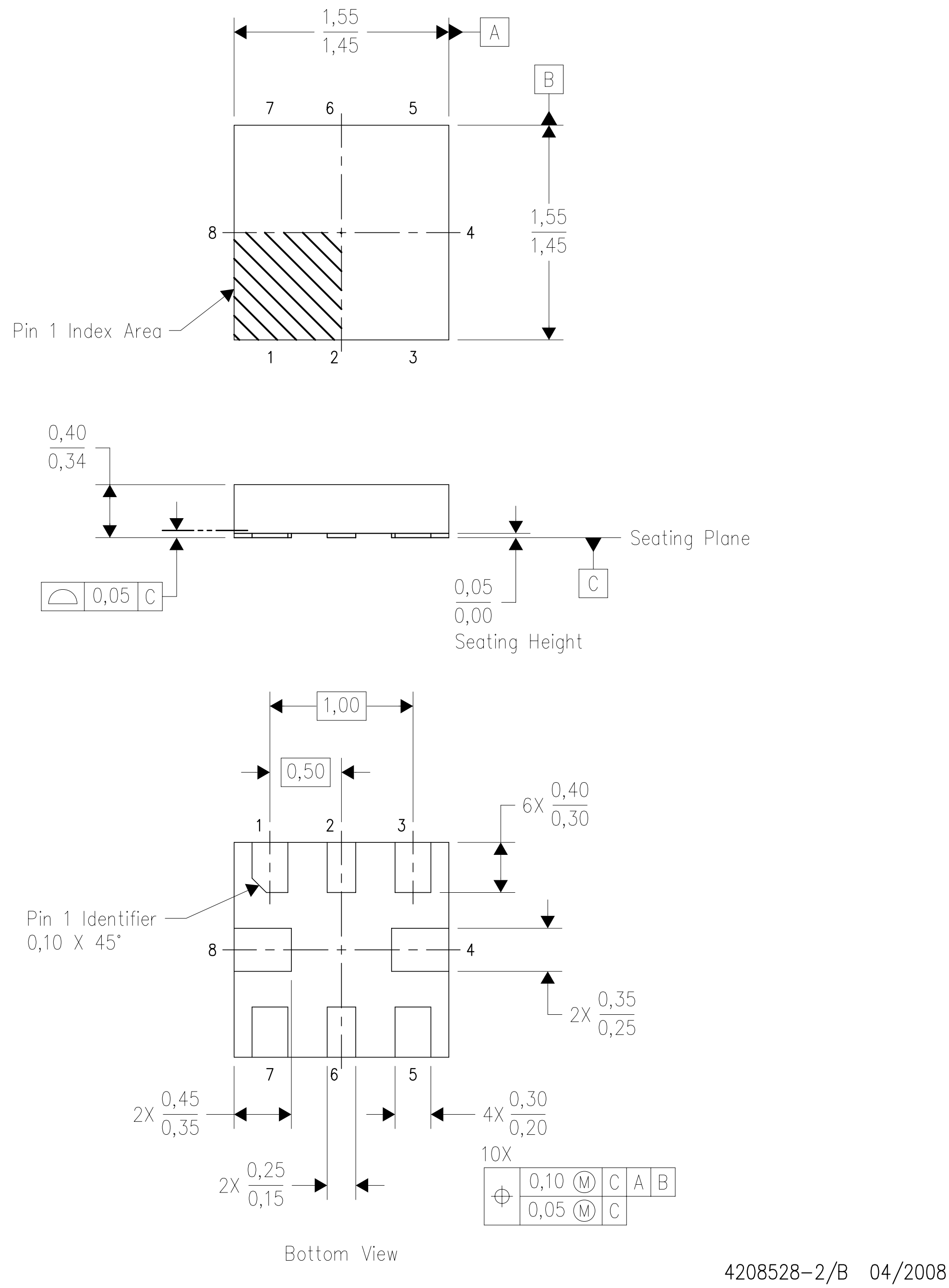
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

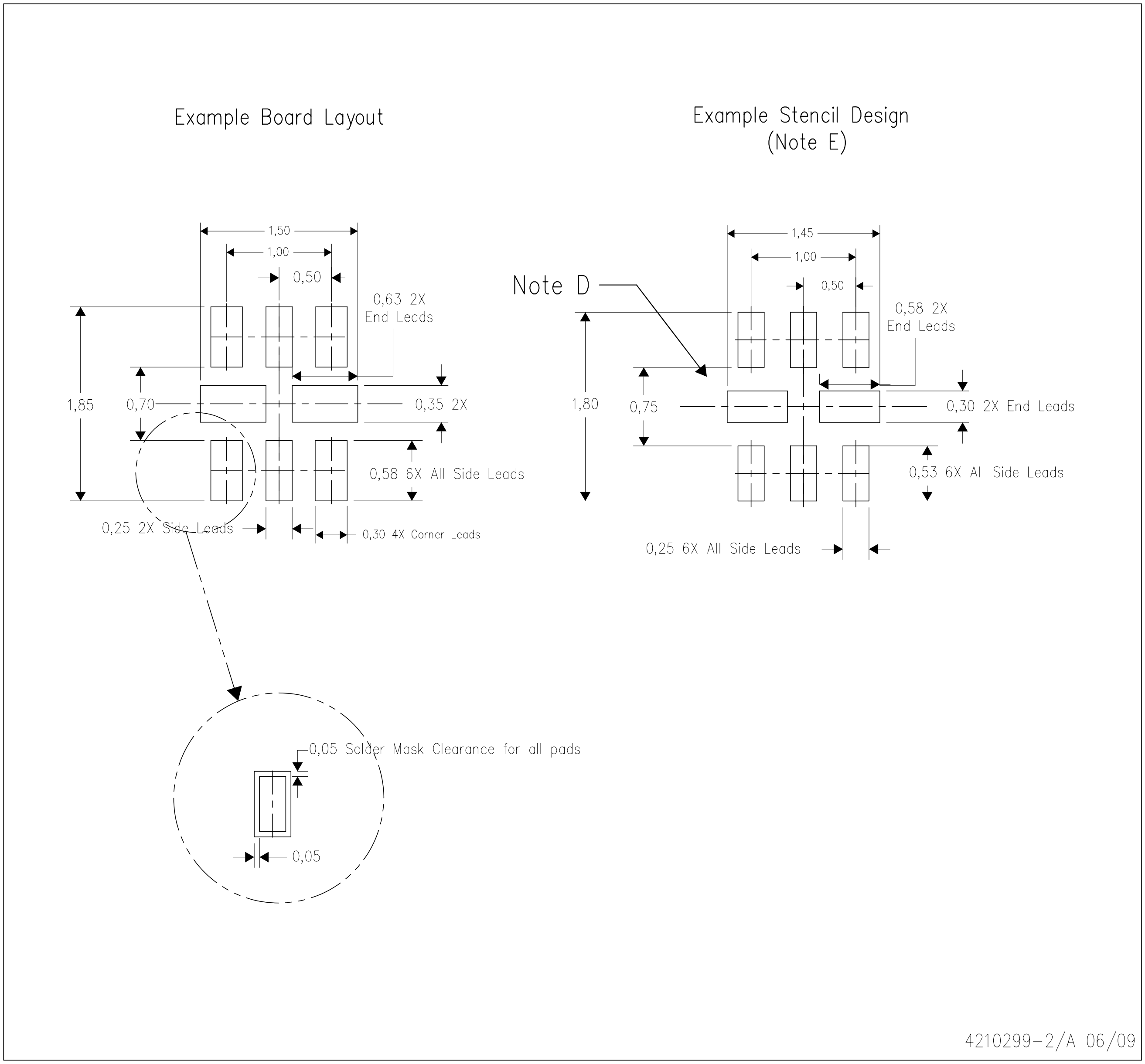
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA5405RUGR	X2QFN	RUG	8	3000	202.0	201.0	28.0

RUG (S-PQFP-N8) PLASTIC QUAD FLATPACK



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. This package complies to JEDEC MO-288 variation X2ECD.

RUG (R–PQFP–N8)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.