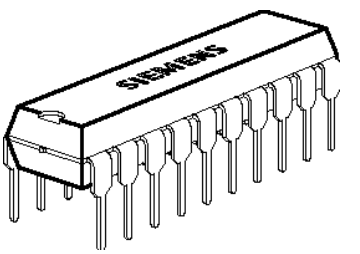
SIEMENS

2-Phase Stepper-Motor Driver TCA 3727

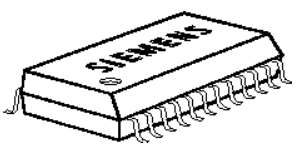
Bipolar IC

Features

- 2 x 0.75 amp. / 50 V outputs
- Integrated driver, control logic and current control (chopper)
- Fast free-wheeling diodes
- Max. supply voltage 52 V
- Outputs free of crossover current
- Offset-phase turn-ON of output stages
- Z-diode for logic supply
- Low standby-current drain
- Full, half, quarter, mini, quasi-sine step



P-DIP-20-3



P-DSO-24-3

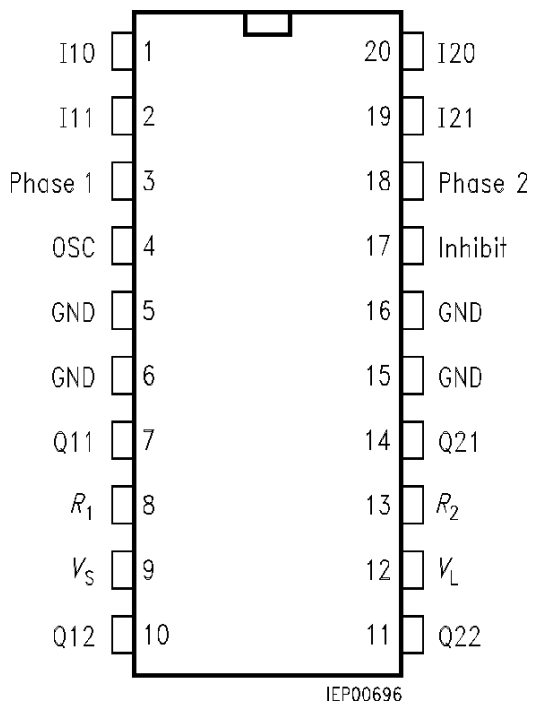
Type	Ordering Code	Package
TCA 3727	Q67000-A8302	P-DIP-20-3
TCA 3727 G	Q67000-A8335	P-DSO-24-3 (SMD)

TCA 3727 is a bipolar, monolithic IC for driving bipolar stepper motors, DC motors and other inductive loads that operate on constant current. The control logic and power output stages for two bipolar windings are integrated on a single chip which permits switched current control of motors with 0.75 A per phase at operating voltages up to 50 V.

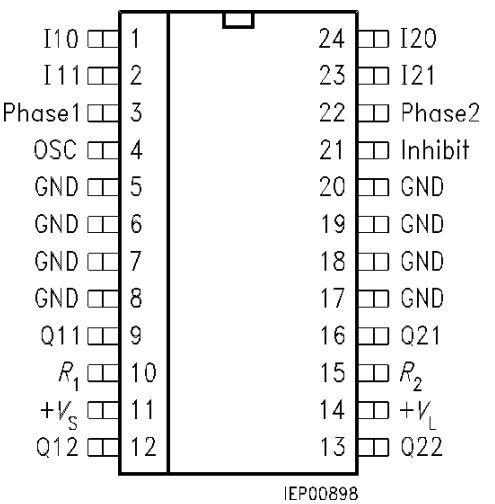
The direction and value of current are programmed for each phase via separate control inputs. A common oscillator generates the timing for the current control and turn-on with phase offset of the two output stages. The two output stages in a full-bridge configuration have integrated, fast free-wheeling diodes and are free of crossover current. The logic is supplied either separately with 5 V or taken from the motor supply voltage by way of a series resistor and an integrated Z-diode. The device can be driven directly by a microprocessor with the possibility of all modes from full step through half step to mini step.

Pin Configuration
(top view)

TCA 3727



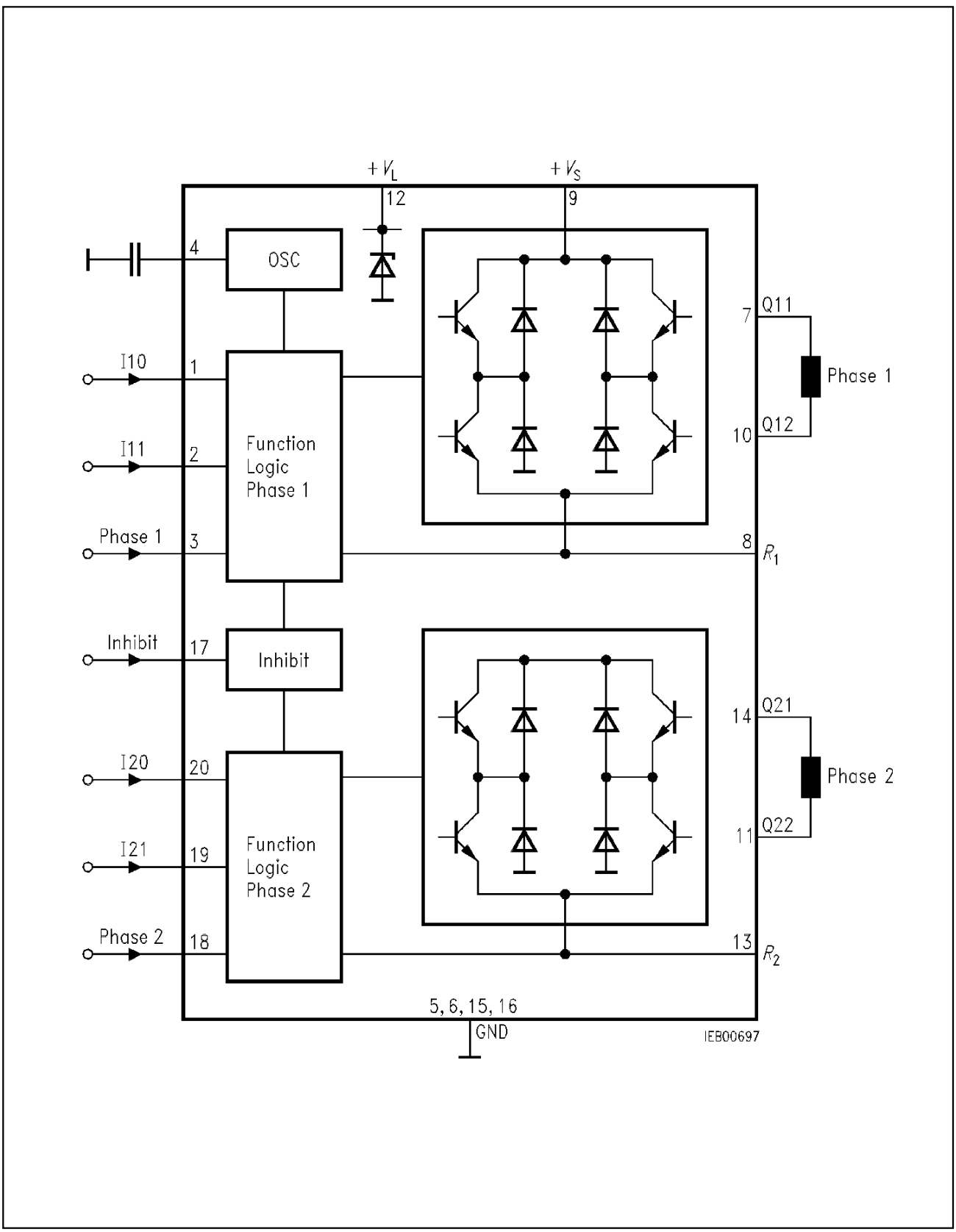
TCA 3727 G



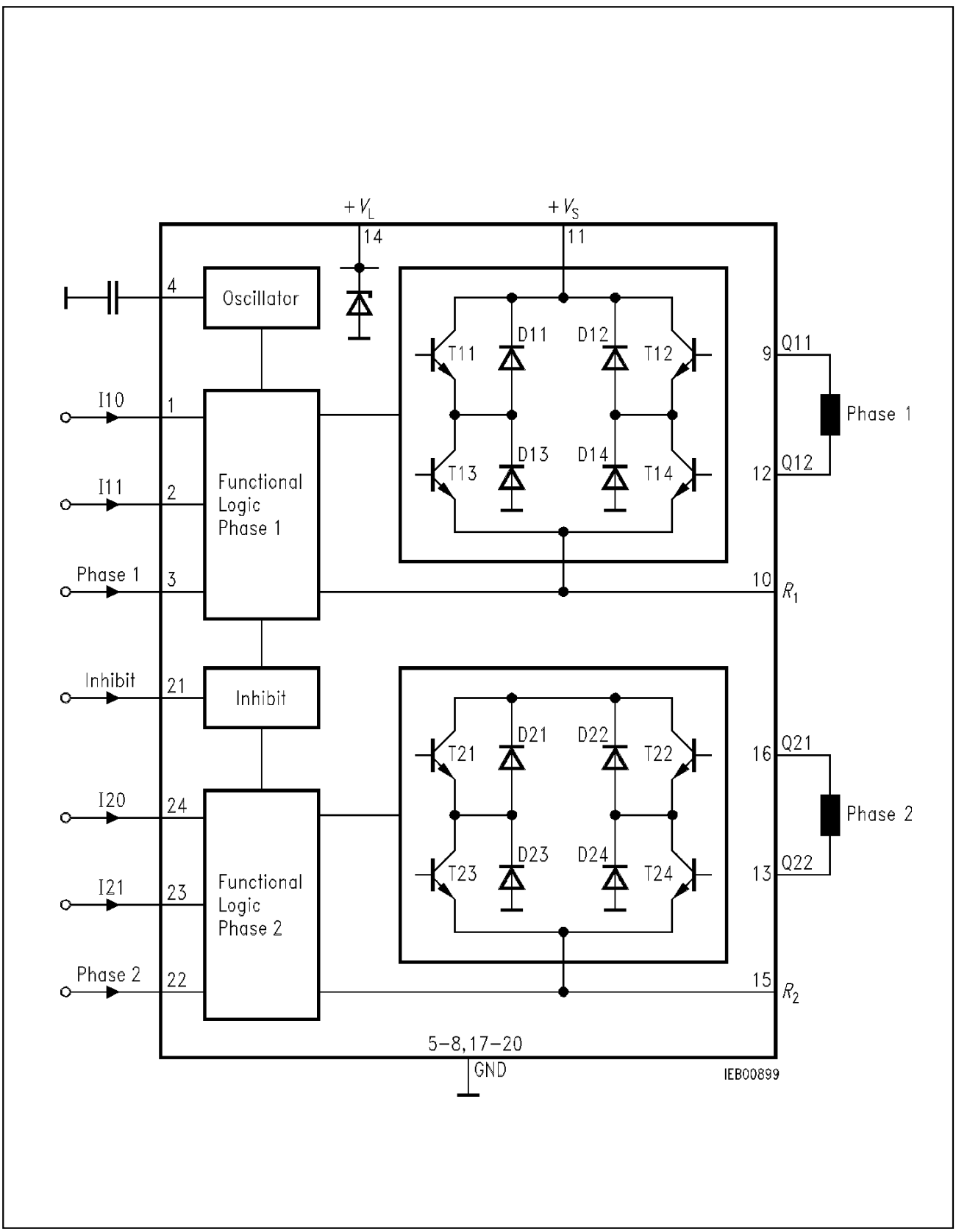
Pin Definitions and Functions

<table>
<tr><th>Pin</th><th>Function</th></tr>
<tr><td>1, 2, 19, 20
(1, 2, 23, 24) [1)]</td><td>Digital control inputs IX0, IX1 for the magnitude of the current of the particular phase.
<table>
<tr><th>IX1</th><th>IX0</th><th>Phase current</th><th>Example of motor status</th></tr>
<tr><td>H</td><td>H</td><td>0</td><td>No current</td></tr>
<tr><td>H</td><td>L</td><td>1/3 I_{max}</td><td>Hold</td></tr>
<tr><td>L</td><td>H</td><td>2/3 I_{max}</td><td>Normal mode</td></tr>
<tr><td>L</td><td>L</td><td>I_{max}</td><td>Accelerate</td></tr>
</table>
typical I_{max} with R_{sense} = 1 Ω : 750 mA</td></tr>
<tr><td>3</td><td>Input Phase 1; controls the current through phase winding 1. On H-potential the phase current flows from Q11 to Q12, on L-potential in the reverse direction.</td></tr>
<tr><td>5, 6, 15, 16
(5, 6, 7, 8, 17, 18, 19, 20) [1)]</td><td>Ground; all pins are connected internally.</td></tr>
<tr><td>4</td><td>Oscillator; works at approx. 25 kHz if this pin is wired to ground across 2.2 nF.</td></tr>
<tr><td>8 (10) [1)]</td><td>Resistor R_1 for sensing the current in phase 1.</td></tr>
<tr><td>7, 10 (9, 12) [1)]</td><td>Push-pull outputs Q11, Q12 for phase 1 with integrated free-wheeling diodes.</td></tr>
<tr><td>9 (11) [1)]</td><td>Supply voltage; block to ground, as close as possible to the IC, with a stable electrolytic capacitor of at least 10 µF in parallel with a ceramic capacitor of 220 nF.</td></tr>
<tr><td>12 (14) [1)]</td><td>Logic supply voltage; either supply with 5 V or connect to + V_S across a series resistor. A Z-diode of approx. 7 V is integrated. In both cases block to ground directly on the IC with a stable electrolytic capacitor of 10 µF in parallel with a ceramic capacitor of 100 nF.</td></tr>
<tr><td>11, 14
(13, 16) [1)]</td><td>Push-pull outputs Q22, Q21 for phase 2 with integrated free wheeling diodes.</td></tr>
<tr><td>13 (15) [1)]</td><td>Resistor R_2 for sensing the current in phase 2.</td></tr>
<tr><td>17 (21) [1)]</td><td>Inhibit input; the IC can be put on standby by low potential on this pin. This reduces the current consumption substantially.</td></tr>
<tr><td>18 (22) [1)]</td><td>Input phase 2; controls the current flow through phase winding 2. On H-potential the phase current flows from Q21 to Q22, on L potential in the reverse direction.</td></tr>
</table>

1) TCA 3727 G only



Block Diagram
TCA 3727



Block Diagram
TCA 3727 G

Absolute Maximum Ratings

T_A = – 40 to 125 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	0	52	V	–
Logic supply voltage	V_L	0	6.5	V	Z-diode
Z-current of V_L	I_L	–	50	mA	–
Output current	I_Q	–	1	A	–
Ground current	I_{GND}	–	2	A	–
Logic inputs	V_{Ixx}	– 6	V_L + 0.3	V	I_{XX} ; Phase 1, 2; Inhibit
R_1 , R_2, oscillator input voltage	V_{RX}, V_{OSC}	– 0.3	V_L + 0.3	V	–
Diode currents to + V_S to ground	 I_{F+} I_{F-}	 – –	 1 1	 A A	 – –
Junction temperature	T_j T_j	– –	125 150	°C °C	– max. 10,000 h
Storage temperature	T_{stg}	50	125	°C	–

Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	5	50	V	–
Logic supply voltage	V_L	4.5	6.5	V	without series resistor
Case temperature	T_C	– 40	110	˚C	measured on pin 5 P_{diss} = 2 W
Output current	I_Q	–	1000	mA	–
Logic inputs	V_{IXX}	– 5	V_L	V	I_{XX} ; Phase 1, 2; Inhibit
Thermal resistances					
system-air	$R_{th\ SA}$	–	56	K/W	P-DIP-20-3
system-air (soldered on a 35 µm thick 20 cm² PC board copper area)	$R_{th\ SA}$	–	40	K/W	P-DIP-20-3
system-case	$R_{th\ SC}$	–	18	K/W	measured on pin 5 P-DIP-20-3
system-air	$R_{th\ SA}$	–	75	K/W	P-DSO-24-3
system-air (soldered on a 35 µm thick 20 cm² PC board copper area)	$R_{th\ SA}$	–	50	K/W	P-DSO-24-3
system-case	$R_{th\ SC}$	–	15	K/W	measured on pin 5 P-DSO-24-3

Characteristics

V_S = 40 V; V_L = 5 V; – 25 ˚C ≤ T_j ≤ 125 ˚C

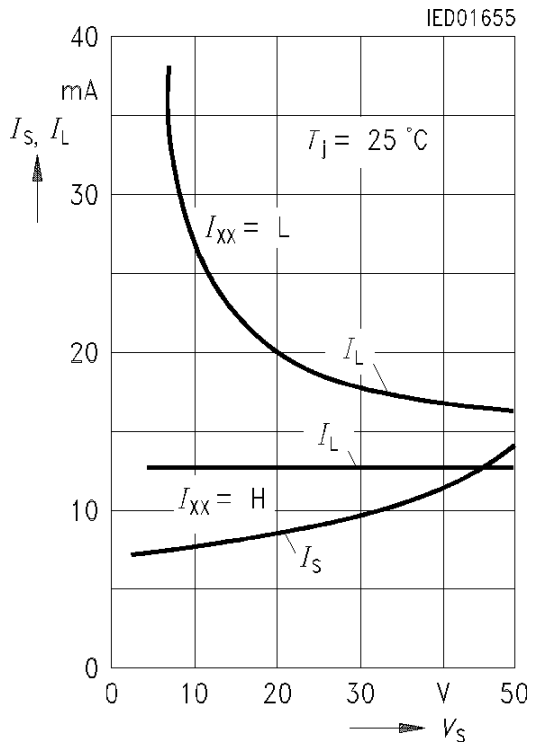
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current Consumption						
from + V_S	I_S	–	0.2	0.5	mA	V_{inh} = L
from + V_S	I_S	–	16	20	mA	V_{inh} = H $I_{Q1/2}$ = 0, I_{XX} = L
from + V_L	I_L	–	1.7	3.0	mA	V_{inh} = L
from + V_L	I_L	–	18	25	mA	V_{inh} = H $I_{Q1/2}$ = 0, I_{XX} = L
Oscillator						
Output charging current	I_{OSC}	–	110	–	µA	
Charging threshold	V_{OSCL}	–	1.3	–	V	
Discharging threshold	V_{OSCH}	–	2.3	–	V	
Frequency	f_{OSC}	18	25	35	kHz	C_{OSC} = 2.2 nF
Phase Current Selection (R_1; R_2) Current Limit Threshold						
No current	V_{sense}	–	0	–	mV	IX0 = H; IX1 = H
Hold	V_{sense}	200	250	300	mV	IX0 = L; IX1 = H
Setpoint	V_{sense}	460	540	620	mV	IX0 = H; IX1 = L
Accelerate	V_{sense}	740	825	910	mV	IX0 = L; IX1 = L
Logic Inputs (I_{X1} ; I_{X0} ; phase x; inhibit)						
Threshold (I_{XX}, Phase X)	V_I	1.4 (H→L)	–	2.3 (L→H)	V	–
L-input current (logic inputs)	I_{ILInh}	– 10	–	–	µA	V_I = 1.4 V
L-input current (i_{X1}, i_{X0}, phase)	I_{IL}	– 100	–	–	µA	V_I = 0 V
H-input current	I_{IH}	–	–	10	µA	V_I = 5 V
Standby Cutout (inhibit)						
Threshold	V_{Inh} (L→H)	2.0	3.0	4.0	V	V_L = 5 V
Threshold	V_{Inh} (H→L)	1.7	2.3	2.9	V	V_L = 5 V
Hysteresis	V_{Inhhy}	0.3	0.7	1.1	V	V_L = 5 V
Internal Z-Diode						
Z-voltage	V_{LZ}	6.5	7.4	8.2	V	I_L = 50 mA

Characteristics (cont'd)

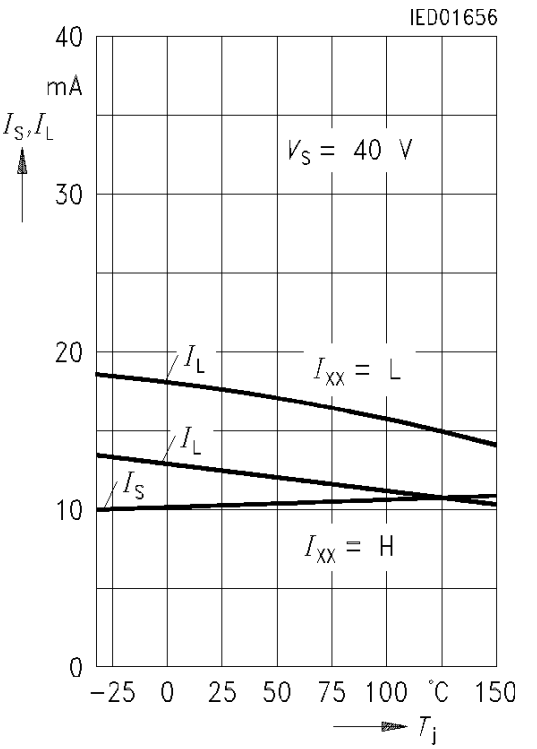
V_S = 40 V; V_L = 5 V; – 25 °C ≤ T_j ≤ 125 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Power Outputs						
Diode Transistor Sink Pair (D13, T13; D14, T14; D23, T23; D24, T24)						
Saturation voltage	V_{satI}	–	0.3	0.6	V	I_Q = – 0.5 A
Saturation voltage	V_{satI}	–	0.5	1.0	V	I_Q = – 0.75 A
Reverse current	I_{RI}	–	–	300	µA	V_Q = 40 V
Forward voltage	V_{FI}	–	0.9	1.3	V	I_Q = 0.5 A
Forward voltage	V_{FI}	–	1.0	1.4	V	I_Q = 0.75 A
Diode Transistor Source Pair (D11, T11; D12, T12; D21, T21; D22, T22)						
Saturation voltage	V_{satuC}	–	0.9	1.2	V	I_Q = 0.5 A; charge
Saturation voltage	V_{satuD}	–	0.3	0.7	V	I_Q = 0.5 A; discharge
Saturation voltage	V_{satuC}	–	1.1	1.4	V	I_Q = 0.75 A; charge
Saturation voltage	V_{satuD}	–	0.5	1.0	V	I_Q = 0.75 A; discharge
Reverse current	I_{Ru}	–	–	300	µA	V_Q = 0 V
Forward voltage	V_{Fu}	–	1.0	1.3	V	I_Q = – 0.5 A
Forward voltage	V_{Fu}	–	1.1	1.4	V	I_Q = – 0.75 A
Diode leakage current	I_{SL}	–	1	2	mA	I_F = – 0.75 A

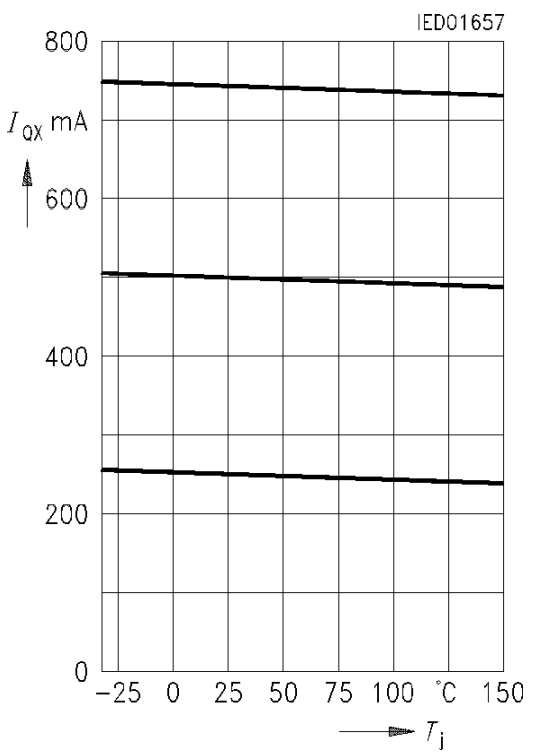
Quiescent Current I_S, I_L versus Supply Voltage V_S



Quiescent Current I_S, I_L versus Junction Temperature T_j



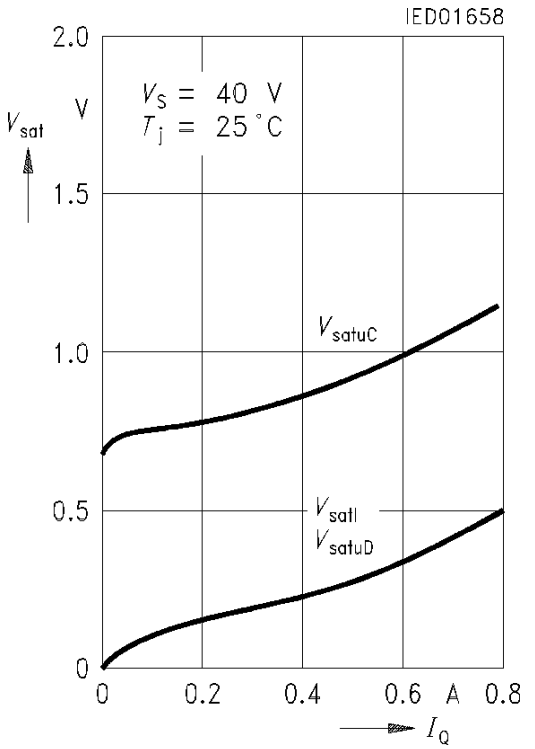
Output Current I_{QX} versus Junction Temperature T_j



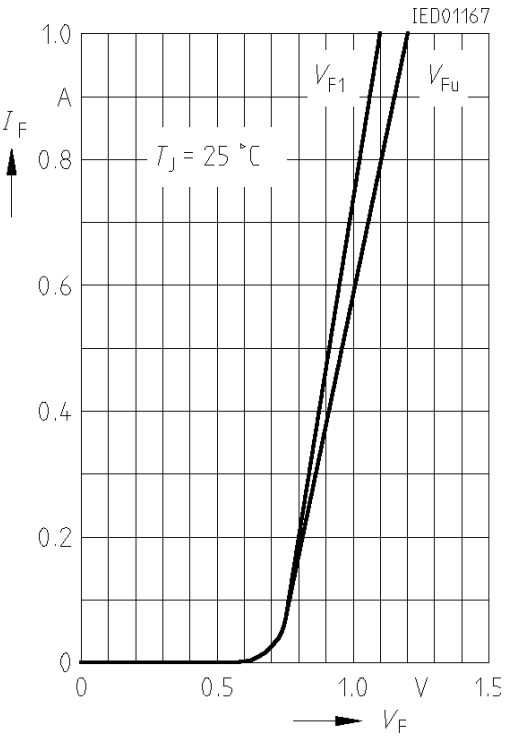
Operating Condition:

V_L = 5 V
V_{Inh} = H
C_{OSC} = 2.2 nF
R_{sense} = 1 Ω
Load: L = 10 mH
R = 2.4 Ω
f_{phase} = 50 Hz
mode: fullstep

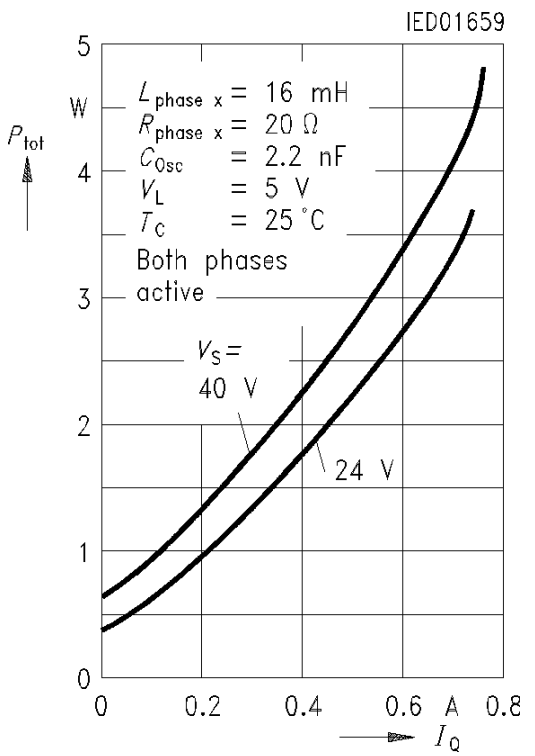
Output Saturation Voltages V_{sat} versus Output Current I_Q



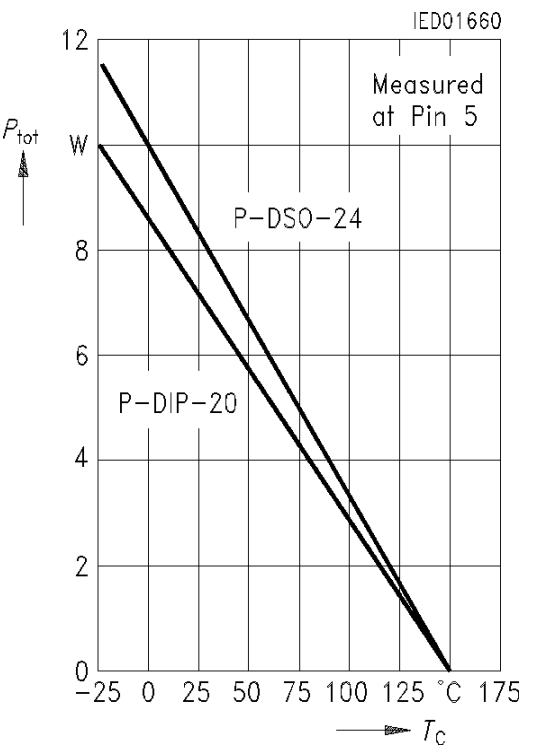
Forward Current I_F of Free-Wheeling Diodes versus Forward Voltages V_F



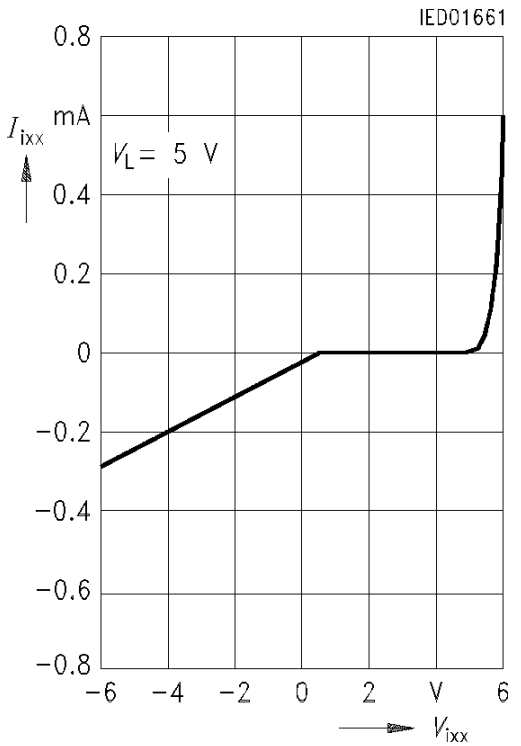
Typical Power Dissipation P_{tot} versus Output Current I_Q (Non Stepping)



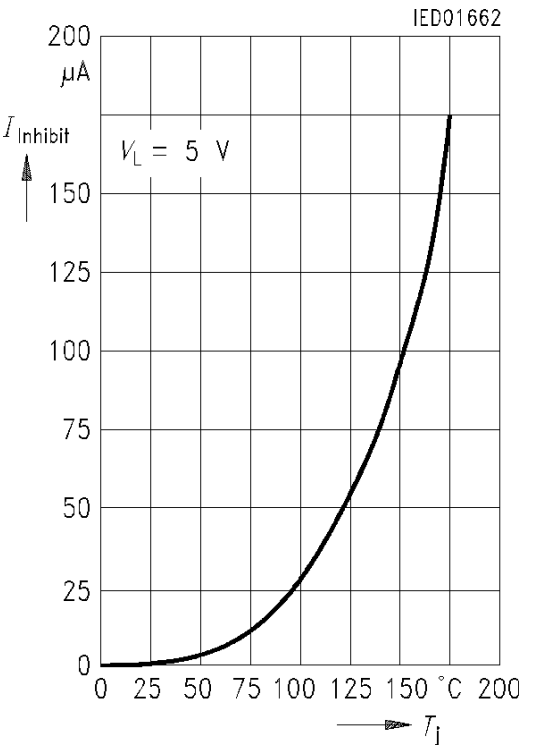
Permissible Power Dissipation P_{tot} versus Case Temperature T_C



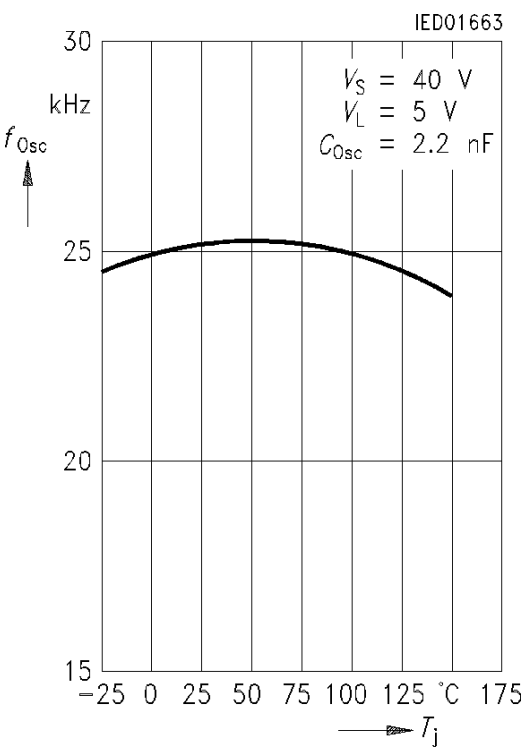
Input Characteristics of I_{xx}, Phase X, Inhibit

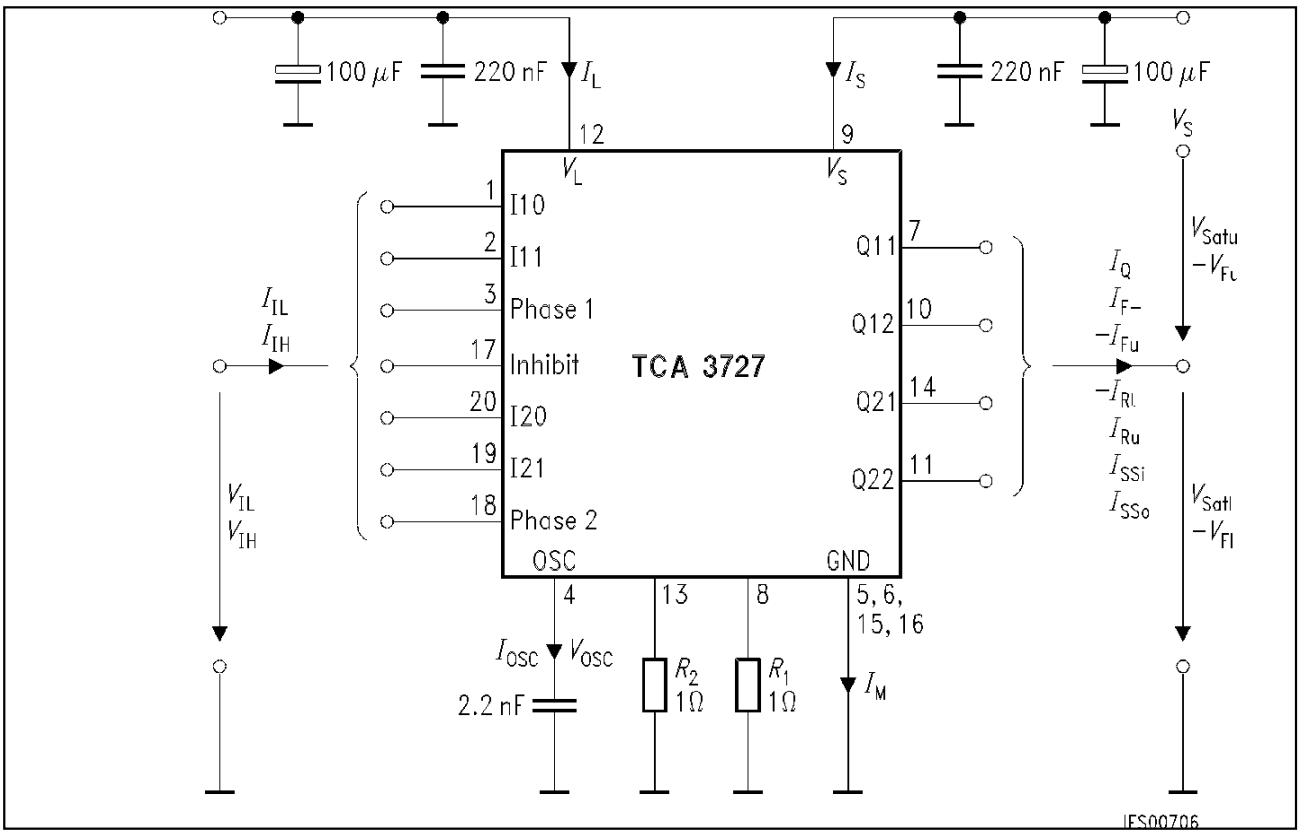


Input Current of Inhibit versus Junction Temperature T_j

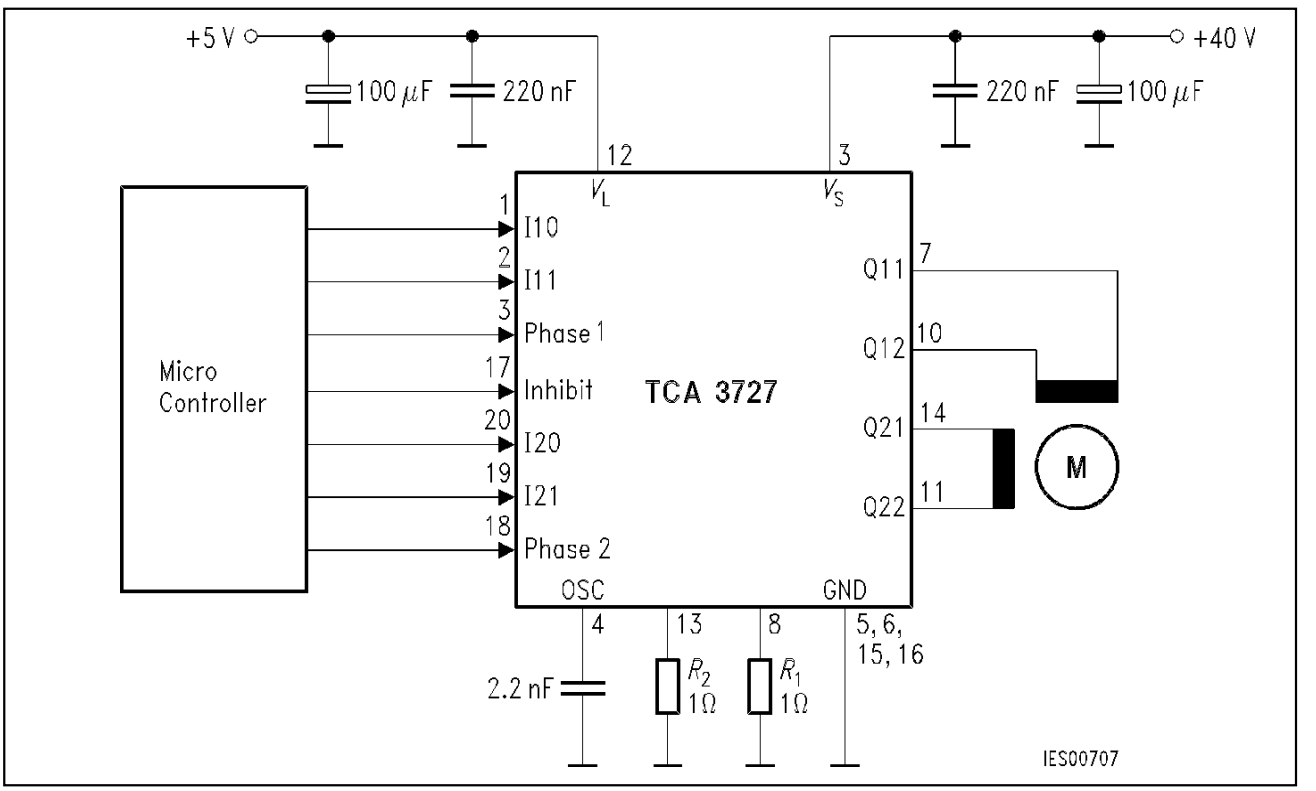


Oscillator Frequency f_{osc} versus Junction Temperature T_j

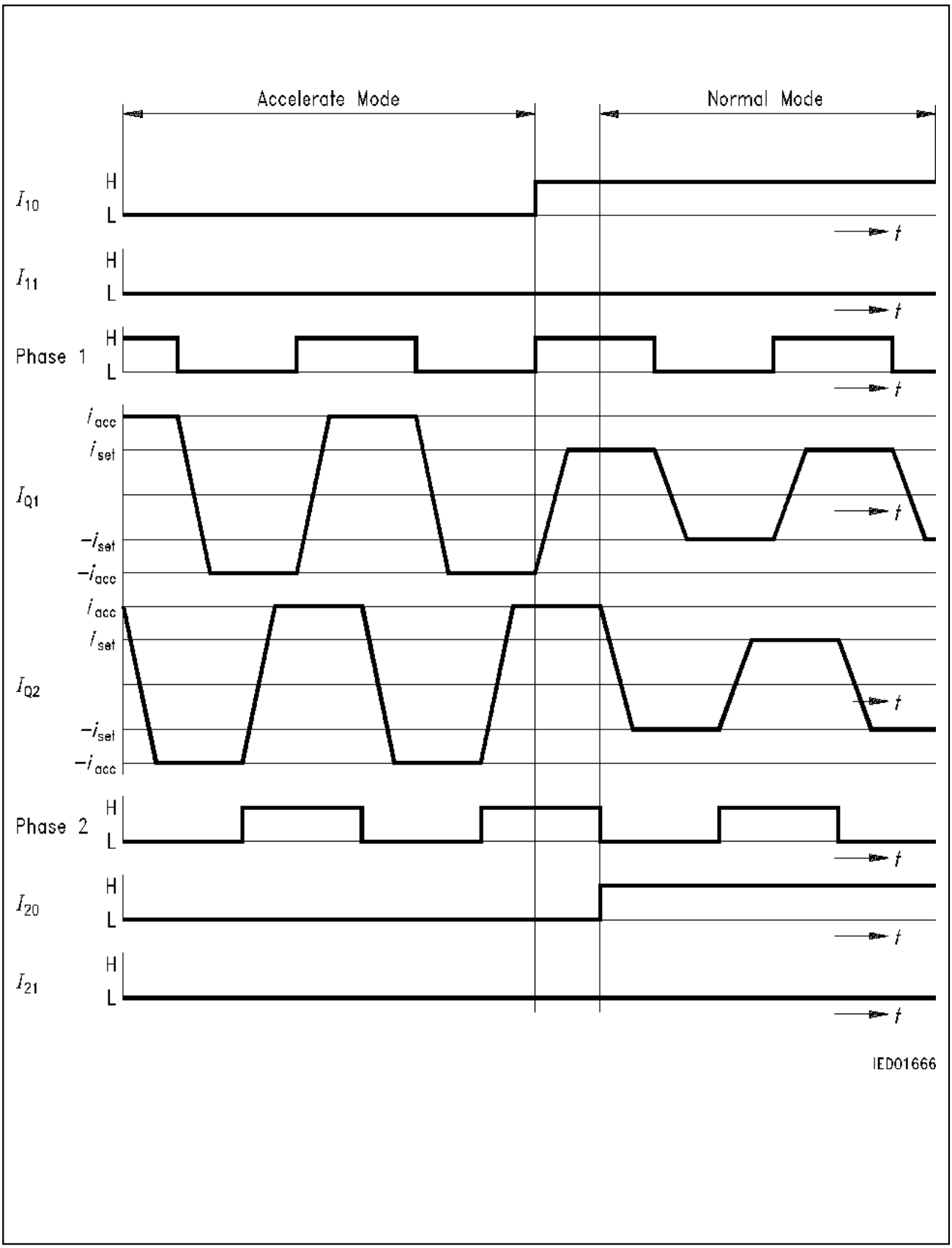




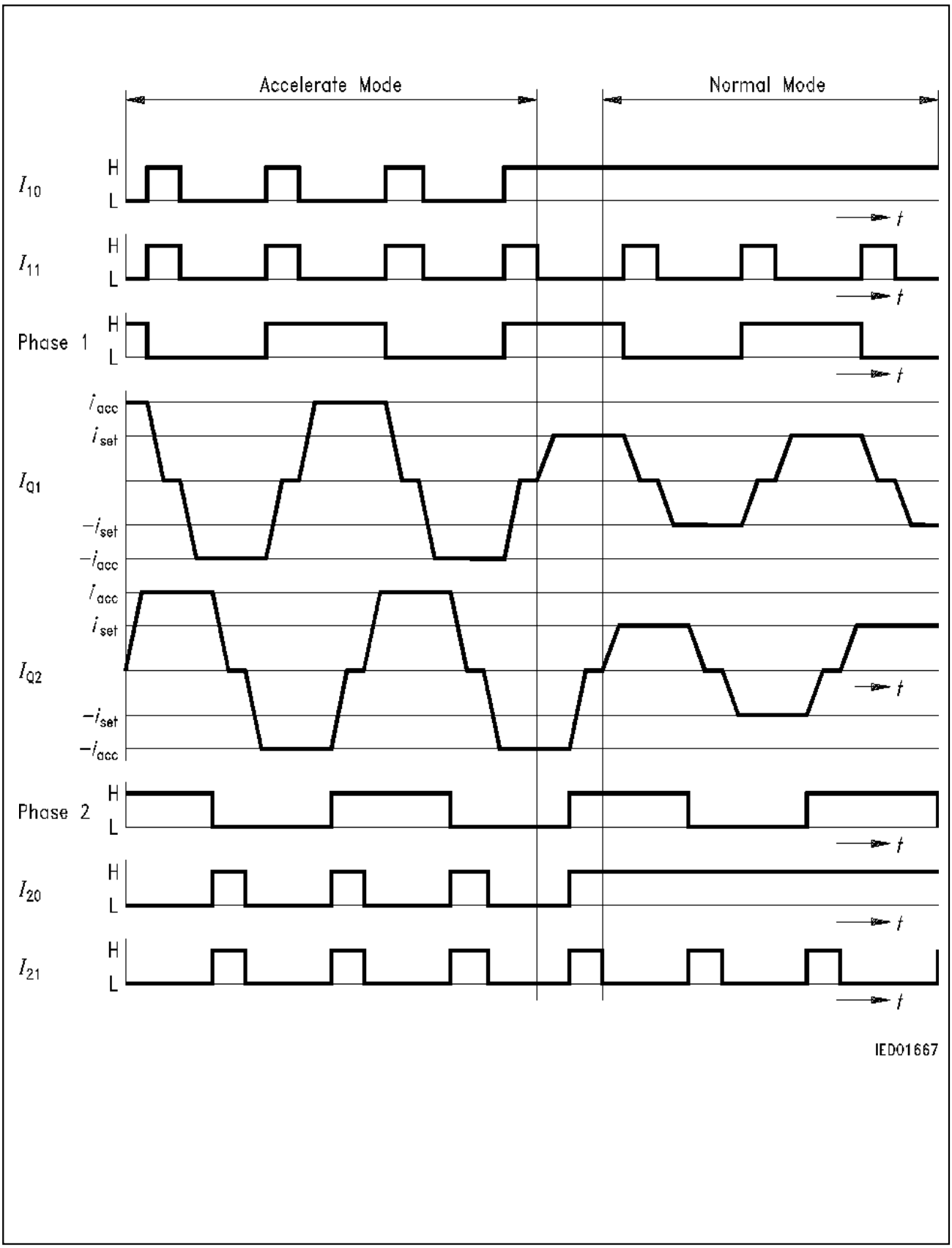
Test Circuit



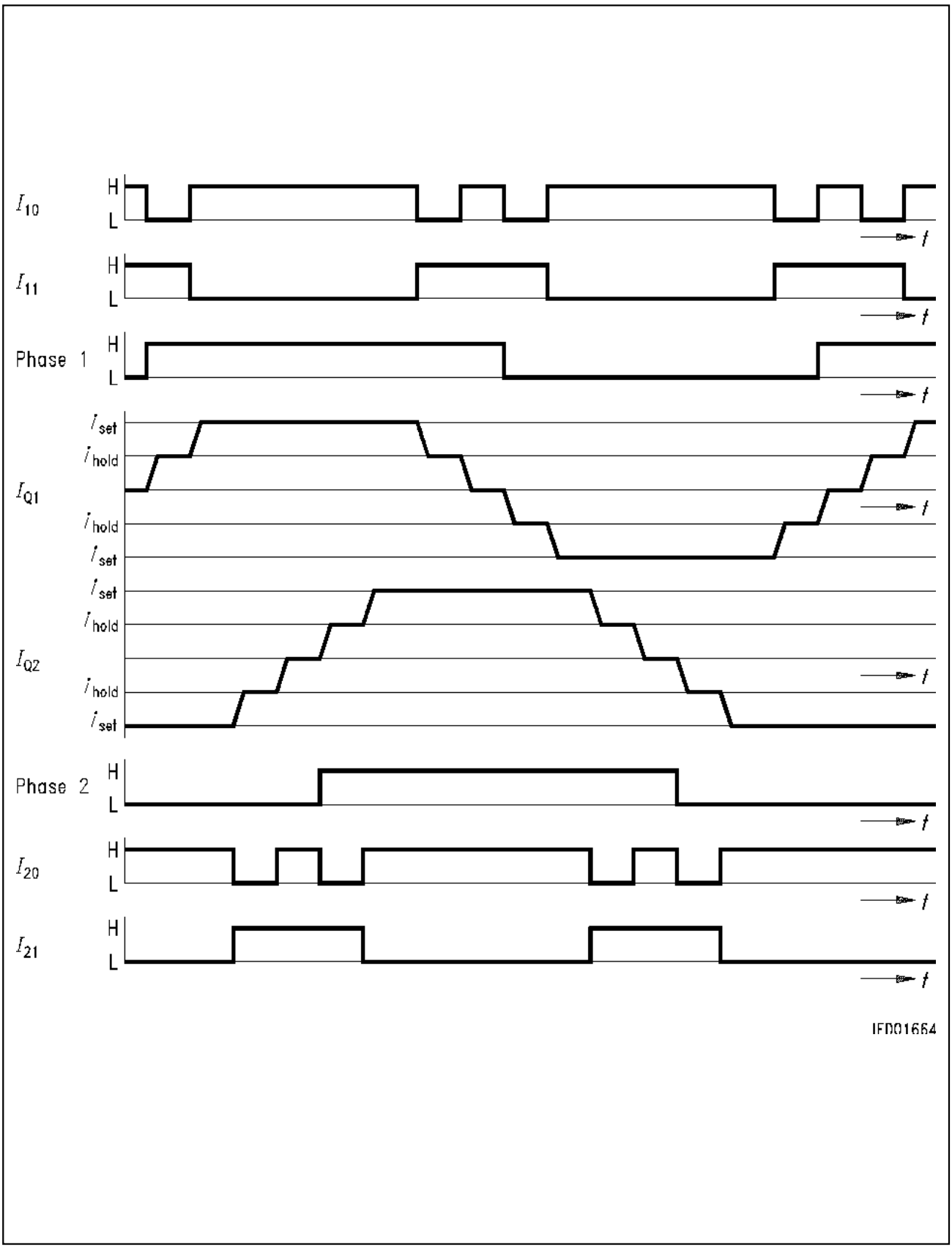
Application Circuit



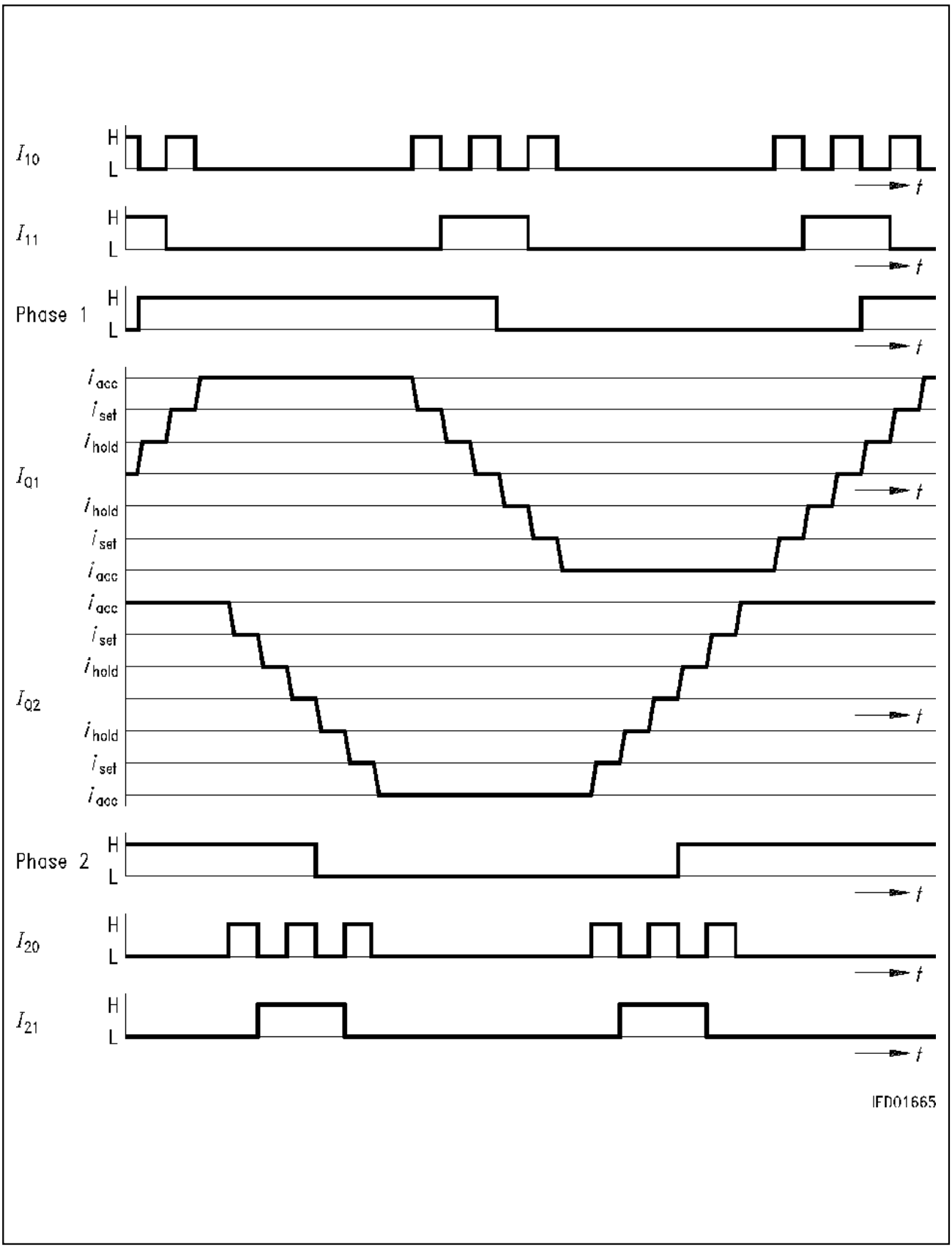
Full-Step Operation



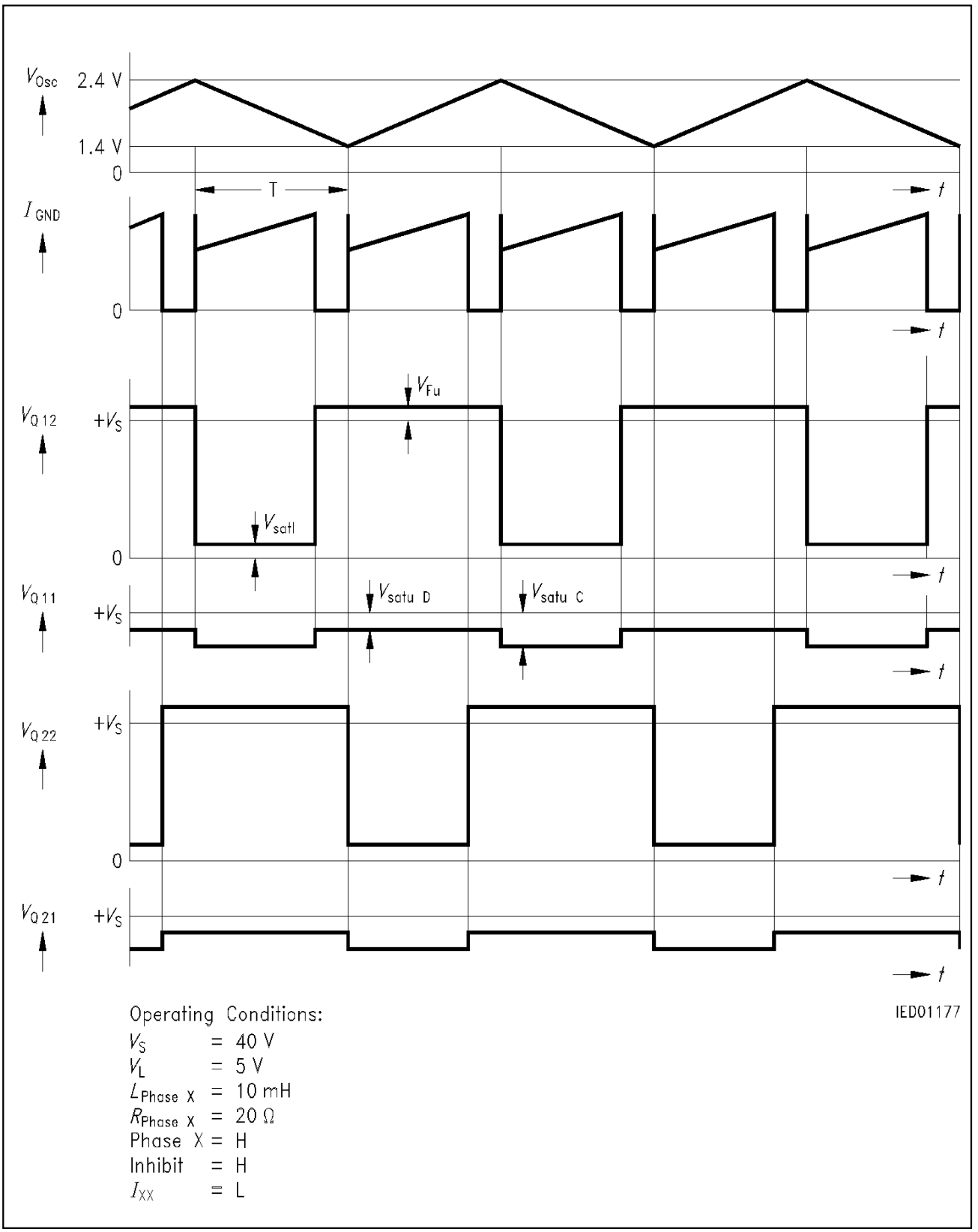
Half-Step Operation



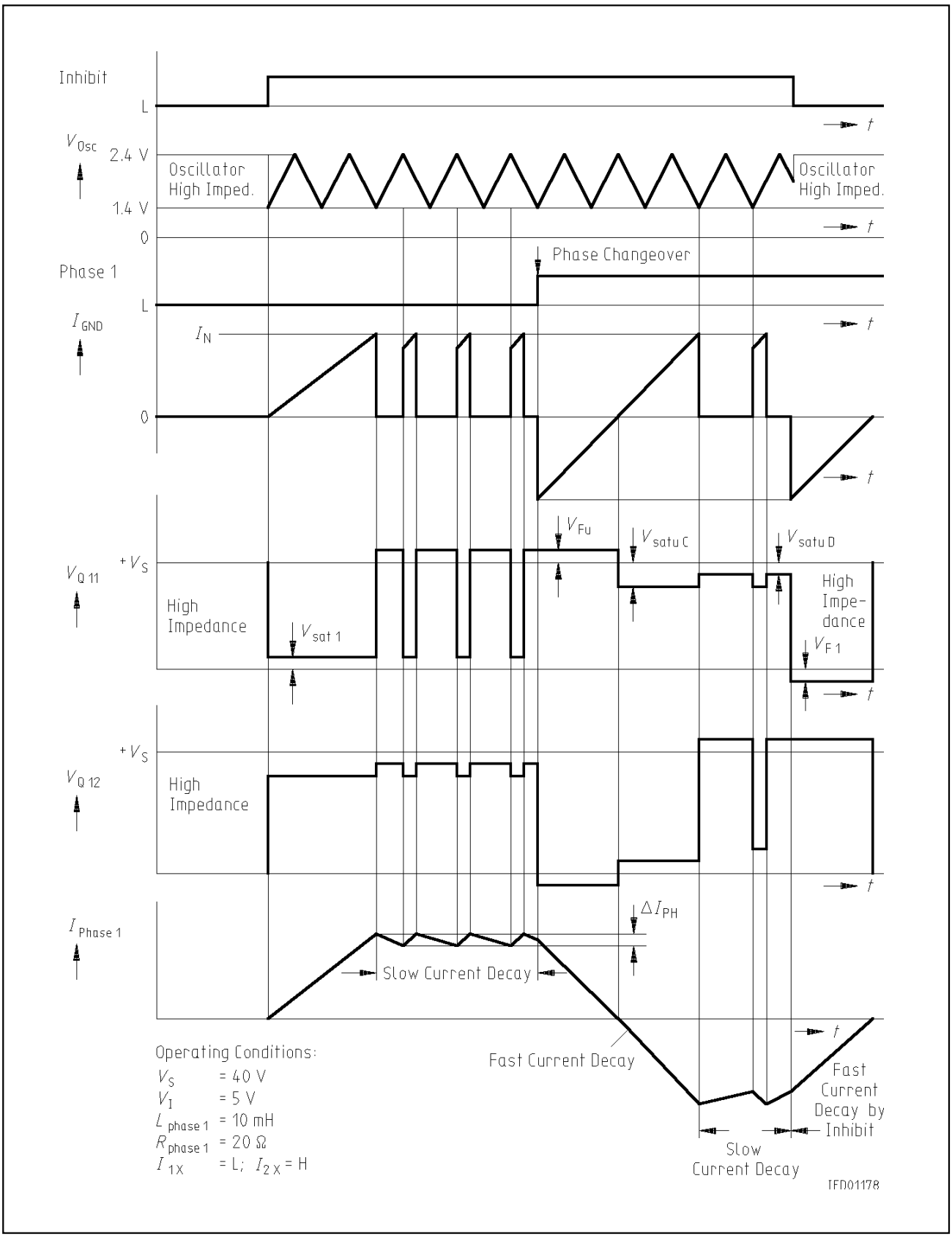
Quarter-Step Operation



Mini-Step Operation



Current Control



Phase Reversal and Inhibit

Calculation of Power Dissipation

The total power dissipation P_{tot} is made up of

saturation losses P_{sat} (transistor saturation voltage and diode forward voltages),
quiescent losses P_q (quiescent current times supply voltage) and
switching losses P_s (turn-ON / turn-OFF operations).

The following equations give the power dissipation for chopper operation without phase reversal. This is the worst case, because full current flows for the entire time and switching losses occur in addition.

$$P_{tot} = 2 \times P_{sat} + P_q + 2 \times P_s$$

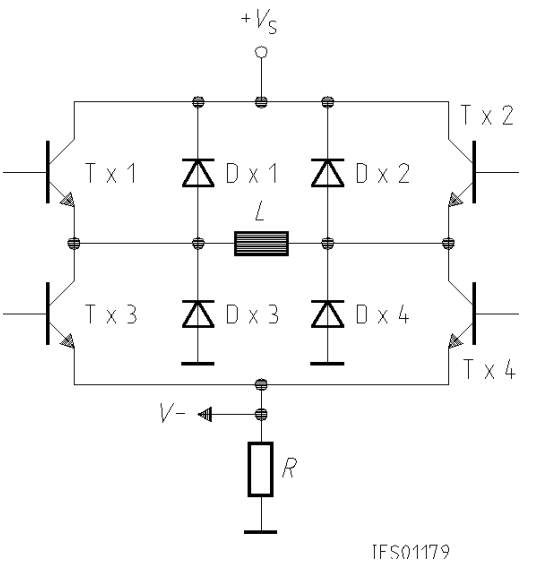
where

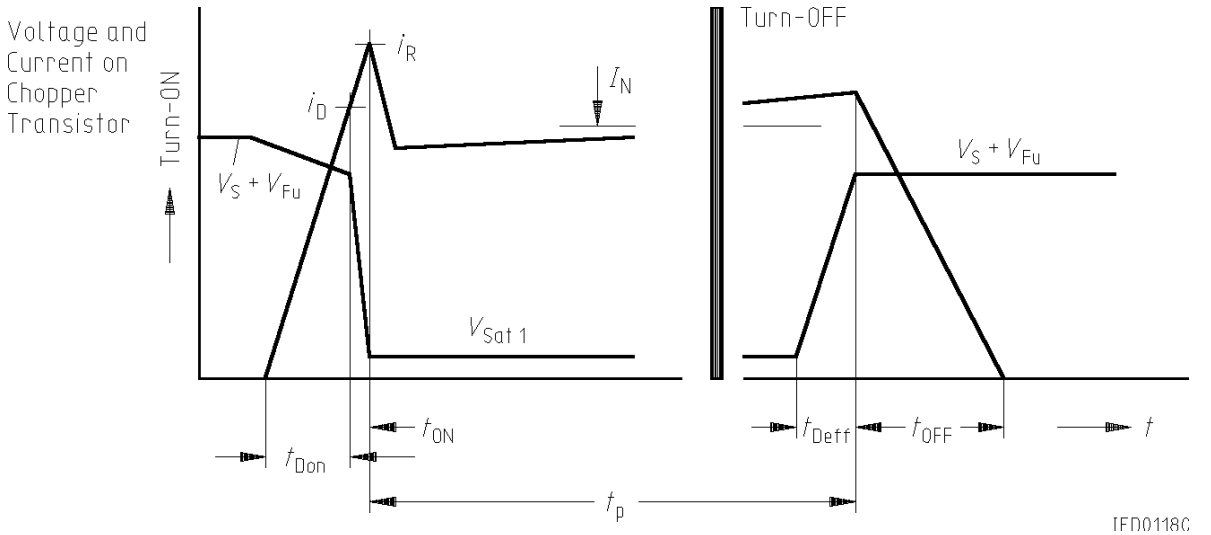
$$P_{sat} \cong I_N \{ V_{sat1} \times d + V_{Fu} (1 - d) + V_{satuC} \times d + V_{satuD} (1 - d) \}$$

$$P_q = I_q \times V_S + I_L \times V_L$$

$$P_S \cong \frac{V_S}{T} \left\{ \frac{i_D \times t_{DON}}{2} + \frac{i_D + i_R \times t_{ON}}{4} + \frac{I_N}{2} t_{DOFF} + t_{OFF} \right\}$$

I_N = nominal current (mean value)
I_q = quiescent current
i_D = reverse current during turn-on delay
i_R = peak reverse current
t_p = conducting time of chopper transistor
t_{ON} = turn-ON time
t_{OFF} = turn-OFF time
t_{DON} = turn-ON delay
t_{DOFF} = turn-OFFdelay
T = cycle duration
d = duty cycle t_p/T
V_{sat1} = saturation voltage of sink transistor (T3, T4)
V_{satuC} = saturation voltage of source transistor (T1, T2) during charge cycle
V_{satuD} = saturation voltage of source transistor (T1, T2) during discharge cycle
V_{Fu} = forward voltage of free-wheeling diode (D1, D2)
V_S = supply voltage
V_L = logic supply voltage
I_L = current from logic supply


+V_S
T x 1
D x 1
D x 2
T x 2
L
T x 3
D x 3
D x 4
T x 4
V-
R
IFS01179


Voltage and Current on Chopper Transistor
Turn-ON
i_R
i_D
I_N
$V_S + V_{Fu}$
$V_{Sat\,1}$
t_{Don}
t_{ON}
t_p
Turn-OFF
$V_S + V_{Fu}$
t_{Deff}
t_{OFF}
t
IFD01180

Application Hints

The TCA 3727 is intended to drive both phases of a stepper motor. Special care has been taken to provide high efficiency, robustness and to minimize external components.

Power Supply

The TCA 3727 will work with supply voltages ranging from 5 V to 50 V at pin V_S. As the circuit operates with chopper regulation of the current, interference generation problems can arise in some applications. Therefore the power supply should be decoupled by a 0.22 µF ceramic capacitor located near the package. Unstabilized supplies may even afford higher capacities.

Current Sensing

The current in the windings of the stepper motor is sensed by the voltage drop across R_1 and R_2. Depending on the selected current internal comparators will turn off the sink transistor as soon as the voltage drop reaches certain thresholds (typical 0 V, 0.25 V, 0.5 V and 0.75 V); (R_1, R_2 = 1 Ω). These thresholds are neither affected by variations of V_L nor by variations of V_S.

Due to chopper control fast current rises (up to 10A/µs) will occure at the sensing resistors R_1 and R_2. To prevent malfunction of the current sensing mechanism R_1 and R_2 should be pure ohmic. The resistors should be wired to GND as directly as possible. Capacitive loads such as long cables (with high wire to wire capacity) to the motor should be avoided for the same reason.

Synchronizing Several Choppers

In some applications synchrone chopping of several stepper motor drivers may be desireable to reduce acoustic interference. This can be done by forcing the oscillator of the TCA 3727 by a pulse generator overdriving the oscillator loading currents (approximately $\geq \pm$ 100 µA). In these applications low level should be between 0 V and 1 V while high level should be between 2.6 V and V_L.

Optimizing Noise Immunity

Unused inputs should always be wired to proper voltage levels in order to obtain highest possible noise immunity.

To prevent crossconduction of the output stages the TCA 3727 uses a special break before make timing of the power transistors. This timing circuit can be triggered by short glitches (some hundred nanoseconds) at the Phase inputs causing the output stage to become high resistive during some microseconds. This will lead to a fast current decay during that time. To achieve maximum current accuracy such glitches at the Phase inputs should be avoided by proper control signals.

Thermal Shut Down

To protect the circuit against thermal destruction, thermal shut down has been implemented. To provide a warning in critical applications, the current of the sensing element is wired to input Inhibit. Before thermal shut down occures Inhibit will start to pull down by some hundred microamperes. This current can be sensed to build a temperature prealarm.

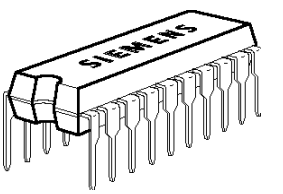
SIEMENS

2-Phase Stepper Motor Driver — TLE 4727

Preliminary Data — **Bipolar IC**

Features

- 2×0.7 amp. outputs
- Integrated driver, control logic and current control (chopper)
- Fast free-wheeling diodes
- Max. supply voltage 45 V
- Outputs free of crossover current
- Offset-phase turn-ON of output stages
- All outputs short-circuit proof
- 5 V output for logic supply
- Error-flag for overload, open load, overtemperature



P-DIP-20-3

Type	Ordering Code	Package
▼ TLE 4727	Q6700-A-9099	P-DIP-20-3

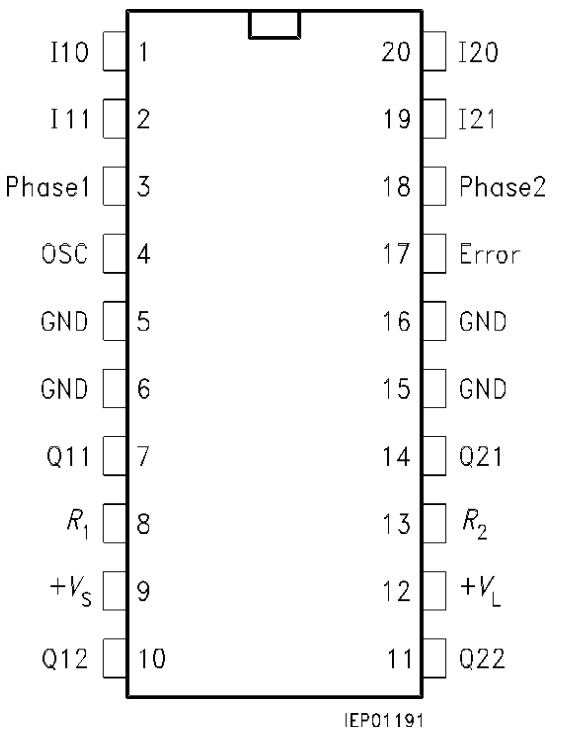
▼ New type

The TLE 4727 is a bipolar, monolithic IC for driving bipolar stepper motors, DC motors and other inductive loads that operate on constant current. The control logic and power output stages for two bipolar windings are integrated on a single chip which permits switched current control of motors with 0.7 A per phase at operating voltages up to 16 V.

The direction and value of current are programmable for each phase via separate control inputs. A common oscillator generates the timing for the current control and turn-on with phase offset of the two output stages. The two output stages in a full-bridge configuration include fast integrated free-wheeling diodes and are free of crossover current. The device can be driven directly by a microprocessor in several modes by programming phase direction and current control of each bridge independently.

A stabilized 5 V output allows the supply of external components up to 5 mA. With the error output the TLE 4727 signals malfunction of the device. Setting the control inputs high resets the error flag and by reactivating the bridges one by one the location of the error can be found.

Pin Configuration
(top view)

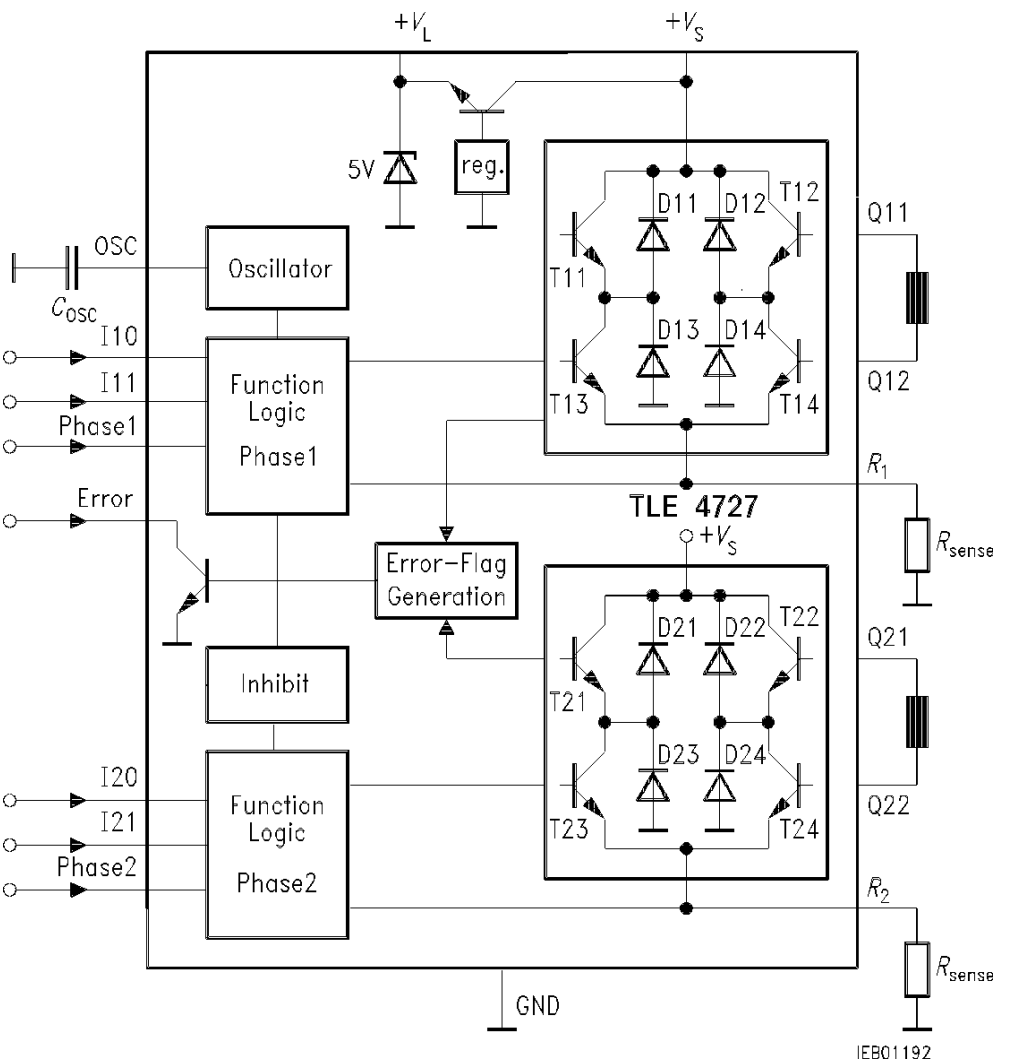


Pin Definitions and Functions

<table>
<tr><th>Pin</th><th>Function</th></tr>
<tr><td>1, 2, 19, 20</td><td>Digital control inputs IX0, IX1 for the magnitude of the current of the particular phase.

I_{set} = 500 mA with R_{Sense} = 1 Ω

<table>
<tr><th colspan="2">Current Control
IX1 IX0</th><th>Phase Current</th><th>Example of Motor Status</th></tr>
<tr><td>H</td><td>H</td><td>0</td><td>No current 1)</td></tr>
<tr><td>H</td><td>L</td><td>$0.14 \times I_{set}$</td><td>Hold</td></tr>
<tr><td>L</td><td>H</td><td>I_{set}</td><td>Normal mode</td></tr>
<tr><td>L</td><td>L</td><td>$1.4 \times I_{set}$</td><td>Accelerate</td></tr>
</table>
1) "No current" in both bridges inhibits the circuit andcurrent consumption will sink below 3 mA.</td></tr>
<tr><td>3</td><td>Input Phase 1; controls the current through phase winding 1. On H-potential the phase current flows from Q11 to Q12, on L-potential in the reverse direction.</td></tr>
<tr><td>4</td><td>Oscillator; works at typ. 25 kHz if this pin is wired to ground across 2.2 nF.</td></tr>
<tr><td>5, 6, 15, 16</td><td>Ground; all pins are connected at leadframe internally.</td></tr>
<tr><td>7, 10</td><td>Push-pull outputs Q11, Q12 for phase 1 with integrated free-wheeling diodes.</td></tr>
<tr><td>8</td><td>Resistor R_1 for sensing the current in phase 1.</td></tr>
<tr><td>9</td><td>Supply voltage; block to ground, as close as possible to the IC, with a stable electrolytic capacitor of at least 47 µF in parallel with a ceramic capacitor of 100 nF.</td></tr>
<tr><td>11, 14</td><td>Push-pull outputs Q22, Q21 for phase 2 with integrated free wheeling diodes.</td></tr>
<tr><td>12</td><td>Logic supply voltage; internally generated 5 V voltage for logic supply up to 5 mA; short circuit protected. Block to ground with a stable electrolytic capacitor of 4.7 µF</td></tr>
<tr><td>13</td><td>Resistor R_2 for sensing the current in phase 2.</td></tr>
<tr><td>17</td><td>Error output; signals with "low" the errors: open load or short circuit to ground of one or more outputs or short circuits of the load or overtemperature.</td></tr>
<tr><td>18</td><td>Input phase 2; controls the current flow through phase winding 2. On H-potential the phase current flows from Q21 to Q22, on L-potential in the reverse direction.</td></tr>
</table>



Block Diagram

Absolute Maximum Ratings

Temperature T_j = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	– 0.3	45	V	–
Error outputs	V_{Err} I_{Err}	– 0.3 –	45 3	V mA	– –
Logic supply voltage	V_L	– 0.3	6.5	V	–
Output current of V_L	I_L	– 5	1)	mA	1) Int. limited
Output current	I_Q	– 1	1	A	–
Ground current	I_{GND}	– 2	–	A	–
Logic inputs	V_{IXX}	– 15	15	V	IXX ; Phase X
Oscillator voltage	V_{Osc}	– 0.3	6	V	
R_1, R_2 input voltage	V_{RX}	– 0.3	5	V	
Junction temperature	T_j	–	125 150	°C °C	 Max. 1.000 h
Storage temperature	T_{stg}	– 50	125	°C	
Thermal resistance Junction ambient Junction ambient (soldered on a 35 µm thick 20 cm² PC board copper area) Junction case	 $R_{th\ ja}$ $R_{th\ ja}$ $R_{th\ jc}$	 – – –	 56 40 18	 K/W K/W K/W	 – – Measured on pin 5

Operating Range

Supply voltage	V_S	5	16	V	–
Current from logic supply	I_L	–	5	mA	–
Case temperature	T_C	– 40	110	°C	Measured on pin 5 P_{diss} = 2 W
Output current	I_Q	– 800	800	mA	
Logic inputs	V_{IXX}	– 5	6	V	IXX ; Phase 1, 2
Error output	V_{Err} I_{Err}	– 0	25 1	V mA	– –

Characteristics

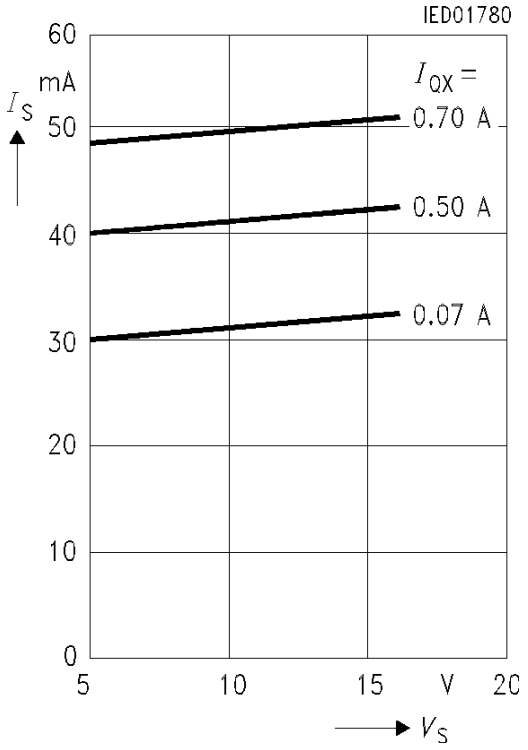
V_S = 6 to 16 V; T_j = – 40 to 130 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current Consumption						
from + V_S	I_S	1.0	2.0	3.0	mA	IXX = H
from + V_S	I_S	20	30	50	mA	IXX = L; $I_{Q1,2}$ = 0 A
Oscillator						
Output charging current	I_{Osc}	90	120	135	µA	
Charging threshold	V_{OscL}	0.8	1.3	1.9	V	
Discharging threshold	V_{OscH}	1.7	2.3	2.9	V	
Frequency	f_{Osc}	18	24	30	kHz	C_{OSC} = 2.2 nF
Phase Current (V_S = 9 to 16 V)						
Mode “no current”	I_Q	– 2	0	2	mA	IX0 = H; IX1 = H
Voltage threshold of current comparator at R_{sense} in mode:						
Hold	V_{ch}	40	70	100	mV	IX0 = L; IX1 = H
Setpoint	V_{cs}	450	500	570	mV	IX0 = H; IX1 = L
Accelerate	V_{ca}	630	700	800	mV	IX0 = L; IX1 = L
Logic Inputs (IX1 ; IX0 ; phase X)						
Threshold	V_I	1.2	1.7	2.2	V	–
Hysteresis	V_{IHy}	–	50	–	mV	
Low-input current	I_{IL}	– 10	– 1	1	µA	V_I = 1.2 V
Low-input current	I_{IL}	– 100	– 20	– 5	µA	V_I = 0 V
High-input current	I_{IH}	– 1	0	10	µA	V_I = 5 V
Error Output						
Saturation voltage	V_{ErrSat}	50	200	500	mV	I_{Err} = 1 mA
Leakage current	I_{ErrL}	–	–	10	µA	V_{Err} = 25 V
Logic Supply Output						
Output voltage	V_L	4.5	5	6.0	V	T_j < 150 °C 1 mA < I_L < 5 mA V_S = 6 to 45 V

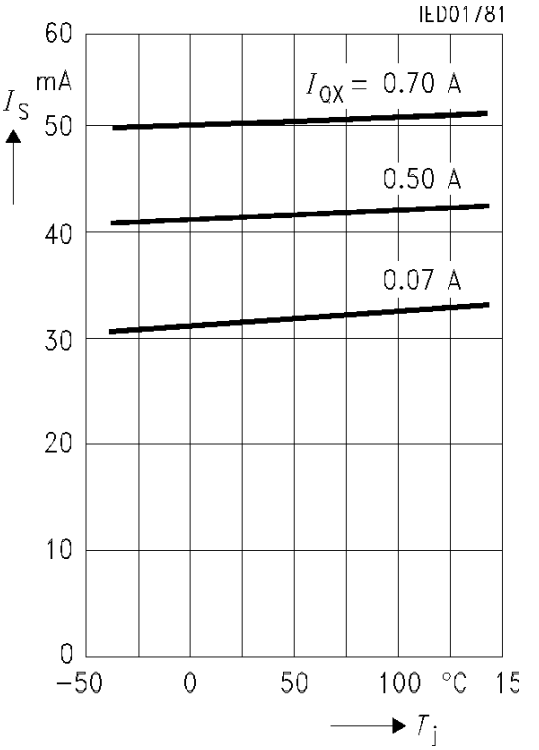
Characteristics (cont'd)
V_S = 6 to 16 V; T_j = – 40 to 130 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Thermal Protection						
Shutdown	T_{jsd}	140	150	160	°C	$I_{Q1,2}$ = 0 A
Prealarm	T_{jpa}	120	130	140	°C	V_{Err} = L
Delta	ΔT_j	10	20	30	K	$\Delta T_j = T_{jsd} - T_{jpa}$
Power Output Sink Diode Transistor Sink Pair (D13, T13; D14, T14; D23, T23; D24, T24)						
Saturation voltage	V_{satI}	0.1	0.4	0.6	V	I_Q = – 0.5 A
Saturation voltage	V_{satI}	0.2	0.5	0.8	V	I_Q = – 0.7 A
Reverse current	I_{RI}	500	1000	1500	µA	$V_S = V_Q$ = 40 V
Forward voltage	V_{FI}	0.6	0.95	1.25	V	I_Q = 0.5 A
Forward voltage	V_{FI}	0.7	1.0	1.3	V	I_Q = 0.7 A
Power Output Source Diode Transistor Source Pair (D11, T11; D12, T12; D21, T21; D22, T22)						
Saturation voltage; charge	V_{satuC}	0.6	1.1	1.3	V	I_Q = 0.5 A
Saturation voltage; discharge	V_{satuD}	0.1	0.4	0.7	V	I_Q = 0.5 A
Saturation voltage; charge	V_{satuC}	0.7	1.2	1.5	V	I_Q = 0.7 A
Saturation voltage; discharge	V_{satuD}	0.2	0.5	0.8	V	I_Q = 0.7 A
Reverse current	I_{Ru}	400	800	1200	µA	V_S = 40 V, V_Q = 0 V
Forward voltage	V_{Fu}	0.7	1.05	1.35	V	I_Q = – 0.5 A
Forward voltage	V_{Fu}	0.8	1.1	1.4	V	I_Q = – 0.7 A
Diode leakage current	I_{SL}	0	3	10	mA	I_F = – 0.7 A

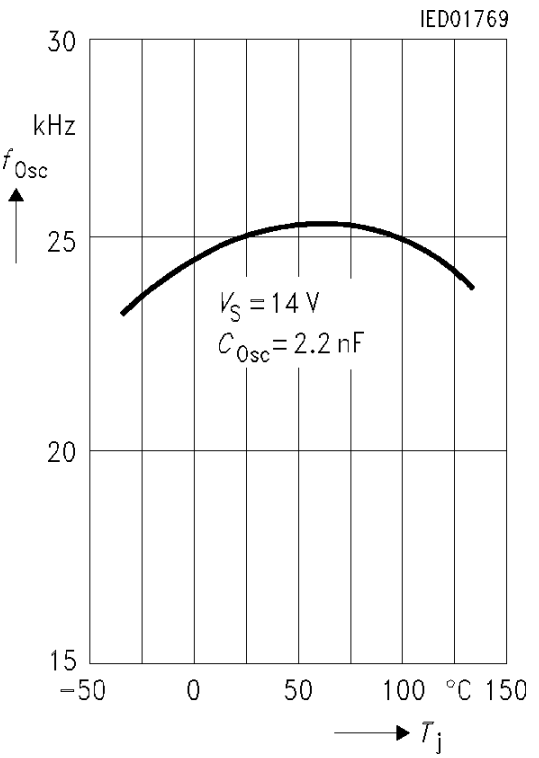
Quiescent Current I_S vs. Supply Voltage V_S;
bridges not chopping; T_j = 25 °C



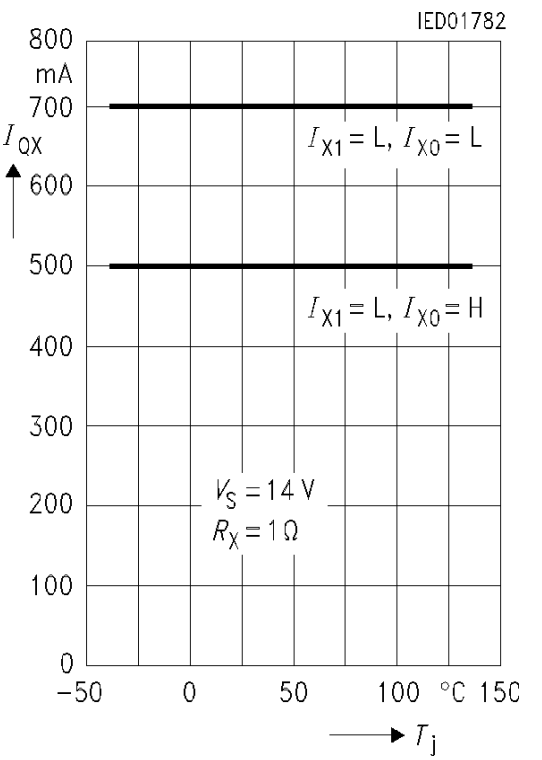
Quiescent Current I_S vs. Junction Temp. T_j;
bridges not chopping; V_S = 14 V



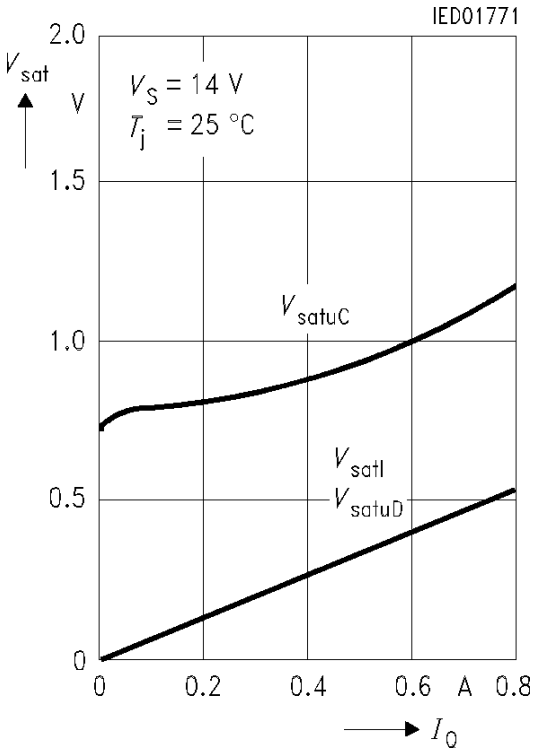
Oscillator Frequency f_{Osc} versus Junction Temperature T_j



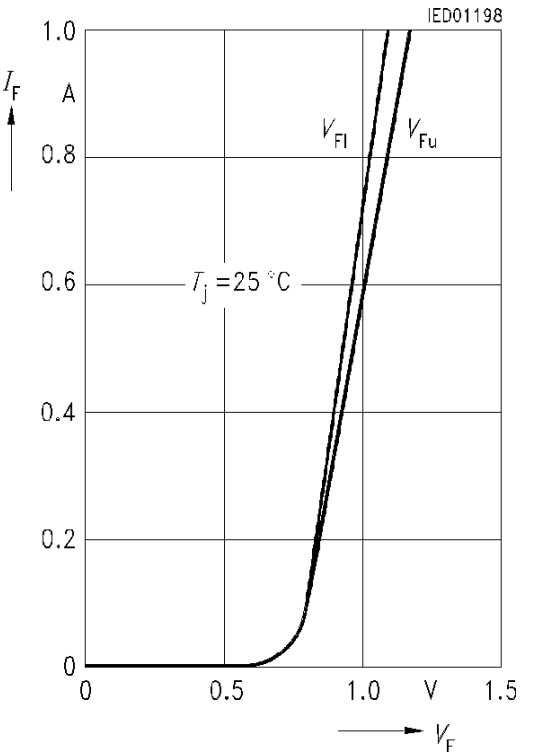
Output Current I_{QX} versus Junction Temperature T_j



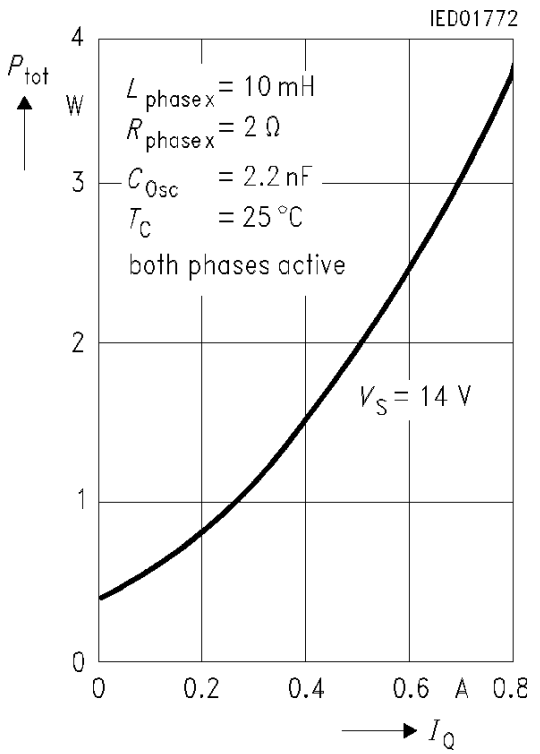
Output Saturation Voltages V_{sat} versus Output Current I_Q



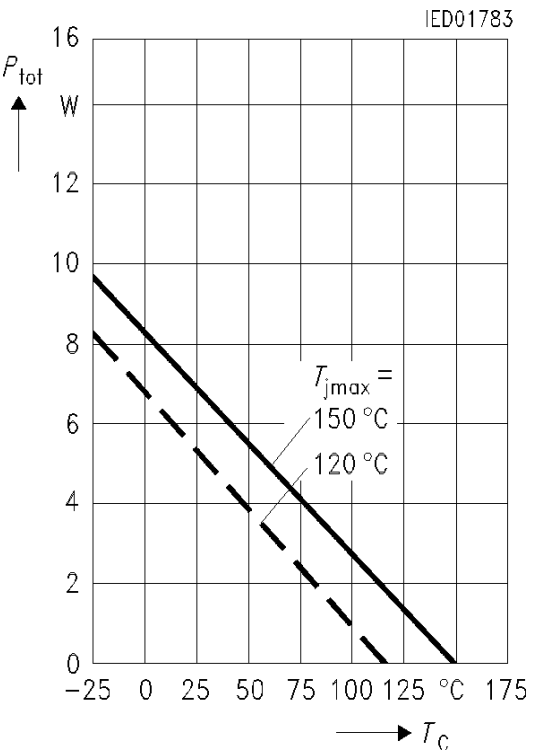
Forward Current I_F of Free-Wheeling Diodes versus Forward Voltages V_F



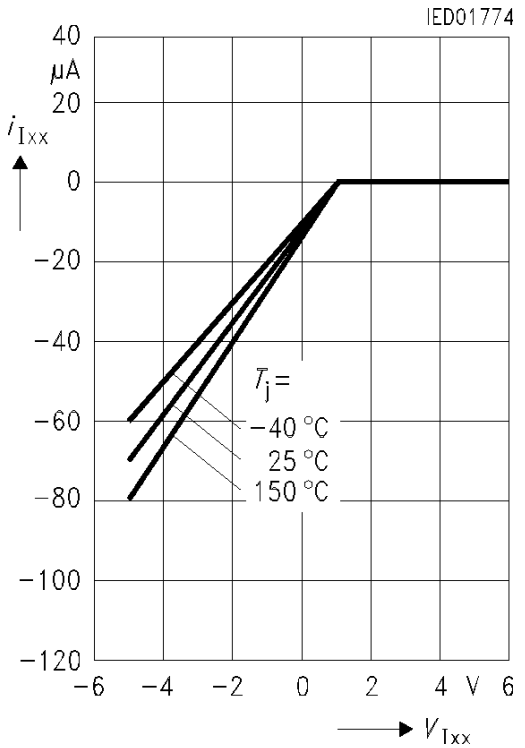
Typical Power Dissipation P_{tot} versus Output Current I_Q (non stepping)



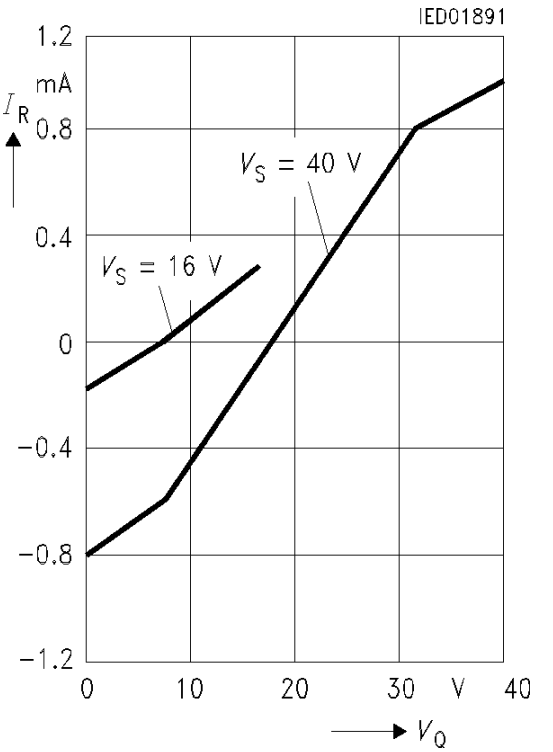
Permissible Power Dissipation P_{tot} versus Case Temp. T_C (measured at pin 5)



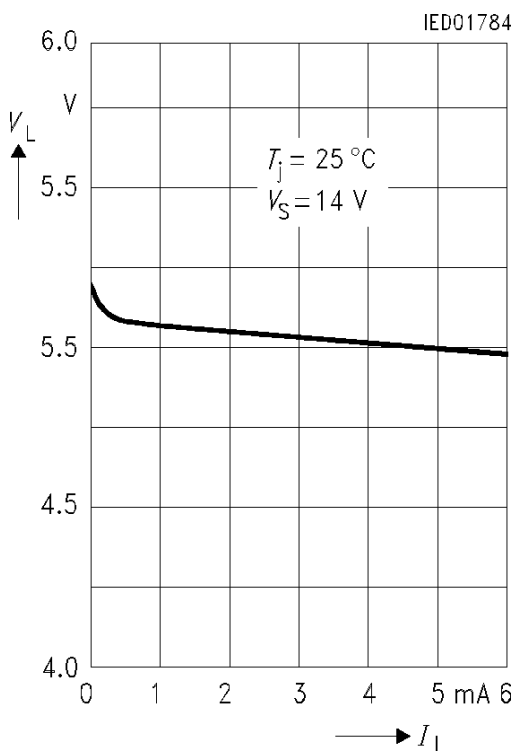
Input Characteristics of IXX , Phase X



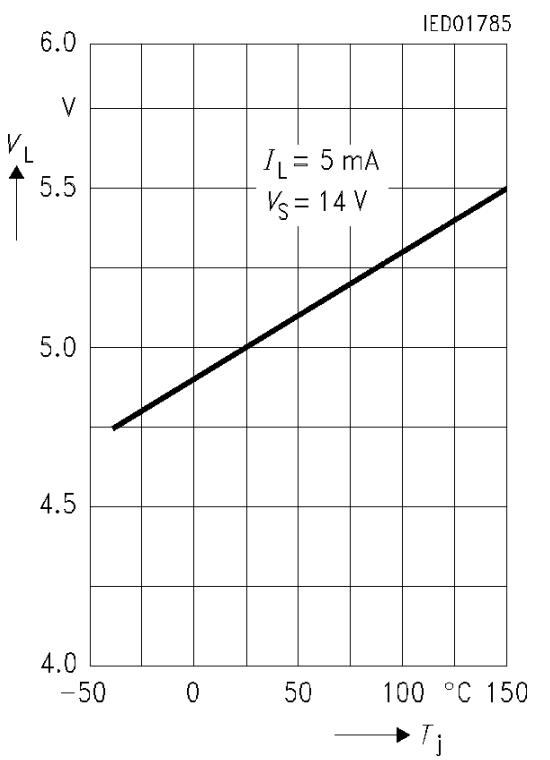
Output Leakage Current

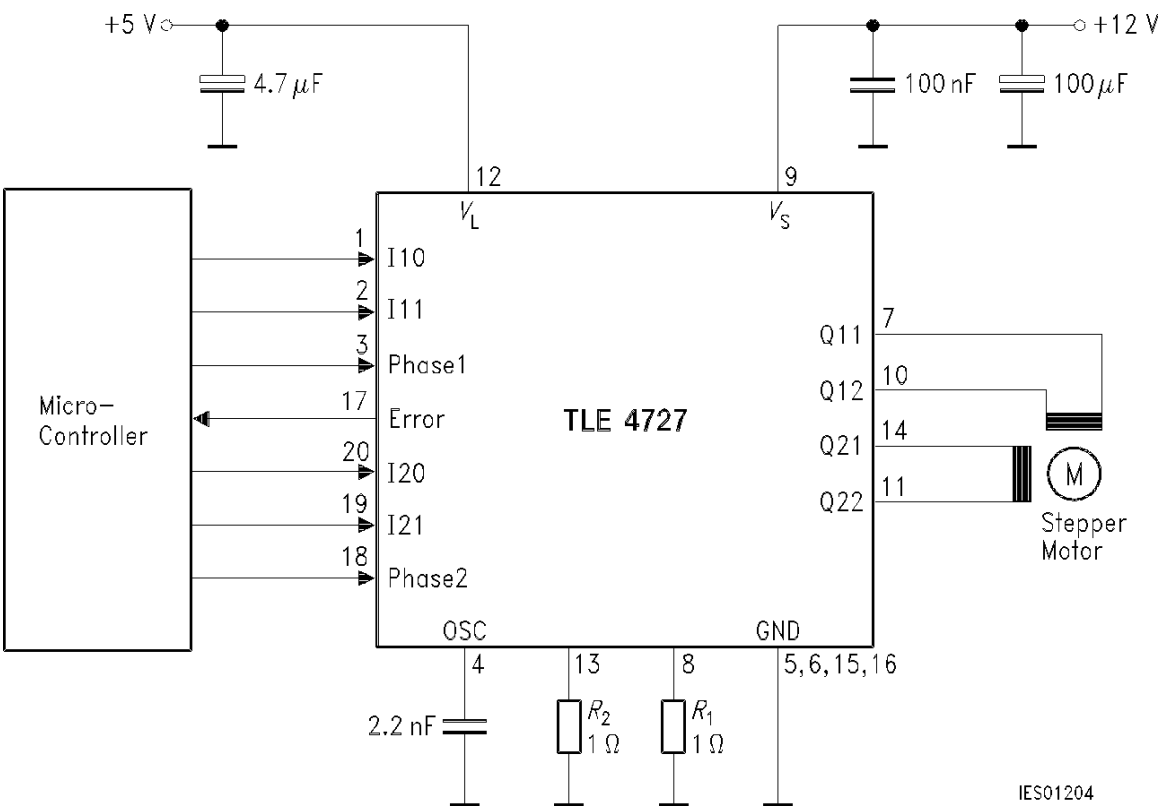


Logic Supply Output Voltage versus Output Current I_L

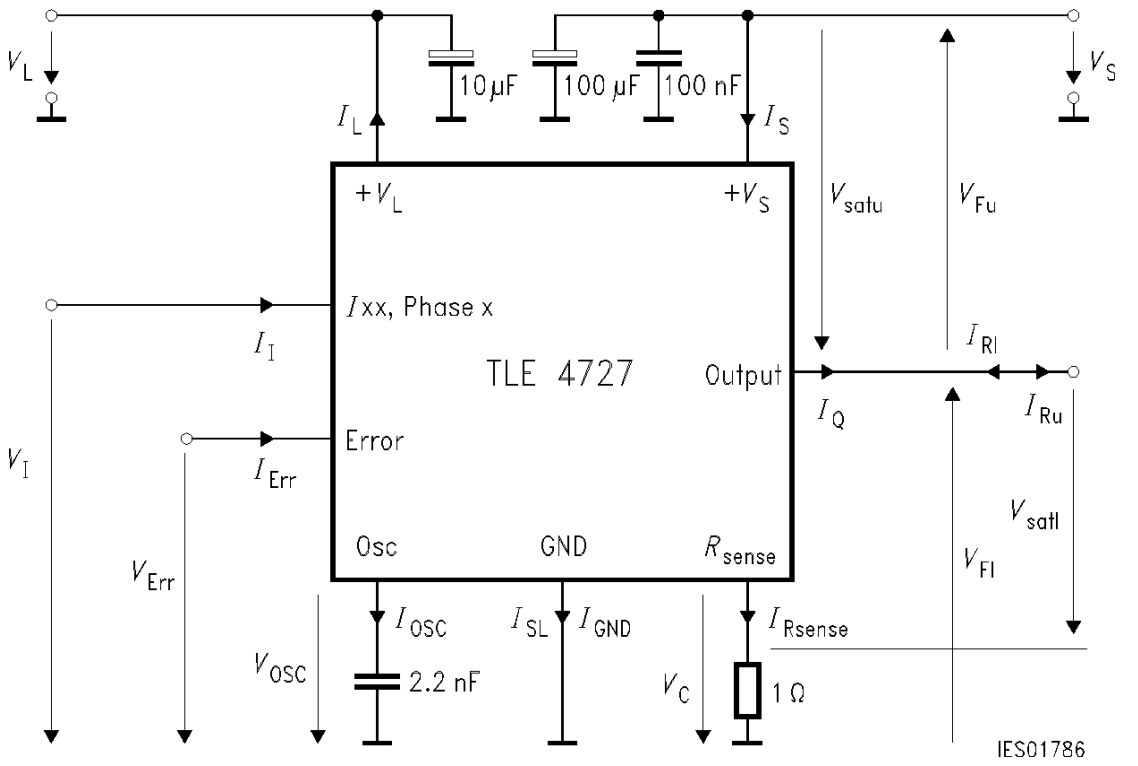


Logic Supply Output Voltage versus Junction Temperature T_j

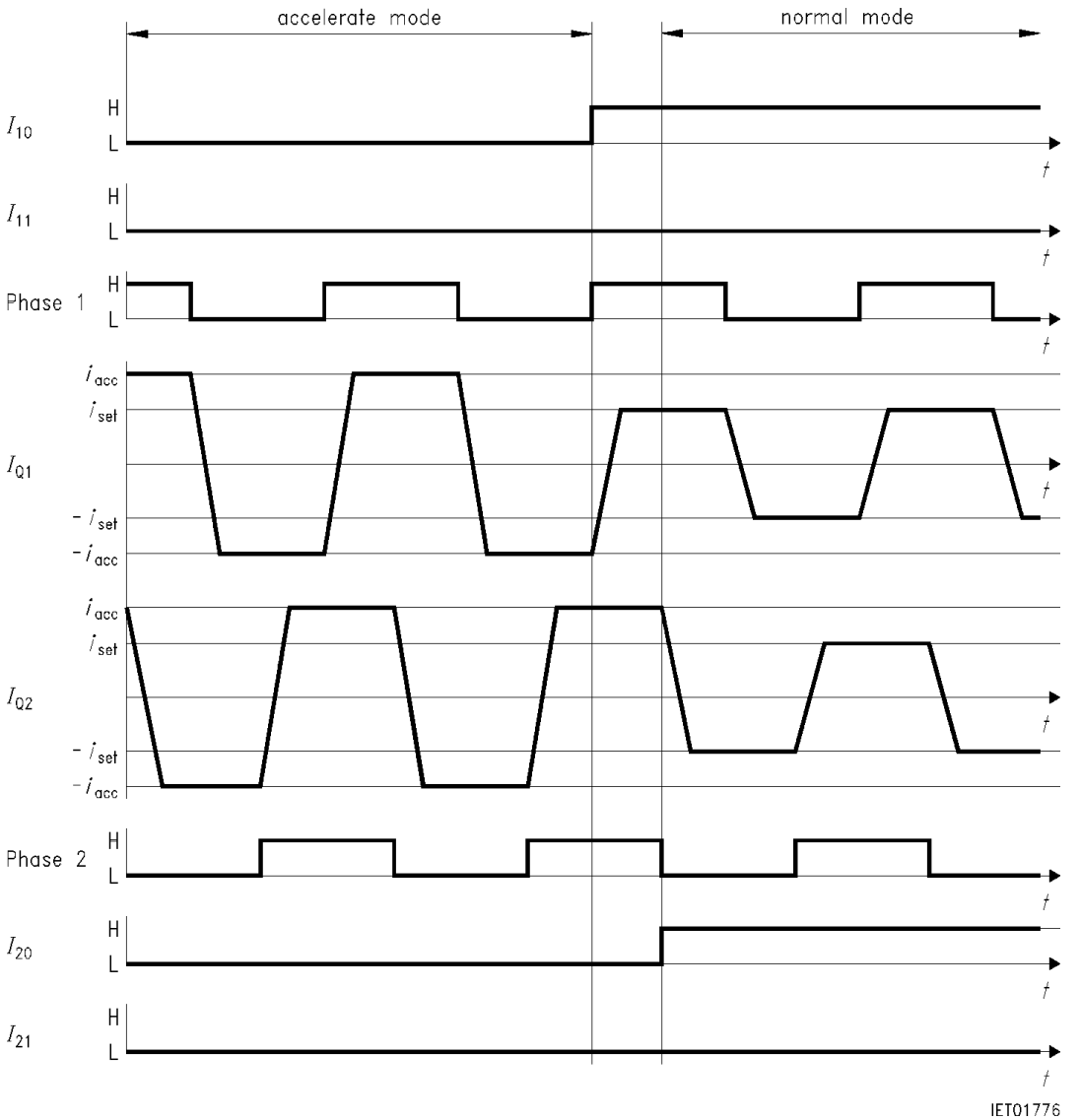




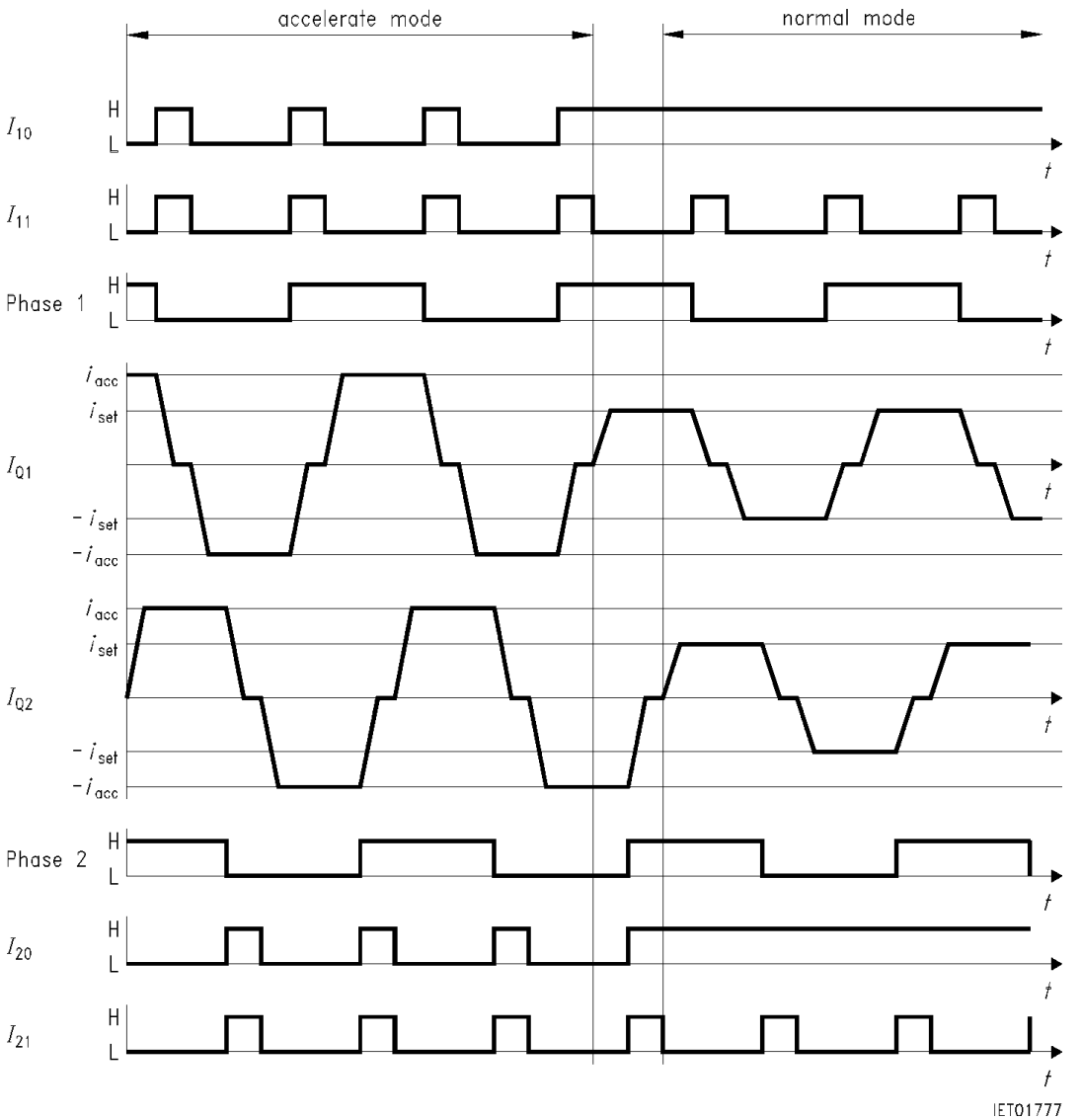
Application Circuit



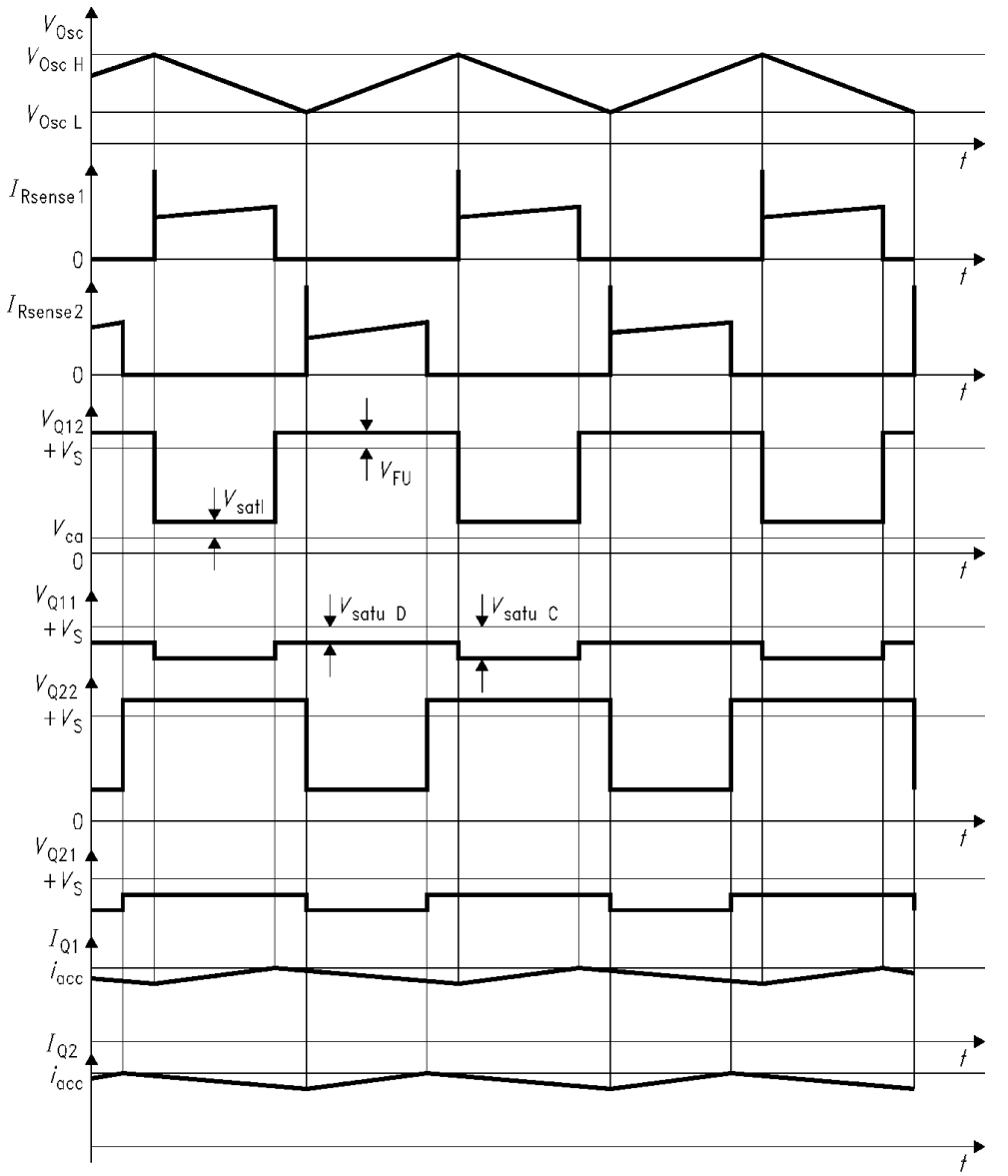
Test Circuit



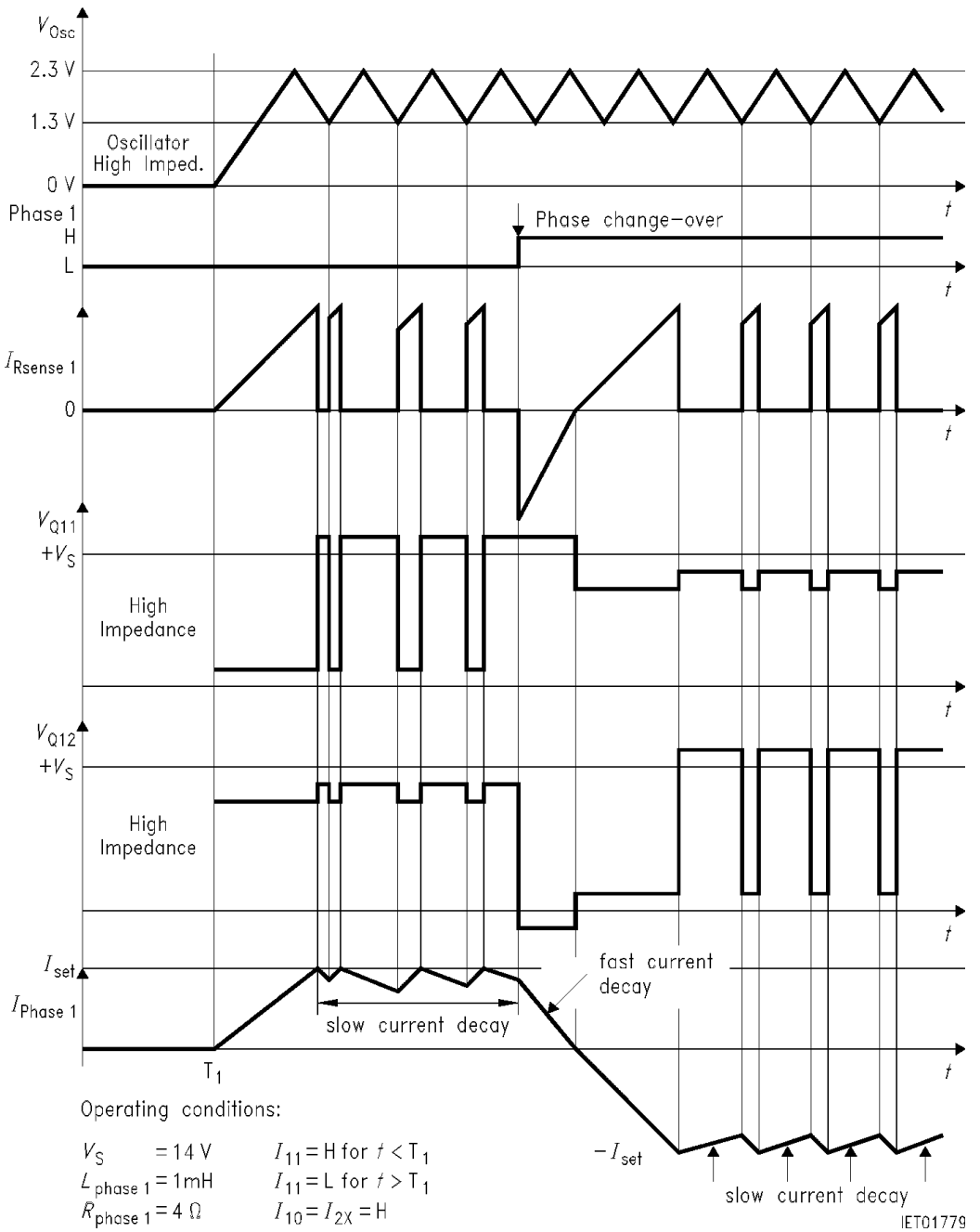
Full-Step Operation



Half-Step Operation



Current Control in Chop-Mode



Operating conditions:

V_S = 14 V I_{11} = H for $t < T_1$

$L_{phase\ 1}$ = 1mH I_{11} = L for $t > T_1$

$R_{phase\ 1}$ = 4 Ω $I_{10} = I_{2X}$ = H

Phase Reversal and Inhibit

Calculation of Power Dissipation

The total power dissipation P_{tot} is made up of

saturation losses P_{sat} (transistor saturation voltage and diode forward voltages),
quiescent losses P_q (quiescent current times supply voltage) and
switching losses P_s (turn-ON / turn-OFF operations).

The following equations give the power dissipation for chopper operation without phase reversal. This is the worst case, because full current flows for the entire time and switching losses occur in addition.

$$P_{tot} = 2 \times P_{sat} + P_q + 2 \times P_s$$

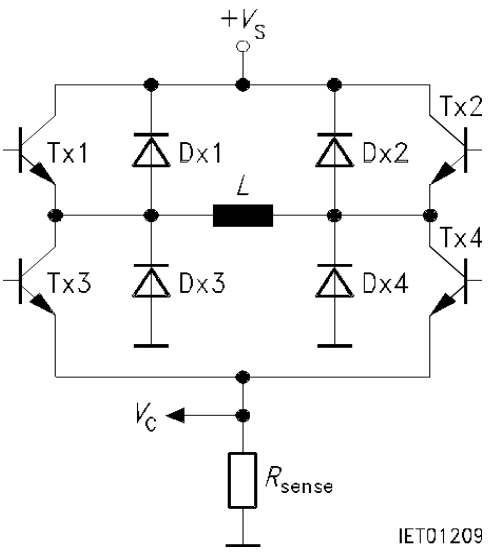
where

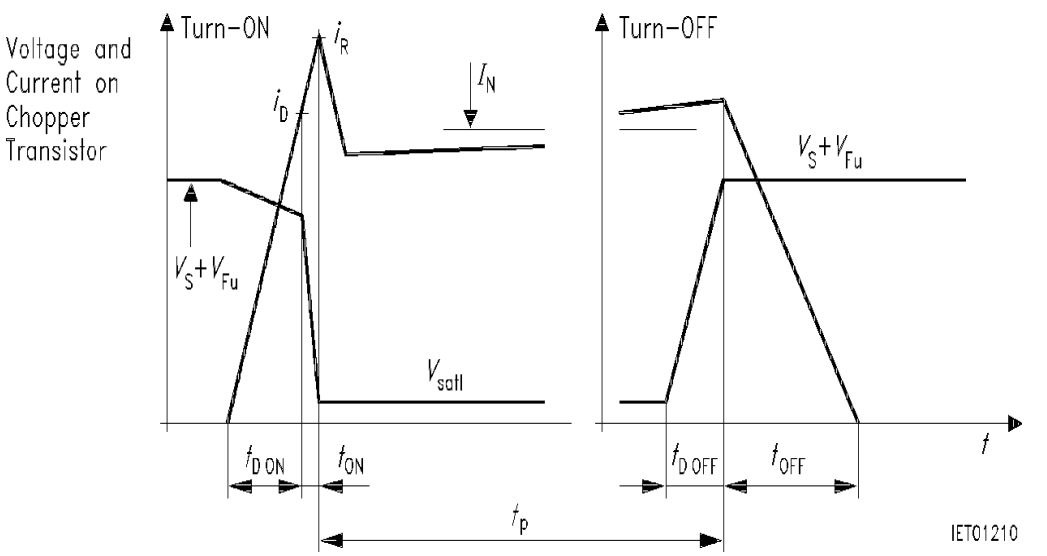
$$P_{sat} \cong I_N \{V_{satI} \times d + V_{Fu} (1 - d) + V_{satuC} \times d + V_{satuD} (1 - d)\}$$

$$P_q = I_q \times V_S$$

$$P_S \cong \frac{V_S}{T} \left\{ \frac{i_D \times t_{DON}}{2} + \frac{(i_D + i_R) \times t_{ON}}{4} + \frac{I_N}{2} (t_{DOFF} + t_{OFF}) \right\}$$

I_N = nominal current (mean value)
I_q = quiescent current
i_D = reverse current during turn-ON delay
i_R = peak reverse current
t_p = conducting time of chopper transistor
t_{ON} = turn-ON time
t_{OFF} = turn-OFF time
t_{DON} = turn-ON delay
t_{DOFF} = turn-OFF delay
T = cycle duration
d = duty cycle t_p / T
V_{satI} = saturation voltage of sink transistor (T_{X3}, T_{X4})
V_{satuC} = saturation voltage of source transistor (T_{X1}, T_{X2}) during charge cycle
V_{satuD} = saturation voltage of source transistor (T_{X1}, T_{X2}) during discharge cycle
V_{Fu} = forward voltage of free-wheeling diode (D_{X1}, D_{X2})
V_S = supply voltage





Voltage and Current at Chopper Transistor

Application Hints

The TLE 4727 is intended to drive both phases of a stepper motor. Special care has been taken to provide high efficiency, robustness and to minimize external components.

Power Supply

The TLE 4727 will work with supply voltages ranging from 5 V to 16 V at pin V_S. Surges exceeding 16 V at V_S won't harm the circuit up to 45 V, but whole function is not guaranteed. As soon as the voltage drops below approximately 16 V the TLE 4727 works promptly again.

As the circuit operates with chopper regulation of the current, interference generation problems can arise in some applications. Therefore the power supply should be decoupled by a 0.1 µF ceramic capacitor located near the package. Unstabilized supplies may even afford higher capacities.

Current Sensing

The current in the windings of the stepper motor is sensed by the voltage drop across R_{sense}. Depending on the selected current internal comparators will turn off the sink transistor as soon as the voltage drop reaches certain thresholds (typical 0 V, 0.07 V, 0.50 V and 0.70 V). These thresholds are not affected by variations of V_S. Consequently unstabilized supplies will not affect the performance of the regulation. For precise current level it must be considered, that internal bonding wire (typ. 60 mΩ) is a part of R_{sense}.

Due to chopper control fast current rises (up to 10A/µs) will occur at the sensing resistors. To prevent malfunction of the current sensing mechanism R_{sense} should be pure ohmic. The resistors should be wired to GND as directly as possible. Capacitive loads such as long cables (with high wire to wire capacity) to the motor should be avoided for the same reason.

Synchronizing Several Choppers

In some applications synchronous chopping of several stepper motor drivers may be desirable to reduce acoustic interference. This can be done by forcing the oscillator of the TLE 4727 by a pulse generator overdriving the oscillator loading currents (approximately $\pm$ 120 µA). In these applications low level should be between 0 V and 0.8 V while high level should be between 3 V and 5 V.

Optimizing Noise Immunity

Unused inputs should always be wired to proper voltage levels in order to obtain highest possible noise immunity.

To prevent crossconduction of the output stages the TLE 4727 uses a special break before make timing of the power transistors. This timing circuit can be triggered by short glitches (some hundred nanoseconds) at the Phase inputs causing the output stage to become high resistive during some microseconds. This will lead to a fast current decay during that time. To achieve maximum current accuracy such glitches at the Phase inputs should be avoided by proper control signals.

To lower EMI a ceramic capacitor of max. 3 nF is advisable from each output to GND.

Thermal Shut Down

To protect the circuit against thermal destruction, thermal shut down has been implemented.

Application Hints (cont'd)

Error Monitoring

The error output signals with low-potential one of the following errors:

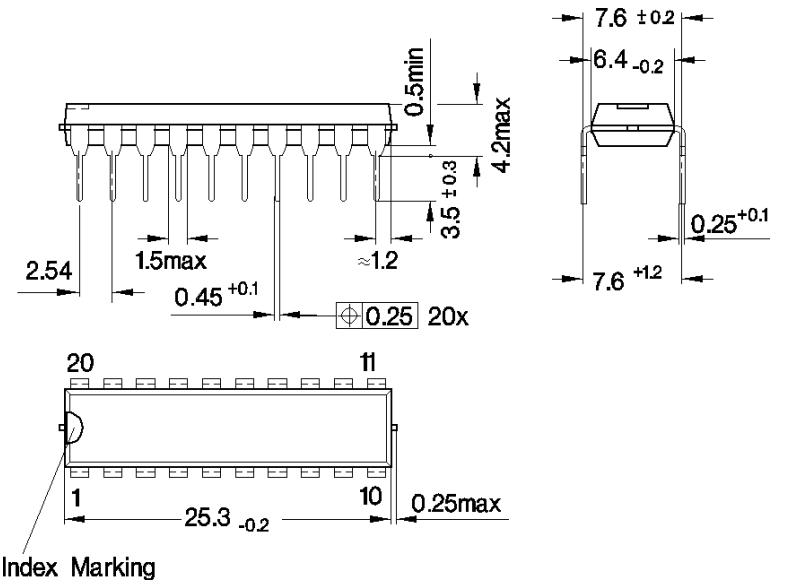
overtemperature implemented as pre-alarm; appears approximately 20 K before thermal shut down.

short circuit a connection of one output to GND for longer than 30 µs sets an internal error flipflop. A phase change-over of the affected bridge resets the flipflop. Being a separate flipflop for each bridge, the error can be located in such way.

underload the recirculation of the inductive load is watched. If there is no recirculation after a phase change-over, the internal error flipflop is set. Additionally an error is signaled after a phase change-over during hold-mode.

Package Outlines

Plastic Package, P-DIP-20-3
(Plastic Dual Small Outline Package)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

SIEMENS

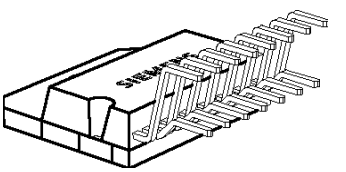
Smart Power Stepper Motor with Diagnostic Interface

TLE 5250

Preliminary Data **SPT-IC**

Features

- Single phase driver for stepper motor 2.5 A
- Low ON-resistance (typical 0.35 Ω)
- Short circuit protection
- Under voltage shutdown
- Overtemperature shutdown
- Serial diagnostic interface
- Fast freewheeling diodes
- Fast nominal/actual comparator for micro stepper mode
- Wide temperature range
- Wide supply range 6 V to 45 V
- TTL-compatible inputs



P-SIP-15-1

	Type	Ordering Code	Package
▼	TLE 5250	Q67000-A9103	P-SIP-15-1

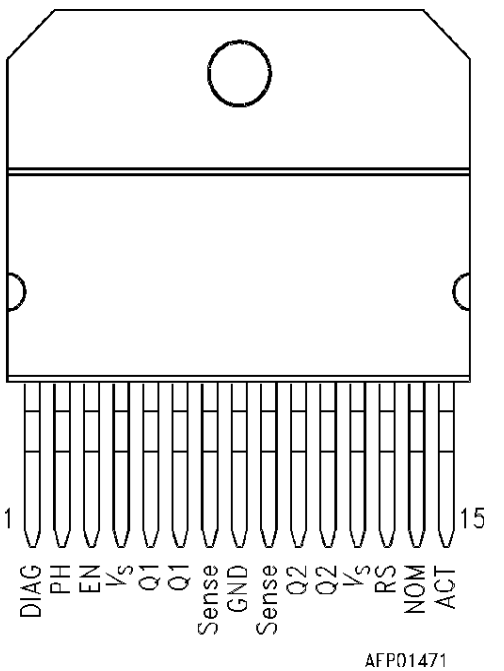
▼ New type

Functional Description

TLE 5250 is a monolithic IC in Smart Power technology for controlling and regulating the motor current in one phase of a bipolar stepping motor. There are other applications in driving DC motors and inductive loads that are operated on constant current.

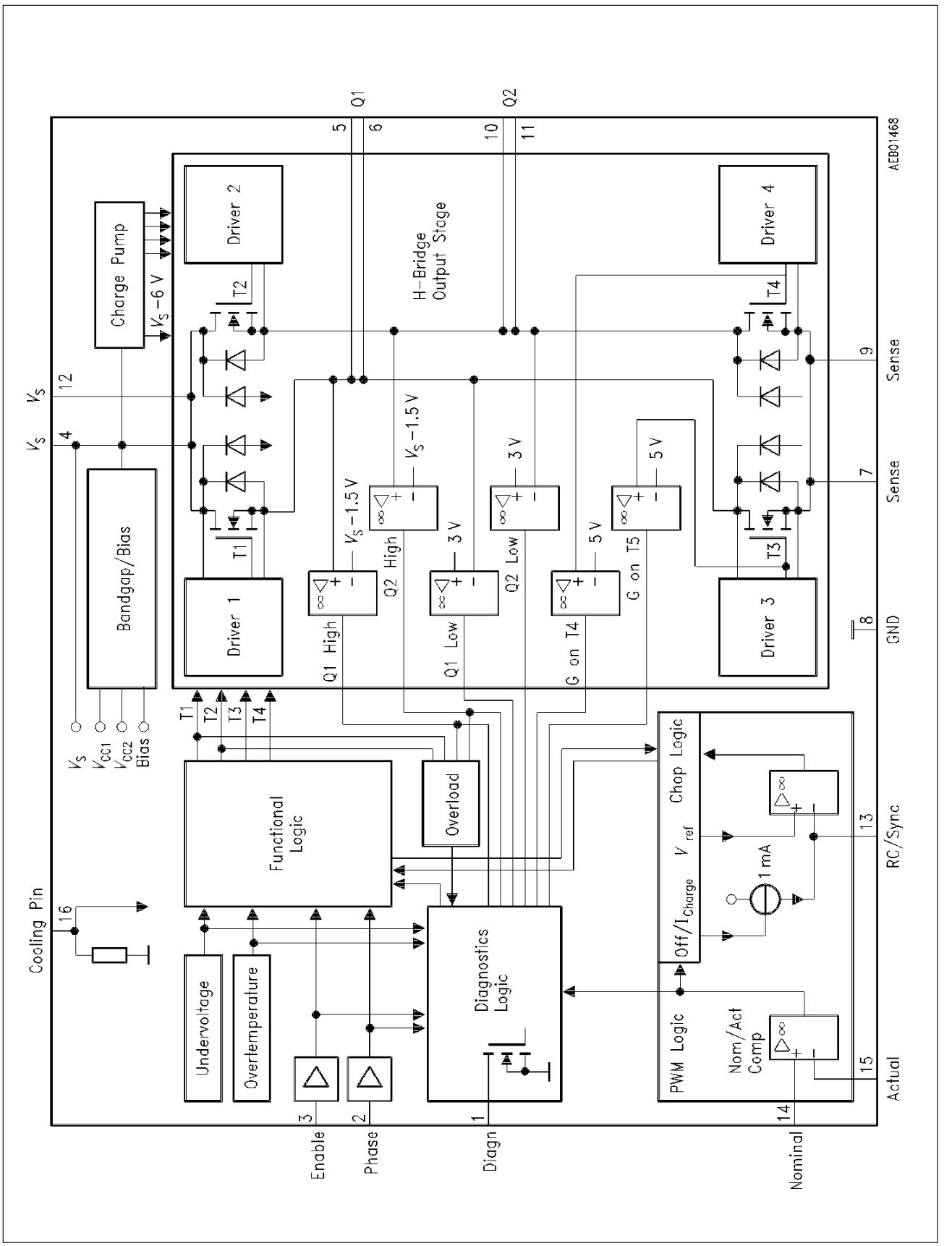
The device has TTL-compatible logic inputs, includes a H-bridge with integrated, fast free-wheeling diodes plus dynamic limiting of the motor current by a chopper mode. The nominal current can be set continuously by a control voltage. Microstep mode can be produced by applying a sinusoidal control voltage. Two TLE 5250s, with a minimum of external circuitry and a single supply voltage, form a complete system - that can be driven direct by an MC - for two-phase, bipolar stepping motors with output current of up to 2.5 A per phase. The outputs of the IC are internally protected against shorted to ground, supply voltage and shorted load. The output stages are also disabled by undervoltage and overtemperature. All fault functions can be detected by the internal diagnostics, which can be read out serially.

Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	DIAG	Open-drain diagnostics output
2	PH	Input for determining source/sink on outputs Q1 and Q2; when Enable = Low, this pin serves as clock input for reading out diagnostics
3	EN	Input for activating or turning off device (all output transistors turned off); Enable High = output active, Enable Low = diagnostics
4, 12	V_S	Supply voltage of IC
5, 6	Q1	Power output with integrated free-wheeling diodes
7, 9	Sense	Actual-current output: shared, open-source output of sink transistors
8	GND	Ground
10, 11	Q2	Power output with integrated free-wheeling diodes
13	RS	Determines turning back on of sink transistor by internally driven, external RC element or external TTL trigger signal
14	NOM	Input for reference potential (nominal current) for nominal/actual comparator
15	ACT	Input for actual current for nominal/actual comparator



Block Diagram

1 Application

Two TLE 5250 drivers are required to operate a bipolar stepping motor. To implement full-step operation, a squarewave voltage with the required stepping frequency is applied to the phase input of the upper driver, and the same squarewave voltage, but offset in phase by 90°el, to the phase input of the lower driver. Motor-current limiting is produced by a DC signal that is applied to both nominal-current inputs. In microstep operation the nominal current tracks sinusoidally and synchronously with the required stepping frequency. This produces a sinusoidal current in the motor windings to ensure very smooth running and a high stepping frequency. If an instantaneous nominal value (sine or cosine) is held on the second driver, it is possible to set a certain angle of rotation while the motor is stationary. The motor current produced by this depends on nominal voltage and sense resistance (normally 0.5 Ω), i.e.

$$I_{\mathrm{M}}[\mathrm{V}] = \frac{V_{\mathrm{nom}}[\mathrm{V}]}{R_{\mathrm{S}}[\Omega]}$$

The actual voltage should be thoroughly filtered for precise current regulation, especially in microstep operation. So the actual input is accessible, and an RC element is necessary between the Sense output and Actual input. The resistance R_{R} should correspond to the internal resistance of the nominal-current input-voltage source to prevent additional voltage offset on the nominal/ actual comparator.

Circuit Description

Outputs

Outputs Q1 and Q2 are fed by push-pull output stages. Four integrated free-wheeling diodes referred to ground or the supply voltage protect the integrated circuit against reverse voltages from an inductive load.

Enable and Phase

Outputs Q1 and Q2 can be disabled by a voltage V_{Inh} of ≤ 0.8 V on the Enable pin. The sink transistors are enabled by V_{Inh} ≥ 2 V.

The voltage on the Phase input determines the phase of the output current. Output Q1 acts as a sink for V_{Ph} ≤ 0.8 V and as a source for V_{Ph} ≥ 2 V.

For output Q2 this is reversed: sink for V_{Ph} ≥ 2 V and source for V_{Ph} ≤ 0.8 V.

The sink transistors are chopped. Low signal on the Enable pin plus a clock signal on the Phase pin enable readout of the multiplexer.

Nominal-Current Input

The peak current in the motor winding is defined by the voltage on the Nominal input. This is compared by a fast comparator to the voltage drop on the actual-current sensor. If the nominal current is exceeded, the sink transistors of the outputs are turned off by the logic.

RC/Sync Input

The outputs are turned on by the signal applied to the RC input. Synchronization is possible by TTL signal or chopper mode with an external RC combination.

Chopper Mode

After the supply voltage is applied, capacitor CT is charged with constant current of 1 mA. A regulator limits the maximum voltage on the capacitor to 2.3 V. As a result of the rising current in the motor winding, the voltage on the actual sensor increases. Once the value defined by the nominal-current input is exceeded, the fast comparator resets an RS flipflop. Thus sink transistors T3 and T4 are turned off by the logic. The charge current is turned off and the parallel RT discharges CT.

The internal logic is designed so that capacitor CT is always charged before the discharge operation is triggered. This guarantees a constant charge time, even for very small coil currents (**see Diagram 1**).

Sync Operation

If a sync signal with TTL level is applied to the RC input, the negative edge will set the RS flipflop - by way of the combined Schmitt trigger and monoflop - if the voltage on the current sensor is smaller than the nominal value on the nominal-current input. As in chopper mode, the appropriate output transistors conduct. They are again turned off by resetting the RS flipflop when the voltage on the current sensor becomes greater than the nominal value (**see Diagram 2**).

Output-Stage Control

This part of the circuit handles turn-off of the output stages when the output is shorted to ground. There is separate current monitoring for this purpose in the source transistors. The temperature of the output stages is also monitored. If this exceeds 175 °C, all output stages are turned off, and then turned on again when the temperature drops. Undervoltage also causes turn-off of the transistors in the output stages. These possible fault states are stored in the diagnostics register.

Diagnostics

The information from the different parts of the circuit is collected in the diagnostics and stored in the fault logic. The information is read out on the Diagnostics output (open collector).

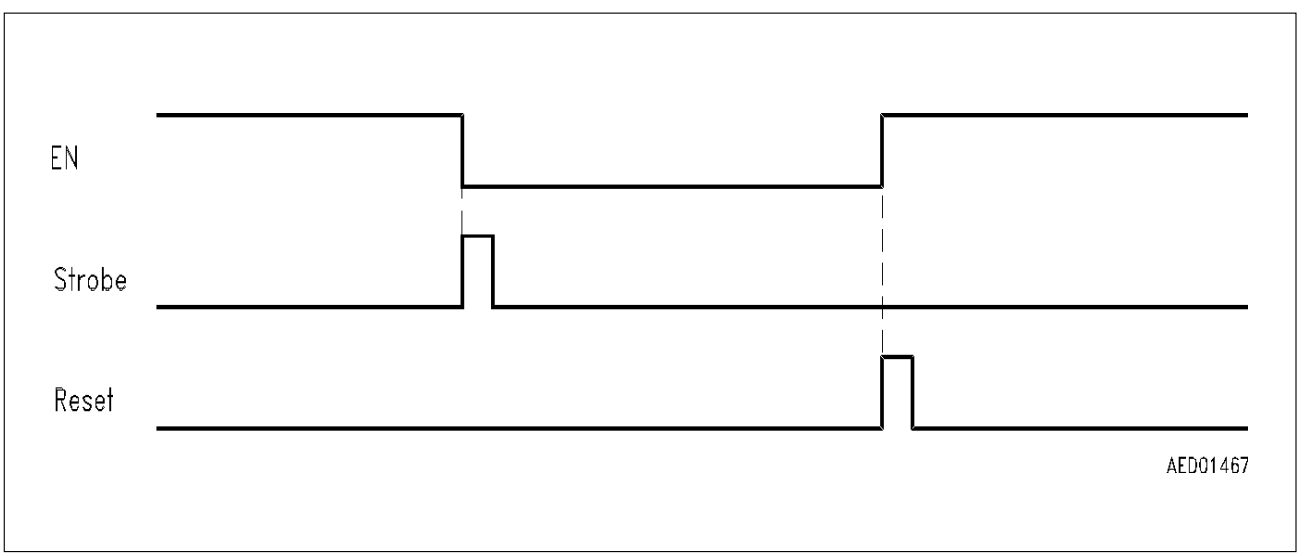
The fault logic consists of a 16-bit multiplexer that switches information in three categories through to the Diagnostics output.

Bit 0 always appears inverted on DIAG when EN is High. This means that, if there is overcurrent on the upper transistor, undervoltage or overtemperature, it will be signaled immediately on the Diagnostics output. DIAG changes from High to Low.

Bit 1: check bit.

Bits 2, 3, 4 and 5 indicate the momentary status of the comparators on the two outputs (**see Block Diagram**). Changes in the status of the comparators for output monitoring can be observed on DIAG when EN is Low and the counter of the multiplexer is on 2, 3, 4 or 5. This is necessary for detecting underload.

Bits 6, 7, 8, 9
The monoflop generates a short strobe signal when the EN edge changes from High to Low. The status of the comparators for output monitoring is stored with this signal and can be read out in bits 6, 7, 8 and 9.
When Enable is Low, the Phase input is used as a clock input. As the edge rises, an internal counter is incremented and the corresponding channel of the multiplexer is switched through. As the edge falls, the signal is output inverted. When Enable is High, the counter is reset to zero.



Bits 10, 11
With these bits it is possible to detect the status of the gate voltages of the lower output-stage transistors T3 and T4. Bit 10: status for EN edge transition. Bit 11: whether the lower transistor has at all been turned on.

Bit 12 indicates whether the nominal/actual comparator has switched. The comparator switches when the output current is regulated.

Bits 13, 14, 15
These bits indicate the presence of overcurrent, undervoltage or overtemperature. A fault is ORed and output direct by bit 0 on DI.

When the multiplexer is read out, bits 0 through 15 are output once non-inverted (Phase = Low) and once inverted (Phase = High).

Bit Assignment in Error Register

Bit 0 = High for overtemperature/undervoltage/overcurrent
Bit 1 = always High
Bit 2 = High when sink transistor Q1 turned on
Bit 3 = High when sink transistor Q2 turned on
Bit 4 = High when source transistor Q1 turned on
Bit 5 = High when source transistor Q2 turned on
Bits 2-5 = momentary states for readout
Bit 6 = bit 2 state for falling edge of Enable signal
Bit 7 = bit 3 state for falling edge of Enable signal
Bit 8 = bit 4 state for falling edge of Enable signal
Bit 9 = bit 5 state for falling edge of Enable signal

Bits 6-10 represent status of outputs for negative change in edge of Enable signal

Bit 11 = High if gate-source voltage of sink transistors is > 5 V at moment of readout

Bits 11-15 are set if event occurs during switching (Enable = High)

Bit 11 = High if sink transistor V_{GS} > 5 V
Bit 12 = High if actual current lower than nominal current
Bit 13 = High if overcurrent detected on source transistors
Bit 14 = High if undervoltage detected
Bit 15 = High if thermal link tripped

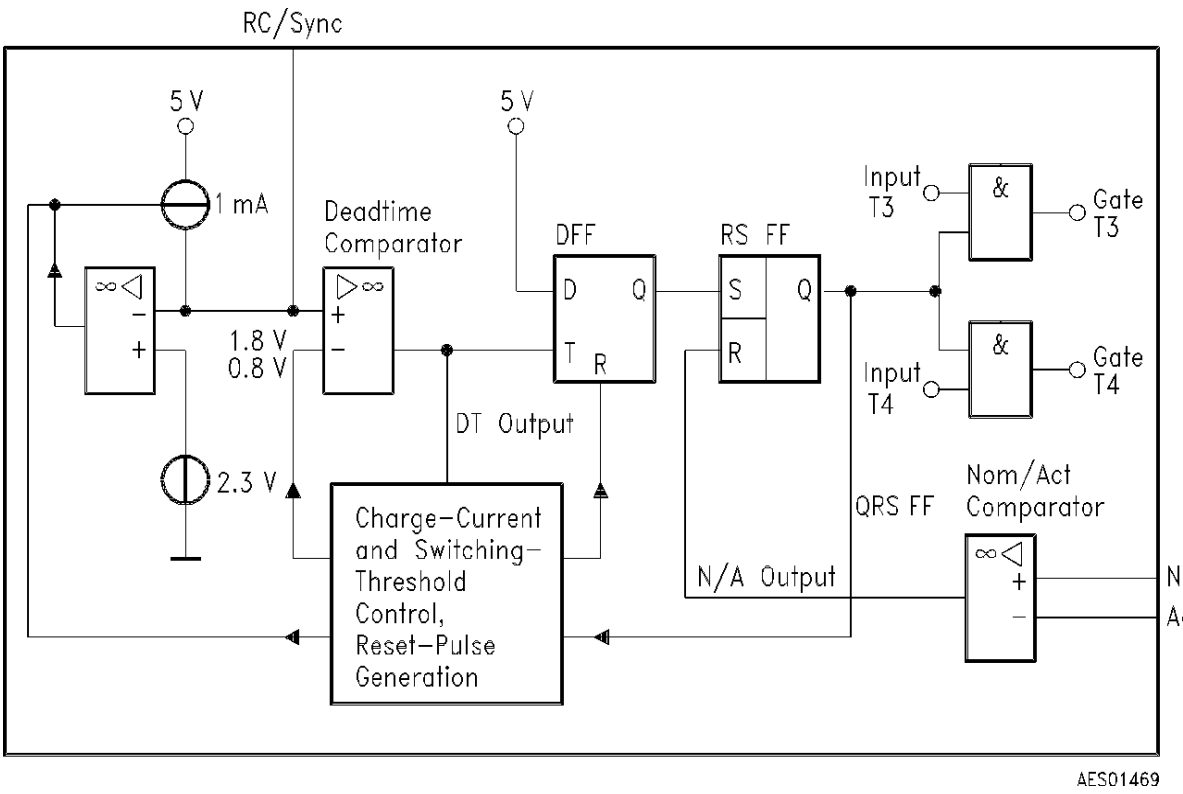
The memories are erased by a rising edge on the Enable input.

Logic Assignment: Control Inputs, Output Transistors

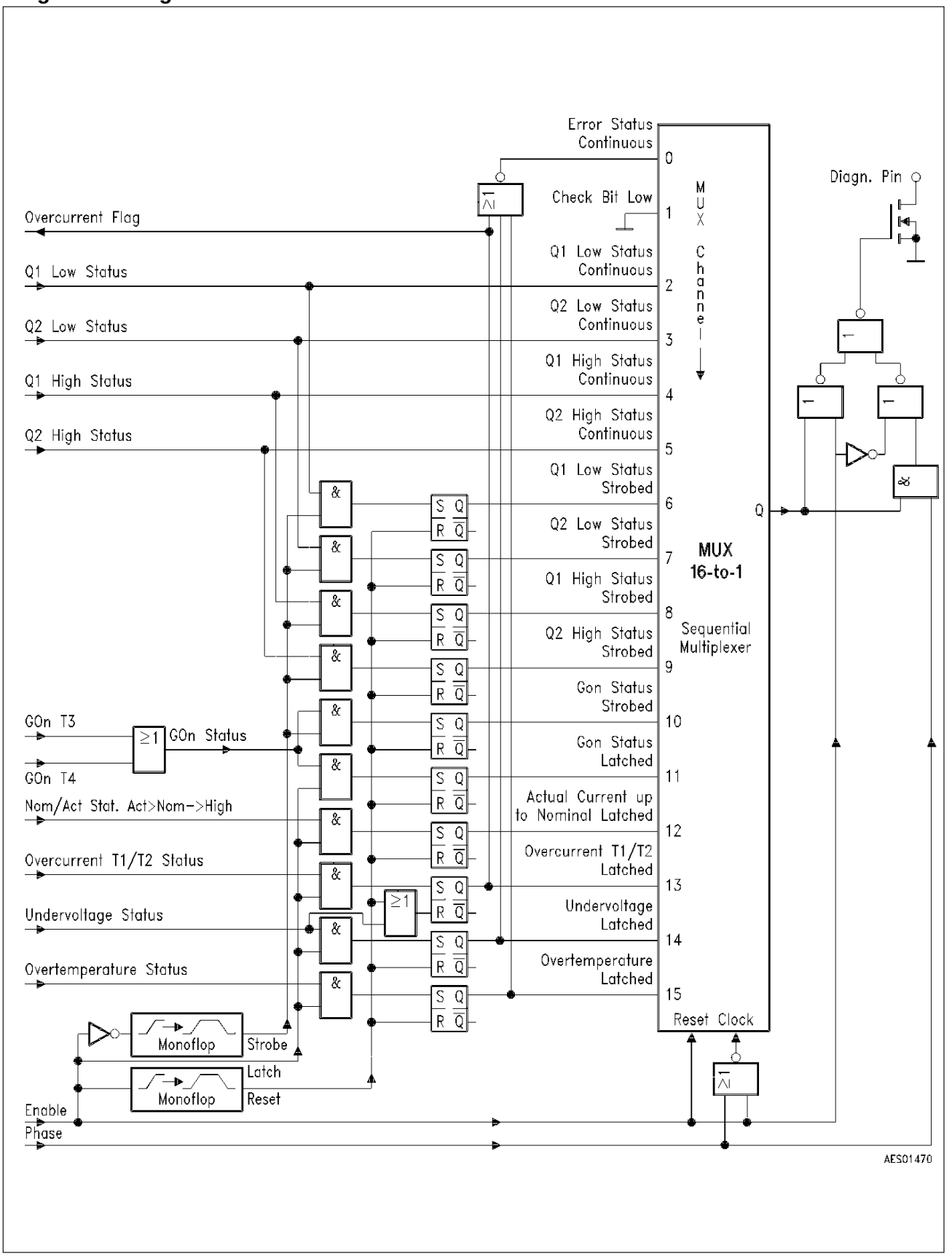
Enable	L	L	H	H
Phase	L	H	L	H
Output Q1	/	/	L	H
Output Q2	/	/	H	L
Transistor T1 Transistor T2 Transistor T3 Transistor T4	X X X X	X X X X	X – – X	– X X –

L = Low voltage level, input open
H = High voltage level
X = transistor turned off
– = transistor conducting
– = transistor conducting, switched in current limiting
/ = output high-impedance

PWM Logic


RC/Sync
5 V
1 mA
1.8 V
0.8 V
2.3 V
Deadtime
Comparator
5 V
DFF
D
Q
T
R
RS FF
S
Q
R
Input
T3
Gate
T3
Input
T4
Gate
T4
DT Output
QRS FF
Nom/Act
Comparator
N/A Output
Nominal
Actual
Charge-Current
and Switching-
Threshold
Control,
Reset-Pulse
Generation
AES01469

Diagnostics Logic



Absolute Maximum Ratings
T_J = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	– 0.3	45	V
Supply current	I_S	0	3	A
Peak currents on outputs	I_Q	– 3	3	A
Diode Forward Currents				
Diode to + V_S	I_{FH}		3	A
Diode to Sense	I_{FL}		3	A
Output current on actual-current pin	I_{Act}		3	A
Voltage on actual-current pin	V_{Act}	– 0.3	5	V
Ground current, pin 6	I_{GND}		3	A
Chip temperature	T_C	– 40	150	°C
Storage temperature	T_{stg}		125	°C
Thermal Resistances				
System-air	R_{thSA}		70	K/W
System-case	R_{thSC}		3	K/W
Operating Range				
Supply voltage	V_S	6	40	V
Input voltage Enable, Phase, RC/Sync	V_I	– 0.3	5.5	V
Voltage on Nominal pin	V_{NOM}	– 0.3	2	V
Voltage on Actual pin	V_{ACT}		2	V
Output current Q1, Q2	I_Q	– 2.5	2.5	A
Chip temperature	T_J	– 40	150	°C
Enable and Phase Inputs				
H input voltage	V_{IH}	2		V
L input voltage	V_{IL}		0.8	V

Characteristics

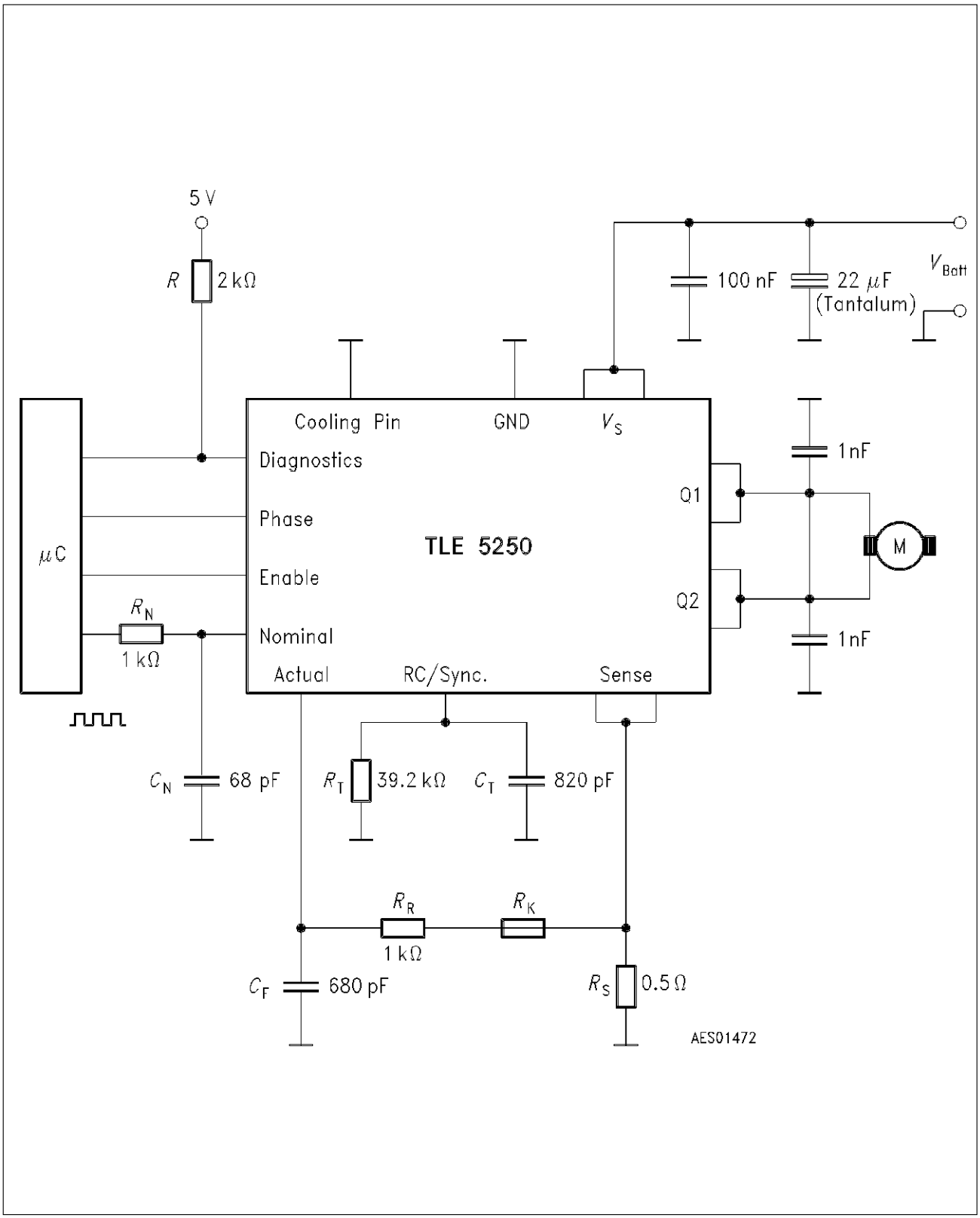
V_S = 6 to 25 V; $T_J \leq 150$ ˚C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply current	I_S			11	mA	Enable = High
Output Q1, Q2						
Turn-on resistance of output transistors	$R_{DS\ ON}$	0.3		0.6	Ω	I = 2.5 A, 150 °C
Phase deadtime	t_D		10		µs	
Diode forward voltage output to + V_S	V_{FQ}			1.5	V	I_{FH} = 2.5 V
Diode forward voltage actual-current pin to output				1.5	V	I_{FH} = 2.5 V
Nominal Current						
Input current	I_{I8}	0	1	2	µA	
Offset voltage measured for 0 V actual/nominal pin	$V_{I(8-4)}$	– 4		8	mV	
Actual Current						
Turn-off delay of nom/act comparator	t_d			0.5	µs	
Common-mode error	V_{Comm}	– 5		10	mV	
RC/Sync						
Sync frequency	f		20	100	kHz	
Trigger threshold lower upper	 V_{tL} V_{tH}	 0.8 1.7		 1 2	 V V	
Maximum charge voltage	V_{Chm}	2.2	2.3	2.4	V	R = 39 kΩ C = 820 pF

Characteristics (cont'd)

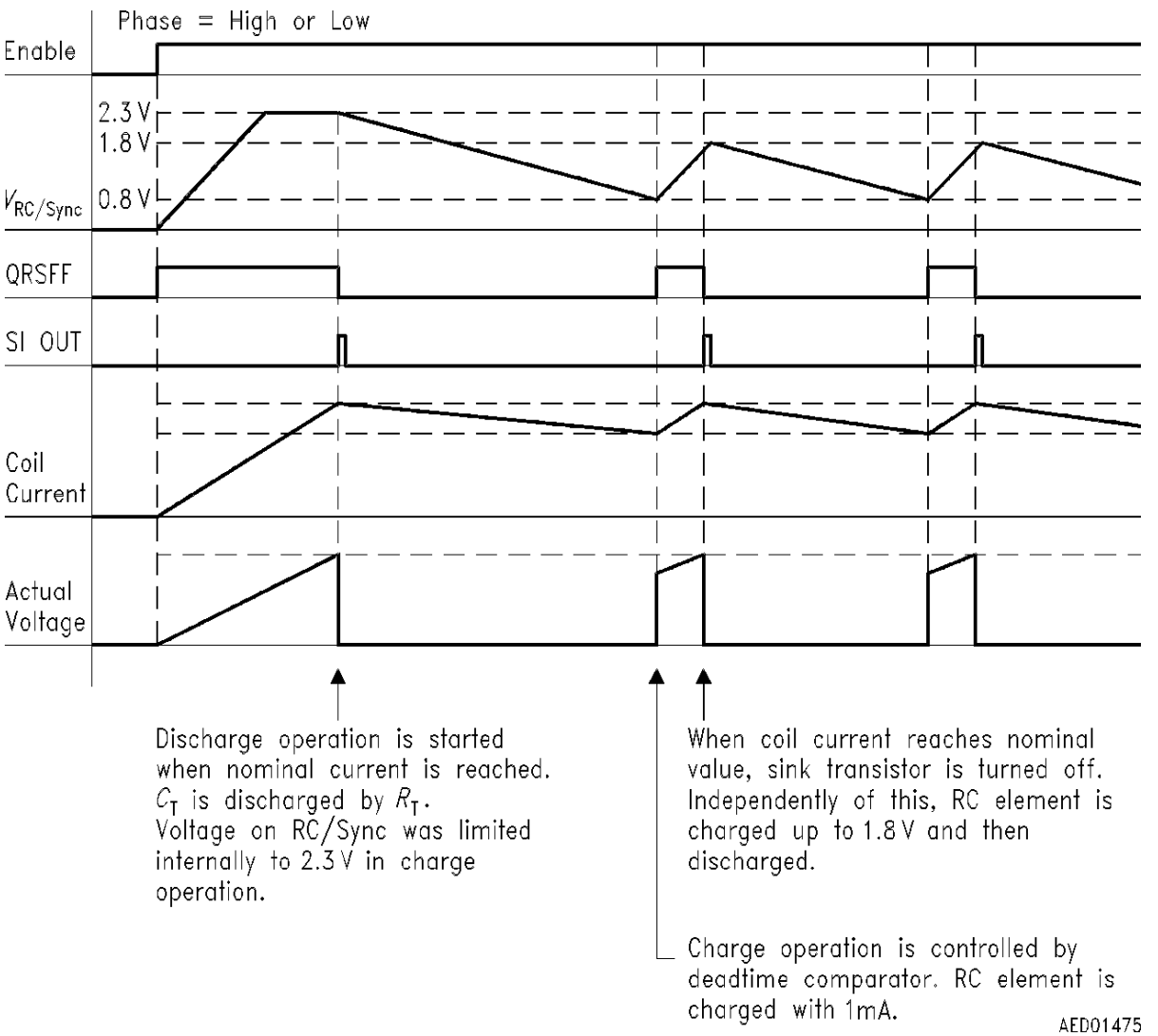
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Undervoltage Cutout						
Disable	V_{UDIAG}	4			V	
Enable	V_{UEN}			5.3	V	
Hysteresis	V_{UH}			400	mV	
Diagnostics Output						
Activating delay (Enable High → Low)	t_{def}			400	ns	
Delay phase low to high	t_{ddr}			500	ns	Enable = Low V_S > 5.5 V
Delay phase high to low	t_{ddf}			450	ns	Enable = Low V_S > 5.5 V
Output voltage low	V_{Diag}			0.4	V	I_{QL} = 5 mA
Leakage current high	I_{Diag}			10	µA	V_{QH} = 5 V

Test Circuit



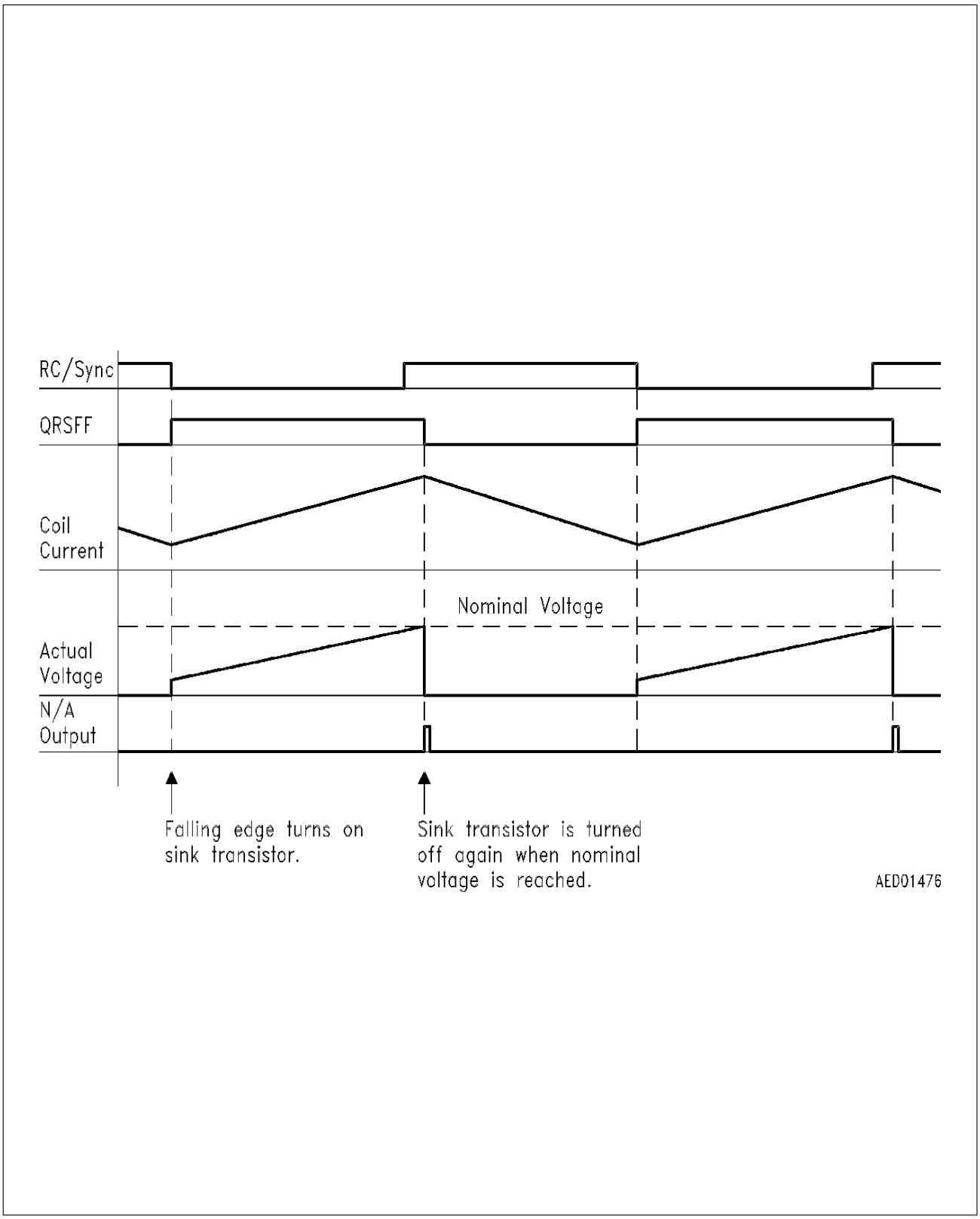
Application Circuit 1

Diagram 1



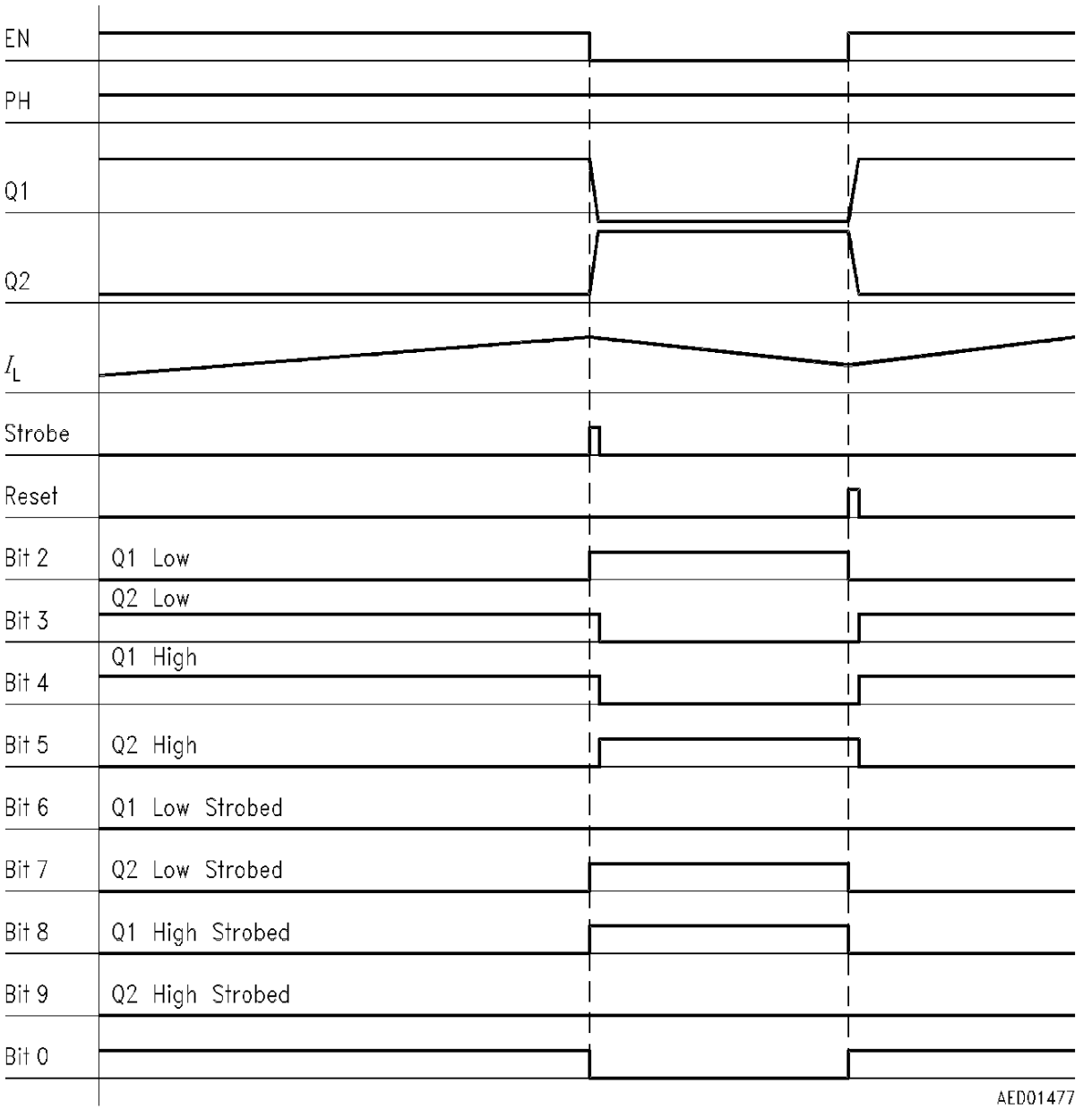
Chopper Mode with External Capacitor CT and Resistor RT

Diagram 2



Synchron Mode

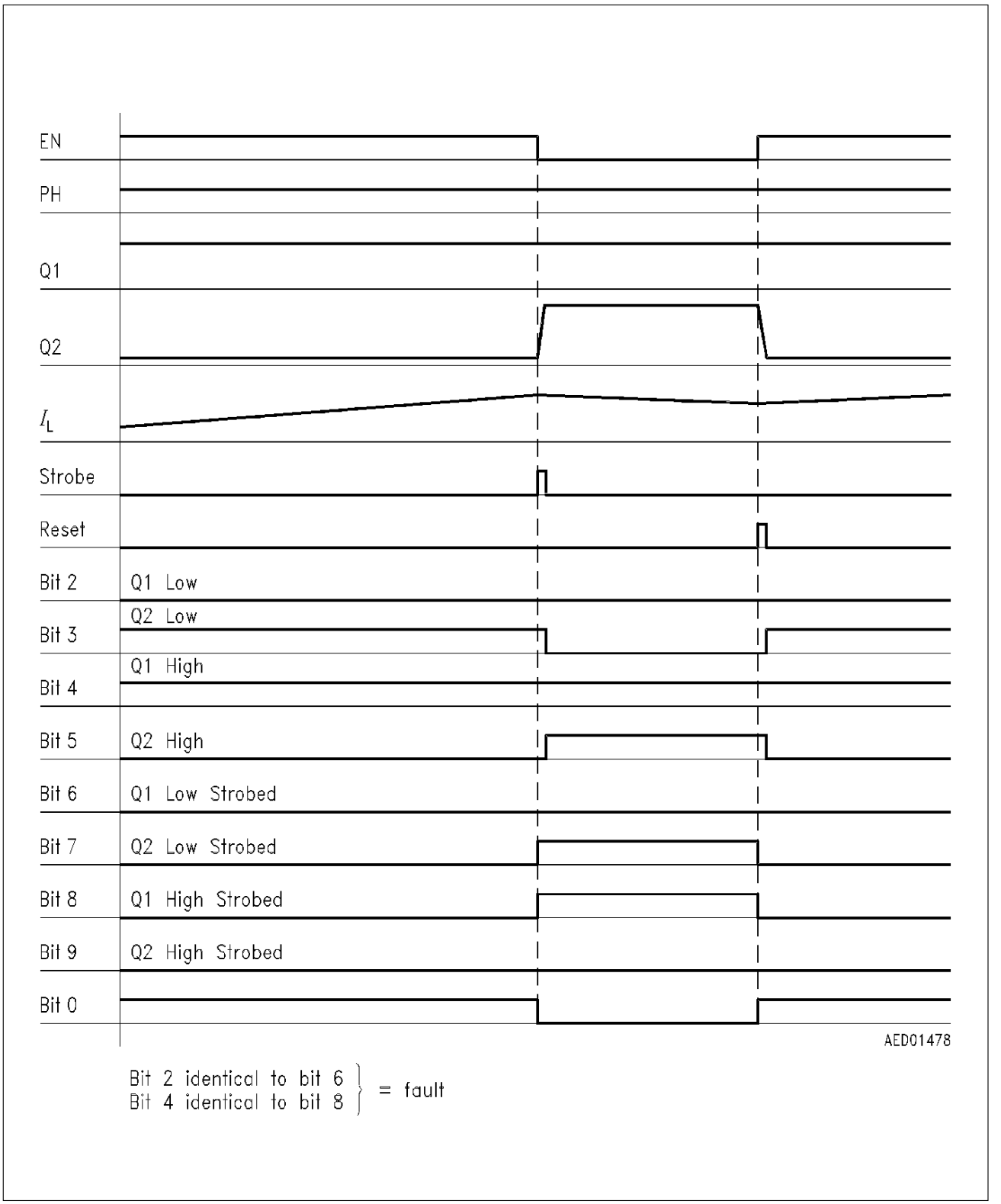
Diagram 3



For inductive load and faultfree operation,
diagnostics when read out must show
bit 2 inverted to bit 6
bit 3 inverted to bit 7
bit 4 inverted to bit 8
bit 5 inverted to bit 9

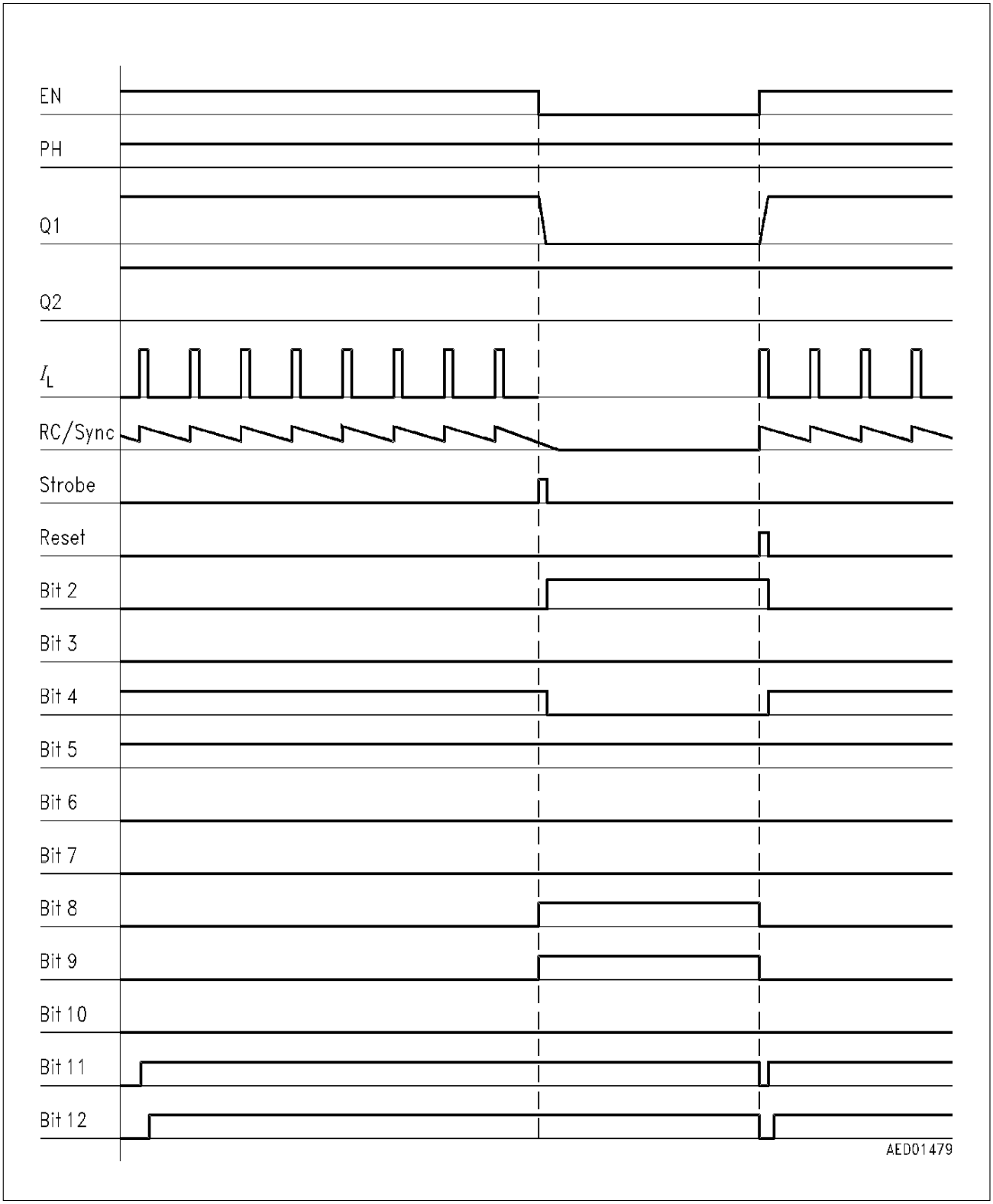
Response to Inductive Loads
a) Normal Operation (no current regulation)

Diagram 4



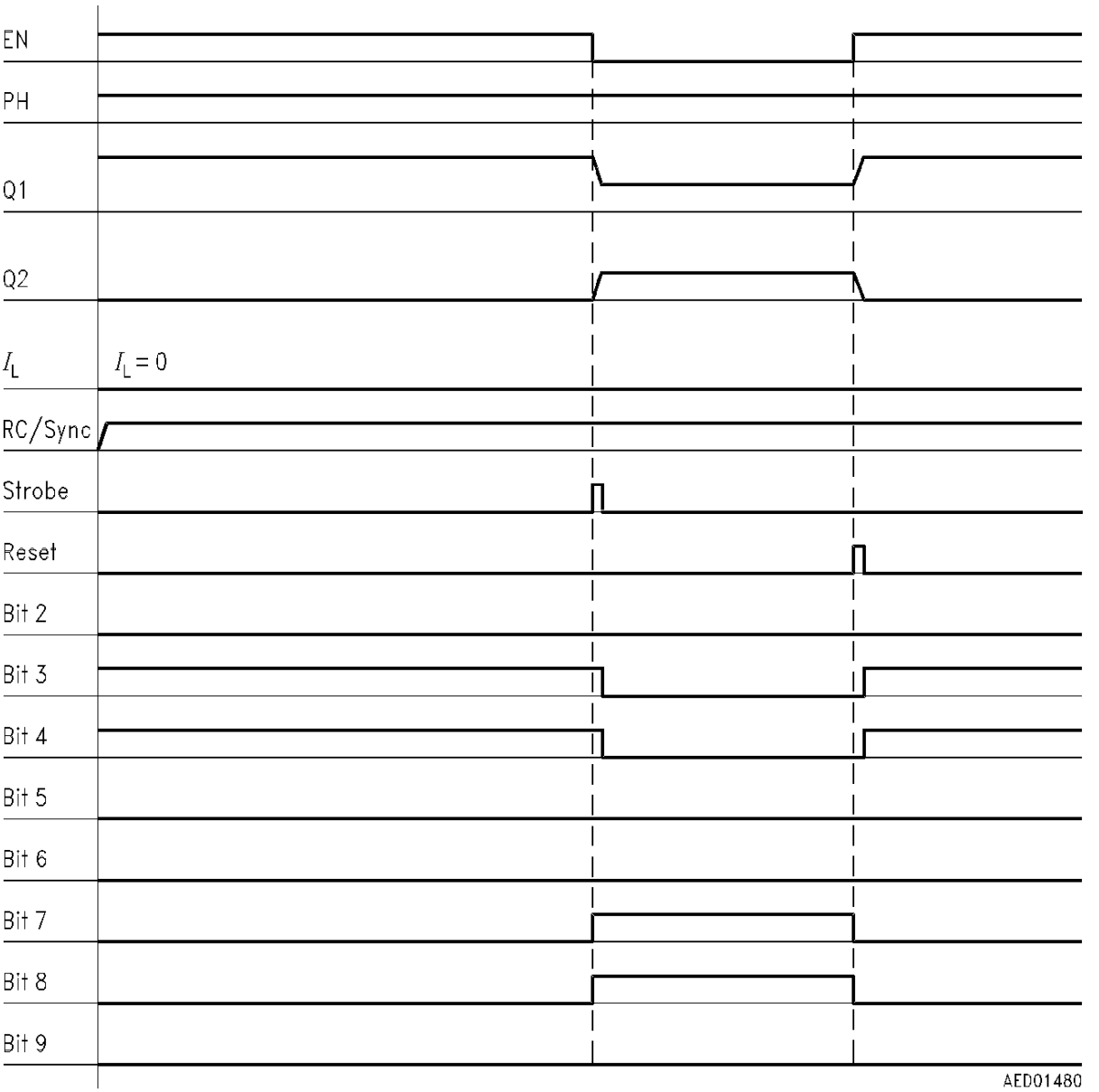
Response to Inductive Loads
b) Q1 Shorted to + V_S (Phase = High)

Diagram 5



Response to Inductive Loads
c) Q2 Shorted to + V_S (Phase = High)

Diagram 6



Indication of low load: bit 2 = bit 3
bit 4 = bit 5
while Enable = Low

And conditions bit 2 = /bit 6
bit 3 = /bit 7
bit 4 = /bit 8
bit 5 = /bit 9 are not all satisfied

Response to Inductive Loads
d) Low Load