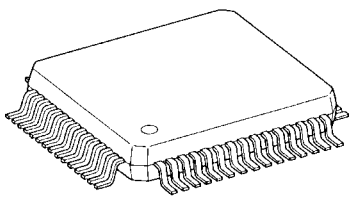
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC9332F

Audio Digital Signal Processor

The TC9332F has a ROM area that holds application programs for digital filters such as equalizers, for dynamic range control of compressors, and for acoustic field control concert hall simulation. These application programs allow real-time digital processing of audio signals.
Thanks to 64 kbit of built- in data delay (audio field control) RAM, no external RAM is necessary and
the built-in voltage-controlled oscillator (VCO) allows easy phase-locked loop configuration.



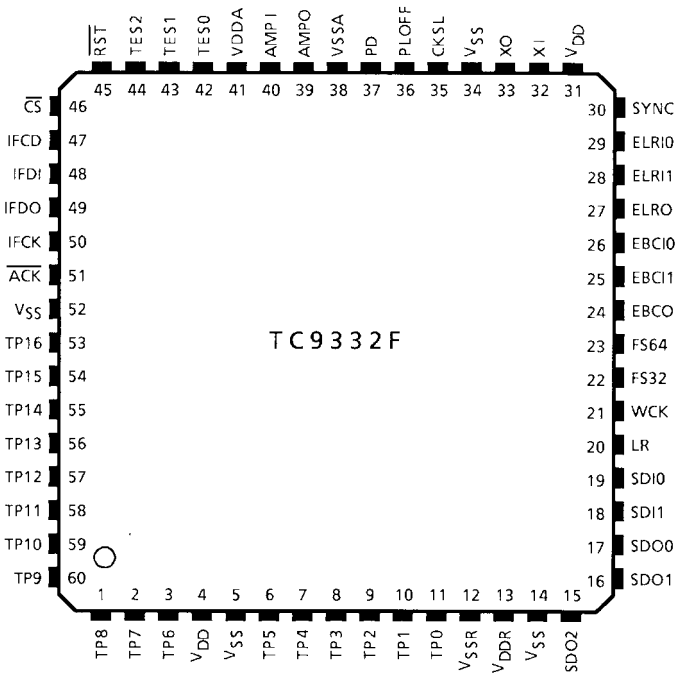
QFP60-P-1414-0.80D

Weight: 1.08 g (typ.)

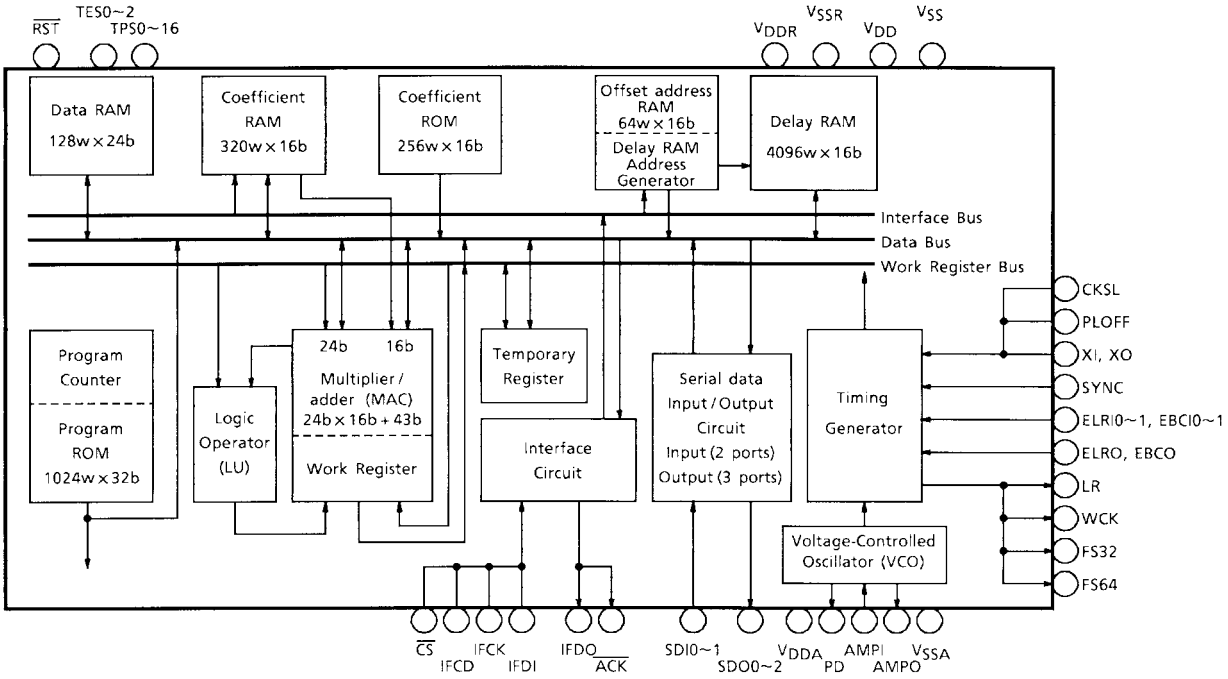
Features

- 24 bit main bus
- The arithmetic operations block is as follows:
  Multiplier/adder: 24 bit × 16 bit + 43 bit → 43 bit
  Accumulator: 43 bit (code extension 4 bit)
  Logic operator: 24 bit (AND, OR, XOR, NOT)
  Work register: 32 bit, 39 bit
  Temporary register: 32 bit
  Shifter: +4 bit, +1 bit shift
- The structure of the program and internal data memory areas are as follows:
  Program ROM: 1024 word × 32 bit
  Data RAM: 128 word × 24 bit
  Coefficient RAM: 320 word × 16 bit
  Coefficient ROM: 256 word × 16 bit
  Offset address RAM: 64 word × 16 bit
- The following five serial data ports are provided:
  Serial data input ports: 2 ports (SDI0, SDI1)
  Serial data output ports: 3 ports (SDO0, SDO1, SDO2)
  Data word length: 24 bit and 16 bit
  Data format: MSB/LSB first (input)
  MSB first (output)
- Built-in RAM for data delay
  Delay RAM: 64 kbit (4096 word × 16 bit)
- Built-in VCO circuit
- Coefficient data and offset data can be set or changed via a microcontroller interface.
- CMOS silicon technology for higher speed.
- 60 pin flat package.

Pin Connection



Block Diagram



Pin Function

Pin No.	Symbol	I/O	Description of Pin Functions		Remarks
1~3	TP8~TP6	O	Test data output terminal, normally open.		—
4	V_{DD}	—	Power supply terminal.		—
5	V_{SS}	—	Ground terminal.		—
6~11	TP5~TP0	O	Test data output terminal, normally open.		—
12	V_{SSR}	—	Ground terminal for internal delay RAM (DLRAM).		—
13	V_{DDR}	—	Power supply terminal for internal delay RAM (DLRAM).		—
14	V_{SS}	—	Ground terminal.		—
15	SDO2	O	Serial data output terminal. Output data length 24 bit or 16 bit, selectable by microcontroller.		—
16	SDO1				—
17	SDO0				—
18	SDI1	I	Serial data input terminal. Input data length 24 bit or 16 bit, selectable by microcontroller.		—
19	SDI0				—
20	LR	O	LR clock output terminal (1 fs).		—
21	WCK	O	Word clock output terminal (2 fs).		—
22	FS32	O	Bit clock output terminal (32 fs).		—
23	FS64	O	Bit clock output terminal (64 fs).		—
24	EBC0	I	Bit clock input terminals. Inputs shift clock for SDO0/1/2 data output.		Schmitt input
25	EBCI1	I	Bit clock input terminals. Inputs shift clock for SDI0/1 data input.	For SDI1 data input	Schmitt input
26	EBCI0			For SDI0 data input	Schmitt input
27	ELRO	I	LR clock input terminal. Inputs LR clock for SDO0/1/2 data output.		Schmitt input
28	ELRI1	I	LR clock input terminals. Inputs LR clock for SDI0/1 data input.	For SDI1 data input	Schmitt input
29	ELRI0			For SDI0 data input	Schmitt input
30	SYNC	I	Synchronous signal input terminal. The synchronous signal forcibly reset the program counter to "zero", and the polarity is set by microcontroller.		Schmitt input
31	V_{DD}	—	Power supply terminal.		—
32	XI	I	Crystal oscillator connection terminal/External clock input terminal.		—
33	XO	O	Crystal oscillator connection terminal.		—
34	V_{SS}	—	Ground terminal.		—
35	CKSL	I	Clock select terminal. “L”: 384 fs, “H”: 512 fs		Pull-up resistor, Schmitt input
36	PLOFF	I	External oscillation/built-in VCO mode select terminal. “L”: VCO mode “H”: External oscillation mode		Pull-down resistor
37	PD	O	Phase-difference output terminal.		Tri-state output
38	V_{SSA}	—	Analog ground terminal.		—
39	AMPO	O	LPF amplifier output.		—
40	AMPI	I	LPF amplifier input.		—
41	V_{DDA}	—	Analog power supply terminal.		—
42~44	TES0 ~ TES2	I	Test terminal, normally high or open.		Pull-up resistor, Schmitt input
45	$\overline{RST}$	I	Reset signal input terminal.		Pull-up resistor

Pin No.	Symbol	I/O	Description of Pin Functions	Remarks
46	$\overline{CS}$	I	Chip select signal input terminal : when $\overline{CS}$ is at low active, data can be sent from the microcontroller.	Schmitt input
47	IFCD	I	Microcontroller command or data input mode select terminal. “H”: commands, “L”: data.	Schmitt input
48	IFDI	I	Microcontroller data input terminal. Commands and data are received LSB first.	Schmitt input
49	IFDO	O	Data bus (DBUS) data output terminal. Data bus data are sent to microcontroller LSB first.	Open-drain output, Pull-up resister
50	IFCK	I	Shift clock input terminal for microcontroller data.	Schmitt input
51	$\overline{ACK}$	O	Acknowledge signal output terminal for microcontroller. Acknowledge signal output is when command and data parity are OK.	Open-drain output, Pull-up resistor
52	V_{SS}	—	Ground terminal.	—
53~60	TP16 ~ TP9	O	Test data output terminal, normally open.	—

Description Of Operation

1. Timing generator

(1) Crystal oscillator

As Figure 1 shows, the clocks required for internal operations can be generated by connecting a crystal oscillator and capacitor. (PLOFF = "H")

As Figure 2 shows, clocks can also be externally input to the XI terminal.

For external clock purposes, a crystal with a good starting potential and low CI value is recommended.

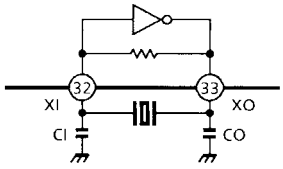


Figure 1
Self-exciting crystal oscillation

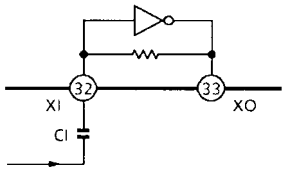


Figure 2
External clock input

(2) Voltage-controlled oscillator (VCO)

The clocks required for internal operations are generated by an built-in VCO. The signal input from the SYNC pin is used as a reference. Configure the phase-locked loop as shown in Figure 3. A phase-difference (PD) signal is output from the PD terminal.

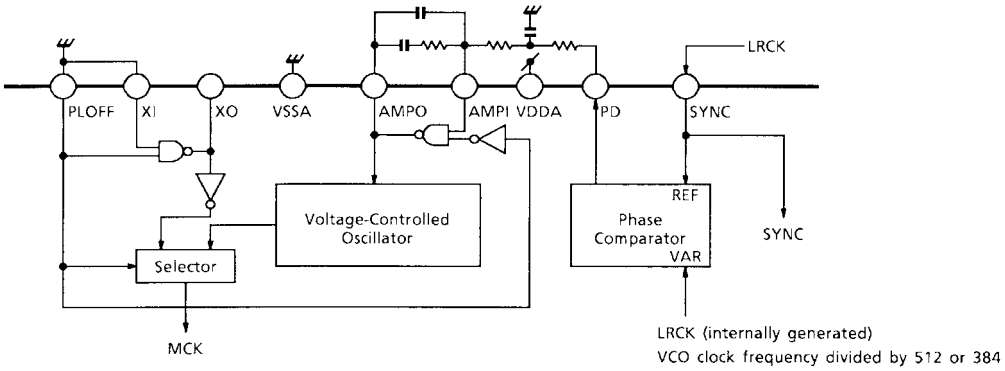


Figure 3 Example of configuration of a basic PLL circuit

(2-1) Phase-difference output

A phase-difference (PD) signal between the REF and VAR signals are output from the PD terminal the PD signal as shown in Figure 4 below.

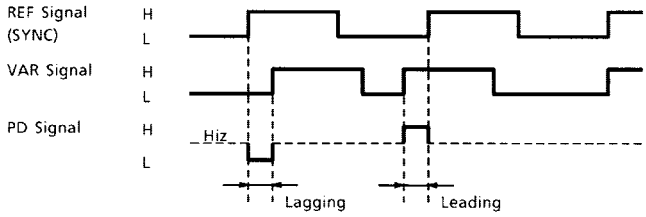


Figure 4 Example of phase-difference output timing

2. Setting audio data input/output format (data, channel clock, and bit clock)

The 16 bit/24 bit serial data input/output channel clocks (LR, ELRI0~1 and ELRO0~2) and bit clocks (FS64, FS32, EBCI0~1 and EBCO) can be either internally generated or externally input. The mode setting is effected by the microcontroller interface (control register). Figure 4 shows the data input/output clock pulse selector.

(1) The channel clock, bit clock and data format for data inputs SDI0~1 are selected by LRIS0~1, BCIS0~1 and SIFMT0~1 of control register 2 (CNT-R2). Table 1 (a) and (b) show setting modes for data inputs SDI0~1.

Table 1 (a) Setting modes for data input SDI0

Control Register 2 (CNT-R2)			Format for Data Input SDI0			
LRIS0	BCIS0	SIFMT0	Data	Bit Clock	Channel Clock	Data Format
0	0	0	16 bit	32 fs (FS32 terminal) Internally generated	LR terminal Internally generated	MSB first
0	0	1				LSB first
0	1	0	24 bit	64 fs (FS64 terminal) Internally generated	LR terminal Internally generated	MSB first, effective data before the change point of LRCK
0	1	1				LSB first, effective data before the change point of LRCK
1	0	0	16 bit	32 fs (EBCI0 terminal) Externally input terminal	ELRI0 terminal Externally input terminal	MSB first
1	0	1				LSB first
1	1	0	24 bit	48/64 fs (EBCI0 terminal) Externally input terminal	ELRI0 terminal Externally input terminal	MSB first, effective data before the change point of LRCK
1	1	1				LSB first, effective data before the change point of LRCK

Table 1 (b) Setting modes for data input SDI1

Control Register 2 (CNT-R2)			Format for Data Input SDI1			
LRIS1	BCIS1	SIFMT1	Data	Bit Clock	Channel Clock	Data Format
0	0	0	16 bit	32 fs (FS32 terminal) Internally generated	LR terminal Internally generated	MSB first
0	0	1				LSB first
0	1	0	24 bit	64 fs (FS64 terminal) Internally generated	LR terminal Internally generated	MSB first, effective data before the change point of LRCK
0	1	1				LSB first, effective data before the change point of LRCK
1	0	0	16 bit	32 fs (EBCI1 terminal) Externally input terminal	ELRI1 terminal Externally input terminal	MSB first
1	0	1				LSB first
1	1	0	24 bit	48/64 fs (EBCI1 terminal) Externally input terminal)	ELRI1 terminal Externally input terminal	MSB first, effective data before the change point of LRCK
1	1	1				LSB first, effective data before the change point of LRCK

(2) The channel clock, bit clock and data format for data outputs SDO0~2 are selected by LROS0~2, BCOS02 and SOFMT0~1 of control register 2 (CNT-R2).
Table 2 (a), (b), and (c) show setting modes for data outputs SDO0-2.

Table 2 (a) Setting modes for data output SDO0

(*: Don't care)

Control Register					Formats for Data Output SDO0				
CNT-R2				CNT-R1	Data	Bit Clock		Channel Clock	Data Format
LROS0	BCOS0	SOFMT0	LROS2	EBCS					
0	0	0	*	0	16 bit	32 fs (FS32 terminal) Internally generated		LR terminal Internally generated	MSB first
0	1	0	*	0	24 bit	64 fs (FS64 terminal) Internally generated		LR terminal Internally generated	MSB first, effective data after the change point of LRCK
*	0	0	*	1	16 bit	32 fs (FS32 terminal) 1/ 2 of EBCI0 (64 fs)		ELRO terminal Internally generated	MSB first
*	1	1	0	0	24 bit	64 fs (FS64 terminal) Internally generated		LR terminal Internally generated (Note 1)	MSB first, effective data after the change point of LRCK (8 clock shift output)
1	*	0	*	0	16 bit	32 fs	EBCO terminal Externally input	ELRO terminal Externally input	MSB first
					24 bit	48 fs			MSB first, effective data after the change point of LRCK
						64 fs			
1	*	1	1	0	16 bit	48 fs	EBCO terminal Externally input	ELRO terminal Externally input	MSB first, effective data after the change point of LRCK (8 clock shift output)
					24 bit	64 fs			

Note 1: Clock output from LR terminal is input to ELRO terminal.

Table 2 (b) Setting modes for data output SDO1

(*: Don't care)

Control Register					Formats for Data Output SDO1				
CNT-R2				CNT-R1	Data	Bit Clock		Channel Clock	Data Format
LROS1	BCOS1	SOFMT1	LROS2	EBCS					
0	0	0	*	0	16 bit	32 fs (FS32 terminal) Internally generated		LR terminal Internally generated	MSB first
0	1	0	*	0	24 bit	64 fs (FS64 terminal) Internally generated		LR terminal Internally generated	MSB first, effective data after the change point of LRCK
*	0	0	*	1	16 bit	32 fs (FS32 terminal) 1/ 2 of EBCI0 (64 fs)		ELRO terminal Internally generated	MSB first
*	1	1	0	0	24 bit	64 fs (FS64 terminal) Internally generated		LR terminal Internally generated (Note 1)	MSB first, effective data after the change point of LRCK (8 clock shift output)
1	*	0	*	0	16 bit	32 fs	EBCO terminal Externally input	ELRO terminal Externally input	MSB first
					24 bit	48 fs			MSB first, effective data after the change point of LRCK
						64 fs			
1	*	1	1	0	16 bit	48 fs	EBCO terminal Externally input	ELRO terminal Externally input	MSB first, effective data after the change point of LRCK (8 clock shift output)
					24 bit	64 fs			

Note 1: Clock output from LR terminal is input to ELRO terminal.

Table 2 (c) Setting modes for data output SDO2

(*: Don't care)

Control Register				Formats for Data Output SDO2				
CNT-R2			CNT-R1	Data	Bit Clock		Channel Clock	Data Format
LROS2	BCOS2	SOFMT2	EBCS					
0	0	0	0	16 bit	32 fs (FS32 terminal) Internally generated		LR terminal Internally generated	MSB first
0	1	0	0	24 bit	64 fs (FS64 terminal) Internally generated		LR terminal Internally generated	MSB first, effective data after the changepoint of LRCK
*	0	0	1	16 bit	32 fs (FS32 terminal) 1/ 2 of EBCI0 (64 fs)		ELRO terminal Internally generated	MSB first
0	1	1	0	24 bit	64 fs (FS64 terminal) Internally generated		LR terminal Internally generated (Note 1)	MSB first, effective data after the change point of LRCK (8 clock shift output)
1	*	0	0	16 bit	32 fs	EBCO terminal Externally input	ELRO terminal Externally input	MSB first
				24 bit	48 fs			MSB first, effective data after the change point of LRCK
					64 fs			
1	*	1	0	16 bit	48 fs	EBCO terminal Externally input	ELRO terminal Externally input	MSB first, effective data after the change point of LRCK (8 clock shift output)
				24 bit	64 fs			

Note 1: Clock output from LR terminal is input to ELRO terminal.

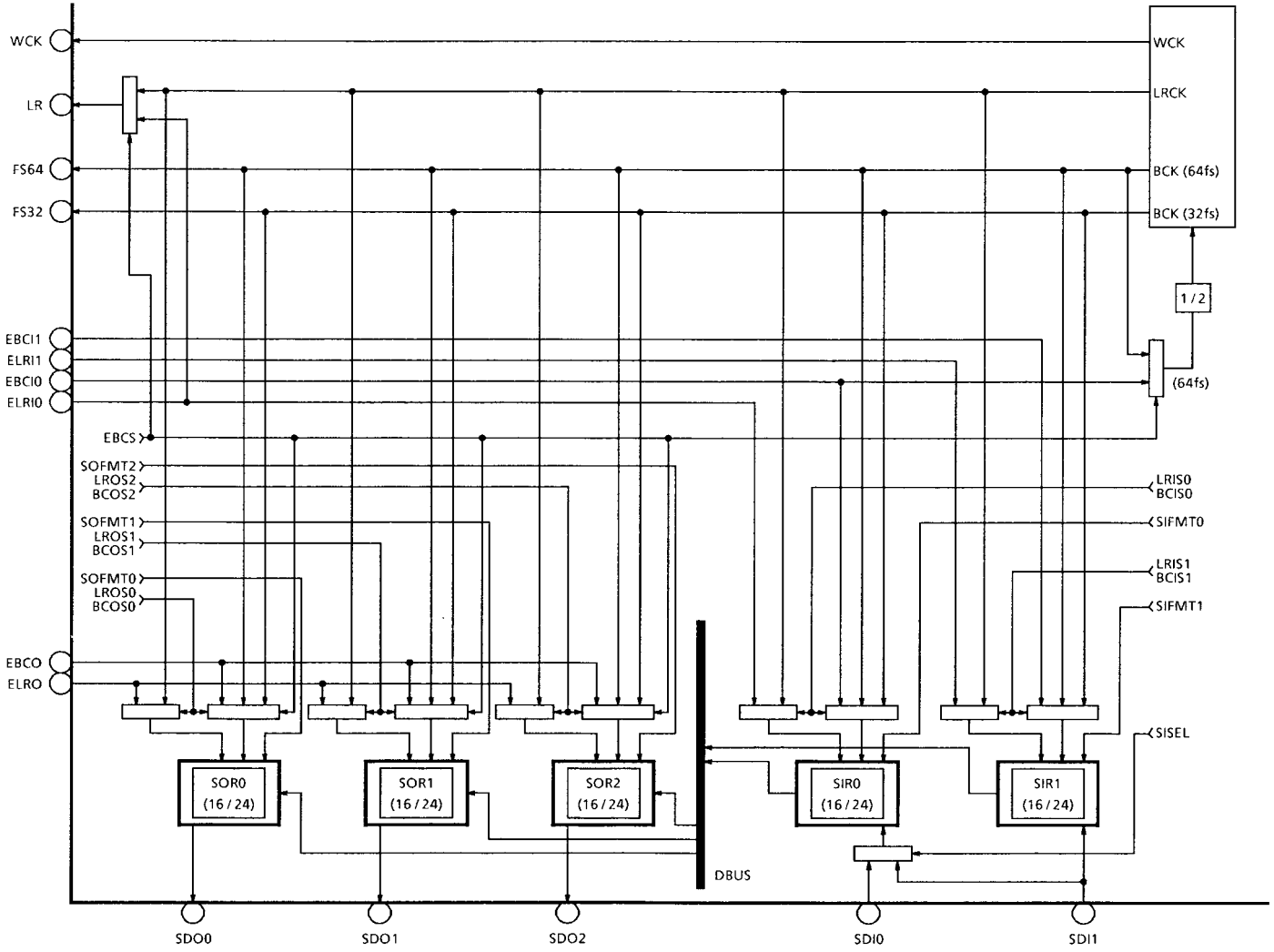


Figure 5 Data input/output clock selector

3. Data input and output circuits

(1) Data input circuits

(1-1) Data input

Data are input in twos complement form, MSB first or LSB first, effective data before the change point of LRCK.
Input registers SIR0 and SIR1 are selectable for either 16 bit or 24 bit data length. The channel clock (LRCK) and bit clock (BCK) signals can be externally input independently as the timing signals for the data input to registers SIR0 and SIR1.
Mode using internally generated LRCK and BCK signals is also provided.
Input data are fetched by sensing the rise and fall of LRCK.
Input register SIR0 can select between input data SDI0 and SDI1 using the control registers of the microcontroller interface.

(1-2) Data input formats

- When input data are 16 bit/channel, see Figure 6 (a).
  When BCK is 32 fs, input is MSB first or LSB first.
- When input data is 24 bit/channel, see Figures 6 (b) and 6 (c).
  When BCK is 48 fs (external input), input is MSB first or LSB first.
  When BCK is 64 fs, input is MSB first or LSB first, with effective data before the change point of LRCK.

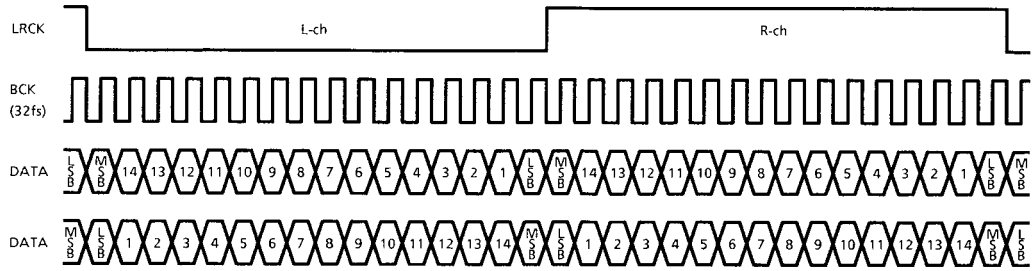


Figure 6 (a) 16 bit data input format

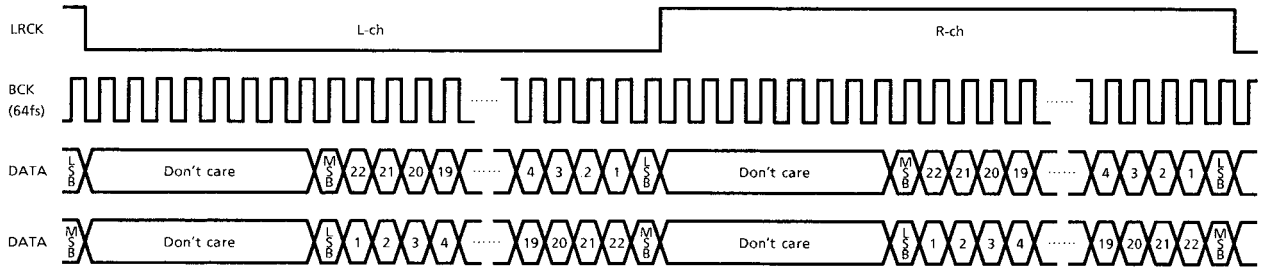


Figure 6 (b) 24 bit data input format

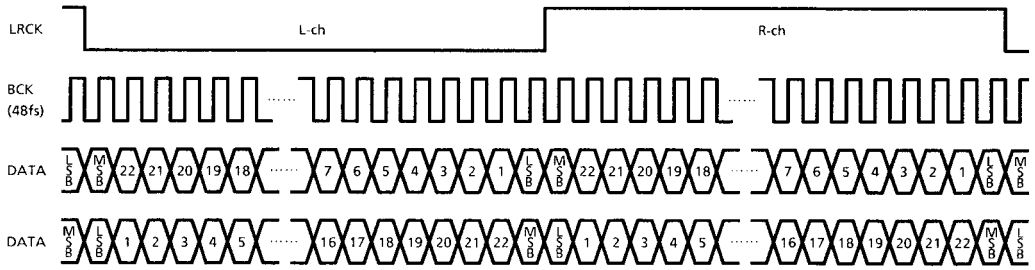


Figure 6 (c) 24 bit data input format

(2) Data output circuits

(2-1) Data output

Data are output in twos complement form, MSB first, with effective data after the change point of LRCK or 8 clock shift with effective data before the change point of LRCK.
Output registers SOR0, SOR1 and SOR2 are selectable for either 16 bit or 24 bit data.
The channel clock (LRCK) and bit clock (BCK) signals can be externally input independently as the timing signals for the data output to registers SOR0, SOR1 and SOR2.
Mode using internally generated LRCK and BCK signals is also provided.
Input data are output to registers SOR0, SOR1 and SOR2 by sensing the rise and fall of LRCK.
Output register SIR0 can select between output data SDI0 and SDI1 using the control registers of the microcontroller interface.

(2-2) Data output formats

16 bit or 24 bit data are output from the data bus starting from the MSB.

- When output data are 16 bit/channel, see Figure 7 (a).
  When BCK is 32 fs, output is MSB first.
- When output data are 24 bit/channel, see Figures 7 (b) and 7 (c).
  When BCK is 48 fs (external output), output is MSB first or the 8 clock shifted highest 16 bit data with effective data before the change point of LRCK.
  When BCK is 64 fs, output is MSB first with effective data after the change point of LRCK or 8 clock shift with effective data before the change point of LRCK.

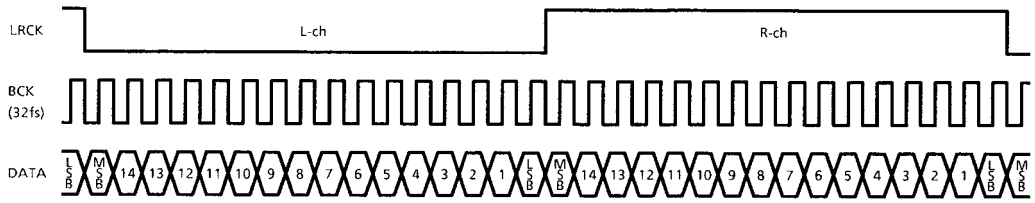


Figure 7 (a) 16 bit data output format

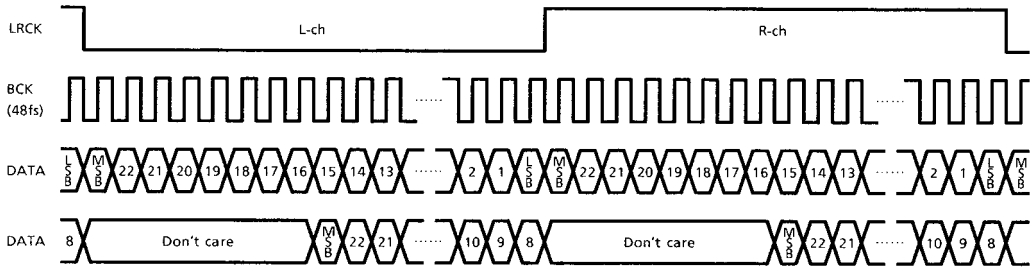


Figure 7 (b) 24 bit data output format

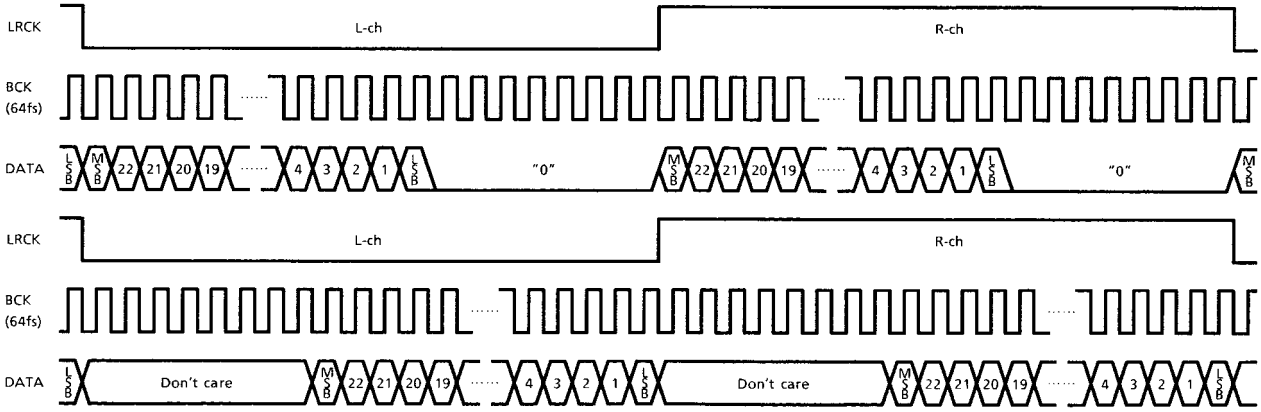


Figure 7 (c) 24 bit data output format

4. Microcontroller interface circuit

The TC9332F transfers synchronous serial data to the host microcontroller using the $\overline{CS}$, IFCD, IFCK, IFDI, IFDO and $\overline{ACK}$ terminals. The microcontroller is used to set data modes, set data in the coefficient RAM (CRAM) and offset RAM (OFRAM), set the module sequencer (MSEQ), and read data from the internal data bus (DBUS).

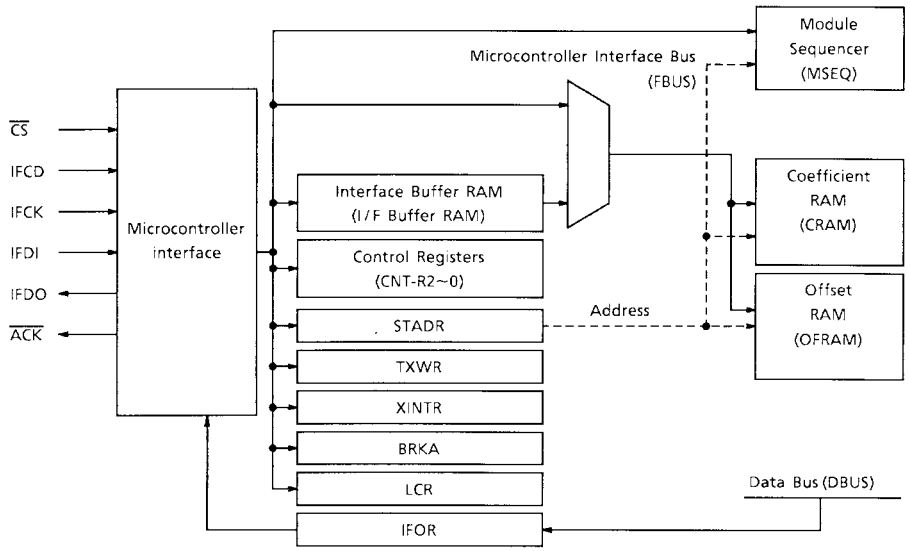


Figure 8 Structure of microcontroller interface block

An example of a connection with the host microcontroller is shown below in Figure 9.

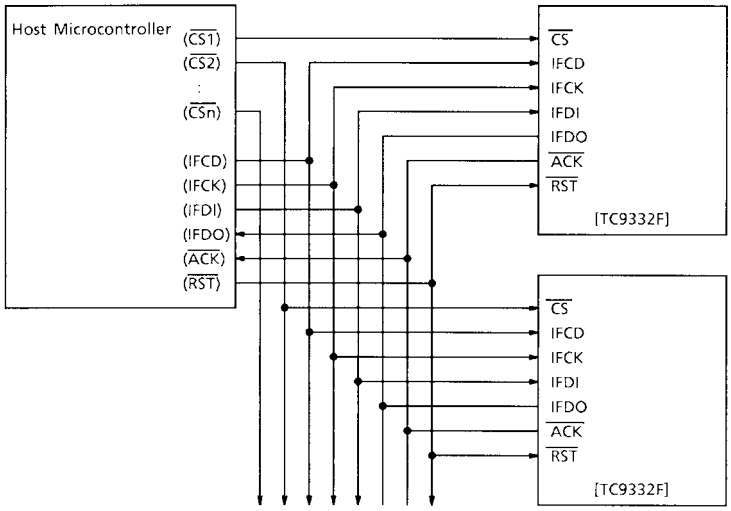


Figure 9 Relationship between host microcontroller and TC9332F

The functions of the signals on the microcontroller interface pins are as shown below:

$\overline{CS}$ signal (input):	Sets TC9332F data receive to active.
IFCD signal (input):	Distinguishes between command words and data words.
IFCK signal (input):	Data signal shift clock
IFDI signal (input):	Data input signal
$\overline{ACK}$ signal (output):	Acknowledges result of parity check.
IFDO signal (output):	Data output signal. Outputs data from the data bus (DBUS) starting from the LSB. Data are output at the rising edge of the IFCK signal.

(1) Data transmission format

At idle, the $\overline{CS}$, IFCD, IFCK and IFDI signals are high-level.

There are two transfer modes that can be used, depending on the length of data to be transferred. There are two types of data transmitted : 1 byte command words, and data words composed of either 1 or 2 bytes. The number of bytes per data word varies according to the command type. Data are transmitted LSB first, and the dummy bit at the MSB of the transmitted data is set to "0".

(1-1) 8 bit transfer mode

Set ICKS on bit 3 of control register 1 to low. (Low is the initial value at reset). Efficient data transfer can be carried out over the serial I/O port of an ordinary microcontroller. Figure10 (a) shows an example of timing for the 8 bit transfer mode.

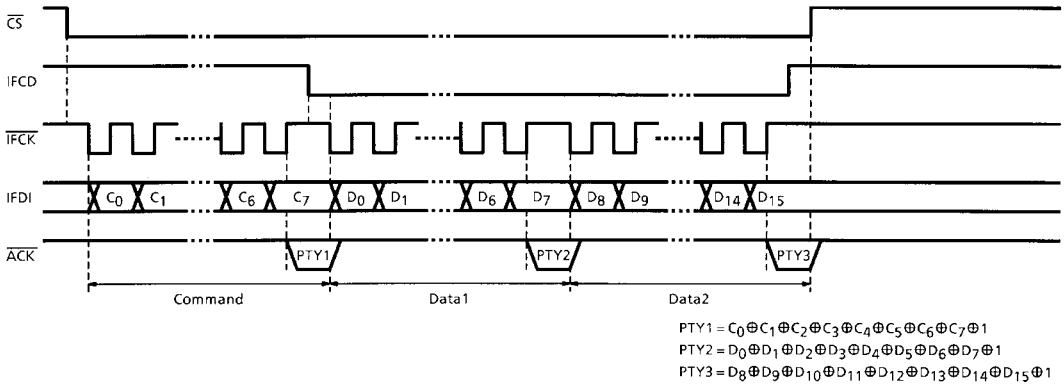


Figure 10 (a) Example of timing for 8 bit transfer mode

(1-2) 9 bit transfer mode

Set ICKS on bit 3 of control register 1 to high. Since low is the initial value at reset, 8 bit data transfer can be performed until ICKS is set to high. The unit of transfer is 9 bit, an 8 bit data plus 1 bit for ODD parity. If the result of the parity check is NG, the TC9332F does not fetch the set data, so always be sure to input the correct parity. Figure 10 (a) shows an example of timing for the 8 bit transfer mode.

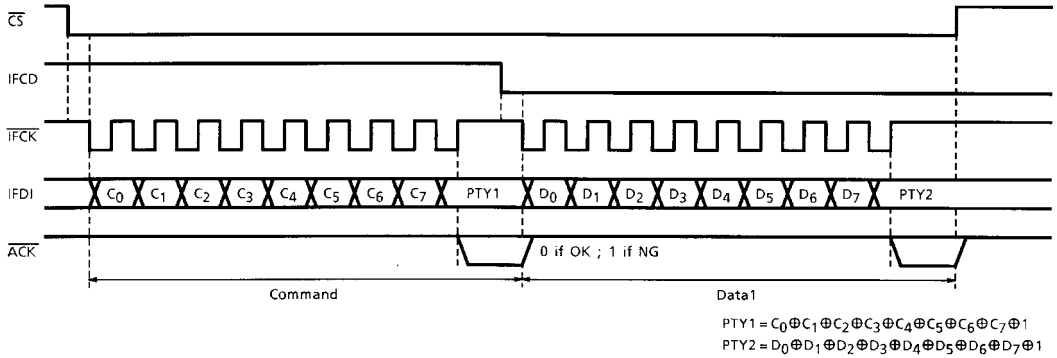


Figure 10 (b) Example of timing for 9 bit transfer mode

(2) Data bus (DBUS) data output format

At idle, the $\overline{CS}$, IFCD, IFCK and IFDI signals are "H" level.

There are two transfer modes that can be used, depending on the length of data to be transferred.

Figure 11 shows examples of timing for the 8 bit and 9 bit transfer modes.

The data transmitted from the microcontroller is a 1 byte command word.

The data output to the microcontroller are the 24 bit on the internal DBUS or the upper 16 bit, and are sent LSB first.

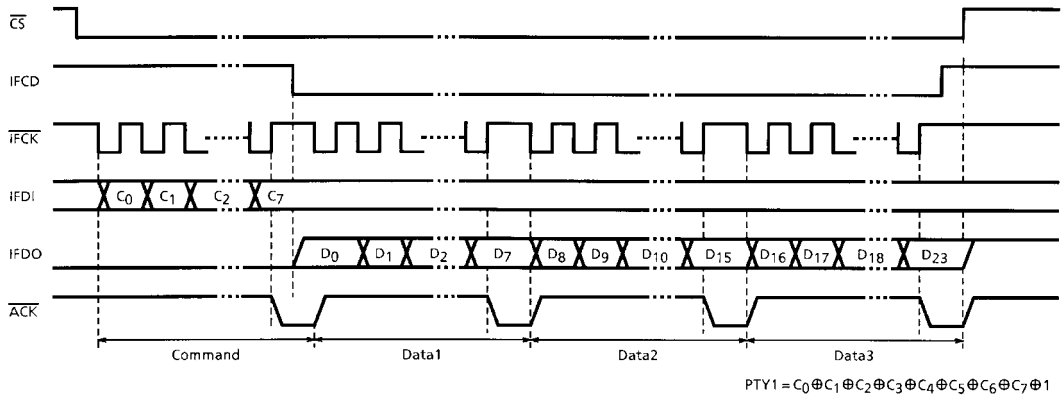


Figure 11 (a) Example of timing for 8 bit transfer mode (3 byte setting)

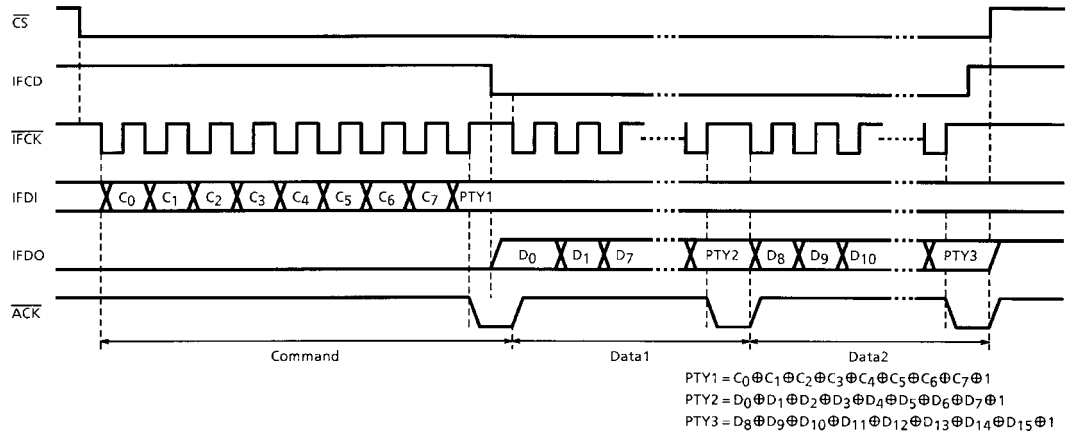


Figure 11 (b) Example of timing for 9 bit transfer mode (2 byte setting)

(3) Control commands

There are 12 commands used to control the TC9332F from a microcontroller. Table 3 shows the commands and command data.

Table 3 Control commands (Note 2)

Commandword (HEX)	Data Word (Exclude Parity Bit)		Register/Memory		Fetch Sync	Continuous Transmission
	Bit Length Used	Bytes Transmitted	Write Destination	Read Source		
FF~20	—	—	Unused	—	—	—
1F	16	2	CNT-R2	—	Async	No
1E	11	2	CNT-R1	—	Async	No
1D	9	2	CNT-R0	—	sync	No
1C	9 9 4	2 2 1	STAD-R	—	Async	No
1B	4	1	TXW-R	—	Async	No
1A	10	2	MSEQ	—	sync	Yes
19	16	2	CRAM	—	Async	Yes
18	16	2	OFRAM	—	Async	Yes
17	3	1	XINT-R	—	sync	No
16	10	2	BRKA-R	—	Async	No
15	8	1	LC-R	—	Async	No
14	24 Upper 16	3 2	—	IFDO-R	—	No
13~00	—	—	Unused	—	—	—

Note 2: Settings for STAD-R (1Ch) are as follows:
9 bit: CRAM address
9 bit: OFRAM address
4 bit: MSEQ address

(4) Control registers and dedicated interface registers

(4-1) Control register 2 (CNT-R2) (Note 3)

(*: default value)

Bit	Symbol	Description of Functions		
15	LRIS1	Selects channel clock or bit clock for audio serial data input from the SDI1 terminal.	0*	Generates internally
			1	ELRI1/EBCI1
14	BCIS1	Selects bit length of audio serial data input from the SDI1 terminal.	0*	16 bit
			1	24 bit
13	SIFMT1	Selects format of audio serial data input from the SDI1 terminal.	0*	MSB first
			1	LSB first
12	LRIS0	Selects a channel clock or bit clock for audio serial data input from the SDI0 terminal.	0*	Generates internally
			1	ELRIO/EBCIO
11	BCIS0	Selects bit length of audio serial data input from the SDI0 terminal.	0*	16 bit
			1	24 bit
10	SIFMT0	Selects format of audio serial data input from the SDI0 terminal.	0*	MSB first
			1	LSB first
9	SISEL	Selects input terminal for input register SDI0.	0*	SDI0
			1	SDI1
8	LROS2	Selects a channel clock or bit clock for audio serial data output to the SDO2 terminal. (Note 4)	0*	Generates internally
			1	ELRO/EBCO
7	BCOS2	Selects an internally generated bit clock for audio serial data output to the SDO2 terminal.	0*	FS32 (16 bit/ch)
			1	FS64 (32 bit/ch)
6	SOFMT2	Selects whether audio serial data output to the SDO2 pin are to be effective data after the change point of LRCK or 8 clock shifted.	0*	Effective data after the change point of LRCK
			1	8 clock shifted
5	LROS1	Selects a channel clock or bit clock for audio serial data output to the SDO1 terminal. (Note 4)	0*	Generates internally
			1	ELRO/EBCO
4	BCOS1	Selects an internally generated bit clock for audio serial data output to the SDO1 terminal.	0*	FS32 (16 bit/ch)
			1	FS64 (32 bit/ch)
3	SOFMT1	Selects whether audio serial data output to the SDO1 terminal are to be effective data after the change point of LRCK or 8 clock shifted.	0*	Effective data after the change point of LRCK
			1	8 clock shifted
2	LROS0	Selects a channel clock or bit clock for audio serial data output to the SDO0 terminal. (Note 4)	0*	Generates internally
			1	ELRO/EBCO terminal input
1	BCOS0	Selects an internally generated bit clock for audio serial data output to the SDO0 terminal.	0*	FS32 (16 bit/ch)
			1	FS64 (32 bit/ch)
0	SOFMT0	Selects whether audio serial data output to the SDO0 terminal are to be effective data after the change point of LRCK or 8 clock shifted.	0*	Effective data after the change point of LRCK
			1	8 clock shifted

Note 3: Normally set only once at initialization.
Data can be set in CNT-R2 asynchronously with the SYNC signal.

Note 4: When a channel clock or bit clock is externally input, (LROS bits 2~0 set to “1”), the data can be output to pins SDO2~0 with 8 clock shifted by setting SOFMT~0.
Data can also be output with 8 clock shifted by program (operation) without the above setting.

(4-2) Control register 1 (CNT-R1) (Note 5)

(*: default value)

Bit	Symbol	Description of Functions		
10	ZST	Switches coefficient ROM mode table for inverse logarithm of a number.	0	2-cycle
			1*	1-cycle
9	EMU	Test emulator mode	0*	Normal
			1	SYNC = ELRI1
8	SYNCS	Selects internal generation or external input (from SYNC terminal) of SYNC signal.	0*	Generates internally
			1	Inputs externally
7	SYNCP	Switches SYNC signal polarity.	0*	Fall
			1	Rise
6	SYRC	Resets the coefficient pointer (CP) for each SYNC signal.	0*	Enable
			1	Disable
5	SYRO	Resets the offset address pointer (OFP) for each SYNC signal.	0*	Enable
			1	Disable
4	EBCS	Modifies LROS2~0, BCOS2~0 and LR terminal output signals.	0*	Disable (normal)
			1	Enable
3	ICKS	Selects transfer data length by microcontroller interface.	0*	8 bit
			1	9 bit
2	IFOS	Selects output format for data (24 bit) read from IFOR (DBUS).	0*	Upper 16 bit
			1	24 bit
1	DLSEP	Divides the delay RAM (DLRAM) into a delay area and a data table area.	0*	Divides.
			1	Does not divide.
0	ACMPRQ	Overwrites when the value of the CRAM or OFRAM pointer matches the overwrite counter address (automatically set to " 0" after executing batch overwrite of the interface buffer RAM.)	0*	Disable
			1	Enable

Note 5: Normally set only once at initialization.
Data can be set in CNT-R1 asynchronously with the SYNC signal.

(4-3) Control register 0 (CNT-R0) (Note 6)

(*: default value)

Bit	Symbol	Description of Functions		
8	SQALL	Renders instruction non-operative and clears the flag.	0	Off (RUN)
			1*	On (NOP)
7	BRKRQ	Setting this bit to "1" after the break address (BRKA) of the program counter is set executes a break.	0*	Break off
			1	Break on
6	DBMRQ	Requests data read from DBUS.	0*	Does not request.
			1	Requests.
5	LCMSK	Compares the loop counter value during data read from DBUS.	0*	Compares.
			1	Does not compare.
4	LCSEL	Selects the counter (LC0 or LC1) to be compared when comparing the loop counter value during data read from DBUS.	0*	LC0
			1	LC1
3	INMT	Mutes input from the SDI0 and SDI1 terminals.	0	Mute off
			1*	Mute on
2	OUTMT2	Mutes output to the SDO2 terminal.	0	Mute off
			1*	Mute on
1	OUTMT1	Mutes output to the SDO1 terminal.	0	Mute off
			1*	Mute on
0	OUTMT0	Mutes output to the SDO0 terminal.	0	Mute off
			1*	Mute on

Note 6: Data are read from CNT-R0 synchronously with the SYNC signal.

(4-4) Dedicated interface registers

Start address register (STADR) (Note 7)

This register sets the address to start writing data to CRAM, OFRAM and MSEQ. It consists of a presettable up-counter. (9 bit)

	8	7	6	5	4	3	2	1	0
CRAM	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
OFRAM	0	0	0	RA5	RA4	RA3	RA2	RA1	RA0
MSEQ	don't care					RA3	RA2	RA1	RA0

When data are set in MSEQ, data are sent 1 byte at a time.

Note 7: Data are set in STADR asynchronously with the SYNC signal.

Transfer exchange write address register (TXWR) (Note 8)

When ACMPRQ in control register 1 (CNT-R1) is set to "1", this register sets the length of data to be overwritten to CRAM or OFRAM using interface buffer RAM.
Overwrites up to 16 word are supported. (4 bit)

Number Of Words Overwritten	TXWR			
	TXW3	TXW2	TXW1	TXW0
1	0	0	0	0
2	0	0	0	1
...	...			
15	1	1	1	0
16	1	1	1	1

Note 8: Data can be set in TXWR asynchronously with the SYNC signal.

Module sequencer (MSEQ) (Note 9)

The module sequencer sets the sequence in which the subroutines grouped in program ROM are called.
It has a 16 word × 10 bit structure, and data are set by the microcontroller one word at a time at the program ROM sequence start address. Set the 4 bit address of the sequencer, which sets the data store sequence, in STADR.
Data cannot be transferred to the MSEQ using the interface buffer RAM.,

Note 9: MSEQ data is read in synchronously with the SYNC signal.

Coefficient RAM (CRAM) (Note 10)

The coefficient RAM has a 320 word × 16 bit structure, and data can be changed one word at a time during each sampling period by the microcontroller communication procedure. Using the interface buffer RAM, 16 word can be overwritten during each sampling period.

Note 10: Data can be set in CRAM asynchronously with the SYNC signal. (during continuous setting)

Offset RAM (OFRAM) (Note 11)

The offset RAM has a 64 word × 16 bit structure, and the overwriting procedure is similar to that of the CRAM.

Note 11: Data can be set in OFRAM asynchronously with the SYNC signal. (during continuous setting)

External interrupt register (XINTR) (Note 12)

The external interrupt register sets data in IFF2-0, which are allocated to the conditional jump flag (F) field. (3 bit)

Flag Field			D_2	D_1	D_0
IFF2	IFF1	IFF0			
Off	Off	Off	0	0	0
Off	Off	On	0	0	1
Off	On	Off	0	1	0
On	Off	Off	1	0	0

Note 12: XINTR data are read synchronously with the SYNC signal.

Break address (BRKAR) register (Note 13)

This register sets the break address. Continuous comparison is made with the program counter (PC) and when BRKRQ of the control register is on, program execution is stopped. Since DBUS data are fetched to IFDOR when the value of the PC matches, it is possible to turn BRKRQ off and read the internal data while program execution is in progress. (10 bit)

Note 13: Data can be set in BRKAR asynchronously with the SYNC signal.

Loop counter compare reference register (LCR) (Note 14)

When reading break or DBUS data, either of loop counters LC0 or LC1 is being compared along with the PC value, this register stores the value of the loop counter to be compared. (8 bit)
Which of the loop counters is being compared is set by LCSEL of control register 0 (CNT-R0).
When break or DBUS data have been read, LCR is automatically decremented by 1.

Note 14: Data can be set in LCR asynchronously with the SYNC signal.

Interface data output register (IFDOR)

This is a buffer register that can read DBUS data. (24 bit)
The microcontroller can read data from IFDOR serially from the LSB. It is also possible to read only the upper 16 bit by setting IFOS of control register 1 (CNT-R1).

Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3~6.0	V
Input voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Power dissipation	P_D	1250	mW
Operating temperature	T_{opr}	−40~85	°C
Storage temperature	T_{stg}	−55~150	°C

Electrical Characteristics (unless otherwise specified, Ta = 25°C, V_{DD} = 5 V)

DC characteristics

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating power supply voltage	V_{DD}	—	Ta = −40~85°C	4.75	5.0	5.25	V
Power supply current-1 (no load, external oscillation)	I_{DD1}	—	f_{opr} = 24.576 MHz	—	75	100	mA
			f_{opr} = 18.432 MHz	—	55	75	
Power supply current-2 (no load, VCO oscillation)	I_{DD2}	—	f_{opr} = 24.576 MHz	—	80	100	mA
			f_{opr} = 18.432 MHz	—	65	85	

Clock terminals (XI, XO)

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Input voltage	"H" level	V_{IH1}	—	XI terminal		3.5	—	—	V
	"L" level	V_{IL1}	—			—	—	1.5	
Output voltage	"H" level	V_{OH1}	—	I_{OH} = −3.0 mA	XO terminal	4.5	—	—	V
	"L" level	V_{OL1}	—	I_{OL} = 6.0 mA		—	—	0.5	
Operation power supply voltage		Rfb	—	—		—	100	500	kΩ

Input terminals

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Input voltage	"H" level	V_{IH2}	—	(Note 15)		4.2	—	—	V
	"L" level	V_{IL2}	—			—	—	0.8	
Input leakage current	"H" level	I_{IH2}	—	V_{IN} = V_{DD}	(Note 15)	—	—	10	μA
	"L" level	I_{IL2}	—	V_{IN} = 0 V		−10	—	—	
Threshold voltage	"H" level	V_P	—	(Note 16)		—	3.2	—	V
	"L" level	V_N	—			—	1.8	—	
Hysteresis voltage		V_H	—	(Note 16)		—	0.6	—	V
Input leakage current	"H" level	I_{IH3}	—	V_{IN} = V_{DD}	(Note 16)	—	—	10	μA
	"L" level	I_{IL3}	—	V_{IN} = 0 V		−10	—	—	

Note 15: SDI0~1, PLOFF, $\overline{RST}$: CKSL, TEST0~2 (Schmitt input terminals with pull-up resistor)

Note 16: SYNC, ELRI0~1, ELRO, EBCI0~1, EBCO, $\overline{CS}$, IFCD, IFDI, IFCK (Schmitt input terminals)

Output terminals

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Output voltage	"H" level	V_{OH2}	—	I_{OH} = −1.0 mA	(Note 17)	4.5	—	—	V
	"L" level	V_{OL2}	—	I_{OL} = 1.0 mA		—	—	0.5	
Output voltage	"H" level	V_{OH3}	—	I_{OH} = −3.0 mA	(Note 18)	4.5	—	—	V
	"L" level	V_{OL3}	—	I_{OL} = 5.0 mA		—	—	0.5	
Output voltage	"H" level	V_{OH4}	—	I_{OH} = −0.6 mA	(Note 19)	4.5	—	—	V
	"L" level	V_{OL4}	—	I_{OL} = 0.6 mA		—	—	0.5	

Note 17: SDO0~2

Note 18: FS64, FS32, WCK, LR

Note 19: AMPO

Three state output terminals (PD)

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Output voltage	"H" level	V_{OH5}	—	I_{OH} = −3.0 mA	—	4.5	—	—	V
	"L" level	V_{OL5}	—	I_{OL} = 5.0 mA		—	—	0.5	
Output off-leakage current		IOZ5	—	V_{OH} = V_{DD}, V_{OL} = 0 V		—	—	±10	μA

Open-drain output terminals (IFDO, $\overline{ACK}$)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
"L" level output voltage	V_{OL7}	—	I_{OL} = 5.0 mA	—	—	0.5	V
Output open leakage current	IOZ7	—	V_{OH} = V_{DD}	—	—	±10	μA

Pull-up and pull-down resistor terminals

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Pull-up resistor	RUP	—	(Note 20)	—	35	200	kΩ
Pull-down resistor-1	Rdwn1	—	(Note 21)	—	25	200	kΩ
Pull-down resistor-2	Rdwn2	—	(Note 22)	—	0.25	80	kΩ

Note 20: IFDO, $\overline{RST}$, $\overline{ACK}$, CKSL, TES0~2

Note 21: PLOFF

Note 22: XI

AC characteristics

External clock input terminal (XI)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
XI clock cycle	t_{XI}	—	—	40	—	—	ns
XI clock "H" duration	t_{XIH}	—	—	—	20	—	ns
XI clock "L" duration	t_{XIL}	—	—	—	20	—	ns

Reset terminal ($\overline{RST}$)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Stand-by time	t_{ST}	—	—	250	—	—	μs
Reset pulse width	t_{RST}	—	—	0.15	—	—	μs

Audio serial interface (fs = 48 kHz)

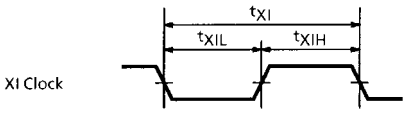
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
ELRI holding time	t_{LIH}	—	C_L = 30 pF	−75	—	75	ns
SDI data setup time	t_{DIS}	—	C_L = 30 pF	50	—	—	ns
SDI data hold time	t_{DIH}	—	C_L = 30 pF	50	—	—	ns
EBCI clock cycle	t_{EBCI}	—	C_L = 30 pF	325	—	—	ns
EBCI clock “H” duration	t_{EBIH}	—	C_L = 30 pF	162	—	—	ns
EBCI clock “L” duration	t_{EBIL}	—	C_L = 30 pF	162	—	—	ns
ELRO hold time	t_{LOH}	—	C_L = 30 pF	−75	—	75	ns
SDO data output delay time (1)	t_{DO1}	—	C_L = 30 pF	—	—	65	ns
SDO data output delay time (2)	t_{DO2}	—	C_L = 30 pF	—	—	65	ns
EBCO clock cycle	t_{EBCO}	—	C_L = 30 pF	325	—	—	ns
EBCO clock “H” duration	t_{EBOH}	—	C_L = 30 pF	162	—	—	ns
EBCO clock “L” duration	t_{EBOL}	—	C_L = 30 pF	162	—	—	ns
WCK output delay time (1)	t_{DHL1}	—	C_L = 30 pF	—	—	13	ns
LR output delay time (1)	t_{DHL2}	—	C_L = 30 pF	—	—	17	ns
FS32 output delay time (1)	t_{DHL3}	—	C_L = 30 pF	—	—	6	ns
WCK output delay time (2)	t_{DLH1}	—	C_L = 30 pF	—	—	23	ns
LR output delay time (2)	t_{DLH2}	—	C_L = 30 pF	—	—	27	ns
FS32 output delay time (2)	t_{DLH3}	—	C_L = 30 pF	—	—	17	ns
BCK clock cycle	t_{BCK}	—	C_L = 30 pF	650	—	—	ns
BCK clock “H” duration	t_{BCH}	—	C_L = 30 pF	325	—	—	ns
BCK clock “L” duration	t_{BCL}	—	C_L = 30 pF	325	—	—	ns

Microcontroller interface

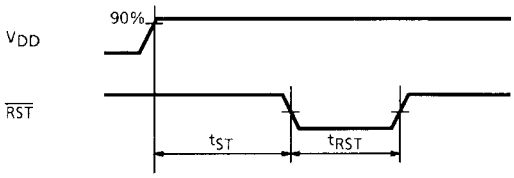
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
$\overline{CS}$ ↓ - IFCK↓ setup time	t_1	—	C_L = 10pF, T = 1/ system clock	6T	—	—	ns
I/F clock “H” duration	t_2	—	C_L = 10pF, T = 1/ system clock	6T	—	—	ns
I/F clock “L” duration							
IFCK↑ - IFCD↓ setup time	t_3	—	C_L = 10pF, T = 1/ system clock	6T	—	—	ns
IFCD↓ - IFCK↓ setup time	t_4	—	C_L = 10pF, T = 1/ system clock	6T	—	—	ns
IFCK↑ - IFCD↑ setup time	t_5	—	C_L = 10pF, T = 1/ system clock	6T	—	—	ns
IFCK↑ - $\overline{CS}$ ↑ setup time	t_6	—	C_L = 10pF, T = 1/ system clock	6T	—	—	ns
$\overline{CS}$ “H” duration	t_7	—	C_L = 10pF	1/fs	—	—	μs
IFDI data setup time	t_8	—	C_L = 10pF, T = 1/ system clock	1T	—	—	ns
IFDI data hold time	t_9	—	C_L = 10pF, T = 1/ system clock	5T	—	—	ns
IFCK↓ - IFDO↑ propagation delay time	t_{10}	—	C_L = 10pF, T = 1/ system clock	—	—	168T	ns
IFCK↓ - IFDO↓ propagation delay time				—	—	10T	ns
IFCK↑ - $\overline{ACK}$ ↓ propagation delay time	t_{11}	—	C_L = 10pF, T = 1/ system clock	—	—	18T	ns
IFCK↓ - $\overline{ACK}$ ↑ propagation delay time	t_{12}	—	C_L = 10pF, T = 1/ system clock	—	—	168T	ns
$\overline{CS}$ ↑ - $\overline{ACK}$ ↑ propagation delay time	t_{13}	—	C_L = 10pF, T = 1/ system clock	—	—	168T	ns
$\overline{CS}$ ↑ - IFDO↑ propagation delay time	t_{14}	—	C_L = 10pF, T = 1/ system clock	—	—	168T	ns
IFCD↓ - $\overline{CS}$ ↓ setup time	t_{15}	—	C_L = 10pF, T = 1/ system clock	2T	—	—	ns
IFDO↓ - $\overline{CS}$ ↓ setup time	t_{16}	—	C_L = 10pF	0	—	—	ns

AC Characteristics Measurement Points

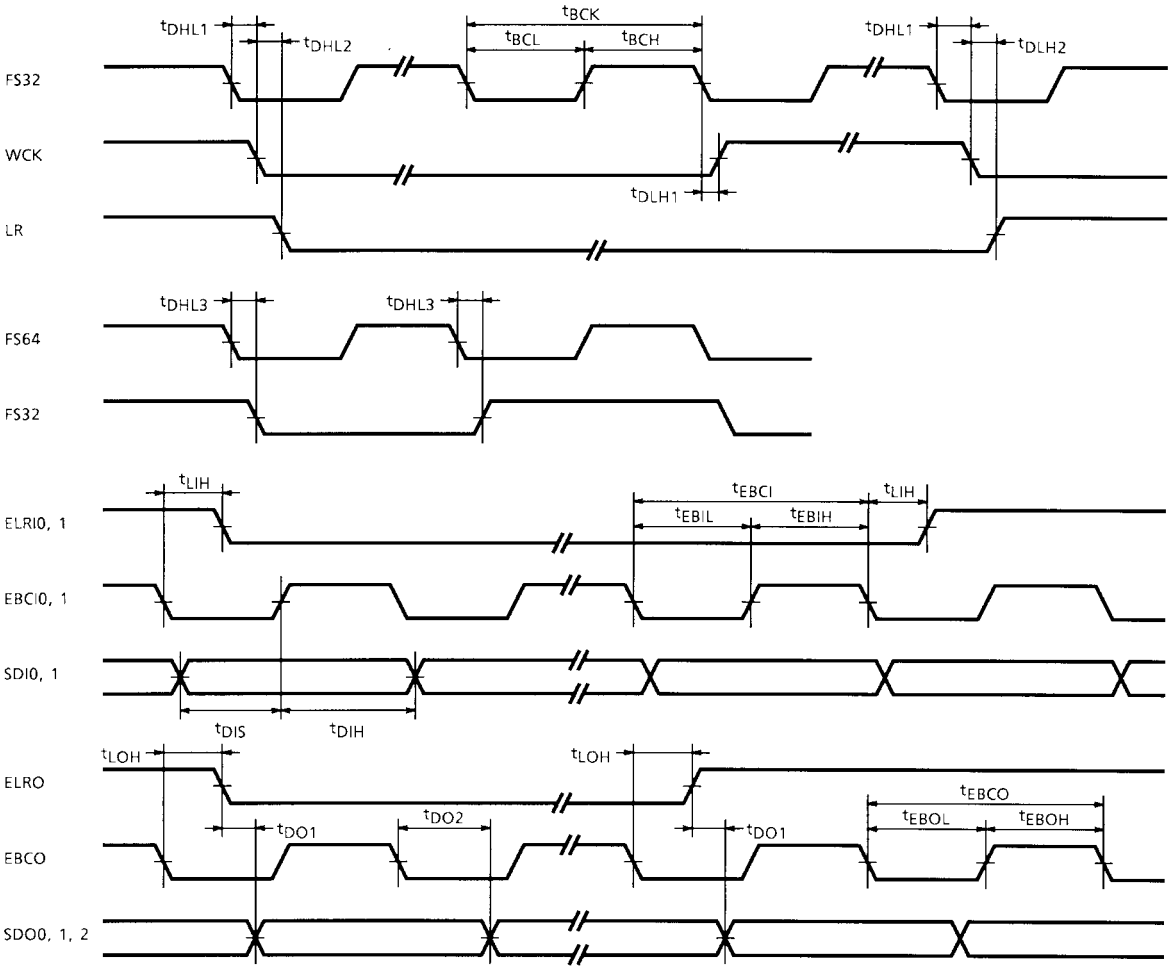
1. External clock input terminal



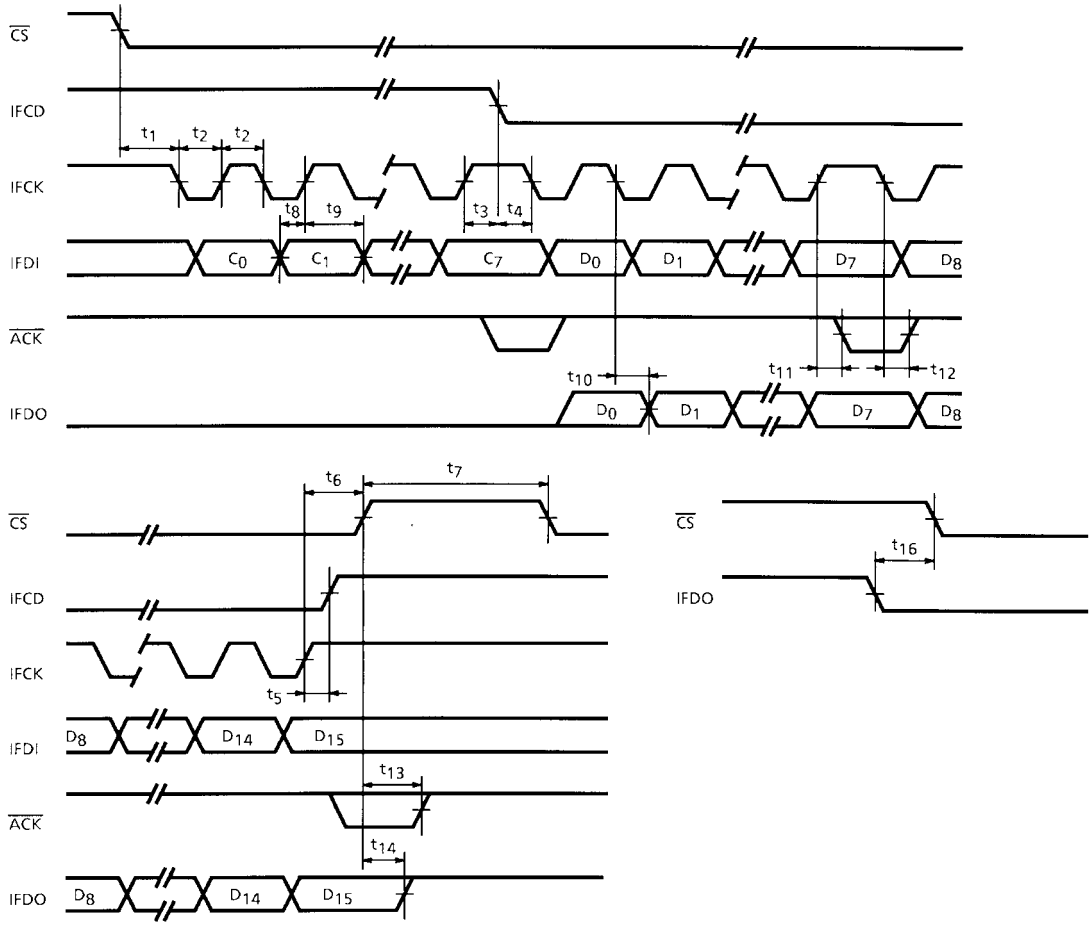
2. Reset terminal



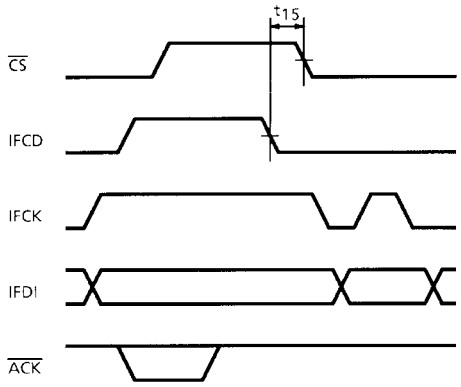
3. Audio serial interface



4. Microcontroller interface

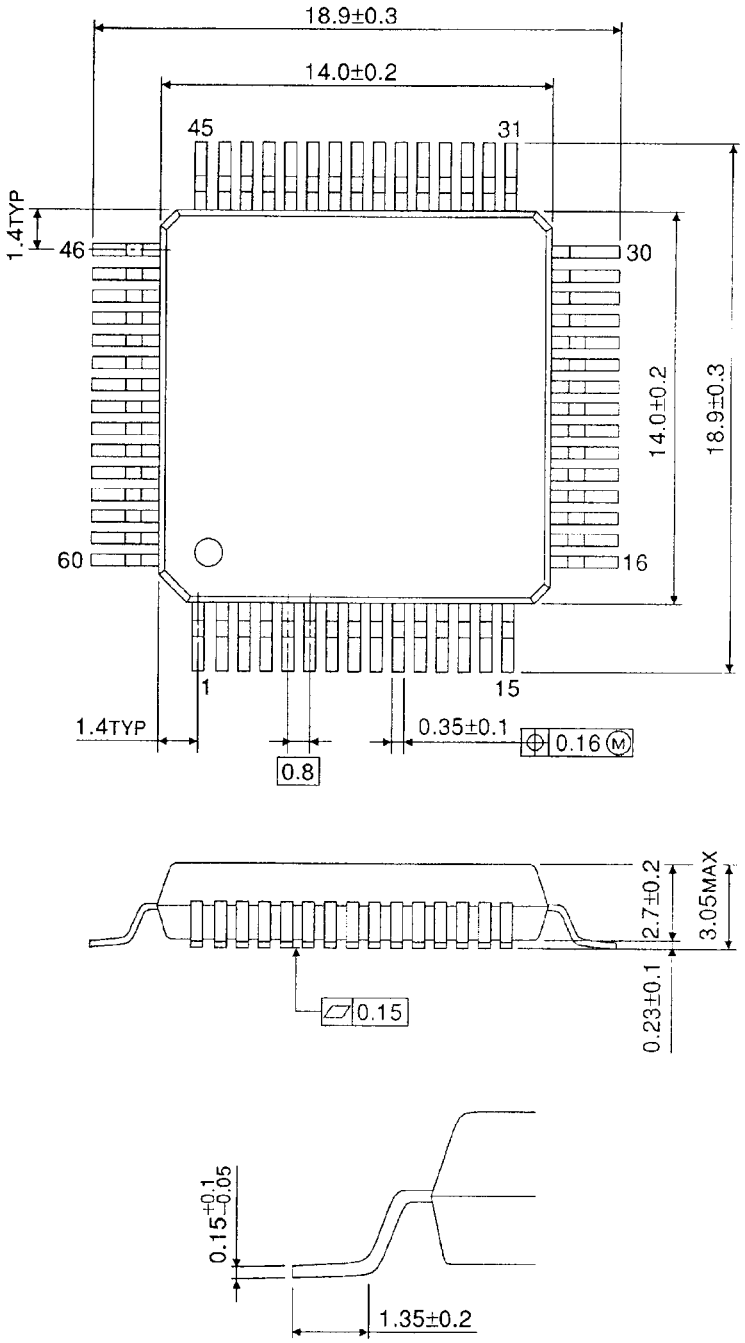


At series transfer mode



Package Dimensions

QFP60-P-1414-0.80D Unit : mm



Weight: 1.08 g (typ.)

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