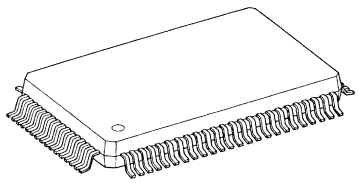
Preliminary TOSHIBA CMOS DIGITAL INTEGRATED CIRCUITS SILICON MONOLITHIC

TC90A74F

NICAM AUDIO SIGNAL PROCESSORS

These LSIs are designed to decode PCM and FM aural signals in UK sound multiplex broadcasts (NICAM728).
The QPSK modulating signal in UK sound multiplex broadcasts are capable of doing digital QPSK demodulation and PCM decoding, and also can demodulate 1-channel FM sound signal. (Simultaneous NICAM and FM outputs are not supported.)
Using a digital PLL for QPSK demodulation and a digital OSC for FM demodulation, these can modulate I, B / G and any carrier used, with a single crystal. In addition, they allow for significant reduction in external part counts and materialize adjustment-free operation.



QFP80-P-1420-0.80B

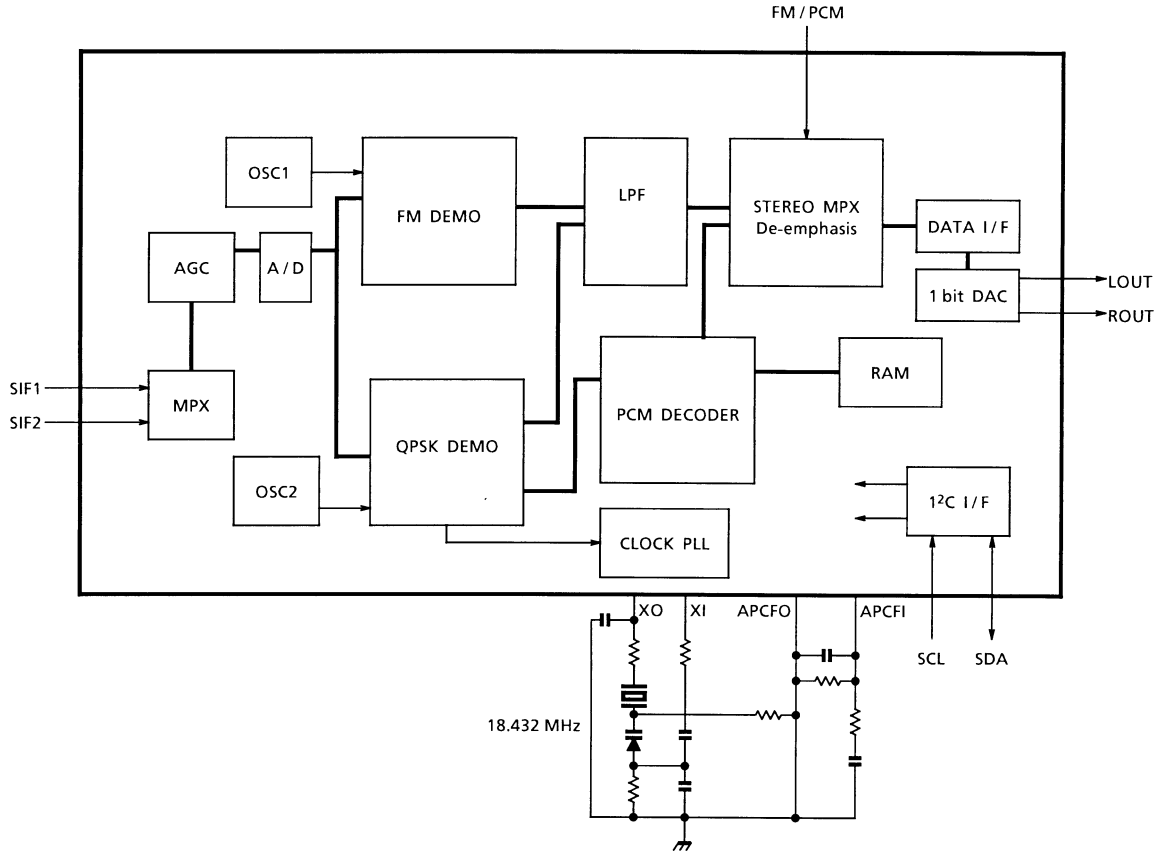
Weight: 1.6 g (Typ.)

FEATURES

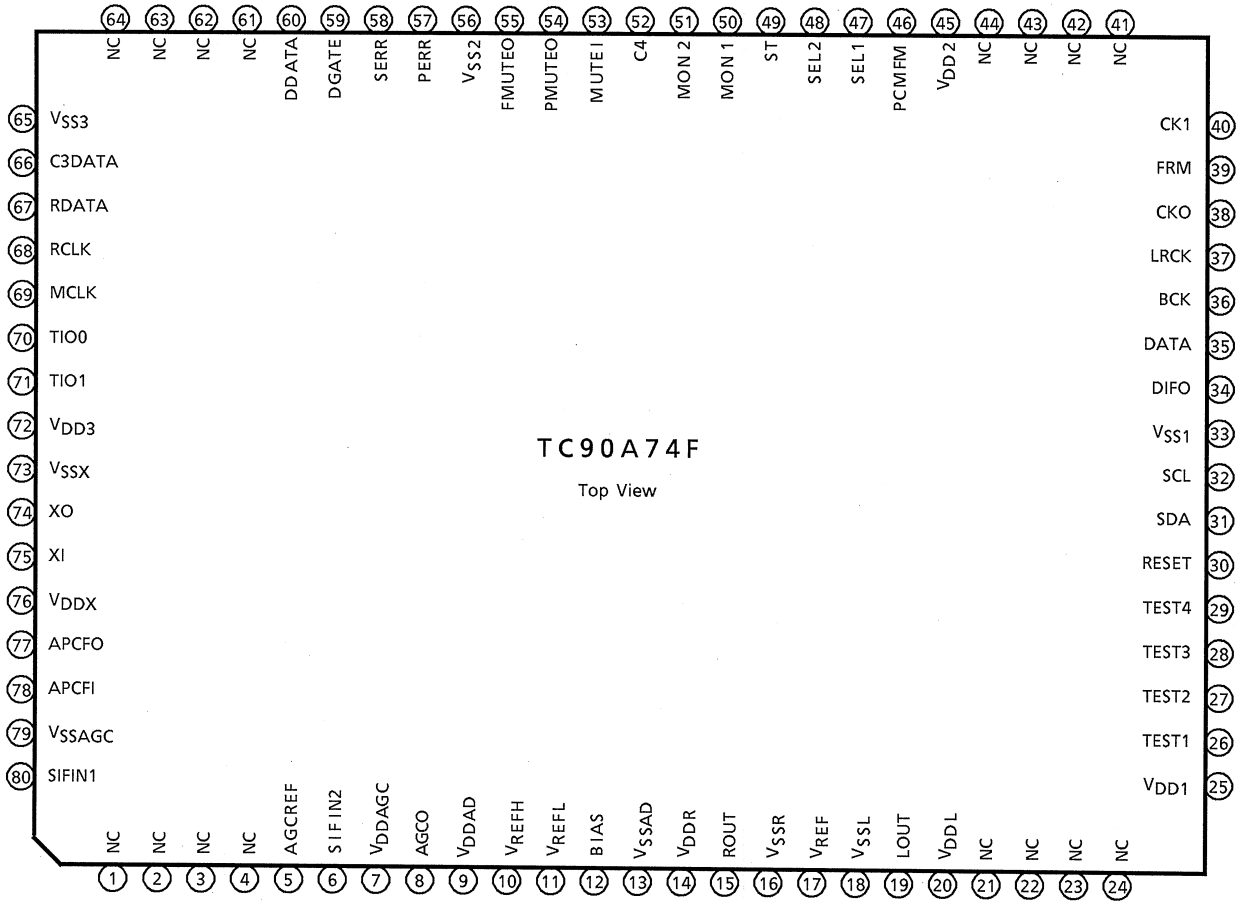
- Decodes NICAM sound.
- Decodes FM sound.
- Uses digital PLL and digital OSC for multicarrier capability.
- Contains digital de-emphasis circuit for FM and PCM.
- Interfaces with a microcomputer via the I^2C bus.
- Uses AGC circuit to stabilize input signal levels.
- Operates with a single crystal (18.432 MHz).
- Greatly reduces part counts thanks to digital processing.
- Operates with a single 5V power supply.
- Package : QFP80

*: These products are under development. Specifications are subject to change without notice.

BLOCK DIAGRAM



PIN CONNECTION



PIN CONNECTION

PIN No.	PIN NAME	I / O	FUNCTION
1	NC	—	(Normally connect with Digital GND)
2	NC	—	(Normally connect with Digital GND)
3	NC	—	(Normally connect with Digital GND)
4	NC	—	(Normally connect with Digital GND)
5	AGC_{REF}	—	AGC reference
6	SIF_{IN2}	I	SIF IN2
7	V_{DDAGC}	—	AGC-V_{DD} (5 V ± 5%)
8	AGCO	I / O	AGC test I / O
9	V_{DDAD}	—	ADC-V_{DD} (5 V ± 5%)
10	V_{REFH}	—	ADC bias pin H
11	V_{REFL}	—	ADC bias pin L
12	BIAS	—	ADC bias pin
13	V_{SSAD}	—	ADC-V_{SS}
14	V_{DDR}	—	Power supply for R-channel sound output filter (5 V ± 5%)
15	R_{OUT}	O	R-channel sound output
16	V_{SSR}	—	GND for R-channel sound output filter
17	V_{REF}	—	1-bit DAC reference power supply
18	V_{SSL}	—	GND for L-channel sound output filter
19	L_{OUT}	O	L-channel sound output
20	V_{DDL}	—	Power supply for L-channel sound output filter (5 V ± 5%)
21	NC	—	(Normally connect with Digital GND)
22	NC	—	(Normally connect with Digital GND)
23	NC	—	(Normally connect with Digital GND)
24	NC	—	(Normally connect with Digital GND)
25	V_{DD1}	—	Digital power supply 1
26	TEST1	I	Test pin 1
27	TEST2	I	Test pin 2
28	TEST3	I	Test pin 3
29	TEST4	I	Test pin 4
30	RESET	I	Reset pin (Low level: Reset, High level: Normal)
31	SDA	I / O	I^2C bus data pin
32	SCL	I	I^2C bus clock pin
33	V_{SS1}	—	Digital GND
34	DIFO	O	Test 5
35	DATA	O	External DAC data output
36	BCK	O	External DAC shift clock output
37	LRCK	O	External DAC L / R clock output
38	CKO	O	External DAC clock output
39	FRM	O	Frame sync signal output
40	CK1	O	Carrier output
41	NC	—	(Normally connect with Digital GND)
42	NC	—	(Normally connect with Digital GND)

PIN No.	PIN NAME	I / O	FUNCTION
43	NC	—	(Normally connect with Digital GND)
44	NC	—	(Normally connect with Digital GND)
45	V_{DD2}	—	Digital power supply 2 (5 V ± 5%)
46	PCMFM	I	Analog sound PCM / FM select switch
47	SEL1	I	Digital sound select switch 1
48	SEL2	I	Digital sound select switch 2
49	ST	O	Stereo mode sound output
50	MON1	O	Monaural mode sound output 1
51	MON2	O	Monaural mode sound output 2
52	C4	O	C4 mode display output
53	MUTEI	I	Sound mute input
54	PMUTEO	O	PCM mute signal output
55	FMUTEO	O	FM mute signal output
56	V_{SS2}	—	Digital GND
57	PERR	O	Parity error output
58	SERR	O	Sync error output
59	DGATE	O	Data GATE signal output
60	DDATA	O	Data output
61	NC	—	(Normally connect with Digital GND)
62	NC	—	(Normally connect with Digital GND)
63	NC	—	(Normally connect with Digital GND)
64	NC	—	(Normally connect with Digital GND)
65	V_{SS3}	—	Digital GND
66	C3DATA	O	C3 data output
67	RDATA	O	QPSK demodulation signal output
68	RCLK	O	Clock output (728 kHz)
69	MCLK	O	Clock output (carrier frequency)
70	TIO0	I / O	Test I / O
71	TIO1	I / O	Test I / O
72	V_{DD3}	—	Digital power supply 3 (5 V ± 5%)
73	V_{SSX}	—	VCXO-GND
74	XO	O	Crystal oscillation output
75	XI	I	Crystal oscillation input
76	$V_{DD}X$	—	VCXO-V_{DD} (5 V ± 5%)
77	APCFO	O	APC filter output
78	APCFI	I	APC filter input
79	V_{SSAGC}	—	V_{SS}-AGC
80	SIF_{IN1}	I	SIF IN1

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{DD}	V_{SS} ~ V_{SS} + 6.0	V
Input Signal Voltage	V_{IN}	−0.3 ~ V_{DD} + 0.3	V
Power Dissipation	P_D	900 (Note 1)	mW
Storage Temperature	T_{stg}	−55 ~ 125	°C

Note 1: When using the device at above Ta = 25°C, decreace the power dissipation by 9.0 mW for each increace of 1°C

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Power Supply Voltage	V_{DD}	—	4.75	5	5.25	V
Input Signal Voltage	V_{IN}	—	0	—	V_{DD}	V
Operating Temperature	T_{opr}	—	−20	—	75	°C

ELECTRICAL CHARACTERISTICS
DC CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, V_{DD} = 5.0 V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Current Dissipation	I_{DD}	—	90	130	145	mA
Power Dissipation	P_D	—	428	650	760	mW
High-level Input Voltage	V_{IH1}	(Note 2)	4.0	—	—	V
	V_{IH2}	(Note 3)	4.0	—	—	
Low-level Input Voltage	V_{IL1}	(Note 2)	—	—	1.0	V
	V_{IL2}	(Note 3)	—	—	1.0	
Hysteresis Width	V_H	—	0.3	—	1.5	V
High-level Input Current	I_{IH}	V_{IH} = V_{DD} (Note 2, 3)	—	—	10	μA
Low-level Input Current	I_{IL}	V_{IL} = V_{SS} (Note 2, 3)	−10	—	—	μA
High-level Output Voltage	V_{OH1}	—	4.0	—	—	V
High-level Output Voltage	V_{OH2}	—	—	—	0.4	V

Note 2: CMOS input: AGCREF, SIF2, XI, APCFI, SIF1

Note 3: CMOS Schmitt input: TEST1, TEST2, TEST3, TEST4, RESET, SDA, SCL, PCMFMSEL1, SEL2, MUTEI

AC CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, V_{DD} = 5.0 V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
SCL Clock Frequency	f_{SCL}	f_{SCL} = 1 / TSCL	0	—	100	kHz
SCL High-level Duration	t_{SH}	C_L = 400 pF	4.0	—	—	μs
SCL Low-level Duration	t_{SL}	C_L = 400 pF	4.7	—	—	μs
Data Setup Time	t_{DS}	C_L = 400 pF	250	—	—	ns
Data Hold Time	t_{DH}	C_L = 400 pF	5.0	—	—	μs
Transmitton Start Condition Hold Time	t_{SCH}	C_L = 400 pF	4.0	—	—	μs
Transmission Stop Condition Hold Time	t_{ECS}	C_L = 400 pF	4.7	—	—	μs
Data Transfer Cycle	t_{BUF}	C_L = 400 pF	4.7	—	—	μs
I^2C Rise Time	t_{lr}	C_L = 400 pF	—	—	1.0	μs
I^2C Fall Time	t_{lf}	C_L = 400 pF	—	—	300	ns

AUDIO OUTPUT CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, V_{DD} = 5.0 V)

	CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX	UNIT		
NICAM	THD	THD_n	—	—	−70	dB	Full Scale	(Note 4)
	S/N	SN_n	—	—	90	dB	Full Scale	(Note 4)
	Output Level	Doutn	—	—	3.4	V_{p-p}		
FM	THD	THD_f				dB		
	S/N	SN_f				dB		
	Output Level	Doutfm	—	—		V_{p-p}	100% modulation	

Note 4: Full scale: Output level 3.4 V_{p-p}

SIF INPUT CHARACTERISTICS (Ta = 25°C, V_{CC}, V_{DD} = 5.0 V)

CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX	UNIT
Input Level	AGC	100	300	500	mV_{p-p}
Input Frequency Range	$SIFIIN_f$	4.0	—	7.0	MHz
Maximum FM Deviation	DEV_{max}	—	—	250	kHz

DIGITAL FILTER CHARACTRISTIC (Ta = 25°C, V_{CC}, V_{DD} = 5.0 V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Digital Filter Pass Band Width Ripple	DFpr		—	0.2	—	dB
Digital Filter Pass Bsnf	DFpb	Gain-1dB frequency	—	15.0	—	kHz
Digital Filter Attenuation	DFrr		—	−40.0	—	dB
Digital De-emphasis Characteristic Error	Derr		—	0.5	—	dB

Specifications of crystal and varactor

Crystal
Dai-Shinku AT-49

Frequency	18.432 MHz
Frequency deviation	$\pm 20 \times 10^{-6}$ at 25°C ± 3°C
Equivalent resistance	40 Ω (max.)
Storage temperature range	−40 ~ 85°C
Operating temperature range	−10 ~ 70°C
Temperature characteristic	$\pm 20 \times 10^{-6}$ (−10 ~ 70°C)
Load capacitance	10.0 pF ± 0.5 pF
Drive Level	10μW ± 2μW
Shunt Capacitance	7.0 pF (max.)
Insulation resistance	500 Ω (min.) / 100 V DC
Vibration type	Basic wave

Varactor
Hitachi HVU17

FUNCTIONS

(1) Outline

1. Input block
   Incorporates an MPX circuit which selects one of the two input signals, an AGC circuit, and an 8-bit AD converter.

2. Digital QPSK demodulation block
   Demodulates AD-converted QPSK modulation signal to PCM data. Multi-support system that modulates any carrier, in addition to I and B/G by digital PLL. Operates differentials and converts between parallel and serial. Use an 18.432 MHz crystal.

   At the same time as QPSK demodulation, can perform FM demodulation for a channel. Output from the DA converter is one of the following : (1) NICAM (two channels), and (2) FM monaural (one channel). Simultaneous output of NICAM and FM monaural is not possible.

3. PCM decoder block
   Generates digital sound data which are passed to the DA converter from the QPSK demodulation digital data. Also, decodes sound data and selects sound output.

4. Digital FM demodulation block
   Demodulates AD-converted FM modulated signal using a digital oscillator and generates digital sound data which are passed to the DA converter. With an FM demodulator which uses a digital oscillator, demodulates any carrier.

5. SW and matrix block
   Incorporates a switch for PCM / FM broadcasting.

6. Digital deemphasis block
   Incorporates a digital deemphasis circuit for FM and PCM. The circuit processes signals in binaseband form.

(2) Description by Block

1. SIF selector circuit
   Switches between two inputs, SIFIN1 and SIFIN2. I^2C bus is used for switching.

2. AGC circuit
   Absorbs level fluctuations in the input signal selected by the SIF selector circuit. Can automatically control gain of signals whose input level is 100 to 500 $mV_{p\text{-}p}$.

3. ADC circuit
   AD-converts the input signal selected by the SIF selector circuit in units of 8 bits.

4. OSC circuit
   Generates a carrier frequency corresponding to that used by broadcasters in various countries. I^2C bus is used to set the carrier frequency.

5. Data playback circuit
   Calculates data differentials, converts between parallel and serial, plays back data, and generates 5.824 MHz and 728 kHz clocks in sync with data.

6. Sync circuit
   Detects an 8-bit sync pattern (Frame Alignment Word, FAW) from the QPSK demodulation signal output by the data playback circuit. Checks the sync patterns are consecutive using the fact that one frame consists of 728 bits. Sync protection starts after two consecutive frames are in sync, when sync status is entered, and lasts until after six consecutive frames are out of sync, when async status is entered. Once FAWsync is established, perform sync on 16 frames using the CO bit in the control bits. CO sync protection starts after two consecutive CO frames are in sync, when sync status is entered, and lasts until after four consecutive CO frames are out of sync, when async status is entered. During async, Low level is output to SERR (pin 58)

7. Descramble circuit
   Operates the built-in PN code generator in sync with the frame using the frame sync pulse from the sync circuit and eliminates the PN code in the QPSK demodulation signal.
   For PN scramble broadcasting, switch the display pin to the decode pin. Switch using DPSL at I^2C bus address B4HEX, subaddress 04HEX.
   For scramble broadcasting, set the FAW initial value using the I^2C bus.

8. Timing generator circuit
   Outputs timing signals which are in sync using the frame sync pulse from the sync signal.

9. Control bit detector circuit
   Performs majority decision on the playback signal from the descramble circuit in units of 16 frames and outputs the control bits. Thus, data are updated every 16 frames. The detected control bits are decoded and output to C4 (pin 52), MONO2 (pin 51), MONO1 (pin 50), and ST (pin 49).

10. Range bit detector circuit
    Detects by multiple decisions the range bit and the control information bit multiplexed with the parity bit.

11. Parity detector circuit
    Using the range bit and the control information bit detected by the range bit detector circuit, eliminates the range bit and the control information bit multiplexed with the parity bit and checks the parity

12. 10 → 14-bit stretch circuit
    According to the range bit detected by the range bit detector circuit, stretches the 10-bit data to 14-bit. Adds " 00 " in the lower two bits and treats the data as 16-bit.

13. Error interpolation circuit
    If an error is detected by the parity detector circuit, performs data interpolation. For a single error, performs mean interpolation; for consecutive errors, holds the previous value.

14. NICAM output selector circuit
    If a received signal is monaural, two-channel, output to the digital filter can be selected using SEL1 and SEL2 at I^2C bus address B4HEX and subaddress 00HEX, or external pin SEL1 (pin 47) and external pin SEL2 (pin 48). Because the control signals are OR-ed internally, when the I^2C bus is used, connecting external pins SEL1 and SEL2 to DGND selects output to the digital filter. When external pins are used, connecting SCL (pin 32) and SDA (pin 31) to DV_{DD} makes the selection.
    If both control signals are set to High level, display output disappears, muting the digital sound output.

15. Muting circuit

(1) PCM muting circuit

The muting circuit outputs High level to PMUTE (pin 54).

- When a sync error occurs.
- When parity errors occur more than the specified number of times during the specified decision duration (approx. 0.5 s).

At this time, it takes seven frames until a sync error occurs. If digital mute is not in use, fix MUTEI to Low level. Switch the mute threshold value using THL0 to THL7 at I^2C bus address B4HEX and subaddress 01HEX. Set the mute duration using CYLCE0 to CYLCE4 at I^2C bus address B4HEX and subaddress 02HEX.

When mute is on, High level is output to PMUTEO (pin 54). In the muting circuit, PMUTEO (pin 54), FMUTEO (pin 55), and MUTEI (pin 53) are OR-ed. Setting the MUTEI pin to High level triggers mute regardless of errors. If the MUTEI pin is not used, connect it to digital GND.

(2) FM muting circuit

When the circuit is in the following condition, the muting circuit mutes the sound output. During muting, High level is output to FMUTEO (pin 55).

- When the FM carrier cannot be detected.

16. I^2C Bus Control Circuit

Extracting control bits, selecting output, or setting the operating mode is performed via the I^2C bus, which is an asynchronous serial interface. A register is selected using an 8-bit address and an 8-bit subaddress which data are sent to or received from. Data are transferred from SDA in sync with the SCL clock.

The contents of a register are initialized to 00HEX by inputting Low level to RESET (pin 30).

Data written to a register are retained until the next data are written.

Note: After power on, set the RESET pin to Low level, then initialize before use.

17. Digital Deemphasis Circuit

(1) NICAM deemphasis circuit

Digitally deemphasizes digital sound signals which are digitally demodulated according to ITU-T Recommendation J.17 characteristics. The gain error is (0.25 dB or below. This circuit can be turned on or off. Switching is done using NIEMP1 and NIEMP2 at I^2C bus address B4HEX and subaddress 42HEX.

(2) FM deemphasis circuit

Deemphasizes digitally demodulated FM sound signals. This circuit can be turned on or off.

Switching is done using FMEMP1 and FMEMP2 at I^2C bus address B4HEX and subaddress 41HEX.

I²C REGISTERS

SUBADDRESS	NAME	
00HEX	FMSEL	FM / NICAM auto select switch
	FMPCM	FM / PCM (NICAM) output select
	ERM	Muting circuit control
	SEL1	Sound output main sound / sub sound switch 1
	SEL2	Sound output main sound / sub sound switch 2
01HEX	THL7	Mute level threshold value switch 7
	THL6	Mute level threshold value switch 6
	THL5	Mute level threshold value switch 5
	THL4	Mute level threshold value switch 4
	THL3	Mute level threshold value switch 3
	THL2	Mute level threshold value switch 2
	THL1	Mute level threshold value switch 1
	THL0	Mute level threshold value switch 0
02HEX	CYCLE4	Error detection duration setting 4
	CYCLE3	Error detection duration setting 3
	CYCLE2	Error detection duration setting 2
	CYCLE1	Error detection duration setting 1
	CYCLE0	Error detection duration setting 0
08HEX	FAW7	FAW scramble broadcasting initial value setting 7
	FAW6	FAW scramble broadcasting initial value setting 6
	FAW5	FAW scramble broadcasting initial value setting 5
	FAW4	FAW scramble broadcasting initial value setting 4
	FAW3	FAW scramble broadcasting initial value setting 3
	FAW2	FAW scramble broadcasting initial value setting 2
	FAW1	FAW scramble broadcasting initial value setting 1
	FAW0	FAW scramble broadcasting initial value setting 0
09HEX	DSPMUTE	Sound mute
	SIFSEL	SIFIN1 / SIFIN2 select
	PSAVE	Power save mode

I²C REGISTERS

SUBADDRESS	NAME	
0DHEX	LVL8	FM1 level setting data 8
	LVL9	FM1 level setting data 9
	LVL10	FM1 level setting data 10
	LVL11	FM1 level setting data 11
	LVL12	FM1 level setting data 12
	LVL13	FM1 level setting data 13
	LVL14	FM1 level setting data 14
	LVL15	FM1 level setting data 15
0FHEX	LVL24	NICAM level data setting data 24
	LVL25	NICAM level data setting data 25
	LVL26	NICAM level data setting data 26
	LVL27	NICAM level data setting data 27
	LVL28	NICAM level data setting data 28
	LVL29	NICAM level data setting data 29
	LVL30	NICAM level data setting data 30
	LVL31	NICAM level data setting data 31
10HEX	FMOVER	FM high deviation mode
11HEX	FMVOL6	FM audio attenuation level 6
	FMVOL5	FM audio attenuation level 5
	FMVOL4	FM audio attenuation level 4
	FMVOL3	FM audio attenuation level 3
	FMVOL2	FM audio attenuation level 2
	FMVOL1	FM audio attenuation level 1
	FMVOL0	FM audio attenuation level 0
12HEX	NICAMVOL6	NICAM audio attenuation level 6
	NICAMVOL5	NICAM audio attenuation level 5
	NICAMVOL4	NICAM audio attenuation level 4
	NICAMVOL3	NICAM audio attenuation level 3
	NICAMVOL2	NICAM audio attenuation level 2
	NICAMVOL1	NICAM audio attenuation level 1
	NICAMVOL0	NICAM audio attenuation level 0
13HEX	OUTGAIN6	FM output level control 6
	OUTGAIN5	FM output level control 5
	OUTGAIN4	FM output level control 4
	OUTGAIN3	FM output level control 3
	OUTGAIN2	FM output level control 2
	OUTGAIN1	FM output level control 1
	OUTGAIN0	FM output level control 0

SUBADDRESS	NAME	
40HEX	OSC23	OSC2 oscillation frequency switch 3
	OSC22	OSC2 oscillation frequency switch 2
	OSC21	OSC2 oscillation frequency switch 1
	OSC13	OSC1 oscillation frequency switch 3
	OSC12	OSC1 oscillation frequency switch 2
	OSC11	OSC1 oscillation frequency switch 1
	DEMMOD2	Demodulator circuit operation select 2
	DEMMOD1	Demodulator circuit operation select 1

I^2C REGISTERS

SUBADDRESS	NAME	
41HEX	FMEMP2	FM emphasis setting 2
	FMEMP1	FM emphasis setting 1
	FMDEV2	FM deviation setting 2
	FMDEV1	FM deviation setting 1
42HEX	ROLOF1	Rolloff filter characteristic switch 1
	ROLOF2	Rolloff filter characteristic switch 2
	NIEMP1	NICAM emphasis characteristic switch 1
	NIEMP2	NICAM emphasis characteristic switch 2
44HEX	SYSSEL4	Receive mode select 4
	SYSSEL3	Receive mode select 3
	SYSSEL2	Receive mode select 2
	SYSSEL1	Receive mode select 1

Description of I^2C bus registers

After power on, the values of the I^2C bus registers are undefined. Thus, perform reset after power on. The initial value after reset is NICAM-I mode.

Write register (B4HEX)
Subaddress 00HEX

MSB							LSB
0	0	0	FMSEL	PCMFM	ERM	SEL2	SEL1

FMSEL : C4 auto select switch

0 : Auto select

1 : PCM / FM selected by FMPCM register

Among control bits transmitted by NICAM, C4 is set to 1 when the contents of NICAM sound are the same as those transferred by FM sound. When C4 = 1, switches between automatic NICAM output (auto select) or selection (PCM / FM) by the FMPCM register.

FMPCM : FM / PCM (NICAM) output select

0 : FM

1 : PCM (NICAM)

Note: FMPCM of the I2C bus register and external pin PCMFM (pin 46) are OR-ed internally. Thus, when external pin PCMFM is not used, connect to digital GND.

ERM : Muting circuit control

0 : Uses muting circuit.

1 : Does not use muting circuit.

TC90A74F incorporates a muting circuit, which uses error frequency detection. This bit selects whether the muting circuit is used or not. For how to set the muting circuit, see subaddresses 01HEX and 02HEX.

SEL1, SEL2 : Sound select

Determines the sound mode. Depending on the type of broadcast being received (FM or NICAM) and the broadcast mode (stereo, monaural, two-channel monaural), the following sound is selected.

External pins SEL1 (pin 47) and SEL2 (pin 48) can also control the sound selection.

Note: SEL1 and SEL2 of the I^2C bus and external pins SEL1 and SEL2 are internally OR-ed. Therefore, if the external pins are not used, connect these pins to digital GND.

NICAM stereo mode

The control bits in the table below are bits sent together with sound data in NICAM broadcasting. The decoder determines the mode by detecting the control bit.

MODE				SOUND SELECTED		SOUND OUTPUT	
Stereo				SEL1	SEL2	L	R
				0	0	L	R
Control Bit				0	1	L	R
C1	C2	C3	C4	1	0	L	R
0	0	0	0/1	1	1	Mute	Mute

MODE				SOUND SELECTED		SOUND OUTPUT	
Monaural Two-channel				SEL1	SEL2	L	R
				0	0	M1	M1
Control Bit				0	1	M2	M2
C1	C2	C3	C4	1	0	M1	M2
0	1	0	0/1	1	1	Mute	Mute

MODE				SOUND SELECTED		SOUND OUTPUT	
Monaural + Data				SEL1	SEL2	L	R
				0	0	Mute	Mute
Control Bit				0	1	Mute	Mute
C1	C2	C3	C4	1	0	Mute	Mute
1	0	0	0/1	1	1	M	M

MODE				SOUND SELECTED		SOUND OUTPUT	
Data				SEL1	SEL2	L	R
				0	0	FM	FM
Control Bit				0	1	FM	FM
C1	C2	C3	C4	1	0	FM	FM
1	1	0	0/1	1	1	FM	FM

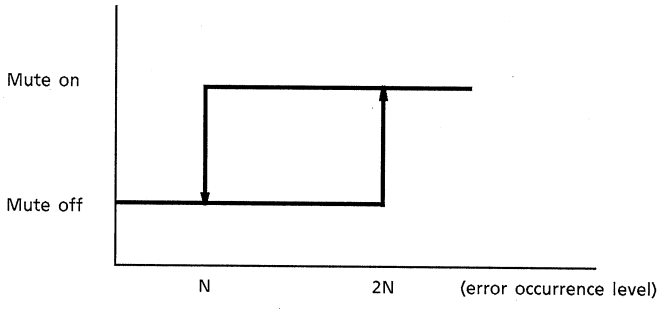
MODE				SOUND SELECTED		SOUND OUTPUT	
Others				SEL1	SEL2	L	R
				0	0	FM	FM
Control Bit				0	1	FM	FM
C1	C2	C3	C4	1	0	FM	FM
×	×	0	0/1	1	1	FM	FM

Subaddress 01HEX

MSB							LSB
THL7	THL6	THL5	THL4	THL3	THL2	THL1	THL0

THL7 to THL0 : Mute level threshold value
Set values : 00 to FF (1 to 256 samples)
This register is used to set level where mute is applied.
Combining the set mute threshold value and the set mute duration at subaddress 02HEX can set mute-on status to any error detection duration and error frequency.
The muting circuit has ON / OFF hysteresis as shown below. When a parity error occurs to (set value × 2) samples, mute turns on.
When errors return to (set value × 1), mute turns off.

*: 1 frame = 64 samples = 1 / 728 s



Subaddress 02HEX

MSB							LSB
0	0	0	CYCLE4	CYCLE3	CYCLE2	CYCLE1	CYCLE0

CYCLE4 to CYCLE0 : Set error detection duration.
Set values : 00 to 1F (0 to 31 super frames*)

*: 1 super frame = 16 frames = 16 × (1 / 728) s

This register is used to set the error detection duration for mute. If a parity error at the level set at subaddress 01HEX is detected during the set duration, mute turns on.

Subaddress 08HEX

MSB							LSB
FAW7	FAW6	FAW5	FAW4	FAW3	FAW2	FAW1	FAW0

FAW7 to FAW0 : Set the FAW scramble broadcasting initial value.

When receiving FAW scramble broadcasting, set the initial value in this register.

Note: After the IC is reset “01001110” which is the NICAM broadcasting specification, is set as the initial value. Note that if the register is accessed, the value is altered and remains altered unless “01001110” is set again (decoding becomes impossible). Do not access the register unless necessary.

Subaddress 09HEX

MSB							LSB
DSPCMUTE	0	0	0	0	0	SIFSEL	1

DSPCMUTE : Sound mute
0 : Normal
1 : Mute

Applies mute to sound output. Valid for both NICAM and FM sounds.
For mute when an NICAM or FM error occurs, see subaddresses 01 and 02HEX.
SIFSEL : Selects SIFIN1 or SIFIN2.
0 : SIFIN1
1 : SIFIN2

Selects input to SIFIN1 (pin 80) or SIFIN2 (pin 6).

Subaddress 0D HEX

MSB							LSB
LVL8	LVL9	LVL10	LVL11	LVL12	LVL13	LVL14	LVL15

LVL8 to LVL15 : Set FM1 level data.

Set an FM1 detection threshold value.

Subaddress 0F HEX

MSB							LSB
LVL24	LVL25	LVL26	LVL27	LVL28	LVL29	LVL30	LVL31

LVL24 to LVL31 : Set NICAM level data.

Set a NICAM detection threshold value.

Subaddress 10 HEX

MSB							LSB
FMOVER	0	0	0	0	0	0	0

FMOVER : High deviation mode
0 : Normal
1 : High deviation mode

Subaddress 11 HEX FM audio output attenuation level

MSB							LSB
0	FMVOL6	FMVOL5	FMVOL4	FMVOL3	FMVOL2	FMVOL1	FMVOL0

FMVOL6 to FMVOL0 : FM audio output attenuation level 0-127

Subaddress 12 HEX NICAM audio output attenuation level

MSB							LSB
0	NICAMVOL6	NICAMVOL5	NICAMVOL4	NICAMVOL3	NICAMVOL2	NICAMVOL1	NICAMVOL0

NICAMVOL6 to NICAMVOL0 : NICAM audio output attenuation level 0-127

Subaddress 13 HEX FM audio output attenuation level

MSB							LSB
0	OUTGAIN6	OUTGAIN5	OUTGAIN4	OUTGAIN3	OUTGAIN2	OUTGAIN1	OUTGAIN0

OUTGAIN6 to OUTGAIN0 : FM output level control

Subaddress 40 HEX

MSB							LSB
OSC23	OSC22	OSC21	OSC13	OSC12	OSC11	DEMMOD2	DEMMOD1

OSC23 to OSC21 : Set the oscillation frequency of internal oscillator 2.

000 6.552 MHz
100 5.85 MHz

OSC13 to OSC11 : Set the oscillation frequency of internal oscillator 1.

000 6.0 MHz
100 5.5 MHz
010 6.5 MHz
110 4.5 MHz

DEMMOD : Selects the demodulator circuit operation.

00 : NICAM + FM
01, 11 : FM (monaural)

Note: When NICAM + FM mode is selected by setting DEMMOD to 00, FM and NICAM are decoded internally but cannot be output simultaneously.

Subaddress 41HEX FM decoder setting switch

MSB							LSB
0	0	FMEMP1	FMEMP1	0	0	FMDEV2	FMDEV1

FMEMP2, FMEMP1 : Set FM emphasis.

00 : 50 μs
10 : 75 μs
01 : Bypasses the emphasis circuit.

FMDEV1, FMDEV2 : Set FM deviation.

FMDEV2, FMDEV1
00 : 50 kHz
01 : 25 kHz

Subaddress 42HEX NICAM decoder setting switch

MSB							LSB
0	0	NIEMP1	NIEMP2	0	ROLOF1	ROLOF2	ROLOF3

The TC90A74F incorporates a NICAM rolloff filter and deemphasis circuit.

ROLOF1, 2, 3 : Switch rolloff filter characteristics.

000 : 100% (I)
010 : 40% (D / K)
110 : 40% (B / G)

NIEMP1, 2 :

00 : J. 17
10 : Bypasses the de-emphasis circuit

Subaddress 44HEX

MSB							LSB
SYSSEL4	SYSSEL3	SYSSEL2	SYSSEL1	0	SCANPRD2	SCANPRD1	0

SYSEL4 to SYSEL1 : Select receive mode

0000 : NICAM I
0001 : NICAM B / G
0100 : NICAM D / K
0101 : FM B / G
0110 : FM I
0111 : FM D / K
Preset mode

1000 : External setting mode − Manual setting mode

To support different broadcasting modes, the TC90A74F contains in internal ROM parameters such as oscillation frequencies, pilot carrier frequencies, FM emphasis characteristics, FM deviations, and NICAM emphasis characteristics.
Setting SYSSEL determines the combination of parameters used to read data. Combinations of parameters are as shown in the table below. The initial value after reset is SYSSEL = 0000.

SYSSEL	CONTENTS	MODE	OSC1 OSCILLATION FREQUENCY	OSC2 OSCILLATION FREQUENCY	FM DEVI-ATIONS	PILOT SIGNAL	FM EMPHASIS	ROLLOFF RATIO	FM MATRIX MODE
0000	NICAM-I	FM+NICAM	6.0 MHz	6.552 MHz	50 kHz	—	50μs	100%	—
0001	NICAM-B / G	FM+NICAM	5.5 MHz	5.85 MHz	50 kHz	—	50μs	40%	—
0100	NICAM-D / K	FM+NICAM	6.5 MHz	5.85 MHz	50 kHz	—	50μs	40%	—
0101	FM-B / G	FM	5.5 MHz	—	50 kHz	—	50μs	—	—
0110	FM-I	FM	6.0 MHz	—	50 kHz	—	50μs	—	—
0111	FM-D / K	FM	6.5 MHz	—	50 kHz	—	50μs	—	—

Setting of actual receive modes

1. Preset mode (mode which can be set by SYSSEL)
   Parameters can be determined at subaddresses 40HEX to 42HEX. However, normally, all the parameters can be set using SYSSEL at subaddress 44HEX only.
   After the IC is reset, set the desired receive mode in SYSSEL.

2. Manual setting mode (mode which cannot be set by SYSSEL)
   To change some SYSSEL parameters, overwrite using the I^2C bus after the mode is set in SYSSEL.
   (1) Set SYSSEL at 44HEX.
   (2) Set the parameters to be changed at 40HEX to 42HEX.
   (3) Set 1000 in SYSSEL and transmit the coefficients.

Note: When the parameters at 40HEX to 42HEX are changed, TYSSEL = 10000 must be set. Otherwise, coefficients will not be transmitted to their destinations.

TC90A74F address B5HEX (read register)

READ ORDER	SIGNAL NAME	FUNCTION	DESCRIPTION
1	C1	Control bits	Indicate the control bits to be transmitted in NICAM broadcast mode.
2	C2		
3	C3		
4	C4		
5	SERR	Sync error	Set to 0 when a sync error occurs.
6	PMUTEO	NICAM mute signal	Set to 1 when mute is applied to NICAM.
7	CIB1	Information bit	
8	CIB2	Information bit	
9	LDET	Level detection result	Indicates the detection result for the mode specified by subaddress 44HEX (SYSSEL). For example, when SYSSEL = 0000 (NICAM-I) is set, detecting FM and NICAM results in LDET = 1.
10	FMMUTEO	FM mute signal	Set to 1 when mute is applied to FM.
11			
12			
13	SYSSEL3	Receive mode	Indicate FM + NICAM or FM receive mode. SYSSEL3 : SYSSEL2 : SYSSEL1 : SYSSEL0 = 0000 = NICAM I, 0001 = NICAM B / G, 0010 = IGR, 0100 = NICAM D / K, 0101 = FM B / G, 0110 = FM I, 0111 = FM D / K
14	SYSSEL2		
15	SYSSEL1		
16	SYSSEL0		

Description of I^2C bus functions

The TC90A74F uses I^2C bus specifications (Philips bus specifications) as the interface for controlling operation. The I^2C bus specifications are designed to transfer data between ICs using a common serial bus. Both TC90A74F is designed so that they can operate on an I^2C bus.

1. Outline

The I^2C bus consists of two lines, SCL and SDA.
Data are transferred on the SDA line in units of 8 bits in sync with the clock of the SCL line. Transfer start and end are controlled by changing SDA when the SCL line is High level. Acknowledge is defined in units of bytes, thus a 1-bit acknowledge is sent after 8-bit data are transferred.
The I^2C bus assumes multimasters but the TC90A74F supports only a slave function. Therefore, data are transferred at a point between the master and the slave (in this case, TC90A74F). Transfer start, end, slave selection, and operating mode are all controlled by the then master. Therefore, the SCL line is always controlled by the master and the slave (TC90A74F) is set to input. The SDA line is bidirectional. Input / output is switched by a register of the slave (TC90A74F). The SCL is driven by the master. The SDA line is driven by an open drain from the master or TC90A74F and pulled up by a pull-up resistor.
The master must control transfer (eg, switch input / output of SDA line) by the operating mode (read / write) of the slave address (TC90A74F).

2. Address

The I^2C bus allocates two 8-bit addresses to a slave. As the list of I^2C bus registers shows, B4HEX is assigned as the write address, B5HEX as the read address. An 8-bit subaddress is also set. To control TC90A74F, data are sent / received by specifying an address and a subaddress.

3. Data Block

The I^2C bus can transfer any number of bytes in units of 8 bits. With the TC90A74F, as the list of I^2C bus registers shows, 8 bits are transferred for B4HEX or B5HEX.
All the TC90A74F registers are static, so the previous values are retained until the next update. The slave registers are undefined after power on. Always input Low level to the RESET pin (pin 30) and initialize to 00HEX.

4. Transfer Sequence

4.1 Transfer Start and End

Data are transferred in sync with the SCL line. In standby mode, both SDL and SDA lines are left at high impedance. Because both lines are pulled up, they are High level. Data transfer starts when the SDA line changes from High to Low while the SCL line is at High level and ends when the SDA line changes from Low to High while the SCL line is at High level. There are no such sequences during data transfer duration (see sequences 1 and 2).

4.2 SCL Line and SDA Line Timing

The SDA line data must be valid between the SCL line rising and falling. To make sure data are valid, the transmitting side should output data to the SDA line after checking that the SCL line changes from High to Low level. Due to this restriction, there are no start and end sequences during data transfer.

4.3 Acknowledge

When 8-bit data are correctly received in the write register, the TC90A74F sets the SDA line to Low level. When the master detects this, it knows that data are received correctly. If acknowledge remains at High level, data are not received correctly. Then, the master must retransmit the data.

4.4 Data Transfer Order

The polarity of the SDA line is positive. Data are transferred from the MSB to the LSB of the address, then the MSB to the LSB of the data.

4.5 Data Transmit / Receive Switch Timing

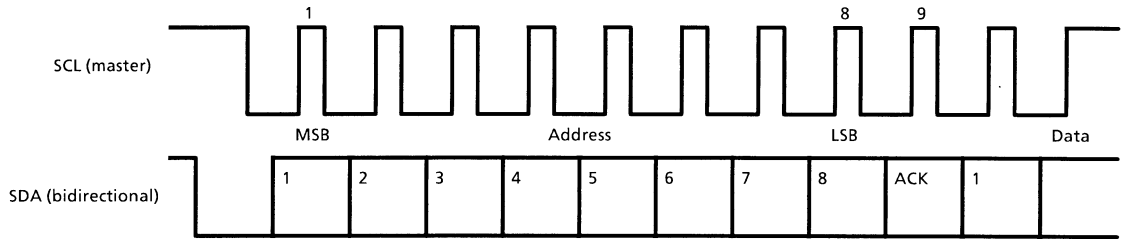
To receive acknowledge after transfer of 8 bits, the master sets the SDA line to high impedance after the SCL line falls after outputting an 8-bit address. The TC90A74F outputs acknowledge to the SDA line in sync with the fall of the SCL line. The SDA line returns to high impedance after the SCL line falls after outputting acknowledge.

I^2C bus control example

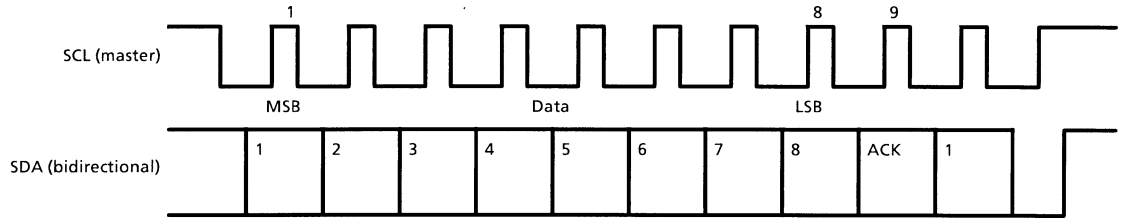
After power on, the master sets the SCL and SDA lines to high impedance.
Then, the TC90A74F inputs Low level to RESET (pin 30) to initialize the IC. Low level can be input to RESET using an external RC or by a pulse from the microcomputer.
At this time, the TC90A74F can be controlled externally and the write register at address B4HEX is initialized to 00HEX.
Here, for slave registers whose initial settings you want to change, send the initial data.
For example, to select NICAM-B / G at automatic system setting, send data 01HEX to subaddress 44HEX. Using this as an example, transfer is described in more detail.
First, output High level to the SCL and SDA lines. Then, to start transfer, set the SDA line to Low level, then the SCL line to Low level.
Next, send the address. Transfer starts from the MSB. As a data string for address B4HEX, send 10110100 (transfer starting from the MSB). For the first bit transfer, set the SDA line to High level, the SCL line to High level, then return to Low level. Then, in sync with the SCL line, change the SDA line to Low level, High level, High level, Low level, High level, Low level, then Low level, transfer the 8-bit address, change the SCL line to High level and confirm that acknowledge is Low level. After confirmation, change the SCL line to Low level then proceed from transfer of the address to transfer of the subaddress.
To transfer the subaddress, start from the MSB. As a data string for subaddress B4HEX, send 01000100 (transfer starting from the MSB). For the first bit transfer, set the SDA line to Low level, the SCL line to High level, then return to Low level. Then, in sync with the SCL line, change the SDA line to High level, Low level, Low level, Low level, High level, Low level, then Low level, transfer the 8-bit subaddress, change the SCL line to High level and confirm that acknowledge is Low level. After confirmation, change the SCL line to Low level then proceed from transfer of the subaddress to transfer of data.
The data string at 01HEX is 00000001. In sync with the SCL line, change the SDA line to Low level, Low level, Low level, Low level, Low level, Low level, Low level, then High level, transfer the 8-bit data.
When transfer of the 8-bit data is complete, change the SCL line to High level and confirm that acknowledge is Low level. After confirmation, change the SCL line to Low level. Finally, to end the transfer, as the end sequence, change the SDA line to Low level, the SCL line to High level, then the SDA line to High level. After that, set both SDA and SCL lines to high impedance. This ends the transfer.
When transferring to another register, apply the same procedure with a different subaddress and data string.

I^2C bus transfer sequences

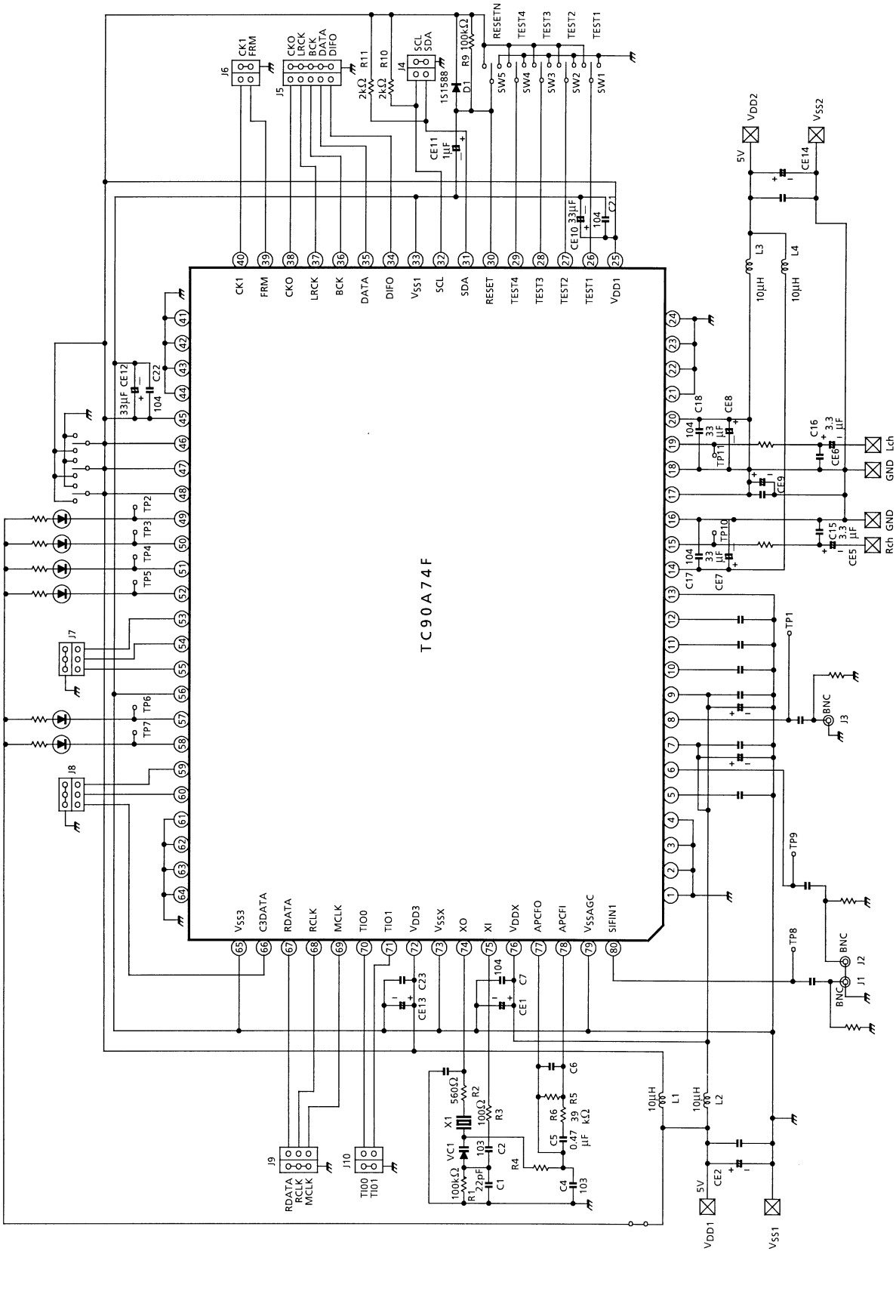
1. Transfer start sequence



2. Transfer end sequence

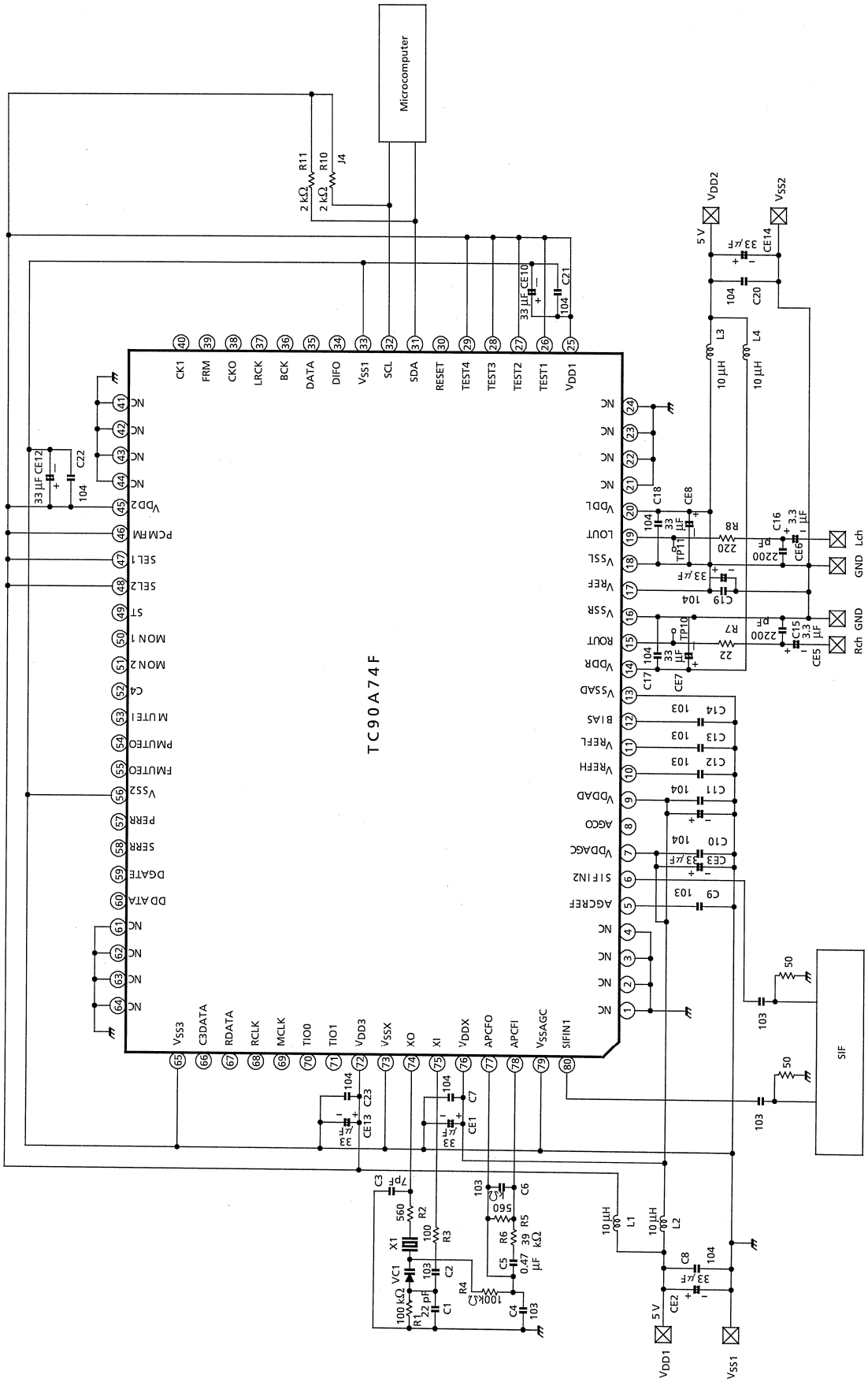


EXAMPLE OF TEST CIRCUIT (TC90A74F)



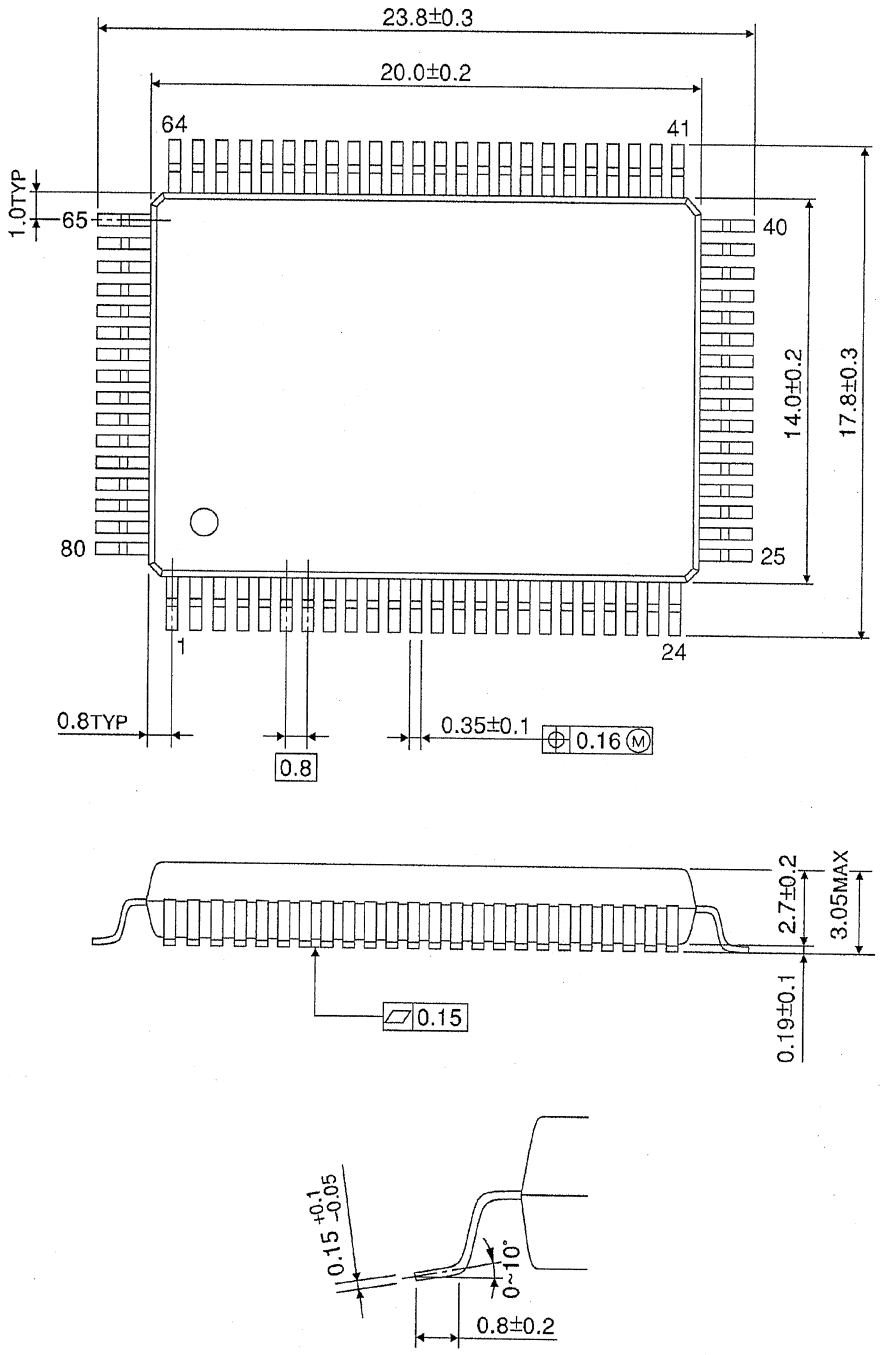
TC90A74N/F—32

APPLICATION CIRCUIT EXAMPLE



PACKAGE DIMENSIONS

QFP80-P-1420-0.80B Unit: mm



Weight: 1.6 g (Typ.)

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