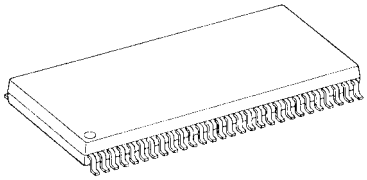
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VCXR162600FT

Low-Voltage 18-Bit Universal Bus Transceiver with 3.6-V Tolerant Inputs and Outputs



TSSOP56-P-0061-0.50

Weight: 0.25 g (typ.)

The TC74VCXR162600FT is a high-performance CMOS 18-bit universal bus transceiver. Designed for use in 1.8-V, 2.5-V or 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

It is also designed with overvoltage tolerant inputs and outputs up to 3.6 V.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock ($\overline{CKAB}$ and $\overline{CKBA}$) inputs. The clock can be controlled by the clock-enable ($\overline{CKENAB}$ and $\overline{CKENBA}$) inputs.

For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CKAB}$ is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of $\overline{CKAB}$.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, $\overline{CKBA}$, and $\overline{CKENBA}$.

When the $\overline{OE}$ input is high, the outputs are in a high-impedance state. This device is designed to be used with 3-state memory address drivers, etc.

The 26-Ω series resistor helps reducing output overshoot and undershoot without external resistor.

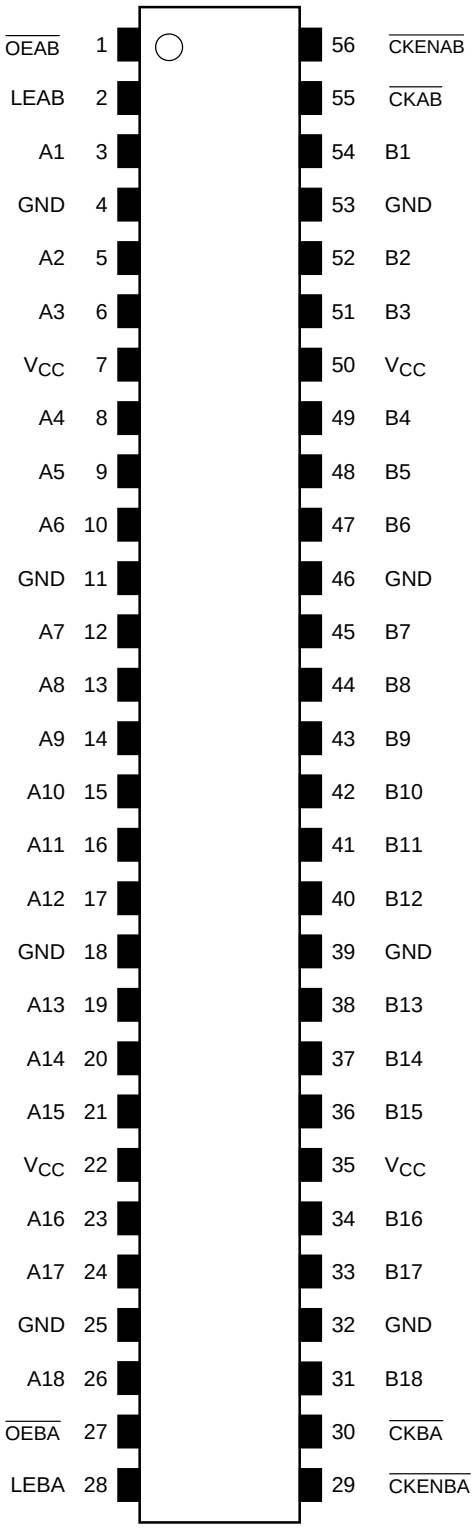
All inputs are equipped with protection circuits against static discharge.

Features

- 26-Ω series resistors on outputs
- Low-voltage operation: V_{CC} = 1.8 to 3.6 V
- High-speed operation : t_{pd} = 3.8 ns (max) (V_{CC} = 3.0 to 3.6 V)
  : t_{pd} = 5.1 ns (max) (V_{CC} = 2.3 to 2.7 V)
  : t_{pd} = 9.8 ns (max) (V_{CC} = 1.8 V)
- Output current : I_{OH}/I_{OL} = ±12 mA (min) (V_{CC} = 3.0 V)
  : I_{OH}/I_{OL} = ±8 mA (min) (V_{CC} = 2.3 V)
  : I_{OH}/I_{OL} = ±4 mA (min) (V_{CC} = 1.8 V)
- Latch-up performance: ±300 mA
- ESD performance: Machine model > ±200 V
  : Human body model > ±2000 V
- Package: TSSOP (thin shrink small outline package)
- Bidirectional interface between 2.5 V and 3.3 V signals.
- 3.6-V tolerant function and power-down protection provided on all inputs and outputs

Note 1: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.
All floating (high impedance) bus pins must have their input level fixed by means of pull-up or pull-down resistors.

Pin Assignment (top view)



Truth Table (A bus → B bus)

Inputs					Outputs
$\overline{CKENAB}$	$\overline{OEAB}$	LEAB	$\overline{CKAB}$	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B0 (Note 3)
H	L	L	X	X	B0 (Note 3)
L	L	L	↓	L	L
L	L	L	↓	H	H
L	L	L	H	X	B0 (Note 2)
L	L	L	L	X	B0 (Note 2)

Note 2: Output level before the indicated steady-state input conditions were established, provided that $\overline{CKAB}$ was low or high before LEAB went low.

Note 3: Output level before the indicated steady-state input conditions were established, provided that . $\overline{CKENAB}$ was low or high before LEAB went low.

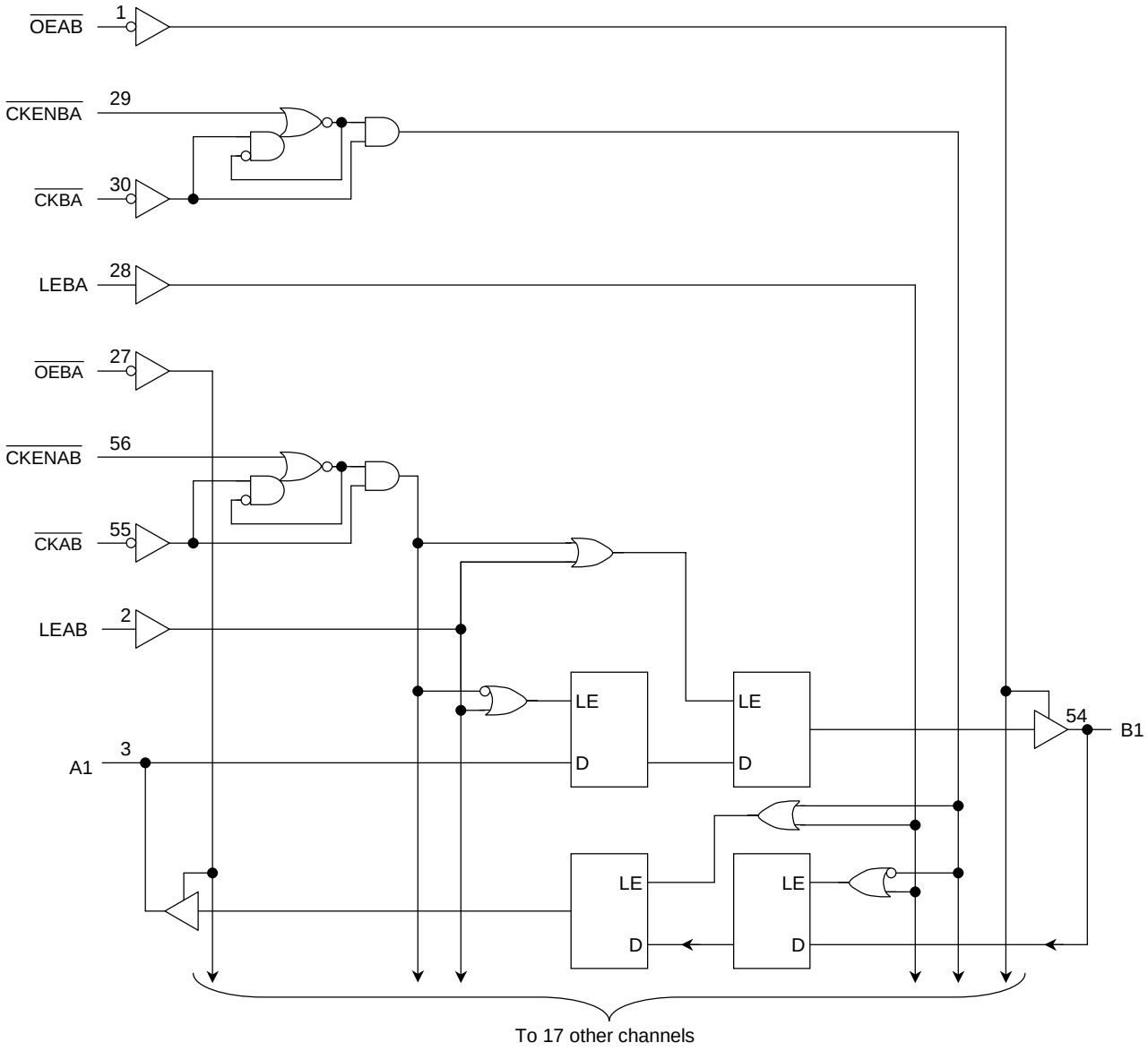
Truth Table (B bus → A bus)

Inputs					Outputs
$\overline{CKENBA}$	$\overline{OEBA}$	LEBA	$\overline{CKBA}$	B	A
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	A0 (Note 5)
H	L	L	X	X	A0 (Note 5)
L	L	L	↓	L	L
L	L	L	↓	H	H
L	L	L	H	X	A0 (Note 4)
L	L	L	L	X	A0 (Note 4)

Note 4: Output level before the indicated steady-state input conditions were established, provided that $\overline{CKBA}$ was low or high before LEBA went low.

Note 5: Output level before the indicated steady-state input conditions were established, provided that . $\overline{CKENAB}$ was low or high before LEAB went low.

System Diagram



Maximum Ratings

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	−0.5 to 4.6	V
DC input voltage ($\overline{OEAB}$, $\overline{OEBA}$, LEAB, LEBA, $\overline{CKAB}$, CKBA , CKENAB , CKENBA)	V_{IN}	−0.5 to 4.6	V
DC bus I/O voltage	$V_{I/O}$	−0.5 to 4.6 (Note 6)	V
		−0.5 to V_{CC} + 0.5 (Note 7)	
Input diode current	I_{IK}	−50	mA
Output diode current	I_{OK}	±50 (Note 8)	mA
DC output current	I_{OUT}	±50	mA
Power dissipation	P_D	400	mW
DC V_{CC}/ground current per supply pin	I_{CC}/I_{GND}	±100	mA
Storage temperature	T_{stg}	−65 to 150	°C

Note 6: OFF state

Note 7: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 8: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Recommended Operating Range

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	1.8 to 3.6	V
		1.2 to 3.6 (Note 6)	
Input voltage ($\overline{OEAB}$, $\overline{OEBA}$, LEAB, LEBA, $\overline{CKAB}$, CKBA , CKENAB , CKENBA)	V_{IN}	−0.3 to 3.6	V
Bus I/O voltage	$V_{I/O}$	0 to 3.6 (Note 7)	V
		0 to V_{CC} (Note 8)	
Output current	I_{OH}/I_{OL}	±12 (Note 9)	mA
		±8 (Note 10)	
		±4 (Note 11)	
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 10 (Note 12)	ns/V

Note 9: Data retention only

Note 10: OFF state

Note 11: High or low state

Note 12: V_{CC} = 3.0 to 3.6 V

Note 13: V_{CC} = 2.3 to 2.7 V

Note 14: V_{CC} = 1.8 V

Note 15: V_{IN} = 0.8 to 2.0 V, V_{CC} = 3.0 V

Electrical Characteristics

DC Characteristics (Ta = –40 to 85°C, 2.7 V < V_{CC} ≦ 3.6 V)

Characteristics		Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Input voltage	H-level	V_{IH}	—		2.7 to 3.6	2.0	—	V
	L-level	V_{IL}	—		2.7 to 3.6	—	0.8	
Output voltage	H-level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –100 μA	2.7 to 3.6	V_{CC} – 0.2	—	V
				I_{OH} = –6 mA	2.7	2.2	—	
				I_{OH} = –8 mA	3.0	2.4	—	
				I_{OH} = –12 mA	3.0	2.2	—	
	L-level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	2.7 to 3.6	—	0.2	
				I_{OL} = 6 mA	2.7	—	0.4	
				I_{OL} = 8 mA	3.0	—	0.55	
				I_{OL} = 12 mA	3.0	—	0.8	
Input leakage current		I_{IN}	V_{IN} = 0 to 3.6 V		2.7 to 3.6	—	±5.0	μA
3-state output OFF state current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		2.7 to 3.6	—	±10.0	μA
Power-off leakage current		I_{OFF}	V_{IN}, V_{OUT} = 0 to 3.6 V		0	—	10.0	μA
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND		2.7 to 3.6	—	20.0	μA
			V_{CC} ≦ (V_{IN}, V_{OUT}) ≦ 3.6 V		2.7 to 3.6	—	±20.0	
Increase in I_{CC} per input		ΔI_{CC}	V_{IH} = V_{CC} – 0.6 V		2.7 to 3.6	—	750	

DC Characteristics (Ta = –40 to 85°C, 2.3 V ≦ V_{CC} ≦ 2.7 V)

Characteristics		Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Input voltage	H-level	V_{IH}	—		2.3 to 2.7	1.6	—	V
	L-level	V_{IL}	—		2.3 to 2.7	—	0.7	
Output voltage	H-level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –100 μA	2.3 to 2.7	V_{CC} – 0.2	—	V
				I_{OH} = –4 mA	2.3	2.0	—	
				I_{OH} = –6 mA	2.3	1.8	—	
				I_{OH} = –8 mA	2.3	1.7	—	
	L-level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	2.3 to 2.7	—	0.2	
				I_{OL} = 6 mA	2.3	—	0.4	
				I_{OL} = 8 mA	2.3	—	0.6	
Input leakage current		I_{IN}	V_{IN} = 0 to 3.6 V		2.3 to 2.7	—	±5.0	μA
3-state output OFF state current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		2.3 to 2.7	—	±10.0	μA
Power-off leakage current		I_{OFF}	V_{IN}, V_{OUT} = 0 to 3.6 V		0	—	10.0	μA
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND		2.3 to 2.7	—	20.0	μA
			V_{CC} ≦ (V_{IN}, V_{OUT}) ≦ 3.6 V		2.3 to 2.7	—	±20.0	

DC Characteristics (Ta = –40 to 85°C, 1.8 V ≦ V_{CC} < 2.3 V)

Characteristics		Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Input voltage	H-level	V_{IH}	—		1.8 to 2.3	0.7 × V_{CC}	—	V
	L-level	V_{IL}	—		1.8 to 2.3	—	0.2 × V_{CC}	
Output voltage	H-level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –100 μA	1.8	V_{CC} – 0.2	—	V
				I_{OH} = –4 mA	1.8	1.4	—	
	L-level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	1.8	—	0.2	
				I_{OL} = 4 mA	1.8	—	0.3	
Input leakage current		I_{IN}	V_{IN} = 0 to 3.6 V		1.8	—	±5.0	μA
3-state output OFF state current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		1.8	—	±10.0	μA
Power-off leakage current		I_{OFF}	V_{IN}, V_{OUT} = 0 to 3.6 V		0	—	10.0	μA
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND		1.8	—	20.0	μA
			V_{CC} ≦ (V_{IN}, V_{OUT}) ≦ 3.6 V		1.8	—	±20.0	

AC Characteristics (Ta = –40 to 85°C, input: $t_r = t_f = 2.0$ ns, $C_L = 30$ pF, $R_L = 500\ \Omega$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit
Maximum clock frequency	f_{max}	Figure 1, Figure 3	1.8	100	—	MHz
			2.5 ± 0.2	200	—	
			3.3 ± 0.3	250	—	
Propagation delay time (An, Bn-Bn, An)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	5.1	
			3.3 ± 0.3	0.6	3.8	
Propagation delay time ($\overline{CKAB}$, $\overline{CKBA}$ -Bn, An)	t_{pLH} t_{pHL}	Figure 1, Figure 3	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	6.4	
			3.3 ± 0.3	0.6	4.4	
Propagation delay time (LEAB, LEBA-Bn, An)	t_{pLH} t_{pHL}	Figure 1, Figure 4	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	5.8	
			3.3 ± 0.3	0.6	4.4	
Output enable time ($\overline{OEAB}$, $\overline{OEBA}$ -Bn, An)	t_{pZL} t_{pZH}	Figure 1, Figure 6	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	5.9	
			3.3 ± 0.3	0.6	4.3	
Output disable time ($\overline{OEAB}$, $\overline{OEBA}$ -Bn, An)	t_{pLZ} t_{pHZ}	Figure 1, Figure 6	1.8	1.5	8.8	ns
			2.5 ± 0.2	0.8	4.9	
			3.3 ± 0.3	0.6	4.3	
Minimum pulse width	$t_{W\ (H)}$ $t_{W\ (L)}$	Figure 1, Figure 3, Figure 4	1.8	4.0	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum setup time	t_s	Figure 1, Figure 3, Figure 4, Figure 5	1.8	2.5	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum hold time	t_h	Figure 1, Figure 3, Figure 4, Figure 5	1.8	2.0	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.0	—	
Output to output skew	t_{osLH} t_{osHL}	(Note 16)	1.8	—	0.5	ns
			2.5 ± 0.2	—	0.5	
			3.3 ± 0.3	—	0.5	

For $C_L = 50$ pF, add approximately 300 ps to the AC maximum specification.

Note 16: Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

Dynamic Switching Characteristics
(Ta = 25°C, input: $t_r = t_f = 2.0$ ns, $C_L = 30$ pF, $R_L = 500\ \Omega$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Quiet output maximum dynamic V_{OL}	V_{OLP}	V_{IH} = 1.8 V, V_{IL} = 0 V (Note 17)	1.8	0.15	V
		V_{IH} = 2.5 V, V_{IL} = 0 V (Note 17)	2.5	0.25	
		V_{IH} = 3.3 V, V_{IL} = 0 V (Note 17)	3.3	0.35	
Quiet output minimum dynamic V_{OL}	V_{OLV}	V_{IH} = 1.8 V, V_{IL} = 0 V (Note 17)	1.8	−0.15	V
		V_{IH} = 2.5 V, V_{IL} = 0 V (Note 17)	2.5	−0.25	
		V_{IH} = 3.3 V, V_{IL} = 0 V (Note 17)	3.3	−0.35	
Quiet output minimum dynamic V_{OH}	V_{OHV}	V_{IH} = 1.8 V, V_{IL} = 0 V (Note 17)	1.8	1.55	V
		V_{IH} = 2.5 V, V_{IL} = 0 V (Note 17)	2.5	2.05	
		V_{IH} = 3.3 V, V_{IL} = 0 V (Note 17)	3.3	2.65	

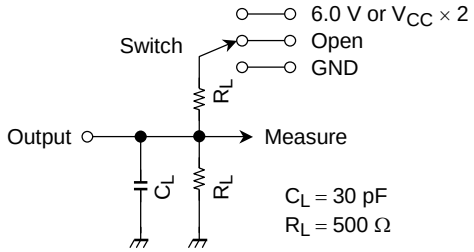
Note 17: Parameter guaranteed by design.

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Input capacitance	C_{IN}	—	1.8, 2.5, 3.3	6	pF
Bus I/O capacitance	$C_{I/O}$	—	1.8, 2.5, 3.3	7	pF
Power dissipation capacitance	C_{PD}	f_{IN} = 10 MHz (Note 18)	1.8, 2.5, 3.3	20	pF

Note 18: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:
$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/18$ (per bit)

AC Test Circuit



Parameter	Switch	
t_{pLH}, t_{pHL}	Open	
t_{pLZ}, t_{pZL}	6.0 V $V_{CC} \times 2$	@V_{CC} = 3.3 ± 0.3 V @V_{CC} = 2.5 ± 0.2 V @V_{CC} = 1.8 V
t_{pHZ}, t_{pZH}	GND	

Figure 1

AC Waveform

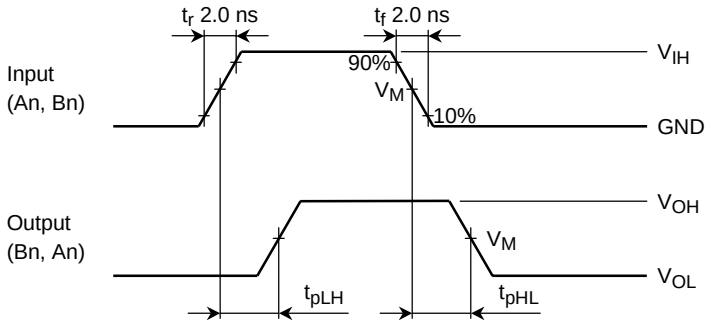


Figure 2 t_{pLH}, t_{pHL}

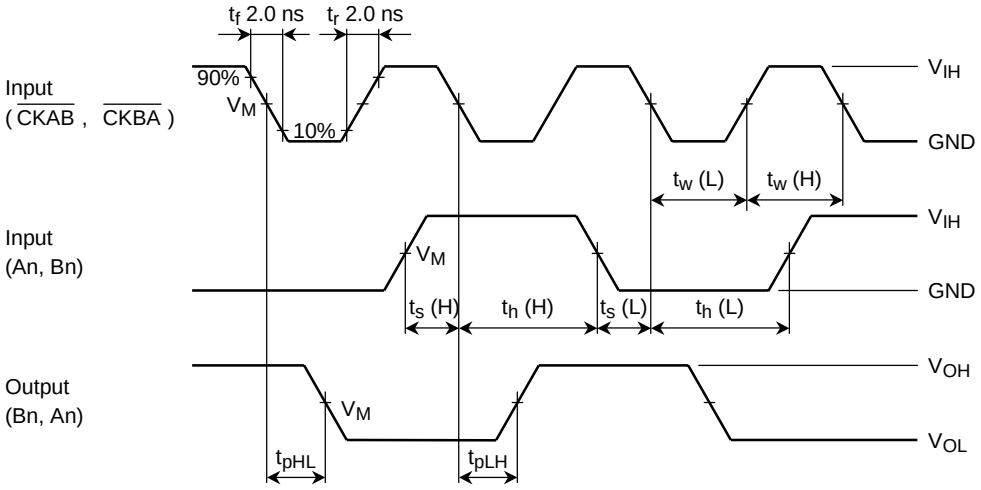


Figure 3 t_{pLH}, t_{pHL}, t_w, t_s, t_h

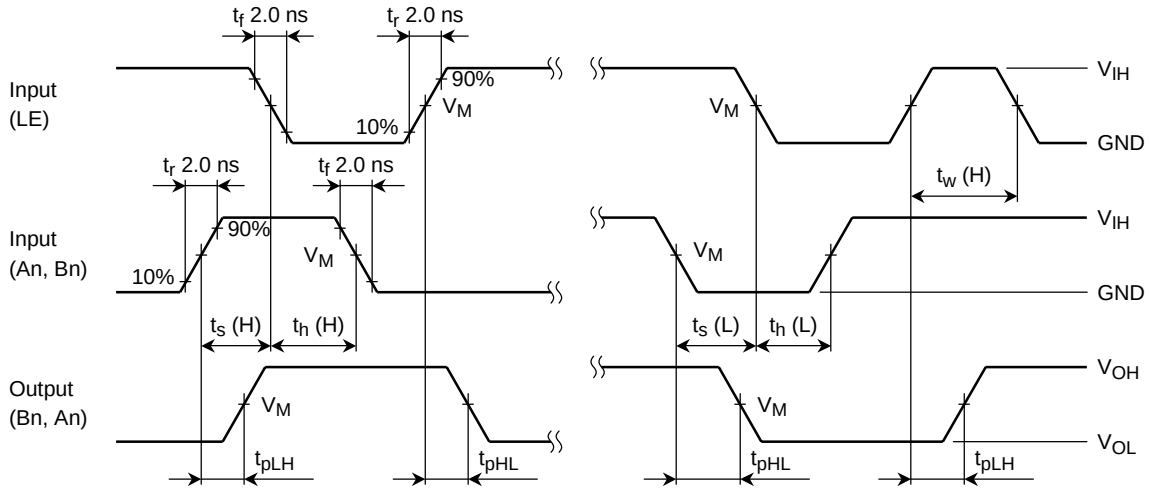


Figure 4 t_{pLH}, t_{pHL}, t_w, t_s, t_h

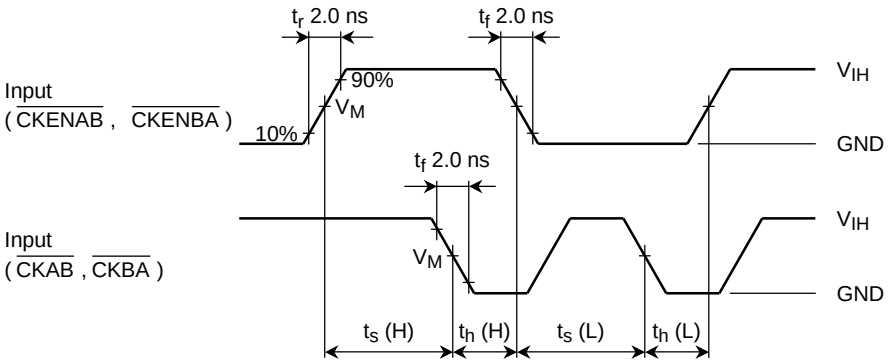


Figure 5 t_s, t_h

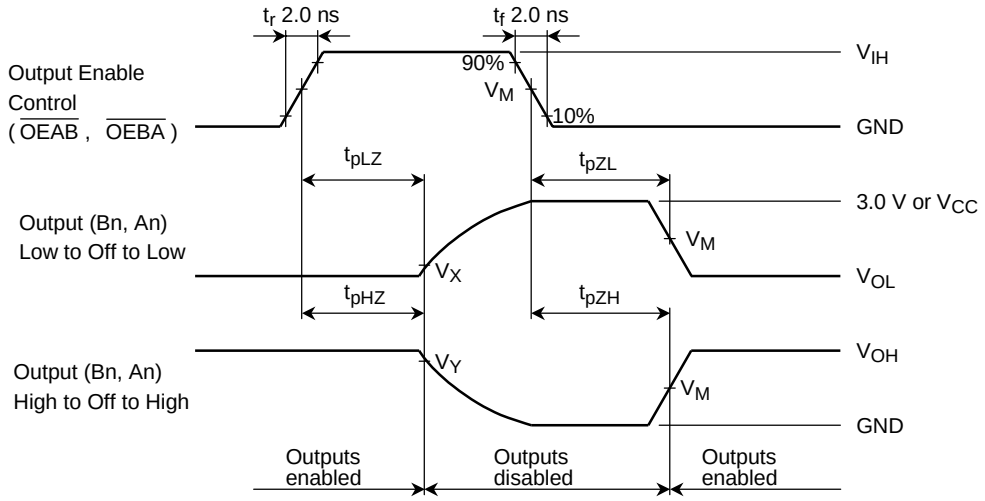
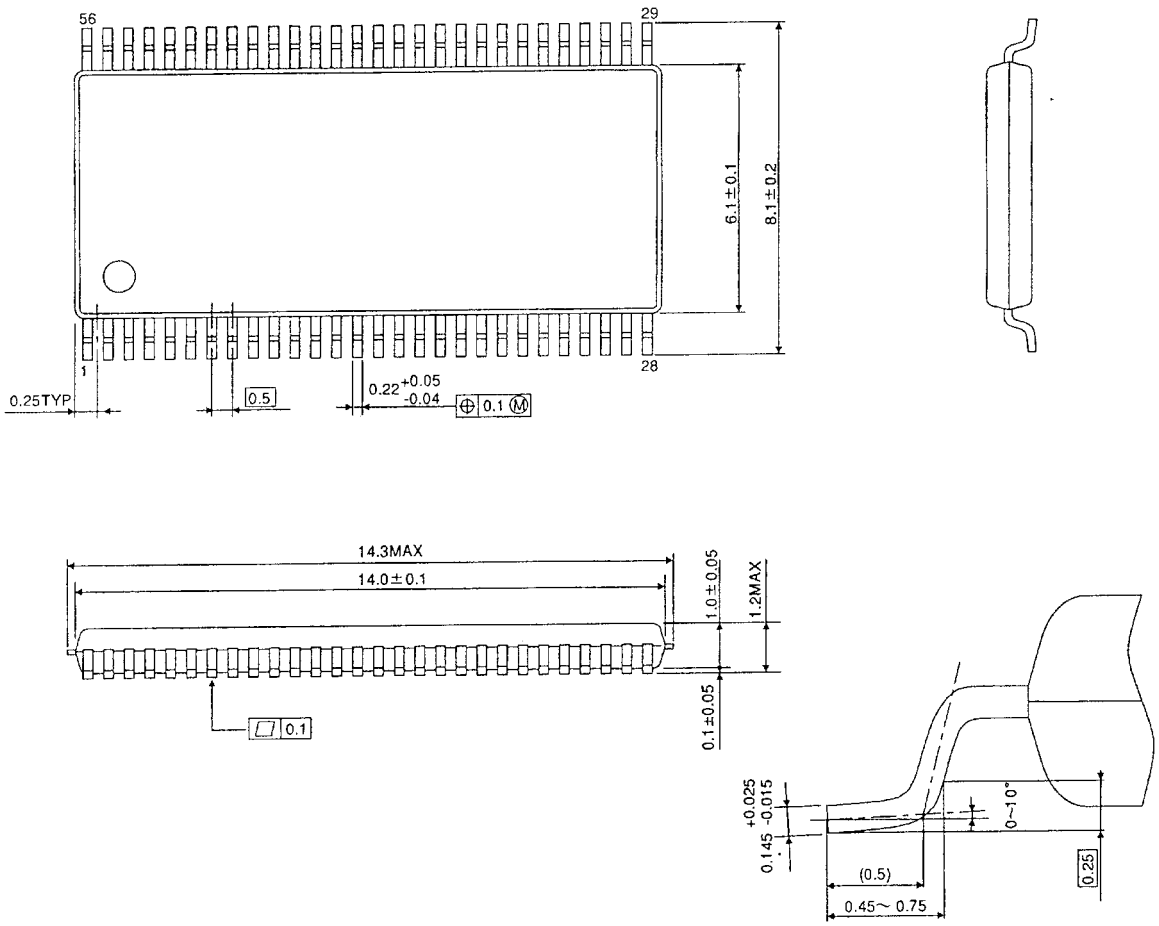


Figure 6 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

Symbol	V_{CC}		
	3.3 ± 0.3 V	2.5 ± 0.2 V	1.8 V
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_M	1.5 V	$V_{CC}/2$	$V_{CC}/2$
V_X	V_{OL} + 0.3 V	V_{OL} + 0.15 V	V_{OL} + 0.15 V
V_Y	V_{OH} − 0.3 V	V_{OH} − 0.15 V	V_{OH} − 0.15 V

Package Dimensions

TSSOP56-P-0061-0.50 Unit : mm



Weight: 0.25 g (typ.)

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