

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VCX16835FT

Low-Voltage 18-Bit Universal Bus Driver with 3.6-V Tolerant Inputs and Outputs

The TC74VCX16835FT is a high-performance CMOS 18-bit universal bus driver. Designed for use in 1.8-V, 2.5-V or 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

It is also designed with overvoltage tolerant inputs and outputs up to 3.6 V.

Data flow from A to Y is controlled by the output-enable (\overline{OE}) input.

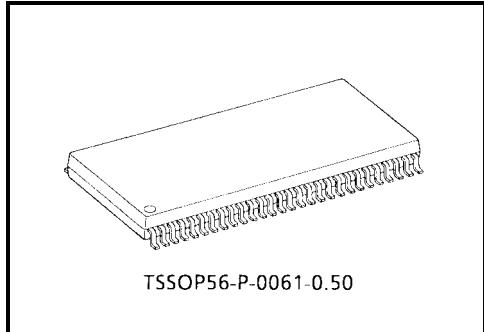
The device operates in the transparent mode when the latch-enable (LE) input is high. When LE is low, the A data is latched if the clock (CK) input is held at a high or low logic level. If LE is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CK.

When \overline{OE} is high, the outputs are in the high-impedance state.

All inputs are equipped with protection circuits against static discharge.

Features

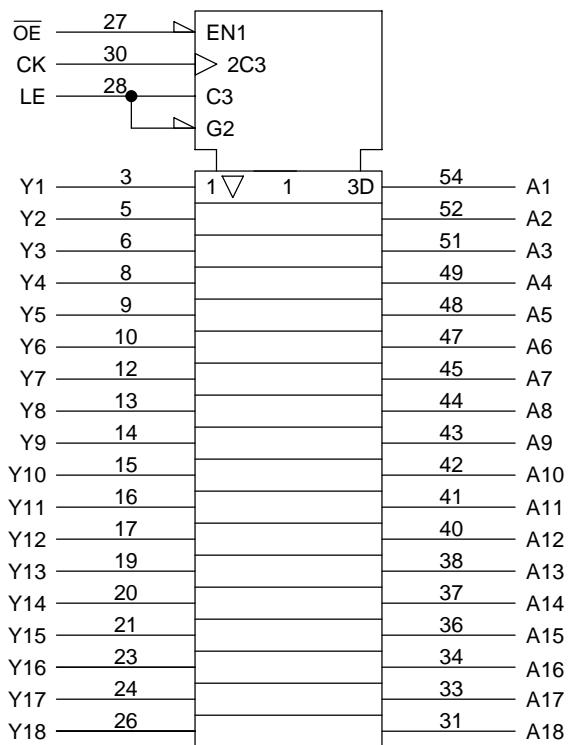
- Low-voltage operation: $V_{CC} = 1.8$ to 3.6 V
- High-speed operation: $t_{pd} = 3.3$ ns (max) ($V_{CC} = 3.0$ to 3.6 V)
 - : $t_{pd} = 4.2$ ns (max) ($V_{CC} = 2.3$ to 2.7 V)
 - : $t_{pd} = 8.4$ ns (max) ($V_{CC} = 1.8$ V)
- Output current: $I_{OH}/I_{OL} = \pm 24$ mA (min) ($V_{CC} = 3.0$ V)
 - : $I_{OH}/I_{OL} = \pm 18$ mA (min) ($V_{CC} = 2.3$ V)
 - : $I_{OH}/I_{OL} = \pm 6$ mA (min) ($V_{CC} = 1.8$ V)
- Latch-up performance: ± 300 mA
- ESD performance: Machine model $> \pm 200$ V
 - : Human body model $> \pm 2000$ V
- Package: TSSOP (thin shrink small outline package)
- 3.6-V tolerant function and power-down protection is provided on all inputs and outputs



Weight: 0.25 g (typ.)

Pin Assignment (top view)

NC	1		56	GND
NC	2		55	NC
Y1	3		54	A1
GND	4		53	GND
Y2	5		52	A2
Y3	6		51	A3
V _{CC}	7		50	V _{CC}
Y4	8		49	A4
Y5	9		48	A5
Y6	10		47	A6
GND	11		46	GND
Y7	12		45	A7
Y8	13		44	A8
Y9	14		43	A9
Y10	15		42	A10
Y11	16		41	A11
Y12	17		40	A12
GND	18		39	GND
Y13	19		38	A13
Y14	20		37	A14
Y15	21		36	A15
V _{CC}	22		35	V _{CC}
Y16	23		34	A16
Y17	24		33	A17
GND	25		32	GND
Y18	26		31	A18
OE	27		30	CK
LE	28		29	GND

IEC Logic Symbol

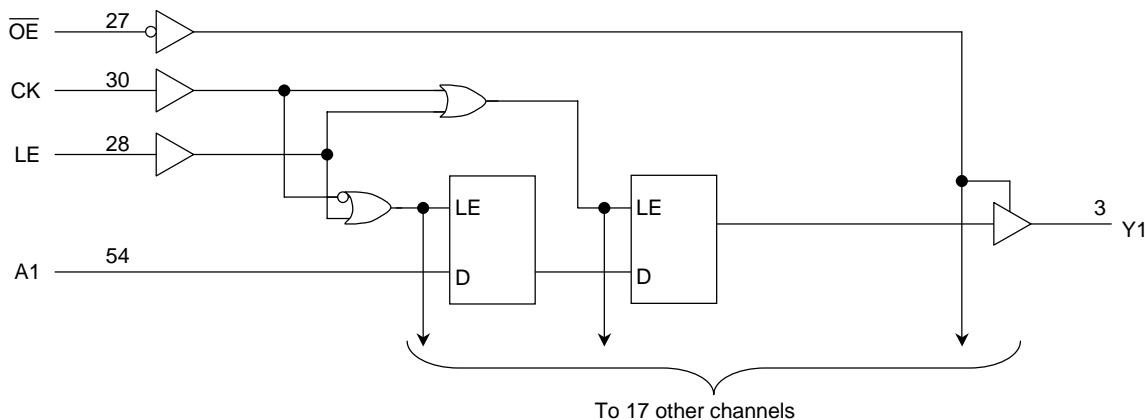
Truth Table

Inputs				Outputs Y
\overline{OE}	LE	CK	A	
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	Y0 (Note 1)
L	L	L	X	Y0 (Note 1)

X: Don't care

Z: High impedance

Note 1: Output level before the indicated steady-state input conditions were established, provided that CK was high or low before LE went low.

System Diagram

Maximum Ratings

Characteristics	Symbol	Rating	Unit
Power supply voltage	V _{CC}	-0.5 to 4.6	V
DC input voltage	V _{IN}	-0.5 to 4.6	V
DC output voltage	V _{OUT}	-0.5 to 4.6 (Note 2)	V
		-0.5 to V _{CC} + 0.5 (Note 3)	
Input diode current	I _{IK}	-50	mA
Output diode current	I _{OK}	±50 (Note 4)	mA
DC output current	I _{OUT}	±50	mA
Power dissipation	P _D	400	mW
DC V _{CC} /ground current per supply pin	I _{CC} /I _{GND}	±100	mA
Storage temperature	T _{stg}	-65 to 150	°C

Note 2: OFF state

Note 3: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 4: V_{OUT} < GND, V_{OUT} > V_{CC}

Recommended Operating Range

Characteristics	Symbol	Rating	Unit
Power supply voltage	V _{CC}	1.8 to 3.6	V
		1.2 to 3.6 (Note 5)	
Input voltage	V _{IN}	-0.3 to 3.6	V
Output voltage	V _{OUT}	0 to 3.6 (Note 6)	V
		0 to V _{CC} (Note 7)	
Output current	I _{OH} /I _{OL}	±24 (Note 8)	mA
		±18 (Note 9)	
		±6 (Note 10)	
Operating temperature	T _{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 10 (Note 11)	ns/V

Note 5: Data retention only

Note 6: OFF state

Note 7: High or low state

Note 8: V_{CC} = 3.0 to 3.6 V

Note 9: V_{CC} = 2.3 to 2.7 V

Note 10: V_{CC} = 1.8 V

Note 11: V_{IN} = 0.8 to 2.0 V, V_{CC} = 3.0 V

Electrical Characteristics**DC Characteristics (Ta = -40 to 85°C, 2.7 V < V_{CC} ≤ 3.6 V)**

Characteristics		Symbol	Test Condition		V _{CC} (V)	Min	Max	Unit	
Input voltage	H-level		—	2.7 to 3.6					
	L-level	V _{IL}	—	2.7 to 3.6	—	0.8	—		
Output voltage	H-level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -100 μA	2.7 to 3.6	V _{CC} - 0.2	—	V	
				I _{OH} = -12 mA	2.7	2.2	—		
				I _{OH} = -18 mA	3.0	2.4	—		
				I _{OH} = -24 mA	3.0	2.2	—		
	L-level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	2.7 to 3.6	—	0.2		
				I _{OL} = 12 mA	2.7	—	0.4		
				I _{OL} = 18 mA	3.0	—	0.4		
				I _{OL} = 24 mA	3.0	—	0.55		
Input leakage current		I _{IN}	V _{IN} = 0 to 3.6 V		2.7 to 3.6	—	±5.0	μA	
3-state output OFF state current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 3.6 V		2.7 to 3.6	—	±10.0	μA	
Power-off leakage current		I _{OFF}	V _{IN} , V _{OUT} = 0 to 3.6 V		0	—	10.0	μA	
Quiescent supply current		I _{CC}	V _{IN} = V _{CC} or GND V _{CC} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V		2.7 to 3.6	—	20.0	μA	
Increase in ICC per input		ΔI _{CC}	V _{IH} = V _{CC} - 0.6 V		2.7 to 3.6	—	750		

DC Characteristics (Ta = -40 to 85°C, 2.3 V ≤ V_{CC} ≤ 2.7 V)

Characteristics		Symbol	Test Condition		V _{CC} (V)	Min	Max	Unit	
Input voltage	H-level		—	2.3 to 2.7	1.6	—			
	L-level	V _{IL}	—	2.3 to 2.7	—	0.7			
Output voltage	H-level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -100 μA	2.3 to 2.7	V _{CC} - 0.2	—	V	
				I _{OH} = -6 mA	2.3	2.0	—		
				I _{OH} = -12 mA	2.3	1.8	—		
				I _{OH} = -18 mA	2.3	1.7	—		
	L-level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	2.3 to 2.7	—	0.2		
				I _{OL} = 12 mA	2.3	—	0.4		
				I _{OL} = 18 mA	2.3	—	0.6		
				I _{OL} = 24 mA	2.3	—	0.8		
Input leakage current		I _{IN}	V _{IN} = 0 to 3.6 V		2.3 to 2.7	—	±5.0	μA	
3-state output OFF state current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 3.6 V		2.3 to 2.7	—	±10.0	μA	
Power-off leakage current		I _{OFF}	V _{IN} , V _{OUT} = 0 to 3.6 V		0	—	10.0	μA	
Quiescent supply current		I _{CC}	V _{IN} = V _{CC} or GND V _{CC} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V		2.3 to 2.7	—	20.0	μA	

DC Characteristics ($T_a = -40$ to 85°C , $1.8 \text{ V} \leq V_{CC} < 2.3 \text{ V}$)

Characteristics		Symbol	Test Condition		$V_{CC} (\text{V})$	Min	Max	Unit	
Input voltage	H-level	V_{IH}	—		1.8 to 2.3	$0.7 \times V_{CC}$	—	V	
	L-level	V_{IL}	—		1.8 to 2.3	—	$0.2 \times V_{CC}$		
Output voltage	H-level	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -100 \mu\text{A}$	1.8	$V_{CC} - 0.2$	—	V	
				$I_{OH} = -6 \text{ mA}$	1.8	1.4	—		
	L-level	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 100 \mu\text{A}$	1.8	—	0.2		
				$I_{OL} = 6 \text{ mA}$	1.8	—	0.3		
Input leakage current		I_{IN}	$V_{IN} = 0$ to 3.6 V		1.8	—	± 5.0	μA	
3-state output OFF state current		I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = 0$ to 3.6 V		1.8	—	± 10.0	μA	
Power-off leakage current		I_{OFF}	$V_{IN}, V_{OUT} = 0$ to 3.6 V		0	—	10.0	μA	
Quiescent supply current		I_{CC}	$V_{IN} = V_{CC}$ or GND		1.8	—	20.0	μA	
			$V_{CC} \leq (V_{IN}, V_{OUT}) \leq 3.6 \text{ V}$		1.8	—	± 20.0		

AC Characteristics (Ta = -40 to 85°C, input: t_r = t_f = 2.0 ns, C_L = 30 pF, R_L = 500 Ω)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Min	Max	Unit
Maximum clock frequency	f _{max}	Figure 1, Figure 3	1.8	100	—	MHz
			2.5 ± 0.2	200	—	
			3.3 ± 0.3	250	—	
Propagation delay time (An-Yn)	t _{pLH}	Figure 1, Figure 2	1.8	1.5	8.4	ns
			2.5 ± 0.2	0.8	4.2	
	t _{pHL}		3.3 ± 0.3	0.6	3.3	
Propagation delay time (CK-Yn)	t _{pLH}	Figure 1, Figure 3	1.8	2.0	9.2	ns
			2.5 ± 0.2	1.5	5.2	
	t _{pHL}		3.3 ± 0.3	1.4	4.2	
Propagation delay time (LE-Yn)	t _{pLH}	Figure 1, Figure 4	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	4.9	
	t _{pHL}		3.3 ± 0.3	0.6	3.8	
Output enable time	t _{pZL}	Figure 1, Figure 5	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	4.9	
	t _{pZH}		3.3 ± 0.3	0.6	3.8	
Output disable time	t _{pLZ}	Figure 1, Figure 5	1.8	1.5	7.6	ns
			2.5 ± 0.2	0.8	4.5	
	t _{pHZ}		3.3 ± 0.3	0.6	3.9	
Minimum pulse width	t _W (H)	Figure 1, Figure 3, Figure 4	1.8	4.0	—	ns
			2.5 ± 0.2	1.5	—	
	t _W (L)		3.3 ± 0.3	1.5	—	
Minimum setup time (An-CK, An-LE)	t _s	Figure 1, Figure 3, Figure 4	1.8	2.5	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum hold time (An-CK, An-LE)	t _h	Figure 1, Figure 3, Figure 4	1.8	1.0	—	ns
			2.5 ± 0.2	0.7	—	
			3.3 ± 0.3	0.7	—	
Output to output skew	t _{osLH}	(Note 12)	1.8	—	0.5	ns
			2.5 ± 0.2	—	0.5	
	t _{osHL}		3.3 ± 0.3	—	0.5	

Note 12: Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

AC Characteristics (Ta = 0 to 85°C, input: $t_r = t_f = 2.0 \text{ ns}$, $C_L = 0 \text{ pF}$, $R_L = 500 \Omega$)

Characteristics	Symbol	Test Condition	$V_{CC} (\text{V})$	Min	Max	Unit
			(Note 13)			
Propagation delay time (An-Yn)	t_{pLH} t_{pHL}	Figure 1, Figure 2	3.3 ± 0.15	0.9	2.0	ns
Propagation delay time (CK-Yn)	t_{pLH} t_{pHL}	Figure 1, Figure 3	3.3 ± 0.15	1.5	2.9	ns
Propagation delay time (LE-Yn)	t_{pLH} t_{pHL}	Figure 1, Figure 4	3.3 ± 0.15	0.7	2.6	ns
Output enable time	t_{pZL} t_{pZH}	Figure 1, Figure 5	3.3 ± 0.15	0.7	2.6	ns
Output disable time	t_{pLZ} t_{pHZ}	Figure 1, Figure 5	3.3 ± 0.15	0.7	2.7	ns
Minimum setup time (An-CK, An-LE)	t_s	Figure 1, Figure 3, Figure 4	3.3 ± 0.15	1.5	—	ns
Minimum hold time (An-CK, An-LE)	t_h	Figure 1, Figure 3, Figure 4	3.3 ± 0.15	0.7	—	ns

Note 13: TOSHIBA SPICE simulation data.

AC Characteristics (Ta = 0 to 85°C, input: $t_r = t_f = 2.0 \text{ ns}$, $C_L = 50 \text{ pF}$, $R_L = 500 \Omega$)

Characteristics	Symbol	Test Condition	$V_{CC} (\text{V})$	Min	Max	Unit
			(Note 13)			
Propagation delay time (An-Yn)	t_{pLH} t_{pHL}	Figure 1, Figure 2	3.3 ± 0.15	1.0	3.6	ns
Propagation delay time (CK-Yn)	t_{pLH} t_{pHL}	Figure 1, Figure 3	3.3 ± 0.15	1.7	4.5	ns
Propagation delay time (LE-Yn)	t_{pLH} t_{pHL}	Figure 1, Figure 4	3.3 ± 0.15	1.0	4.1	ns
Output enable time	t_{pZL} t_{pZH}	Figure 1, Figure 5	3.3 ± 0.15	1.0	4.1	ns
Output disable time	t_{pLZ} t_{pHZ}	Figure 1, Figure 5	3.3 ± 0.15	1.0	4.2	ns
Minimum setup time (An-CK, An- LE)	t_s	Figure 1, Figure 3, Figure 4	3.3 ± 0.15	1.5	—	ns
Minimum hold time (An-CK, An-LE)	t_h	Figure 1, Figure 3, Figure 4	3.3 ± 0.15	0.7	—	ns

Dynamic Switching Characteristics(Ta = 25°C, input: t_r = t_f = 2.0 ns, C_L = 30 pF, R_L = 500 Ω)

Characteristics	Symbol	Test Condition		V _{CC} (V)	Typ.	Unit
		V _{IH}	V _{IL}			
Quiet output maximum dynamic V _{OL}	V _{OLP}	V _{IH} = 1.8 V, V _{IL} = 0 V	(Note 14)	1.8	0.35	V
		V _{IH} = 2.5 V, V _{IL} = 0 V	(Note 14)	2.5	0.7	
		V _{IH} = 3.3 V, V _{IL} = 0 V	(Note 14)	3.3	0.9	
Quiet output minimum dynamic V _{OL}	V _{OLV}	V _{IH} = 1.8 V, V _{IL} = 0 V	(Note 14)	1.8	-0.35	V
		V _{IH} = 2.5 V, V _{IL} = 0 V	(Note 14)	2.5	-0.7	
		V _{IH} = 3.3 V, V _{IL} = 0 V	(Note 14)	3.3	-0.9	
Quiet output minimum dynamic V _{OH}	V _{OHV}	V _{IH} = 1.8 V, V _{IL} = 0 V	(Note 14)	1.8	1.3	V
		V _{IH} = 2.5 V, V _{IL} = 0 V	(Note 14)	2.5	1.7	
		V _{IH} = 3.3 V, V _{IL} = 0 V	(Note 14)	3.3	2.0	

Note 14: Parameter guaranteed by design.

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition		V _{CC} (V)	Typ.	Unit
		V _{CC}	V _{IN}			
Input capacitance	C _{IN}	—	—	1.8, 2.5, 3.3	6	pF
Output capacitance	C _{OUT}	—	—	1.8, 2.5, 3.3	7	pF
Power dissipation capacitance	C _{PD}	f _{IN} = 10 MHz	(Note 15)	1.8, 2.5, 3.3	20	pF

Note 15: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/18 \text{ (per bit)}$$

AC Test Circuit

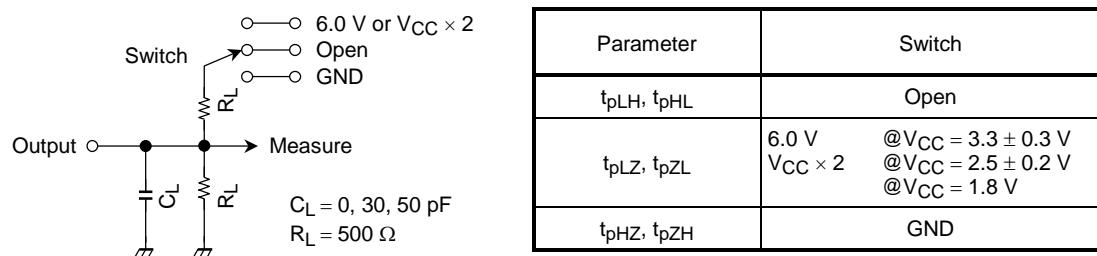
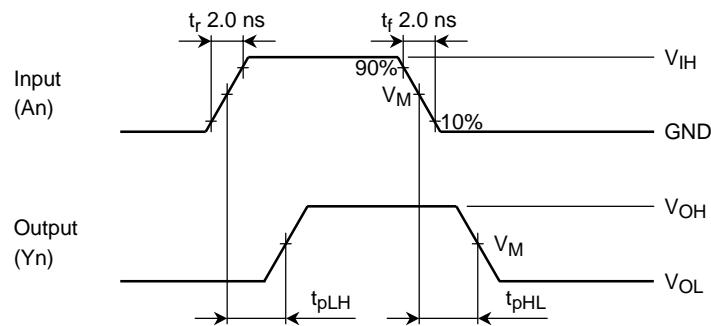
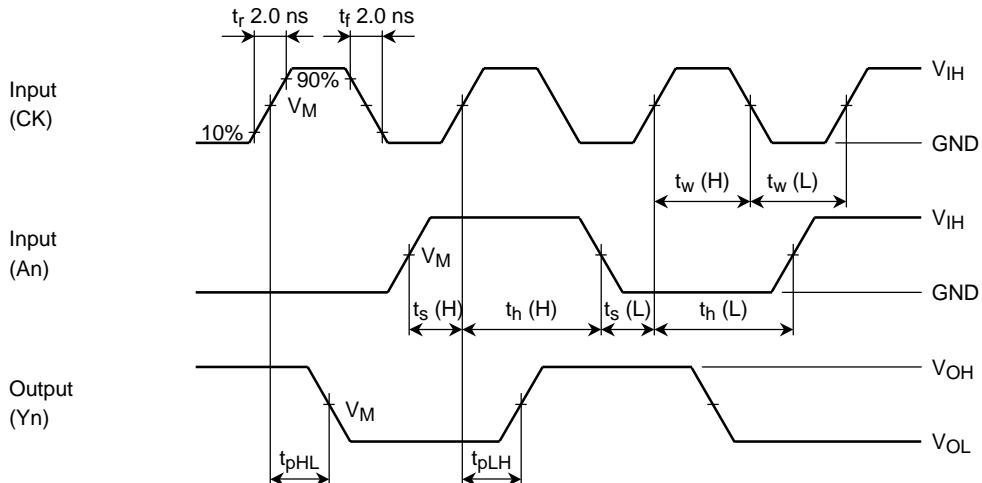
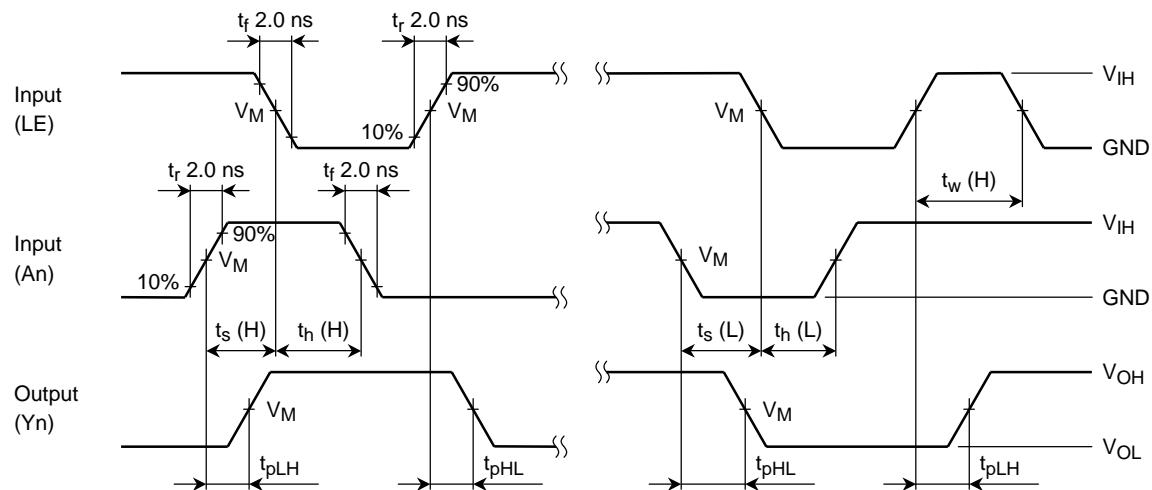
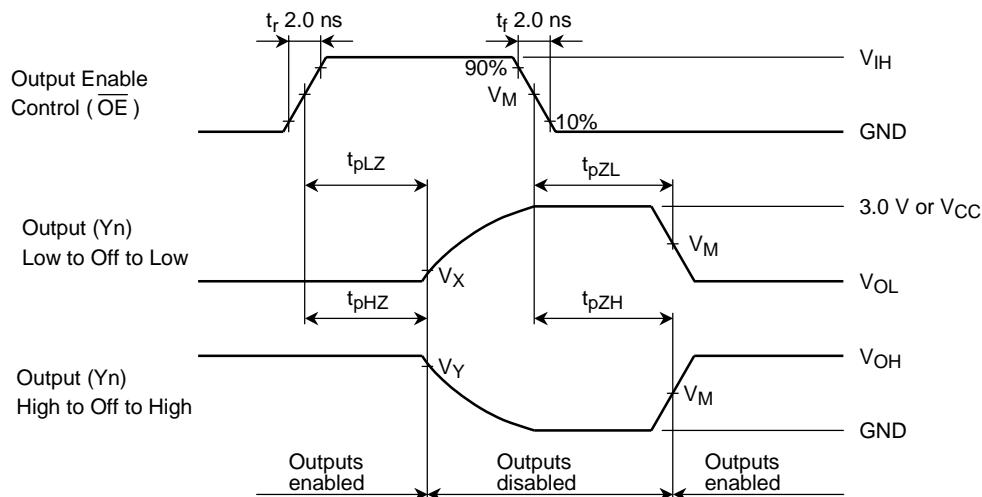


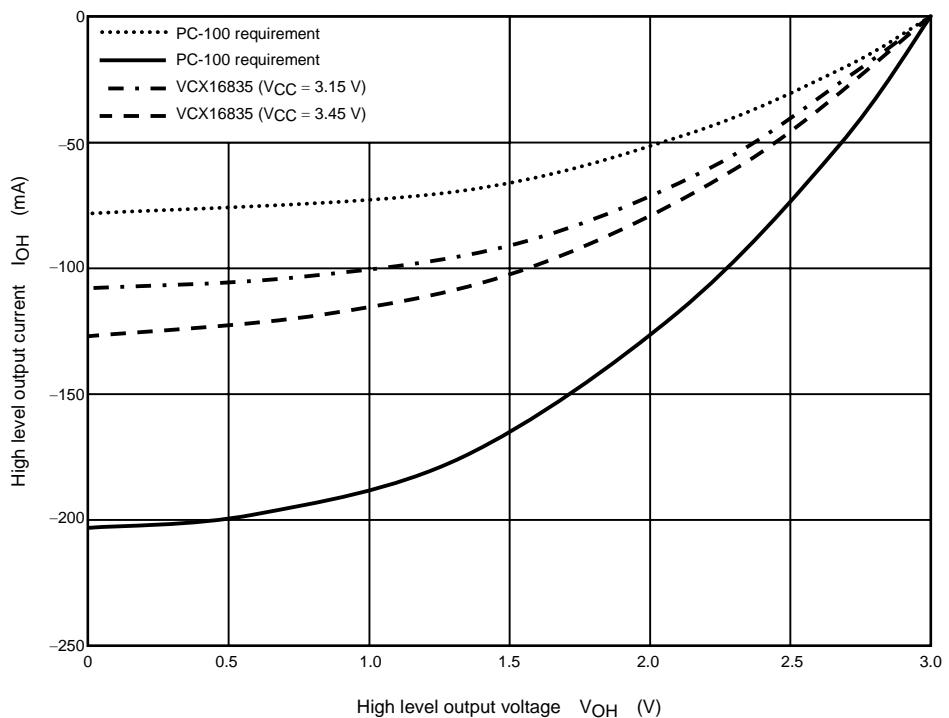
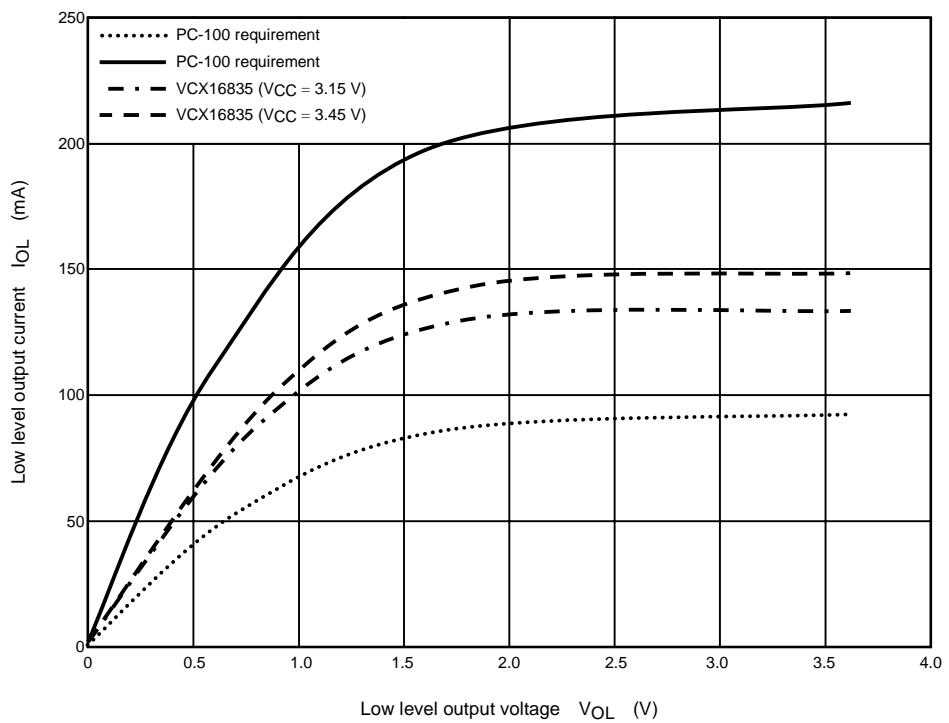
Figure 1

AC Waveform

Figure 2 t_{pLH}, t_{pHL} Figure 3 $t_{pLH}, t_{pHL}, t_w, t_s, t_h$

Figure 4 t_{pLH} , t_{pHL} , t_w , t_s , t_h Figure 5 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}

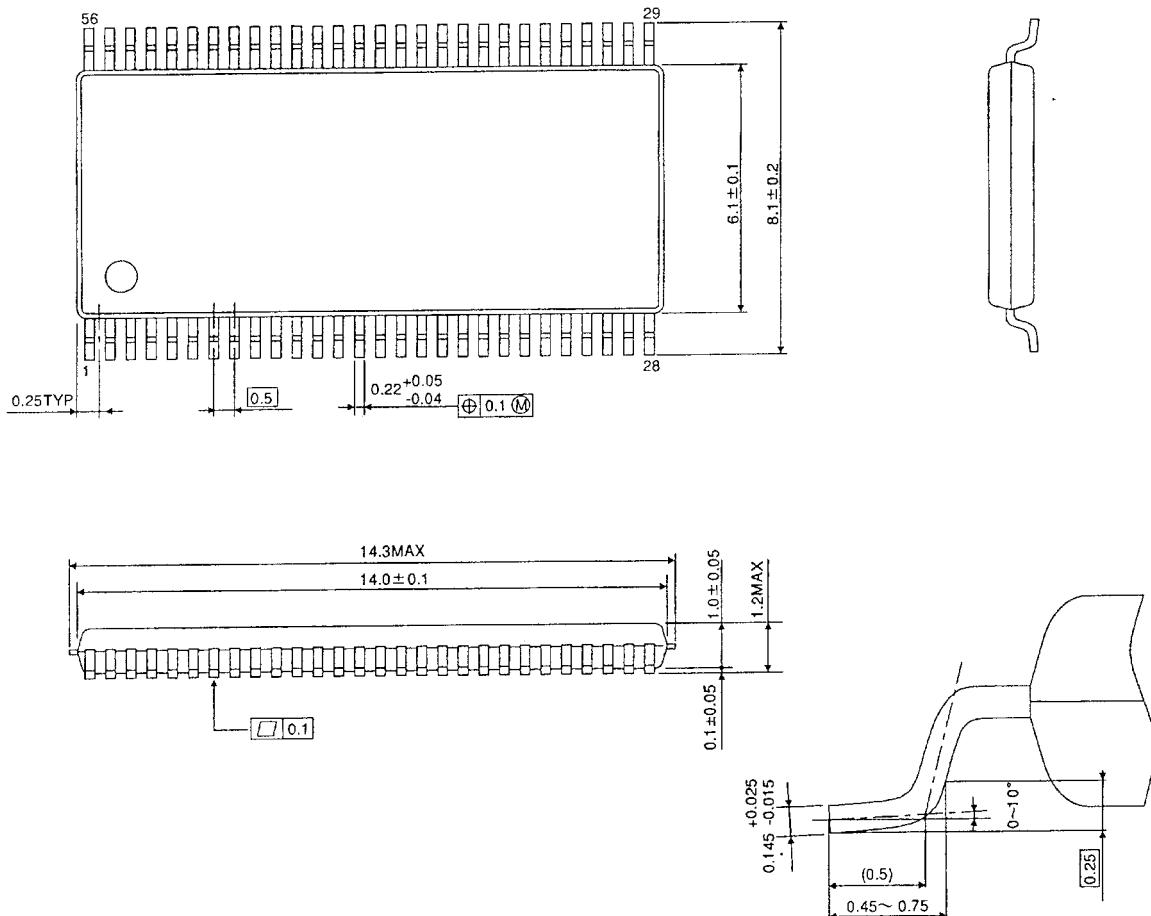
Symbol	V_{CC}		
	$3.3 \pm 0.3\text{ V}$	$2.5 \pm 0.2\text{ V}$	1.8 V
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_M	1.5 V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3\text{ V}$	$V_{OL} + 0.15\text{ V}$	$V_{OL} + 0.15\text{ V}$
V_Y	$V_{OH} - 0.3\text{ V}$	$V_{OH} - 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$

IBIS Characteristics (typ.)**Figure 6 I/V Characteristics-Pullup****Figure 7 I/V Characteristics-Pulldown**

Package Dimensions

TSSOP56-P-0061-0.50

Unit : mm



Weight: 0.25 g (typ.)

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