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Product Brief

TC358791XBG Automotive Infotainment Companion Chip

Highlights

- Gigabit Ethernet® (supports AVB) interface to connect multiple audio and video sources; supports up to 8 streams
- USB 3.0/2.0 and MIPI® CSI-2 connectivity to the host processor
- Differential CVBS (composite) interfaces for analog composite video sources (examples: rear-view camera, DVD player)
- Early back-up camera view (CVBS to LVDS)
- High-resolution display support (up to 2560 x 1600) for LVDS panels
- HDMI® 1.4 receiver interface to connect smartphones and other HDMI enabled devices
- Packetized IQ audio tuner data to the host via USB
- AEC-Q100 Grade 3 qualified device to host processor
- Addresses applications such as automotive, mobile, smart TVs, professional audio, etc.

Description

The Toshiba TC358791XBG is an automotive infotainment chipset supporting high-resolution multimedia (audio, video) camera connectivity for next-generation automotive infotainment applications in the connected car.

The TC358791XBG supports the latest[1] automotive Ethernet® AVB standard for applications such as front/rear/surround-view cameras, digital audio, transferring high-resolution video content to head unit and rear seat entertainment systems, etc.

The TC358791XBG can seamlessly interface with leading-edge application processors in the automotive market via USB 3.0 and MIPI® CSI2 connectivity for both audio and video.

The TC358791XBG is capable of accepting multiple camera feeds such as rear view and front view, and directly drive LVDS digital displays (head unit, instrument cluster, etc.), supporting up to 2560 x 1600 resolution. It can also send high-resolution audio and video data from the host processor to multiple displays or other Electronic Control Units (ECU) in the car. It accepts HDMI® video and audio streams.

Features

Gigabit Ethernet Interface (RGMII)

- Supports legacy Ethernet, AVB traffic
- Support for Generalized Precision Timing Protocol (IEEE 802.1AS), IEEE 802.1Qav, IEEE 1722
- Supports IEEE 802.3az-2010 for Energy Efficient Ethernet (EEE)

CVBS Interface

- Two differential or two single ended CVBS sources can be connected (only one active at a time)
- Supports NTSC (480i)/PAL (576i) format

HDMI-RX Interface

- HDMI Rev 1.4b compliant
- Maximum pixel clock rate @ 297 MHz (Up to 4K x 2K @ 30 fps)
- Video format support
  - RGB888, YCbCr444: 24-bpp
  - YCbCr422 24-bpp
- Support for HDCP (High-bandwidth Digital Content Protection) Rev 1.4
- Support for DDC (Display Data Channel)

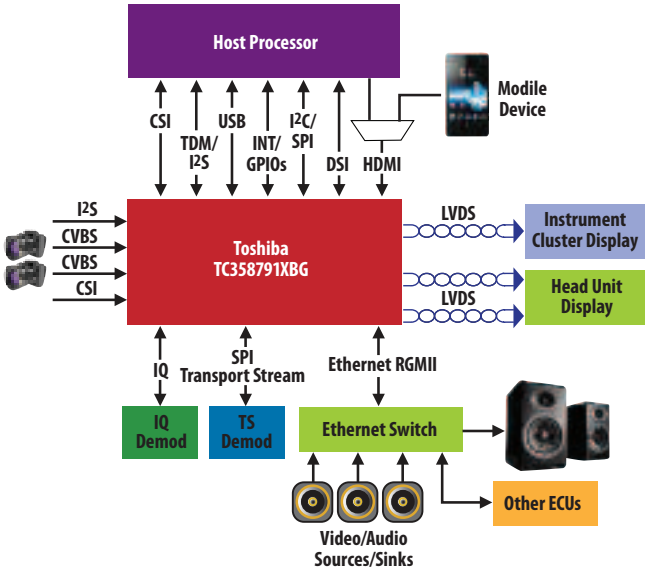
CSI-2/DSI RX Interface

- Supports up to 4 data lanes, 1 Gbps/lane
- Supports either CSI-2 RX or DSI RX protocol
- DSI data format supported: RGB888 and RGB666

Data Paths Supported

Input Interface	Output Interface
CVBS	OPENLDI 0 (LVDS Display)
CVBS	MIPI CSI2-Tx
MIPI CSI2-Rx	MIPI CSI2-Tx
MIPI CSI2-Rx	OPENLDI 0/1 (LVDS Display)
DSI-Rx	OPENLDI 0/1 (LVDS Display)
HDMI-Rx	OPENLDI 0/1 (LVDS Display)
HDMI-Rx	USB 3.0/2.0
Ethernet RGMII	USB 3.0/2.0
Ethernet RGMII	TDM 0/1
SPI	USB 3.0/2.0
IQ (Raw audio data)	USB 3.0/2.0
I²S	TDM 2

TC358791XBG System Block Diagram



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- MIPI CSI-2 compliant (Version 1.01 Revision 0.04 – 2 April 2009)
  - Data format supported: RAW 8/10/12, YUV422 (CCIR/ITU 8-bit), RGB888/666/565 and user-defined 8-bit

CSI-2 TX Interface

- MIPI CSI-2 compliant (Version 1.01 Revision 0.04 – 2 April 2009)
  - Supports up to 4 data lanes
- Supports up to 1 Gbps per data lane
  - Video, audio and InfoFrame data can be transmitted

I²S TDM Interface

- I²S input ports and TDM output port
  - Three I²S input ports
  - One TDM output port
  - One, two or three I²S inputs multiplexed into one TDM output port
- TDM input ports and I²S output ports
  - One TDM input port
  - Three I²S output ports
  - TDM input streams can be de-mux to one, two or three I²S outputs streams

USB 3.0/2.0 Device Interface

- Full speed, high speed or super speed

TDM Audio Interfaces

- Time division multiplexed (multi-stream and multi-channel) audio stream bus.
  - Maximum bit clock rate @50 MHz
- Two independent TDM ports
  - Full duplex for each port
- Support 16/24/32-bit wide time slot
- Input mode
  - Supports up to 4 different audio streams per TDM port with up to eight channels each
- Output mode:
  - Source: Ethernet AVB; supports single audio stream with up to eight channels
  - Source: HDMI; supports single audio stream with up to eight channels

LVDS Display Interfaces

- Supports one single-link and one dual-link LVDS interface
- Supports video splitter function
- Single-link LVDS interface (OPENLDI 1):
  - Maximum pixel clock frequency: 85 MHz
  - Maximum panel size: 1400 x 900 pixels
- Dual-link LVDS interface (OPENLDI 0):
  - Maximum panel size: 2560 x 1600 pixels
  - Maximum pixel clock frequency: 135 MHz
  - Supports video up scaling

I²C/SPI0 Slave Interface

- I²C mode
  - Support for normal (100 KHz), fast mode (400 KHz) and high-speed mode (1 MHz)
- SPI mode
  - Maximum frequency is 30 MHz

SPI1 Transport Stream Interface

- Maximum frequency is 50 MHz
- Input: Transport video stream only to be transmitted over USB

IQ In Audio Interfaces

- Supports two independent IQ input ports
- Supports slave clock mode only, maximum bit clock rate @12.288 MHz
- Audio sample frequency, f_S: 44.1 KHz or 48 KHz only

Power Supply Inputs

- 1.1V Core voltage
- 1.2V MIPI D-PHY
- 1.8V USB PHY
- 2.5V RGMII
- 3.3V HDMI PHY and USB PHY

Package

- FBGA257, 15.0 x 15.0 mm
  0.8 mm ball pitch, 1.7 mm height

AEC-Q100 Qualified Device

- Grade 3

[1] As of 10/23/14

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