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Product Brief

TC358770XBG Display Interface Converter Chipset for High Resolution Display

(Dual MIPI® Input to Display Port)

Highlights

- TC358770XBG concatenates two video streams coming into its dual MIPI® receivers into one image and converts it into a Display Port video stream.
- Solutions are based on the latest versions of industry standard MIPI DSI 1.01 and VESA Display Port 1.1a.
- Support for high-resolution display port panels that require more than 4 Gbps data bandwidth.
- Applicable to portable products such as tablets and netbooks with high-resolution display port panels.

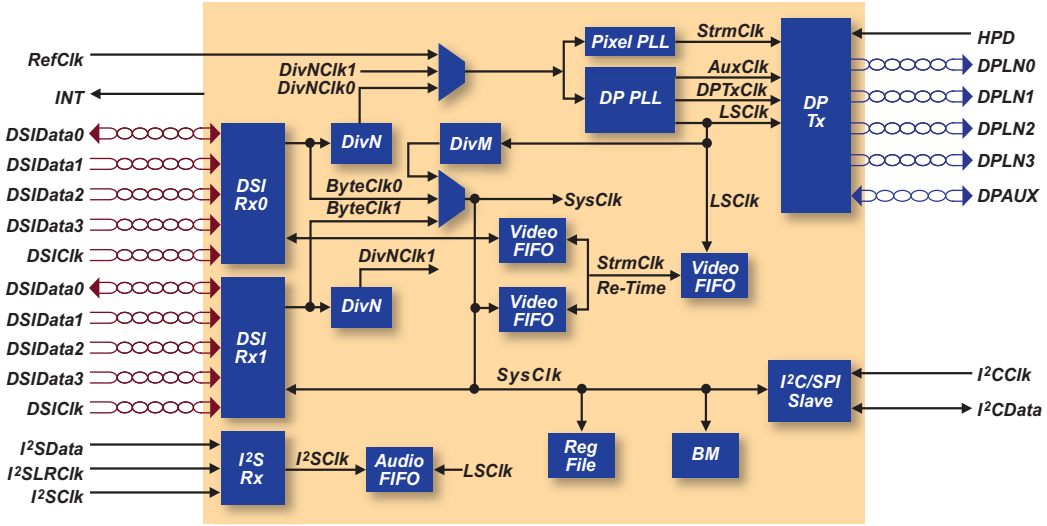
Description

The Toshiba Mobile Industry Processor Interface (MIPI®) Display Serial Interface (DSI) to Display Port converter chipset enables Application Processors to support high-resolution Display Port panels that require bandwidth above 4 Gbps. Designated TC358770XBG, the chipset incorporates dual MIPI DSI receivers, and accepts multiple video packets simultaneously over dual DSI receivers. The Application Processor should be able to divide one high-resolution image and send the data over two DSI transmitter ports. The bridge concatenates the video packets from the dual ports into a single video packet row by row. After converting the MIPI DSI data into Display Port data, the bridge is able to drive a Display Port panel. Each DSI receiver port has four lanes, with data speed of 1 Gbps per lane, times two ports, for a total throughput bandwidth of up to 8 Gbps. Each MIPI DSI receiver port supports 1 to 4-lane configurations. As the Display Port interface uses fewer lines and efficient power consumption, availability and usage of high-resolution Display Port panels is becoming a feature in handheld applications such as tablets and netbooks. The Toshiba TC358770XBG display bridge enables connectivity of Display Port panels to Application Processors with MIPI DSI interfaces. The bridge supports the Synchronous Clock mode of the Display Port interface standard. High- resolution panels such as 1920 x 1200 at 24 bit per pixel can be supported with a single DSI receiver. Higher resolutions than 1920 x 1200, such as Quad-WXGA, (2560x1600, 24-bit per pixel), creates difficulty as the bandwidth requirement is higher than 4 Gbps. This bridge offers solution in supporting high-resolution panels by utilizing the two DSI ports that most Application Processors already have.

The TC358770XBG bridge supports audio streaming from the application processor via I²S interface to the Host. The audio data is transmitted through the Display Port link if the application requires, i.e. connecting to an external panel. The bridge can support either an internal or external Display Port panel at one time.

The Toshiba TC358770XBG is a 100-pin device and is optimized for handheld applications such as thin notebooks. It has a small package size of 5 mm x 5 mm, 0.4 mm ball pitch.

TC358770XBG Block Diagram



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Features

DSI RX Ports

- MIPI DSI compliant version 1.01
- Supports two independent DSI RX ports
  - — Supports 1 to 4-data lane configurations per port
  - — Supports up to 1 Gbps per data lane
  - — Bidirectional support on Data Lane 0
  - — Receives and concatenates video packets from each DSI link and outputs them as one row of Display Port video packet
- Video input data formats: RGB565, RGB666 and RGB888

Display Port TX Port

- VESA Display Port 1.1a compliant
- Supports a four-lane main link for high bandwidth applications
  - — Supports data rates at 1.62 Gbps or 2.7 Gbps per lane of Display Port link with voltage swings at 0.4, 0.6, 0.8 or 1.2V
  - — AUX channel supported at 1 Mbps
- HPD (Hot Plug Detect) support through GPIO based interrupts
- SSCG with ~30 KHz modulation to reduce EMI
- Built in PRBS7 and colorbar generators to test Display Port link
- Supports content protection schemes such as HDCP encryption for external DP panels and ASSR (Alternative Scrambler Seed Reset) for embedded DP panel
- Supports audio data as secondary data packets

Audio Interface

- Either I^2S or TDM Audio interface are available (pins are multiplexed)
- I^2S Audio Interface
  - — Supports single stereo channel
  - — Supports 16, 18, 20 or 24-bit data
  - — Supports sampling frequencies of 32, 44.1, 48, 88.2, 96, 176.4 and 192 KHz
- TDM Audio Interface
  - — Supports single data link
  - — Supports 2, 4, 6 or 8 channels
  - — Supports 16, 18, 20 or 24-bit PCM audio data word

I^2C Interface

- I^2C slave interface for access to bridge set of registers
- I^2C compliant slave interface support for normal (100 KHz) and fast mode (400 KHz)

Clock Source

- Display Port clock source from an external clock input or clock can be derived from the DSI interface – generates all internal and output clocks to display devices
- Built-in PLLs generate a high speed Display Port serializing clock

Power Supply Inputs

- Core and MIPI D-PHY: 1.2V +/- 0.1V
- Digital I/O: 1.8 +/- 0.15V
- Display Port: 1.8V

Package

- TC358770XBG: 100-pin, 5.0 mm x 5.0 mm, 0.40 mm ball pitch, 1.0 mm height

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