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Product Brief

TC358763 Serializer Display Bridge

Highlights

- Serializer display bridge for connectivity of MIPI® DSI panels to the Baseband or Application Processor using legacy parallel LCD interfaces.
- Solutions are based on the latest versions of industry standard MIPI DSI 1.01 interface to ensure high speed data rates of up to 500 Mbps per lane.
- Legacy interfaces such as MIPI DPI and MIPI DBI are supported as Host interfaces.
- Applicable to a range of mobile product platforms such as smartphones, netbooks, smartbooks, MIDs and PNDs.

Description

The Toshiba TC358763XBG serializer display bridge is optimized for mobile handsets using a high-resolution display panel with MIPI® Display Serial Interface (DSI) connectivity. As mobile handsets are integrating higher resolutions, wider color depth, and larger sized displays, panels with high-speed serial interface protocols are becoming a more suitable solution.

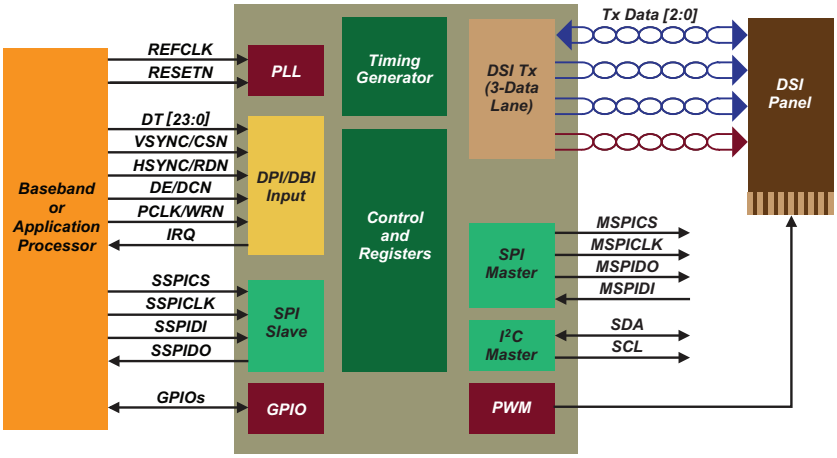
The TC358763XBG bridge supports legacy display interface protocols such as MIPI Display Pixel Interface (DPI) and MIPI Display Bus Interface (DBI) as Host interfaces; and serializes the data to enable connectivity to panel with MIPI DSI protocol. The bridge supports MIPI DSI connectivity on the panel side with up to 500 Mbps per data lane times three data lanes.

The TC358763XBG is a 72-pin device in a small 4.5 mm x 4.5 mm body, 1.0 mm height package with 0.4 mm ball pitch suitable for mobile applications.

Features

- LCD module interface
  - MIPI DSI-TX Data 3-lane, CLK 1-lane with data rates up to 500 Mbps/lane
  - Support for XGA size LCD panel when MIPI DPI is selected as Host interface
  - Output format: RGB888, RGB666 and RGB565
- Host interface
  - MIPI DPI 24-bit bus interface
  - MIPI DBI Type-B 16-bit bus interface
    - 18-bit bus RGB 666 format supported. When this format is selected, the valid command and data bus width is 16-bit

System Block Diagram of TC358763XBG



The TC358763XBG supports data transfer from input port (Host interface) to output port (Display Interface) as shown in the following use case scenarios:

Use Case 1: MIPI DPI to MIPI DSI
Use Case 2: MIPI DBI to MIPI DSI

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- Serial input interface
  - 3 or 4-wire 8-bit SPI synchronous transfer
  - 3-wire 9-bit SSI synchronous transfer
- Peripheral control ports
  - SPI or SSI serial I/F ports
  - Single I²C serial I/F port
  - Up to 13 General Purpose I/O ports
  - One PWM signal for LED intensity control
- PLL: external reference clock needed to generate internal clock
- Power supply
  - Core : 1.2V ±0.1V
  - DSI I/O : 1.2 ±0.1V
  - I/O : 1.8 ±0.1V to 3.0 ±0.3V
- Package
  - P-VFBGA 72-pin 4.5mm x 4.5mm, 1.0mm height, 0.4mm ball pitch

Toshiba Mobile Initiative

This chipset is a member of the Toshiba mobile initiative product family. The Toshiba Mobile Strategic Initiative is a comprehensive program designed to offer its U.S.-based mobile handset/mobile consumer device customers a product portfolio that aims to provide faster timeto-market and helps them stay competitive.

As part of this initiative, Toshiba provides local application and design-in support and access to a host of analog peripheral ICs, including the Toshiba CMOS image sensor family, display controllers/drivers, I/O expander, bridge ICs, memory products and LCD modules.

The expanded portfolio also includes support tools, reference designs and evaluation boards.

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