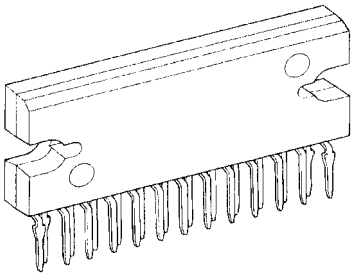
TOSHIBA Bi−CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB6500AH

2 PHASE BIPOLAR STEPPER + FULL BRIDGE DRIVER

The TB6500AH is Stepping Motor Driver IC incorporates Dual Bipolar Stepping Motor Drivers.
DC Motor Driver and Serial to Parallel signal conversion circuit (12bit Serial to Parallel shift Resistor with Latch) which control the 3 output drivers states by means of input serial signal trains.



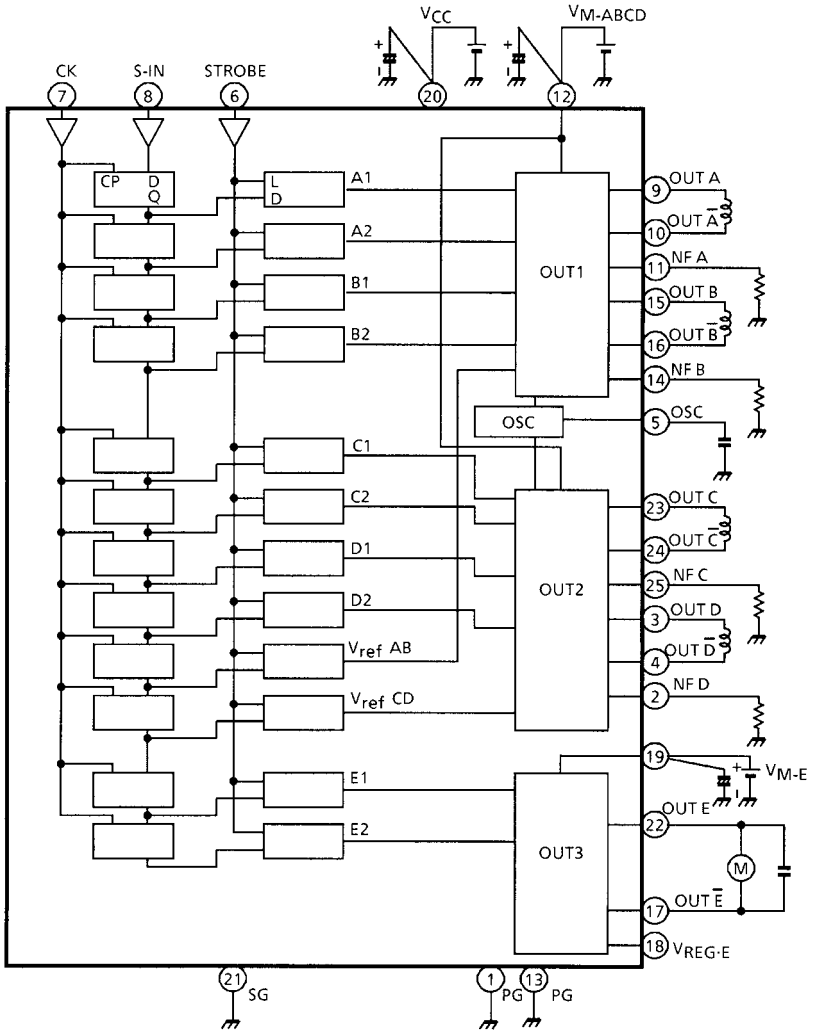
HZIP25-P-1.27

Weight: 9.86 g (Typ.)

FEATURES

- Package : HZIP25−P
- All CMOS compatible input
- 2 Bipolar Stepping Motors and 1 Full Bridge Motor are controlled by input serial signal trains.
- Output current up to 0.8 A (for Stepper) and 0.6 A (for DC Motor)
- PWM chopper type Stepping Motor Drivers.
- Wide range of operating supply voltage : V_M = 0~27 V
  : V_{CC} = 4.5~5.5 V
- Built−in thermal shut down, power supply monitor circuit.

BLOCK DIAGRAM



Capacitance connect to each power supply terminal is required to change to optimum value for noise elimination and also required to connect directly to each power supply terminal (V_{CC}, V_M) and the corresponding GND terminal (see Table 1) for stable operations.

Table 1

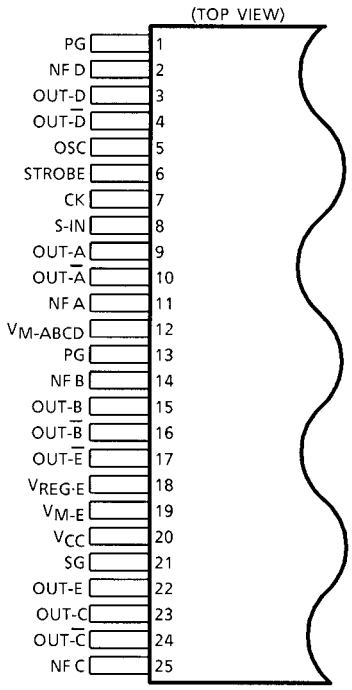
GND	POWER SUPPLY
Pin (21)	Pin (20) (V_{CC})
Pin (13)	Pin (12) (V_{M-ABCD})
Pin (1)	Pin (19) (V_{M-E})

Heat Fin is connect to GND terminal with Low Impedance.

PIN FUNCTION

PIN No.	SYMBOL	FUNCTIONAL DESCRIPTION
1	PG	Power GND terminal
2	NF D	D channel current detective terminal
3	OUT−D	Output D channel
4	OUT− $\overline{D}$	Output $\overline{D}$ channel
5	OSC	Internal oscillation frequency setting terminal
6	STROBE	STROBE signal input terminal
7	CK	CLOCK signal input terminal
8	S−IN	Serial signal input terminal
9	OUT−A	Output A channel
10	OUT− $\overline{A}$	Output $\overline{A}$ channel
11	NF A	A channel current detective terminal
12	V_{M-ABCD}	Power voltage supply terminal for motor driver
13	PG	Power GND terminal
14	NF B	B channel current detective terminal
15	OUT−B	Output B terminal
16	OUT− $\overline{B}$	Output $\overline{B}$ terminal
17	OUT− $\overline{E}$	Output $\overline{E}$ terminal
18	$V_{REG\cdot E}$	External reference voltage input terminal
19	V_{M-E}	Power voltage supply terminal for motor driver
20	V_{CC}	Power voltage supply terminal for control
21	SG	Signal GND terminal
22	OUT−E	Output E terminal
23	OUT−C	Output C terminal
24	OUT− $\overline{C}$	Output $\overline{C}$ terminal
25	NF C	C channel current detective terminal

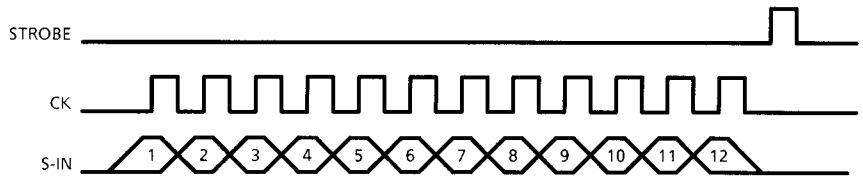
PIN CONNECTION



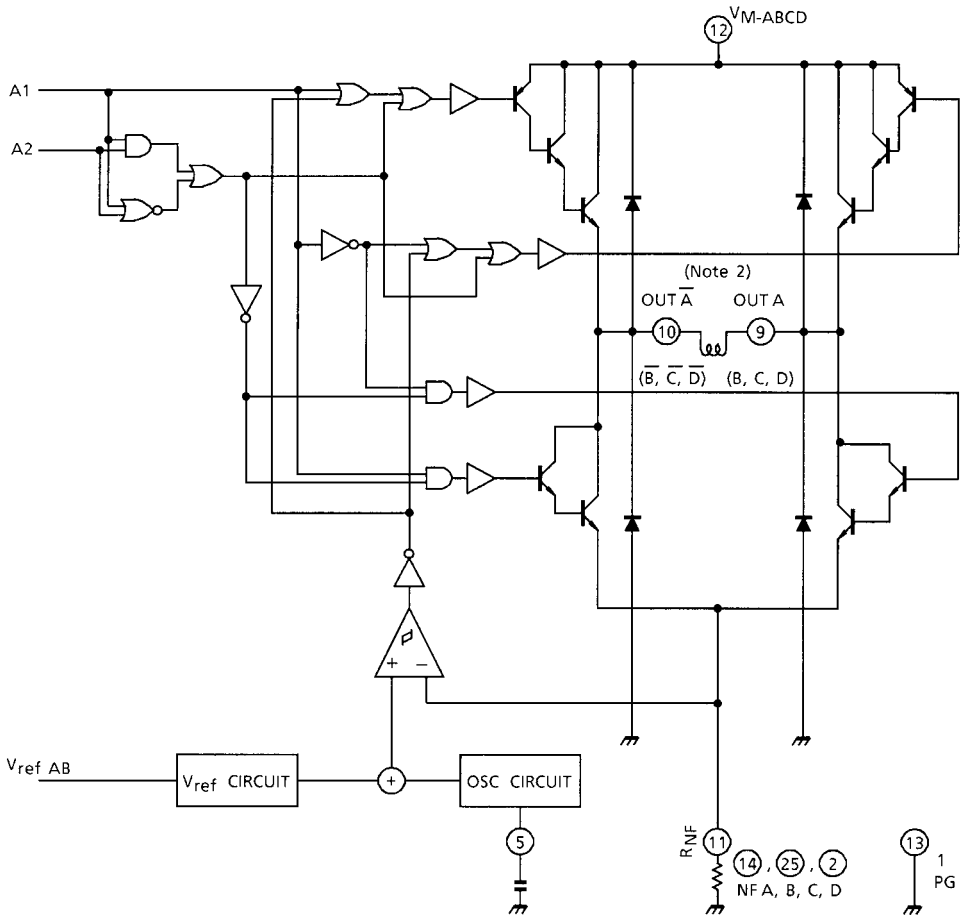
INPUT SERIAL PULSE TRAIN AND POWER OUTPUT STATES

<table>
<tr><th colspan="2">SERIAL INPUT
SIGNAL TRAIN</th><th>CONTROL</th><th>OPERATION</th></tr>
<tr><td>1</td><td>E2</td><td rowspan="2">DC motor control</td><td rowspan="2">
<table>
<tr><th colspan="2">INPUT</th><th colspan="2">OUTPUT</th><th rowspan="2">MODE</th></tr>
<tr><th>E1</th><th>E2</th><th>E</th><th>$\overline{E}$</th></tr>
<tr><td>L</td><td>L</td><td>∞</td><td>∞</td><td>STOP</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>L</td><td>CW / CCW</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>H</td><td>CCW / CW</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>L</td><td>BREAK</td></tr>
</table>
</td></tr>
<tr><td>2</td><td>E1</td></tr>
<tr><td>3</td><td>$V_{ref\cdot CD}$</td><td>Stepping motor 2 chapping rate control (V_{ref} CD)</td><td rowspan="2">V_{ref} = 0.85 V (Typ.) (at “H” mode)
V_{ref} = 0.65 V (Typ.) (at “L” mode)</td></tr>
<tr><td>4</td><td>$V_{ref\cdot AB}$</td><td>Stepping motor 1 chapping rate control (V_{ref} AB)</td></tr>
<tr><td>5</td><td>D2</td><td rowspan="4">Stepping motor 2 control
(Out C, D)</td><td rowspan="5">
<table>
<tr><th colspan="2">INPUT</th><th colspan="2">OUTPUT</th><th rowspan="2">MODE</th></tr>
<tr><th>A1</th><th>A2</th><th>A</th><th>$\overline{A}$</th></tr>
<tr><td>L</td><td>L</td><td>∞</td><td>∞</td><td>STOP</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>L</td><td>CW / CCW</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>H</td><td>CCW / CW</td></tr>
<tr><td>H</td><td>H</td><td>∞</td><td>∞</td><td>STOP</td></tr>
</table>
B1, B2 → B, $\overline{B}$
C1, C2 → C, $\overline{C}$
D1, D2 → D, $\overline{D}$
are all the same.
</td></tr>
<tr><td>6</td><td>D1</td></tr>
<tr><td>7</td><td>C2</td></tr>
<tr><td>8</td><td>C1</td></tr>
<tr><td>9</td><td>B2</td><td rowspan="4">Stepping motor 1 control
(Out A, B)</td></tr>
<tr><td>10</td><td>B1</td></tr>
<tr><td>11</td><td>A2</td></tr>
<tr><td>12</td><td>A1</td></tr>
</table>

INPUT SERIAL PULSE TRAIN TIMING CHART



OUTPUT STAGE 1, 2 1 / 2 CIRCUIT



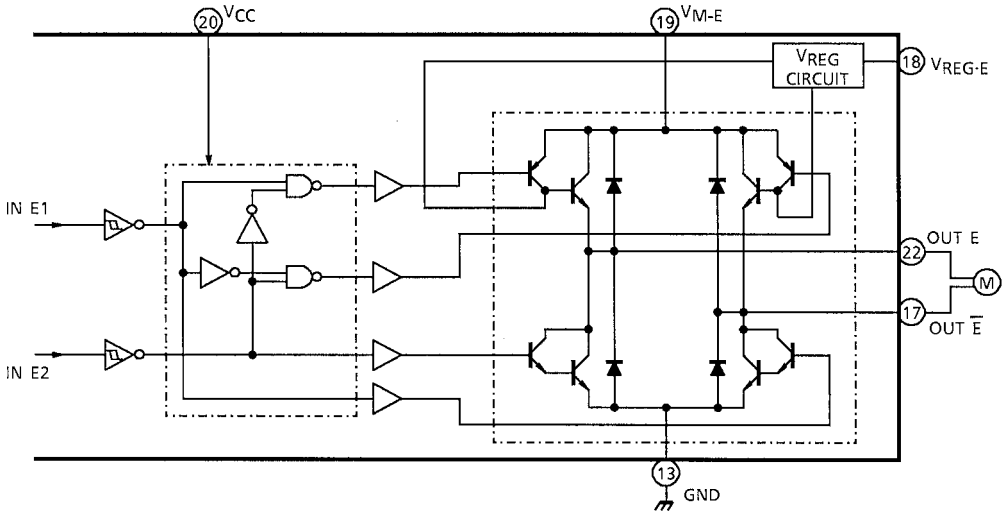
FUNCTION (Comp.+ > Comp. −) Note 1

A1	A2	OUT A	OUT $\overline{A}$	MODE
L	L	∞	∞	STOP
H	L	H	L	CW / CCW
L	H	L	H	CCW / CW
H	H	∞	∞	STOP

Note 1: In case of Comp.+ < Comp. −, Upper side power transistor turned off.

Note 2: Free wheeling diode connects between output A terminal and GND is required for stable operating. And also recommend to connect free wheeling diodes other output terminals for reliable operations.

OUTPUT STAGE 3

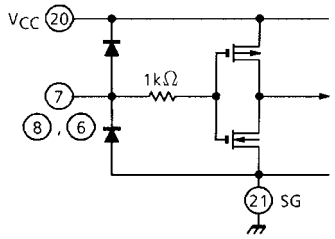


FUNCTION

INPUT		OUTPUT		MODE
IN E1	IN E2	OUT E	OUT Ē	
L	L	∞	∞	STOP
H	L	H	L	CW / CCW
L	H	L	H	CCW / CW
H	H	L	L	BREAK

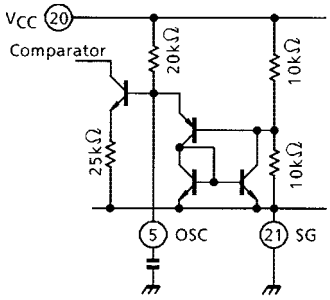
∞ : High Impedance
Note: Inputs are all high active type

INPUT STAGE (CK, S−IN, STROBE terminal)



$$f_{OSC} = \frac{1}{21.4 \cdot C_{OSC}} \text{ (kHz)} \quad (C_{OSC}\ \mu F)$$

OSC STAGE (OSC terminal)



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage (Motor)	V_M	30	V
Supply Voltage (Control)	V_{CC}	7.0	V
Input Voltage	V_{IN}	7.0	V
Output Current	$I_{O\ ABCD}$	±0.8	A
	$I_{O\ E}$	±0.6	
Power Dissipation	P_D	43 (Note)	W
		5	
Operating Temperature	T_{opr}	−40~85	°C
Storage Temperature	T_{stg}	−55~150	°C

Note: Tc = 85°C

RECOMMENDED OPERATING CONDITION (Ta = −20~75°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage (Control)		V_{CC}		4.5	5.0	5.5	V
Supply Voltage (Motor)		V_M		21.6	24	26.4	V
Input Voltage		V_{IN}		0	—	V_{CC}	V
Output Current	$I_{OUT\ ABCD}$	I_{OUT}		—	—	0.7	A
	$I_{OUT\ E}$			—	—	0.6	
Clock Frequency		f_{CK}		—	—	1.0	MHz
		f_{STROBE}		—	—	1.0	
Clock Pulse Width		tw_{CK}		500	—	—	ns
		tw_{STROBE}		500	—	—	
Data Set Up Time		$tsu_{CK-S\cdot IN}$		250	—	—	ns
		tsu_{ST-CK}		250	—	—	
Data Hold Time		$th_{CK-S\cdot IN}$		250	—	—	
		th_{ST-CK}		250	—	—	
PWM Oscillation Frequency		f_{PWM}		20	—	100	kHz

ELECTRICAL CHARACTERISTICS

Output stage (Ta = 25°C, V_{CC} = 5 V, V_M = 24 V)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN	TYP.	MAX	UNIT
Operation Power Supply Voltage		V_M (opr.)				0	—	27	V
Saturation Voltage	AB CD	V_{SATU-1}	1	I_{OUT} = 0.7 A	Output−V_M	—	2.2	2.7	V
				I_{OUT} = 0.5 A		—	2.0	2.5	
	AB CD	V_{SATL-1}		I_{OUT} = 0.7 A	Output−N_F	—	1.5	2.0	
				I_{OUT} = 0.5 A		—	1.3	1.8	
	E	V_{SATU-2}		I_{OUT} = 0.5 A	Output−V_M	—	2.2	2.7	
				I_{OUT} = 0.3 A		—	2.0	2.5	
	E	V_{SATL-2}		I_{OUT} = 0.5 A	Output−OG	—	1.5	2.0	
				I_{OUT} = 0.3 A		—	1.2	1.7	
E−ch Output Voltage		V_{OE}	1	I_{OUT} = 0.5 A	$V_{REG\cdot E}$ = 15 V	—	15	—	V
				I_{OUT} = 0.3 A		—	15	—	
Reference Current		I_{REG}	1	$V_{REG\cdot E}$ = 15 V		—	50	100	μA
Reference Voltage		$V_{REG\cdot E}$ (opr.)	1			0	—	22	V
Output Leak Current		I_{OL-H}	2	V_{CE} = 30 V		—	—	50	μA
		I_{OL-L}				—	—	50	
Clamp Diode Forward Voltage	AB CD	V_{F-U1}	3	I_F = 0.7 A, Output A−D		—	1.6	2.0	V
		V_{F-L1}				—	1.2	1.6	
	E	V_{F-U2}		I_F = 0.5 A, Output E		—	1.5	1.9	
		V_{F-L2}				—	1.3	1.7	

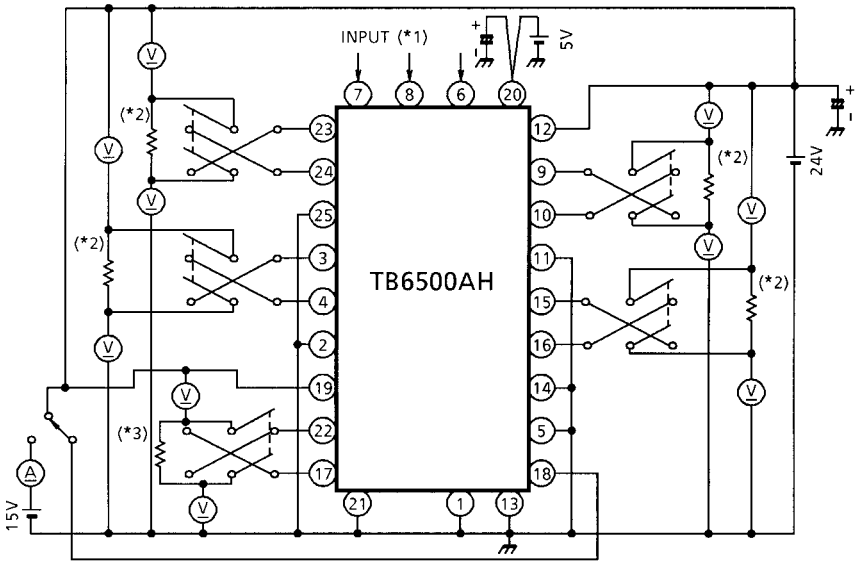
Small signal stage (Ta = 25°C, V_{CC} = 5 V, V_M = 24 V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Operation Supply Voltage	V_{CC} (opr.)	4		4.5	—	5.5	V
Quiescent Current	I_{CC1}		CK, ST, S−IN : Open	—	30	50	mA
	I_{CC2}		CK : 1 MHz, DATA : 1 / 2 f_{CLK} Output ON	—	30	50	
	I_{CC3}		CK : 1 MHz, DATA : 1 / 2 f_{CLK} Output OFF	—	30	50	
	I_{M-ABCD}		Output open, Input serial signal Output ON (A1, B1, C1, D1 = "H" A2, B2, C2, D2 = "H")	—	30	40	
			Output open Output OFF	—	—	50	μA
	I_{M-E}		CW, CCW, BREAK Output ON, Output open	—	5	12	mA
			Output open Output OFF	—	—	50	μA
Input Voltage	$V_{IN\ (H)}$	5	CK, S−IN, ST	3.5	—	V_{CC} +0.4	V
	$V_{IN\ (L)}$			GND −0.4	—	1.5	
Input Current	$I_{IN\ (H)}$	5	V_{INH} = 5.4 V	−3	—	3	μA
	$I_{IN\ (L)}$		V_{INL} = 0.4 V	−3	—	3	
Chopping Voltage Level	$V_{ref\ (H)}$	6	T_j = −40~125°C, C_{OSC} = 3300 pF, R_{NF} = 3.3 Ω, L = 19.5 mH; V_{ref} IN = H	0.75	0.85	0.95	V
	$V_{ref\ (L)}$		V_{ref} IN = L	0.55	0.65	0.75	
V_{ref} Level Differential Voltage	ΔVchop		V_{ref} (H)−V_{ref} (L)	—	0.2	—	V
Reset Voltage	V_{CCR}	7		3.6	3.8	4.1	V
Min. Reset Pulse	tV_{CCR}			—	—	1	μs
Min. PWM Frequency	f_{PWML}	4		—	—	10	kHz
Max. PWM Frequency	f_{PWMH}			200	—	—	
Thermal Shut Down	TSD (ON)	—	T_j	120	140	160	°C
Thermal Shut Down	TSD (OFF)			110	130	150	
Differential Temperature	ΔTSD		TSD (ON)−TSD (OFF)	—	10	—	

AC characteristics (Ta = 25°C, VCC = 5 V)

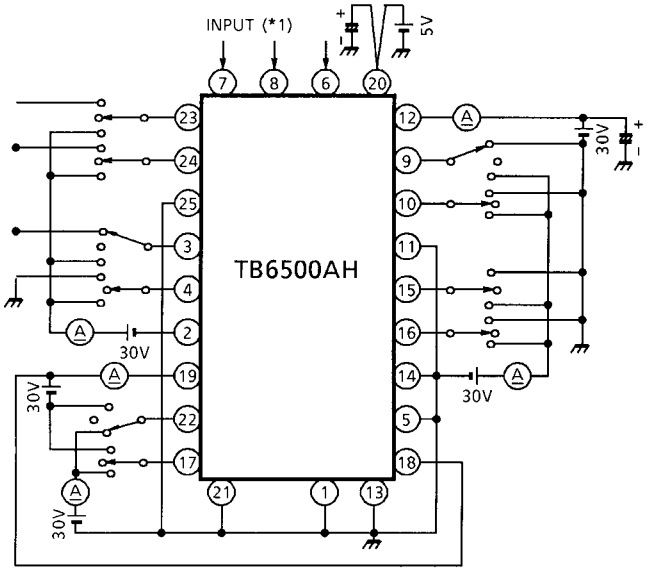
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN	TYP.	MAX	UNIT
CLOCK Frequency	f_{CK}	7			—	—	1.5	MHz
	f_{STROBE}				—	—	1.5	
Min. Clock Pulse Width	t_{CK}	7			340	—	—	ns
	t_{STROBE}				340	—	—	
Data Set Up Time	$t_{suCK-SIN}$	7			170	—	—	ns
	$t_{suST-CK}$				170	—	—	
Data Hold Up Time	$t_{hCK-SIN}$				170	—	—	
	t_{hST-CK}				170	—	—	
Output Propagation Time	t_{pLH}	7	CK-OUT	R_L = 40 Ω C_L = 15 pF	—	2	—	μs
	t_{pHL}				—	2	—	
	t_{pLH}		STROBE-OUT		—	2	—	
	t_{pHL}				—	2	—	
	t_{pON-Z}		V_{CC}·R-OUT		—	2	—	
	t_{pZ-ON}				—	2	—	
Max. Clock Rise Time	t_{rMAX}	7			—	—	1	μs
Max. Clock Fall Time	t_{fMAX}				—	—	1	
Output Rise Time	t_r		R_L = 40 Ω C_L = 15 pF		—	1	—	
Output Fall Time	t_f				—	1	—	
E-ch Output Dead Time	t·dead		R_L = 100 Ω C_L = 15 pF		—	250	—	

TEST CIRCUIT 1 $V_{SATU-1\cdot2}$, $V_{SATL-1\cdot2}$



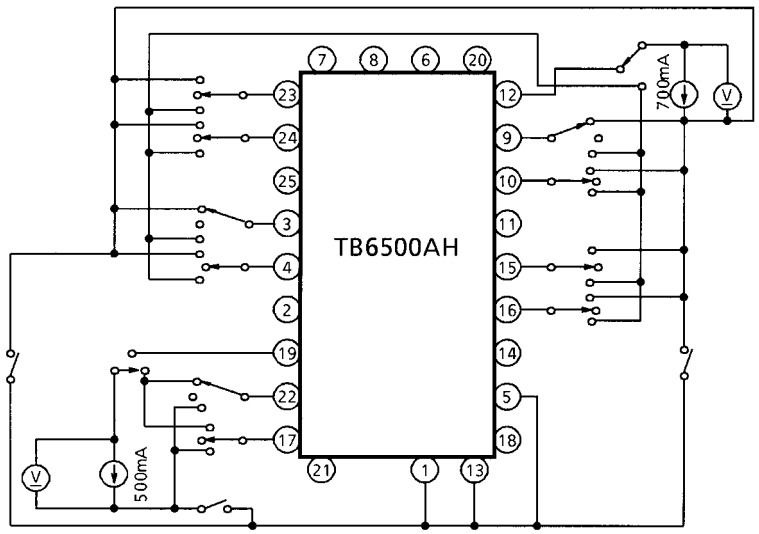
* 1: Set output transistor active with input mode select.
* 2: Calibrate output current becomes 0.5 A (or 0.7 A) with this resistor.
* 3: Calibrate output current becomes 0.3 A (or 0.5 A) with this resistor.

TEST CIRCUIT 2 I_{OL-H}, I_{OL-L}



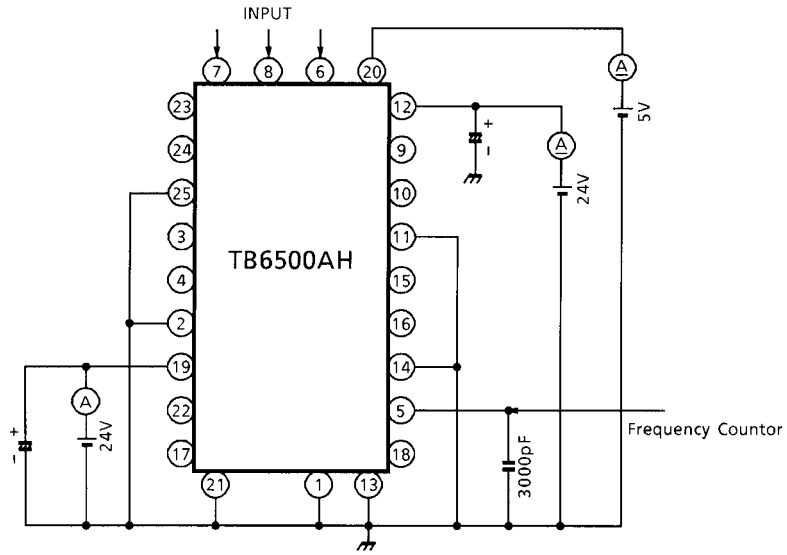
* 1: All “L” level S−IN signal, normal CK and STROBE signals are required to measure.

TEST CIRCUIT 3 $V_{F-U1\cdot2}$, $V_{F-L1\cdot2}$

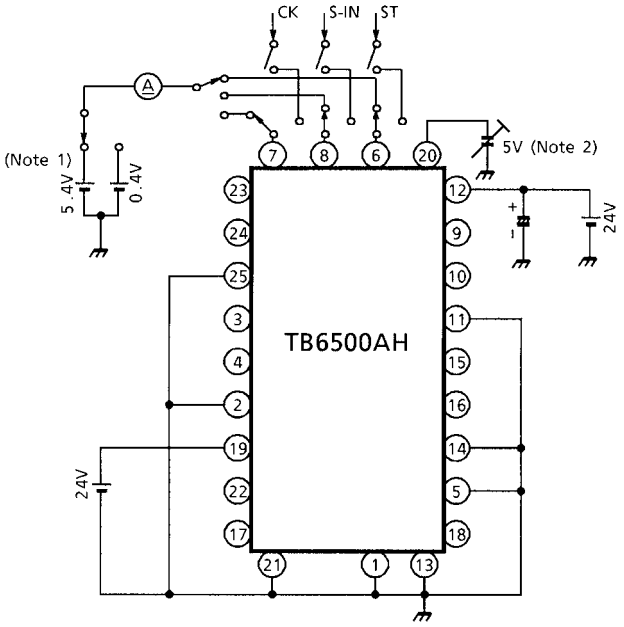


Note: Not to take a GND with any non−connecting pins.

TEST CIRCUIT 4 $I_{CC1\cdot2\cdot3}$, I_M : ABCD·E, $f_{PWML\cdot H}$



TEST CIRCUIT 5 I_{INH}, I_{INL}, V_{INH}, V_{INH}, V_{INL}, V_{CCR}



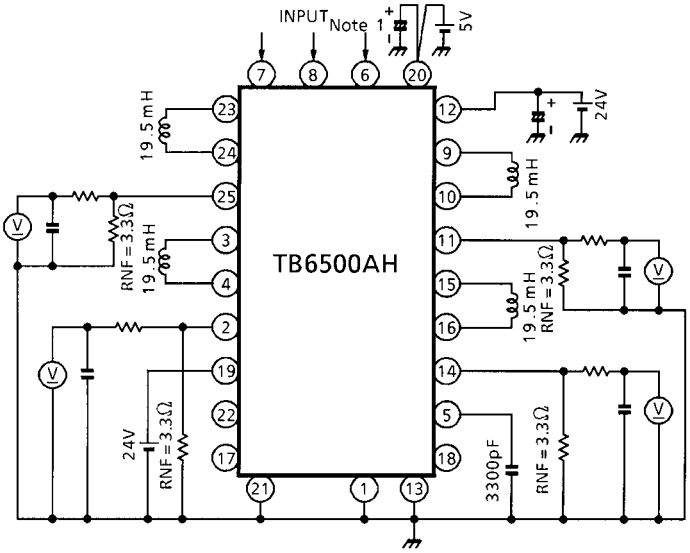
V_{IN} level

Note 1: Apply signals to CK, S−IN, and STROBE at the levels shown in the diagram and check function.

Power supply monitor level

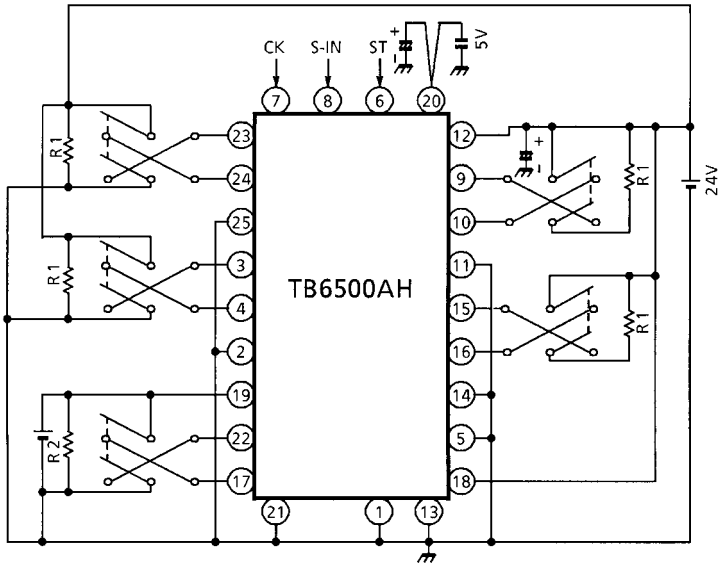
Note 2: Change the power supply voltage and check the output operation.

TEST CIRCUIT 6 V_{refH}, V_{refL}, ΔV_{ref}



Note 1: Hold the state (2 phase excitation mode) and measure.

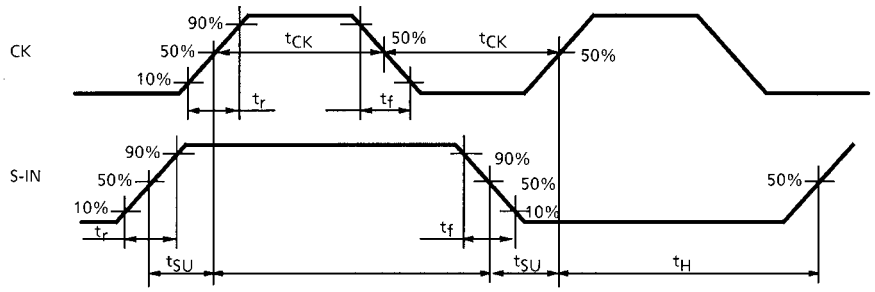
TEST CIRCUIT 7 (Calibrate I_O to 0.6 A by R1, 0.5 A by R2)



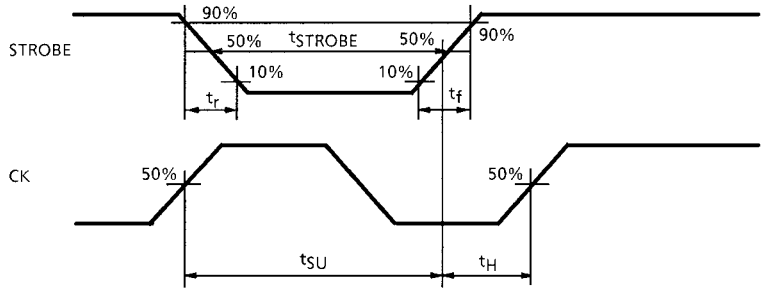
- 7−1. Set the STROBE terminal to high level and compare the output with the data in the waveform shown in Fig.7−1.
- 7−2. Check that the output is latched in the waveform as shown in Fig.7−2.
- 7−3. Check the CK or STROBE, and the output delay time in the waveform as shown in Fig.7−3.
- 7−4. Change the V_{CC} voltage, and check the delay with the output in the waveform as show in Fig.7−4.

AC ELECTRICAL CHARACTERISTICS

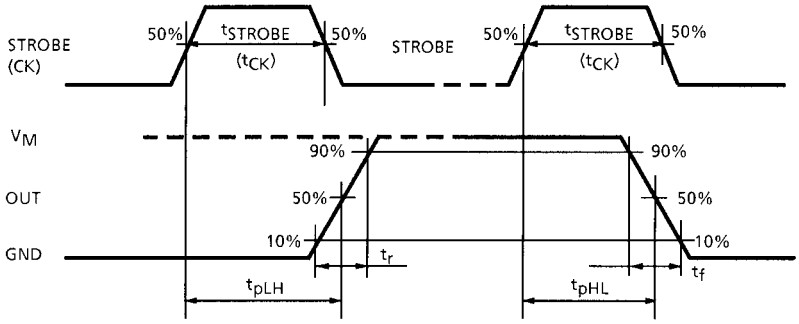
7−1 : CK−S−IN



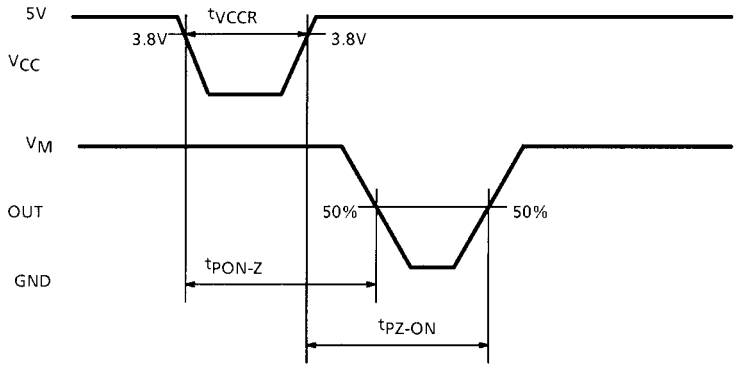
7−2 : STROBE−CK



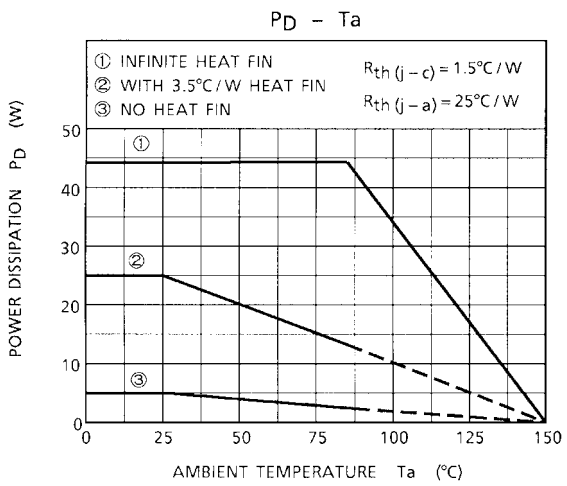
7−3 : STROBE (CK)−OUT

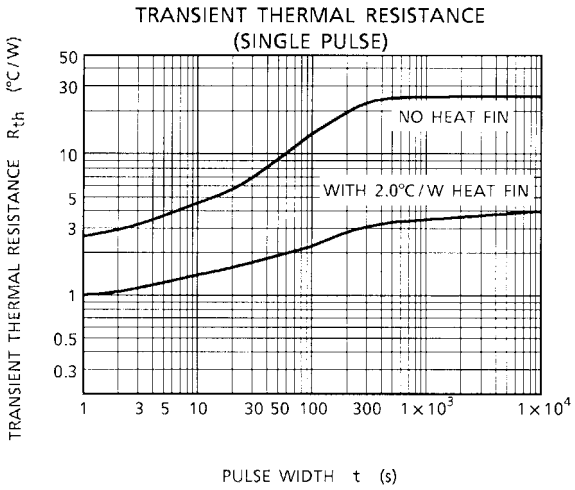


7−4 : V_{CCR}−OUT

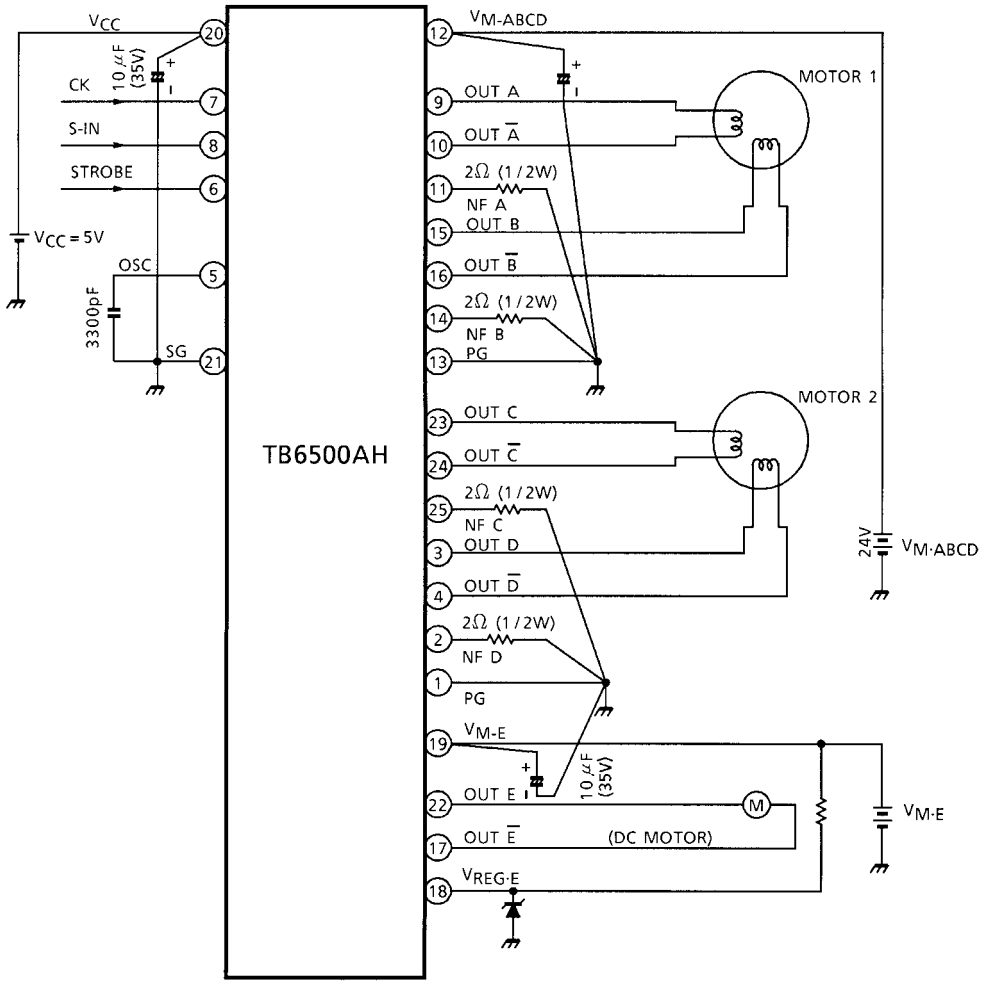


When measuring the upper transistor, set the external load resistor between the output and GND, then measure at the output terminal.
When measuring the lower transistor, set the external load resistor between the output and V_M then measure at the output terminal.





APPLICATION CIRCUIT

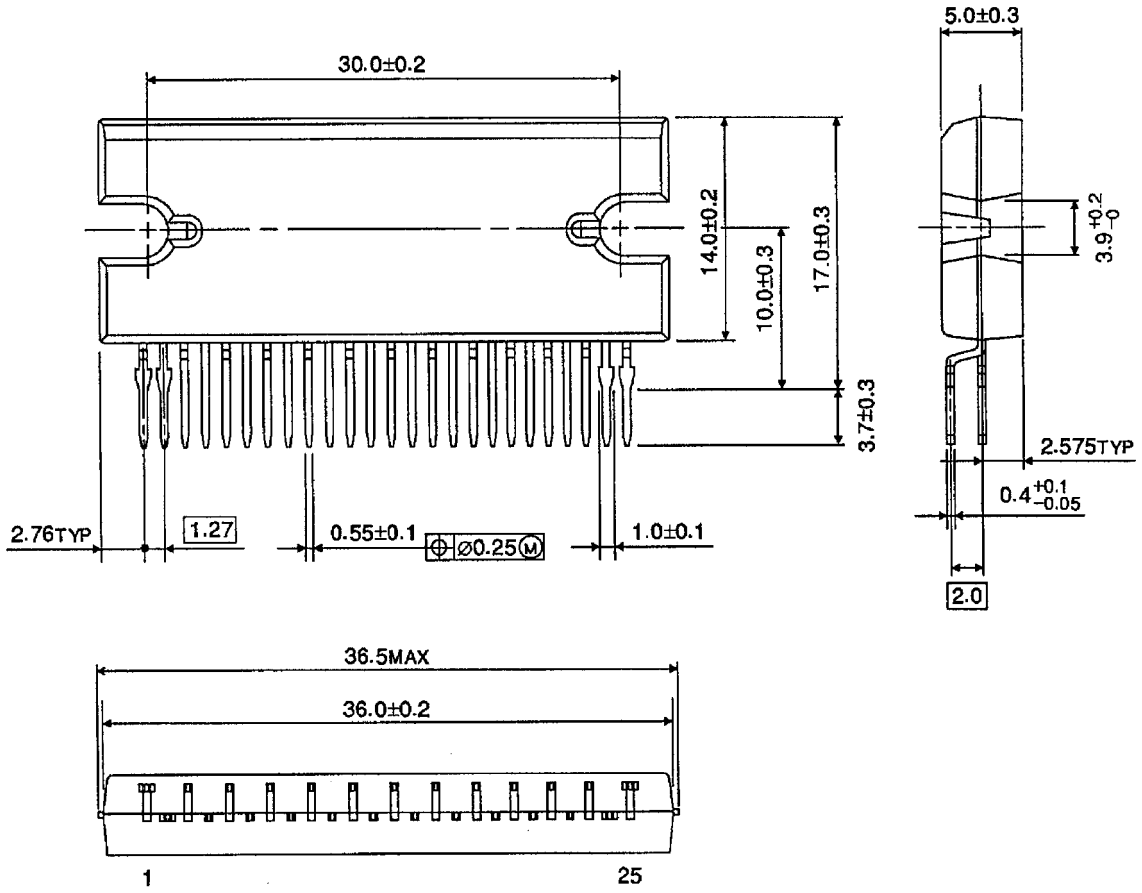


Note 1: Care should be taken not to have a common impedance with output current pass of each motor (NF A, NF B for MOTOR 1, NF C, MOTOR 2 and PG for DC MOTOR) and any other signal lines. And recommended to take one point GND with each output current pass and corresponding PG terminal. (see table 1 of BLOCK Diagram)

Note 2: Utmost care is necessary in the design of the output line, V_M and GND line since IC may be destroyed due to short−circuit between outputs, air contamination fault, or fault by improper grounding.

PACKAGE DIMENSIONS

HZIP25−P−1.27 Unit: mm



Weight: 9.86 g (Typ.)

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000707EBA

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