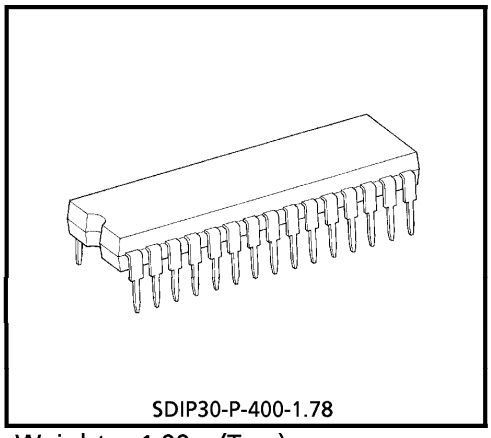
TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB1031N

INTERFACE DRIVER IC FOR WASHING MACHINE

As an interface between the microcontroller and peripheral devices, TB1031N is an ideal driver IC. Because it contains various drivers on one chip, TB1031N effectively reduces the number of parts.
The device features built-in registers that can simplify software design when used in combination with an eight-bit microcontroller.



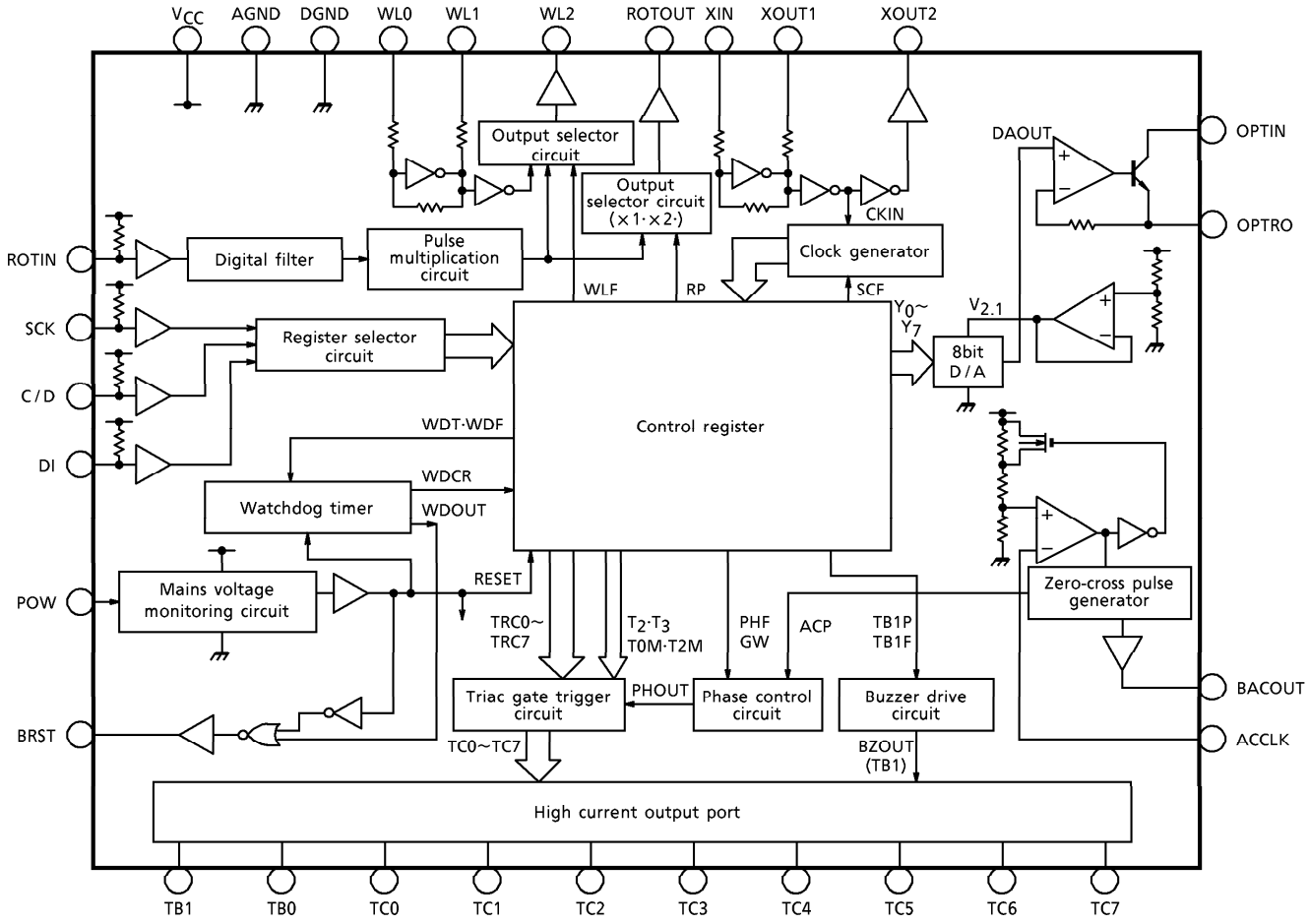
SDIP30-P-400-1.78

Weight : 1.99g (Typ.)

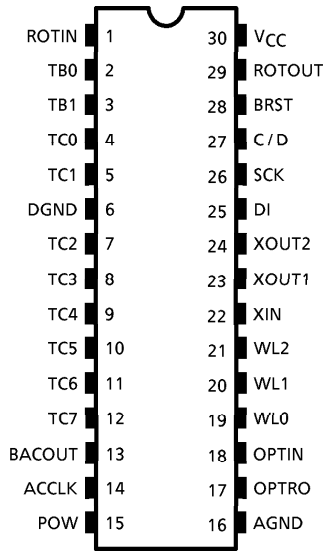
FEATURES

- Built-in zero-cross detector circuit
- High-current output ports (two 70mA, two 60mA, two 50mA ports ; four 30mA ports)
- Direct drive for triac buzzer
- Built-in buzzer drive circuit (2.7kHz)
- Built-in pulse multiplication (×2) function
- 8bit serial interface
- Built-in watchdog timer (30ms, 15ms settings)
- Built-in mains voltage monitoring circuit
- Built-in LC oscillator circuit
- Built-in 8bit D / A converter for constant-current control

BLOCK DIAGRAM



PIN CONNECTION



PIN FUNCTIONS

PIN No.	PIN NAME	DESCRIPTION
1	ROTIN	Pulse multiplication circuit input pin
2	T_{B0}	High-current output port 1 (open collector) 60mA output
3	T_{B1}	High-current output port 2 (open collector) 60mA output
4	TC0	High-current output port 3 (open collector) 70mA output
5	TC1	High-current output port 4 (open collector) 70mA output
6	DGND	Digital GND
7	TC2	High-current output port 5 (open collector) 50mA output
8	TC3	High-current output port 6 (open collector) 50mA output
9	TC4	High-current output port 7 (open collector) 30mA output
10	TC5	High-current output port 8 (open collector) 30mA output
11	TC6	High-current output port 9 (open collector) 30mA output
12	TC7	High-current output port 10 (open collector) 30mA output
13	BACOUT	Mains power zero-cross detection output pin
14	ACCLK	Mains power zero-cross detection input pin
15	POW	Mains voltage monitoring input pin
16	AGND	Analog GND
17	OPTRO	Constant-current control circuit output pin
18	OPTIN	Constant-current control circuit input pin
19	WL0	LC oscillator circuit input pin
20	WL1	LC oscillator circuit output pin 1
21	WL2	LC oscillator circuit output pin 2
22	XIN	Oscillator input pin
23	XOUT1	Oscillator output pin 1
24	XOUT2	Oscillator output pin 2
25	DI	Serial data input pin
26	SCK	Serial clock input pin
27	C / D	Command / data switching signal input pin
28	BRST	Reset signal output pin (low reset)
29	ROTOUT	Pulse multiplication circuit output pin
30	V_{CC}	System power supply

MAXIMUM RATINGS (Ta = 25 ± 1.5°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	− 0.3~7.0	V
Input Voltage	V_{IN}	− 0.3~V_{CC} + 0.3	V
POW Pin Input Voltage	VINPOW	− 0.3~16	V
TB0 And TB1 Pin Input Voltage	VINTB	− 0.3~12	V
Power Dissipation	P_D (Note 1)	1.5	W
Operating Temperature	T_{opr}	− 20~75	°C
Storage Temperature	T_{stg}	− 55~125	°C
Electrostatic Destruction	ESD (Note 2)	± 250	V
Latch Up Current	IL	± 10	mA

(Note 1) The power dissipation decreases about 12mW for every degree of temperature increase.
(Note 2) C = 200pF and R = 0Ω, one discharge for each polarity.

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{CC} = 5.0V, Ta = 25 ± 1.5°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage	V_{CC}	—	—	4.0	5.0	6.0	V
Operating Current Dissipation	I_{CC}	—	8.0MHz oscillation with no load	—	—	20	mA
Operating Frequency Band	FOPRAN	—	—	4	—	8	MHz
Pin 1 (ROTIN)							
Open Pin Voltage (Design Target)	VOPRTIN	—	When idle	4.95	5.0	5.05	V
Low-level Input Current	IILRRTIN	—	When idle and V_{in} = 0V	− 77	− 100	− 143	μA
High-level Input Voltage	VIHRTIN	—	—	0.8 V_{CC}	—	V_{CC}	V
Low-level Input Voltage	VILRTIN	—	—	0	—	0.2 V_{CC}	V
Pin 2 (TB0), Pin 3 (TB1)							
Off-leak Current	IOFFTB01	—	When idle and V_{in} = 5V	− 1	—	1	μA
Low-level Output Current	IOLTB01	—	V_{OL} = 1.0V	60	—	—	mA

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Pin 4 (TC0), Pin 5 (TC1)							
Off-leak Current	IOFFTC01	—	When idle and V_{in} = 5V	− 1	—	1	μA
Low-level Output Current	IOLTC01	—	V_{OL} = 1.0V	70	—	—	mA
Pin 7 (TC2), Pin 8 (TC3)							
Off-leak Current	IOFFTC23	—	When idle and V_{in} = 5V	− 1	—	1	μA
Low-level Output Current	IOLTC23	—	V_{OL} = 1.0V	50	—	—	mA
Pin 9 (TC4), Pin 10 (TC5), Pin 11 (TC6), Pin 12 (TC7)							
Off-leak Current	IOFFTC47	—	When idle and V_{in} = 5V	− 1	—	1	μA
Low-level Output Current	IOLTC47	—	V_{OL} = 1.0V	30	—	—	mA
Pin 13 (BACOUT)							
High-level Output Voltage	VOHACOUT	—	I_{OH} = − 1mA	4.5	—	5.0	V
Low-level Output Voltage	VOLACOUT	—	I_{OL} = 1mA	0	—	0.5	V
Pin 14 (ACCLK)							
Threshold Voltage	VTHACCLK	—	When input goes from high to low, voltage to change BACOUT from high to low	0.25	0.35	0.45	V
Hysteresis Width	VHYSACCK	—	When input goes from low to high, difference between VTHACCLK and voltage needed to change BACOUT pin from low to high	50	100	150	mV
Pin 15 (POW)							
High-level Threshold Voltage	VTHPOW	—	When input changes from high to low, voltage to change BRST pin from high to low	5.2	5.4	5.6	V
Hysteresis Width	VHYSPOW	—	When input goes from low to high, difference between VTHPOW and voltage needed to change BRST pin from low to high	1.35	1.45	1.55	V
Input Voltage Range	VINPOW	—	Voltage that can be applied to POW pin	0	—	16	V

Recommended oscillator : Murata 8MHz Ceralock ceramic oscillator (CST8.0MTW)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Pin 17 (OPTRO)							
Output Current 1	IOP1	—	V_{CC} = 5V, When 30Ω external resistor connected, 3.0V applied to OPTIN pin, and DAC = FF	67	70	73	mA
Output Current 2 (Design Target)	IOP2	—	V_{CC} = 5V, When 30Ω external resistor connected, 3.0V applied to OPTIN pin, and DAC = 01	0	0.55	1.24	mA
Output Current 3	IOP3	—	V_{CC} = 5V, When 30Ω external resistor connected, 3.0V applied to OPTIN pin, and DAC = 80	33.1	35.3	37.6	mA
Output Current 4	IOP4	—	V_{CC} = 5V, When 30Ω external resistor connected, 3.0V applied to OPTIN pin, and DAC = 02	0.12	0.82	1.53	mA
Output Current 5	IOP5	—	V_{CC} = 5V, When 30Ω external resistor connected, 3.0V applied to OPTIN pin, and DAC = 04	0.64	1.37	2.10	mA
Output Current 6	IOP6	—	V_{CC} = 5V, When 30Ω external resistor connected, 3.0V applied to OPTIN pin, and DAC = 08	1.69	2.46	3.24	mA
Output Current 7	IOP7	—	V_{CC} = 5V, When 30Ω external resistor connected, 3.0V applied to OPTIN pin, and DAC = 10	3.78	4.65	5.53	mA
Output Current 8	IOP8	—	V_{CC} = 5V, When 30Ω external resistor connected, 3.0V applied to OPTIN pin, and DAC = 20	7.97	9.02	10.1	mA
Output Current 9	IOP9	—	V_{CC} = 5V, When 30Ω external resistor connected, 3.0V applied to OPTIN pin, and DAC = 40	16.3	17.8	19.3	mA

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Current 10	IOP10	—	When V_{CC} = 4.5V, 30Ω external resistor connected, 2.5V applied to OPTIN pin, and DAC = FF	60	63	66	mA
Output Current 11	IOP11	—	V_{CC} = 5.5V, When 30Ω external resistor connected, 3.5V applied to OPTIN pin, and DAC = FF	74	77	80	mA
Pin 18 (OPTIN)							
Off-leak Current	IOFFOPIN	—	When DAC data are 00 and V_{in} = 4.5~5.5V	−1	—	1	μA
8bit D / A Converter (DAC) Characteristics							
DAC Reference Voltage 1 (Design Target)	VREF1	—	When V_{CC} = 5.0V	2.03	2.10	2.18	V
DAC Reference Voltage 2 (Design Target)	VREF2	—	When V_{CC} = 4.5V	1.83	1.89	1.96	V
DAC Output Voltage 1	VOPTRO1	—	V_{CC} = 5.0V When DAC data FF and 30Ω external resistor connected to OPTRO pin	2.01	2.10	2.20	V
DAC Output Voltage 2	VOPTRO2	—	When V_{CC} = 4.5V, DAC data FF, and 30Ω external resistor connected to OPTRO pin	1.81	1.89	1.98	V
Monotony	ΔIDAC1	—	IDAC (n + 1) − IDAC (n) n = 0~255	0.01	0.27	0.55	mA
DAC Linearity 1	DALINTY1	—	$\frac{(IOP1 - IOP9) / 191}{(IOP1 - IOP3) / 127}$	0.98	1.00	1.02	—
DAC Linearity 2	DALINTY2	—	$\frac{(IOP1 - IOP8) / 223}{(IOP1 - IOP3) / 127}$	0.98	1.00	1.02	—
Pin 19 (WL0)							
High-level Input Current	IIHRWL0	—	V_{in} = 5V, WL1 pin open	4.3	8.6	17.1	μA
Low-level Input Current	IILRWL0	—	V_{in} = 0V, WL1 pin open	−4.3	−8.6	−17.1	μA

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Pin 20 (WL1)							
High-level Output Current	IOHWL1	—	V_{in} = 0V, 0V applied to WL0 pin	− 0.9	—	—	mA
Low-level Output Current	IOLWL1	—	V_{in} = 5V, 5V applied to WL0 pin	0.9	—	—	mA
Pin 21 (WL2)							
High-level Output Voltage	VOHWL2	—	I_{OH} = − 1mA	4.5	—	V_{CC}	V
Low-level Output Voltage	VOLWL2	—	I_{OL} = 1mA	0	—	0.5	V
Pin 22 (XIN)							
High-level Input Voltage	IIHXIN	—	V_{in} = 5V	1.5	—	7.0	μA
Low-level Input Voltage	IILXIN	—	V_{in} = 0V	− 1.5	—	− 7.0	μA
Pin 23 (XOUT1)							
High-level Output Voltage	VOHXOUT1	—	I_{OH} = − 300μA	4.5	—	V_{CC}	V
Low-level Output Voltage	VOLXOUT1	—	I_{OL} = 300μA	0	—	0.5	V
Pin 24 (XOUT2)							
High-level Output Voltage	VOHXOUT2	—	I_{OH} = − 1mA	4.5	—	V_{CC}	V
Low-level Output Voltage	VOLXOUT2	—	I_{OL} = 1mA	0	—	0.5	V
Oscillator Characteristics							
Oscillation Start Voltage	VSTA	—	When using 4~8MHz oscillation	—	—	4.0	V
Oscillation Holding Voltage	VHOLD	—	When using 4~8MHz oscillation	—	—	4.0	V
Oscillation Start Time	TSTA	—	When using 4~8MHz oscillation	—	—	1.0	ms
Pin 25 (DI)							
Open Pin Voltage (Design Target)	VOPDI	—	When idle	4.995	5.000	5.005	V
Low-level Input Current	IILRDI	—	When idle and V_{in} = 0V	− 0.77	− 1.0	− 1.43	mA
High-level Input Voltage	VIHDI	—	—	0.8 V_{CC}	—	V_{CC}	V
Low-level Input Voltage	VILDI	—	—	0	—	0.2 V_{CC}	V

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Pin 26 (SCK)							
Open Pin Voltage (Design Target)	VOPSCK	—	When idle	4.995	5.000	5.005	V
Low-level Input Current	IILRSCK	—	When idle and V_{in} = 0V	− 0.77	− 1.0	− 1.43	mA
High-level Input Voltage	VIHSCK	—	—	0.8 V_{CC}	—	V_{CC}	V
Low-level Input Voltage	VILSCK	—	—	0	—	0.2 V_{CC}	V
Pin 27 (C / D)							
Open Pin Voltage (Design Target)	VOPCD	—	When idle	4.995	5.000	5.005	V
Low-level Input Current	IILRCD	—	When idle and V_{in} = 0V	− 0.77	− 1.0	− 1.43	mA
High-level Input Voltage	VIHCD	—	—	0.8 V_{CC}	—	V_{CC}	V
Low-level Input Voltage	VILCD	—	—	0	—	0.2 V_{CC}	V
Pin 28 (BRST)							
High-level Output voltage	VOHBRST	—	I_{OH} = − 1mA	4.5	—	V_{CC}	V
Low-level Output Voltage	VOLBRST	—	I_{OL} = 1mA	0	—	0.5	V
Pin 29 (ROTOUT)							
High-level Output Voltage	VOHRTOUT	—	I_{OH} = − 1mA	4.5	—	V_{CC}	V
Low-level Output Voltage	VOLRTOUT	—	I_{OL} = 1mA	0	—	0.5	V

DESCRIPTION OF OPERATION

(1) Control registers

To control the TB1031N operation, set the internal registers through serial communications with the microcontroller. The control registers are 8bit registers organized as in the following table.

1.1 Control registers

REGISTER NAME	SYMBOL
Command Register 0	C_0
Command Register 1	C_1
Triac Register	TRC0~7
Phase Data Register 1	PD00~07
Phase Data Register 2	PD10~17
D/A Data Register	$Y_{0\sim7}$

Command register (C_0, C_1) functions

REGISTER NAME	SYMBOL	FUNCTION
C_0	T_0	IC testing
	T_1	IC testing
	WDF	Watchdog timer operation enable/disable
	WDT	Watchdog timer time selection
	WLF	WL2 output selection
	RP	Pulse multiplication circuit (ROTOUT) output selection
	TB1P	TB1 port output mode selection
	SCF	System clock selection
C_1	T_2	TC0 and TC1 simultaneous ON enable/disable
	T_3	TC2 and TC3 simultaneous ON enable/disable
	PHF	Phase control enable/disable
	GW	TC0~TC3 triac gate pulse width selection
	T0M	TC0 and TC1 pulse mode selection
	T2M	TC2 and TC3 pulse mode selection
	TB1F	TB1 ON/OFF control
	TB0F	TB0 ON/OFF control

Control register 0 (C_0)

BIT STATE	MSB							LSB
	T_0	T_1	WDF	WDT	WLF	RP	TB1P	SCF
0	Normal mode		Disable	15ms	WL2	×1	2.7kHz	4MHz
1	Test mode		Enable	30ms	ROTOUT	×2	DC	8MHz
After reset	0	0	0	0	0	0	0	0

(Note) Set bits T_0 and T_1 to "0".

Control register 1 (C_1)

BIT STATE	MSB							LSB
	T_2	T_3	PHF	GW	T0M	T2M	TB1F	TB0F
0	Disable	Disable	Disable	1ms	DC	DC	OFF	OFF
1	Enable	Enable	Enable	2ms	4kHz	4kHz	ON	ON
After reset	0	0	0	0	0	0	0	0

1.2 Triac register (TRC0~7)

The triac register is organized as in the following table. This register is used to select a port (pins TC0~TC7) to drive.

Triac register (TRC)

BIT NAME	MSB							LSB
	TRC7	TRC6	TRC5	TRC4	TRC3	TRC2	TRC1	TRC0
Corresponding pin	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
1	ON	ON	ON	ON	ON	ON	ON	ON
After reset	0	0	0	0	0	0	0	0

1.3 Phase data registers 1 and 2 (P_{D00}~P_{D07}, P_{D10}~P_{D17})

The phase data registers are organized as in the following table. When performing phase control, the delay time data from the zero-cross point can be set.

Phase data register 1 (P_{D0})

BIT NAME	MSB							LSB
	PD07	PD06	PD05	PD04	PD03	PD02	PD01	PD00
After reset	0	0	0	0	0	0	0	0

Phase data register 1 (P_{D1})

BIT NAME	MSB							LSB
	PD17	PD16	PD15	PD14	PD13	PD12	PD11	PD10
After reset	0	0	0	0	0	0	0	0

1.4 D / A data register (Y_0~Y_7)

The D / A data register is organized as in the following table. The register can be used to set the built-in 8bit D / A converter data.

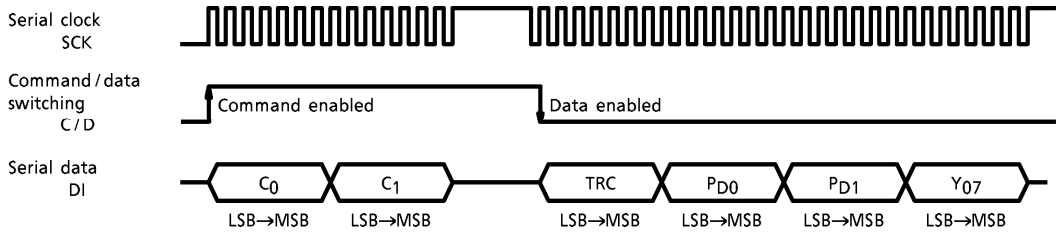
D / A data register (Y_{07})

BIT NAME	MSB							LSB
	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
After reset	0	0	0	0	0	0	0	0

(2) Communication with microcontroller

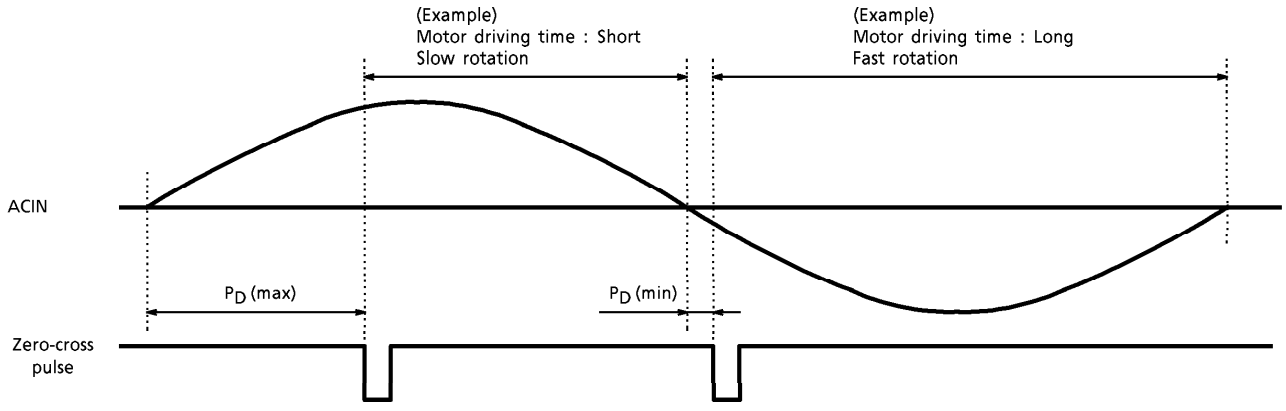
Communication with the microcontroller is based on serial communications controlled by the data received from the microcontroller. Transfer data consist of 2-byte commands (C_0, C_1) and 4-byte data (TRC, P_{D0}, P_{D1}, Y_{07}). Command transfer is enabled on the rising edge of the C / D pin. Data transfer is enabled on the falling edge of the C / D pin.

Transfer timing chart



(3) Phase data resolution

The delay time from the zero-cross point is set using the internal 32kHz-clock as a reference. The maximum delay is 8ms (at FFH) ; the minimum delay is 31.25μs (at 00H).



(4) Data register combination during phase control

Four pins are provided as phase-controllable port pins : TC0, TC1, TC2, TC3
The C_1 register contains two bits (T_2, T_3) to select a combinations of the four pins to be used simultaneously. During phase control, these bits can be set to change the combination of the phase data output to the port pins.

Phase data combinations using simultaneous ON control bits T_2 and T_3.

SIMULTANEOUS ON CONTROL BIT		HIGH-CURRENT OUTPUT PORT PIN			
T_2	T_3	TC0	TC1	TC2	TC3
0	0	PD0		PD1	
1	0	PD0	PD1	—	—
0	1	PD0		PD1	—
1	1	PD0	PD1	—	—

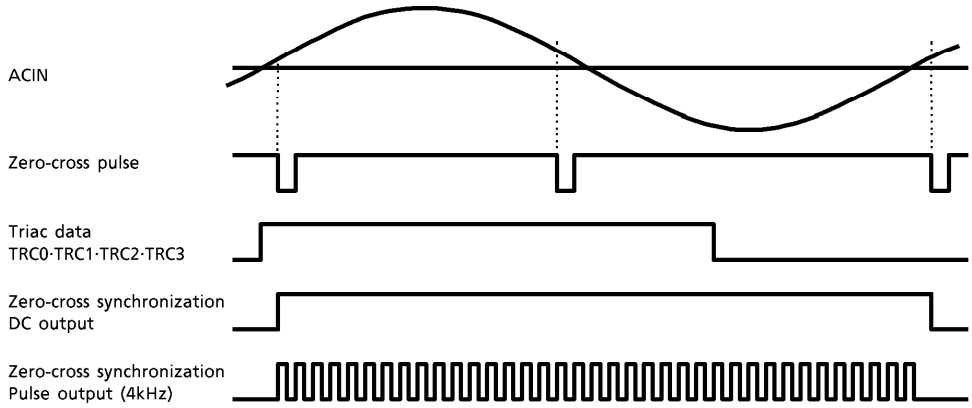
When performing phase control, set the PHF bit in the C_1 register to "1".

(5) TC0~TC3 pins zero-cross synchronization / pulse output

To avoid radio-frequency impulse noise and triac degradation, the TB1031N is designed so that the triac trigger can be turned ON at a timing synchronized to the zero-cross point. Also, to reduce power dissipation, the pulse signals can be used to trigger the triacs. The internal 4kHz-clock can also be used for pulse output.
Bits T0M and T2M of command register 1 (C_1) can select DC and pulse output.

BIT NAME	T0M	T2M
Corresponding pin	TC0·TC1	TC2·TC3
0	DC output	DC output
1	Pulse output (4kHz)	Pulse output (4kHz)

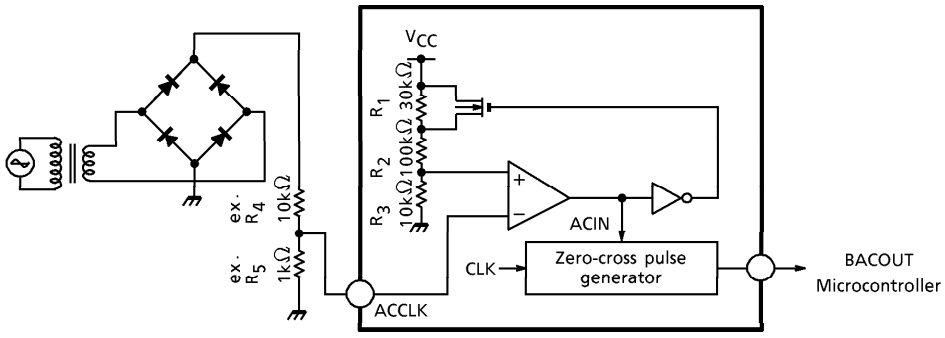
Timing chart



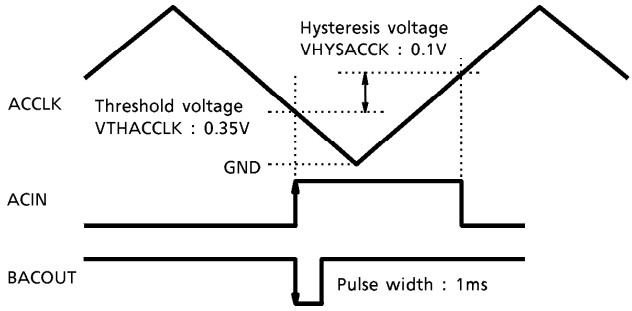
(6) Zero-cross detector circuit

The voltage divided from full-wave rectified AC power is input to ACCLK. The circuit detects the rising edge of the ACIN and can generate a 1ms-zero-cross pulse at BACOUT.

Block diagram



Timing chart



(7) Triac gate signal width selection (GW)

During phase control, the pulse width of the gate signal for the triac connected to pins TC0~TC3 can be selected from two pulse widths in accordance with the triac sensitivity. Register C_1 is used for the gate signal width selection.

BIT STATE	GW
0	1ms
1	2ms

(8) TB0 and TB1 pin control

The bits (TB1F and TB0F) to turn the output of pins TB0 and TB1 ON and OFF are assigned to register C_1. Pin TB1 also has a bit (TB1P) to select DC output or the pulse output (2.7kHz) for driving a buzzer, for example.

BIT STATE	TB1F	TB0F	TB1P
0	OFF	OFF	2.7kHz output
1	ON	ON	DC output

(9) System clock selection (SCF)

TB1031N includes an internal clock generator to generate several basic clocks and supply the clocks to the logic circuits. When the source clock is 8MHz, be sure to set the SCF bit of the C_0 register to "1". When the source clock is 4MHz, set SCF to "0".

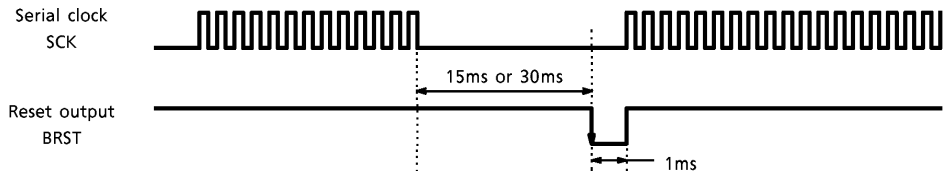
BIT STATE	SCF
0	Using 4MHz oscillator
1	Using 8MHz oscillator

(10) Watchdog timer

The watchdog timer is cleared each time one byte of serial data is sent from the microcontroller. If serial data are not sent for 15ms or 30ms, a 1ms-width reset signal can be output to the BRST pin to reset the microcontroller. The watchdog timer control bits (WDF and WDT) are assigned to register C_0.

BIT STATE	WDF	WDT
0	Disabled	Detection time 15ms
1	Enabled	Detection time 30ms

Timing chart

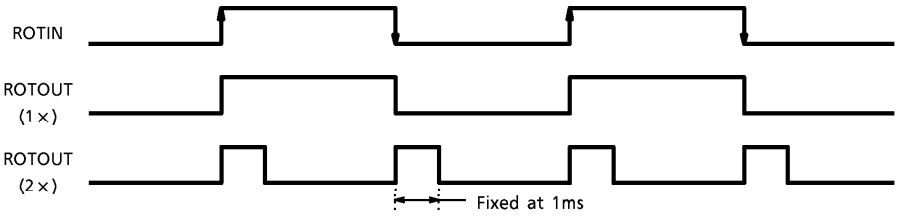


(11) Pulse multiplication circuit

This circuit can detect the rising or falling edge of the pulse input from the ROTIN pin, and output a 1× or 2× pulse to the ROTOUT pin. The ROTOUT output selection bit (RP) is assigned to register C_0. When 2×, the pulse width is fixed at 1ms.

BIT STATE	RP
0	ROTOUT : Outputs 1×ROTIN pulse
1	ROTOUT : Outputs 2×ROTIN pulse

Timing chart

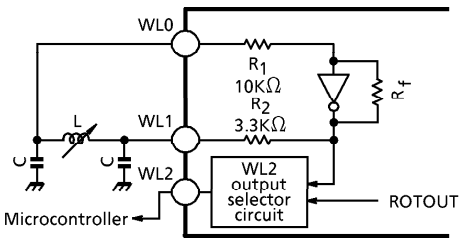


(12) LC oscillator circuit

An LC oscillator circuit can be configured simply by attaching an external variable coil (L) and a fixed capacitor (C). The square wave signal (WLOUT) formed from the WL1 output is output to pin WL2. Bit WLF, located in the C_0 register, can be used to select either WLOUT output or ROTOUT output.

BIT STATE	WLF
0	WL2 : WLOUT (WL1) output
1	WL2 : ROTOUT output

Example circuit

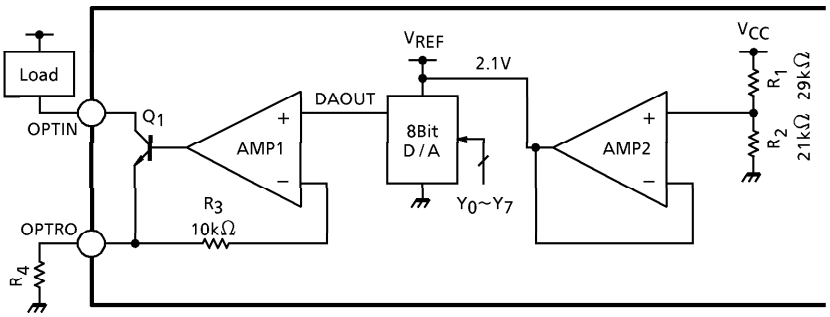


Example design : L = 0.38mH C = 0.022μF

(13) 8Bit D / A converter for constant-current control

To make the load current constant, attach a load such as a sensor to the OPTIN pin, set the data in the D / A data register, and connect a resistor to the OPTRO pin.

Block Diagram

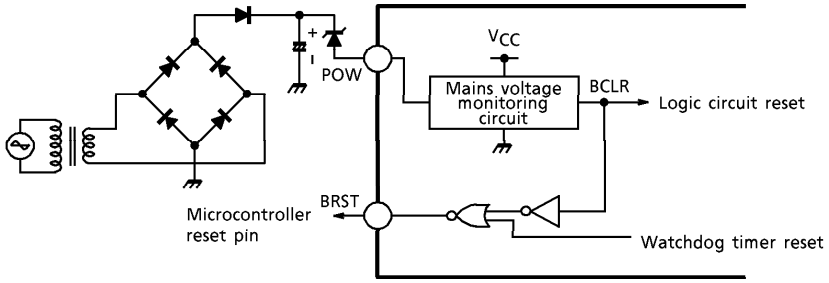


(Note) Because the AMP1 output is held low when the D / A data are 00H, Q1 is OFF. Therefore, the effective data length is seven bits (Y1~Y7).
The 8bit D / A resolution is : V_{REF} (2.1V) / 256 = about 8.2mV (@V_{CC} = 5V)

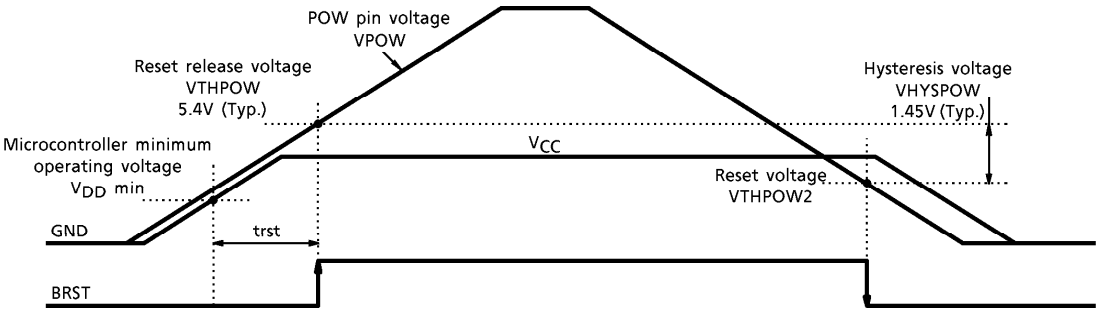
(14) Mains voltage monitoring circuit

Implement full-wave rectification on the secondary side output of the transformer and step down the smoothed voltage. By monitoring the stepped-down voltage at the POW pin (pin 15), a reset can be performed on the internal registers and logic circuits.
Also, by connecting the BRST pin to the reset pin of the microcontroller, the entire application system can be reset.
As the following timing chart shows, the reset voltage has hysteresis, which guarantees operation during momentary outages, for example.

Block diagram



Timing chart

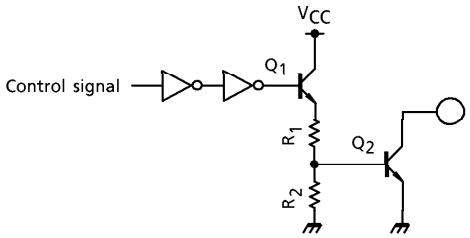


The above chart shows the recommended design for the relationship between the mains power monitoring voltage (VPOW) and the system power supply (V_{CC}).

(15) High-current output port

The high-current output port (pins TB0, TB1, TC0~TC7) are NPN open collector circuits and can directly drive devices such as a triac or buzzer.
Select the most suitable triac or buzzer in accordance with the use conditions.

Block diagram



Resistors R_1 and R_2 are configured for each port as in the following table.

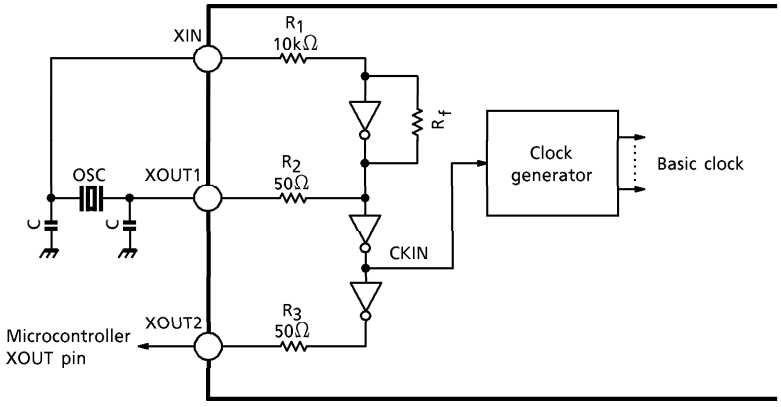
PIN	OUTPUT CURRENT CAPACITY (min) V_{OL} = 1.0V	R_1 (Typ.)	R_2 (Typ.)	PIN	OUTPUT CURRENT CAPACITY (min) V_{OL} = 1.0V	R_1 (Typ.)	R_2 (Typ.)
TB0	60mA	340Ω	70kΩ	TC4	30mA	650Ω	70kΩ
TB1				TC5			
TC0	70mA	290Ω		TC6			
TC1				TC7			
TC2	50mA	400Ω					
TC3							

(Note) Depending on the number of high-current output ports ON simultaneously, the power dissipation shown in the maximum ratings may be inadvertently exceeded. Take care not to exceed the rating.

(16) Oscillator circuit

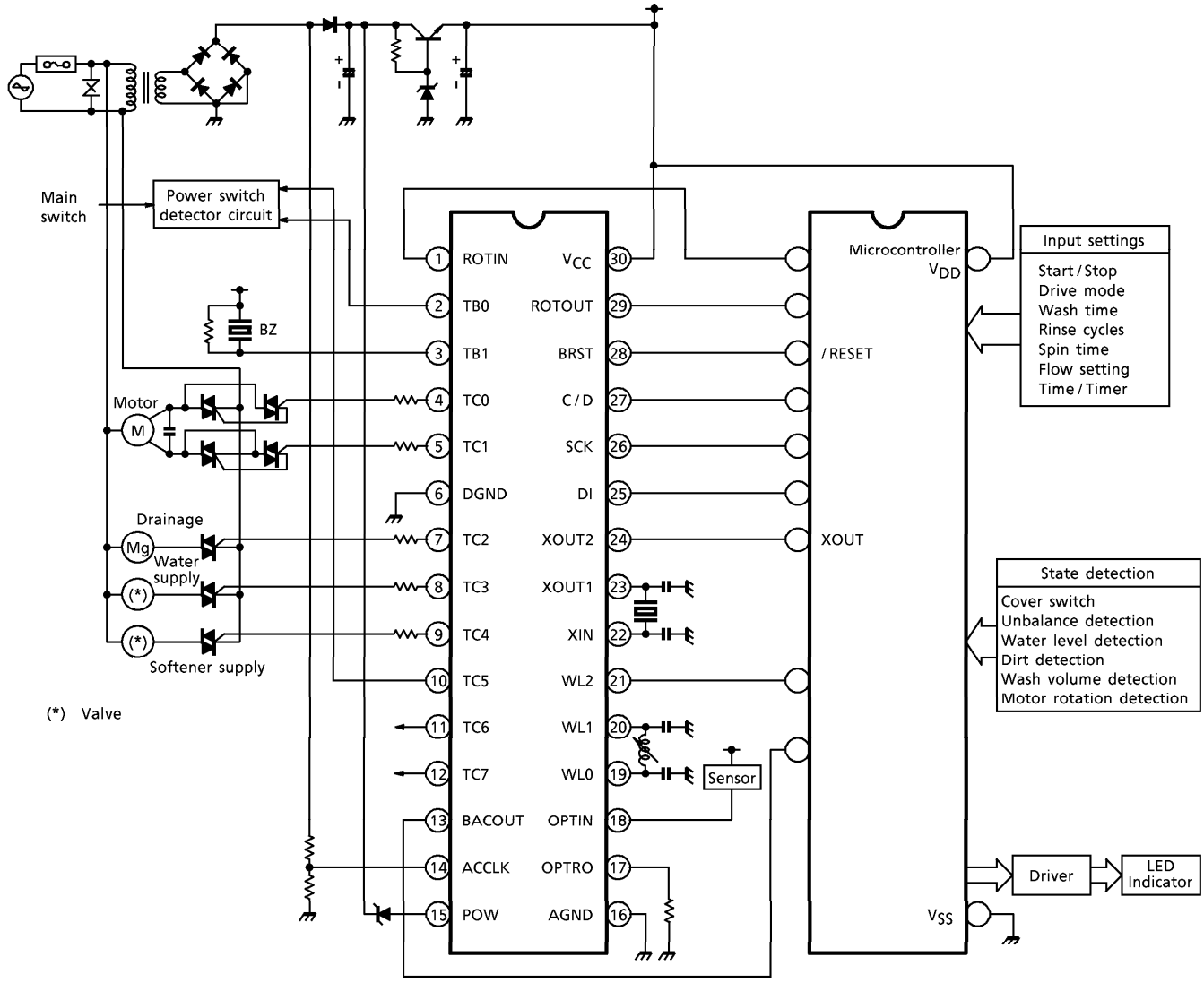
The oscillator circuit is configured as in the following diagram. Connecting 4MHz~8MHz oscillators creates a system clock. To supply a clock to the microcontroller, connect the XOUT2 pin to the microcontroller's XOUT pin.

Block diagram



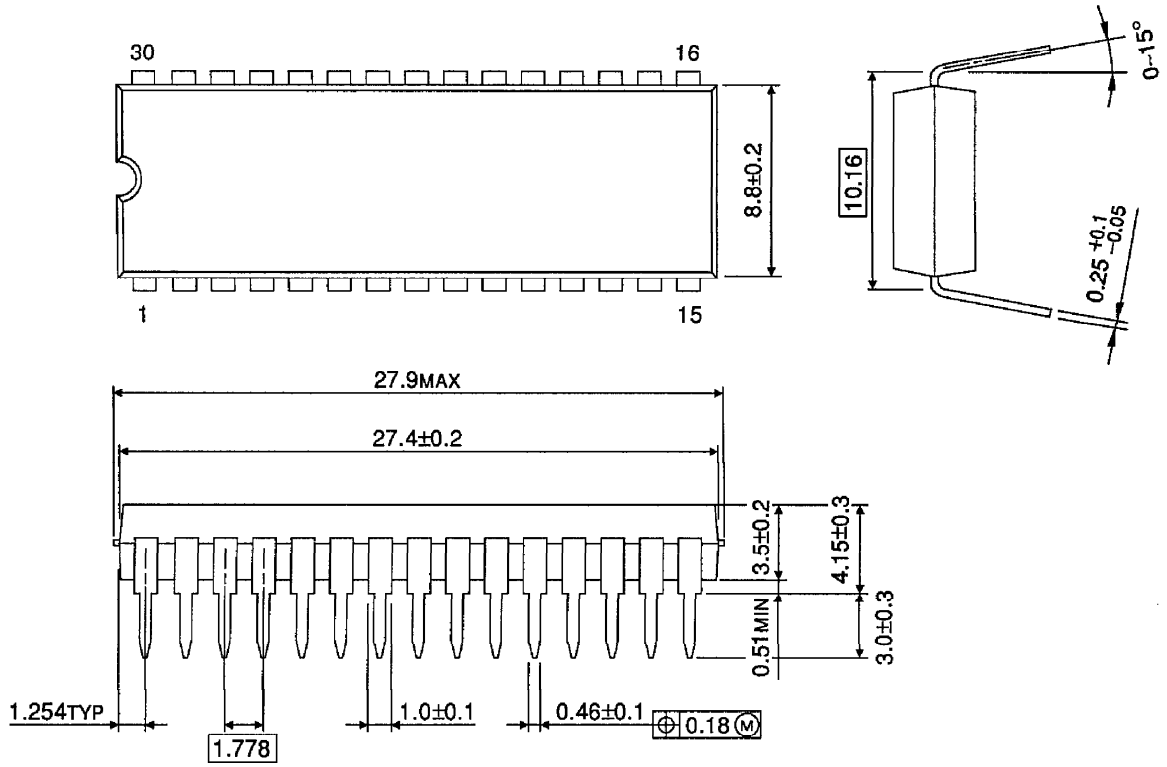
Recommended oscillators : 8MHz : Murata 8MHz Ceralock ceramic oscillator (CST8, 0MTW)
4MHz : Murata 4MHz Ceralock ceramic oscillator (CST4, 0MGW)

APPLICATION CIRCUIT EXAMPLE



PACKAGE DIMENSIONS

SDIP30-P-400-1.78 Unit : mm



Weight : 1.99g (Typ.)

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