TAS5760M-Q1 2x25-W Digital Input Closed-Loop Automotive Class-D Audio Amplifier

1 Features

- Minimum Supply Voltage down to 4.5 V
- Qualified for Automotive Applications
- Adjustable Switching Frequencies
- Selectable Hardware or Software Control
- Audio Performance (PVDD = 12 V, R_{SPK} = 8 Ω, SPK_GAIN[1:0] Pins = 00)
  - Idle Channel Noise = 66 µVrms (A-Wtd)
  - THD+N = 0.02% (at 1 W, 1 kHz)
  - SNR = 99.7 dB A-Wtd (Ref. to THD+N = 1%)
- Audio I/O Configuration:
  - Single Stereo I²S Input
  - Stereo Bridge Tied Load (BTL) or Mono Parallel Bridge Tied Load (PBTL) Operation
  - 32, 44.1, 48, 88.2, 96 kHz Sample Rates
- General Operational Features:
  - Integrated Digital Output Clipper
  - Programmable I²C Address (1101100[$^{R}/_{W}$] or 1101101[$^{R}/_{W}$])
  - Closed-Loop Amplifier Architecture
- Robustness Features:
  - Clock Error, DC, and Short-Circuit Protection
  - Overtemperature and Programmable Overcurrent Protection

2 Applications

- Automotive Telematics
- eCall (Emergency Call)
- Acoustic Vehicle Alerting System (AVAS)
- EV/HEV Sound Generation

3 Description

The TAS5760M-Q1 is a stereo digital input Class-D audio amplifier which is ideal for use in automotive emergency call (eCall), telematics, acoustic vehicle alerting system (AVAS) and EV/HEV sound generation applications. The device provides up to 25 W instantaneous power into 4 Ω at 10% THD+N at 14.4 V. The TAS5760M-Q1 also includes hardware and software (I²C) control modes, an integrated digital clipper, selectable gain options, and a wide power supply operating range (4.5 V – 26.4 V).

An optimal mix of thermal performance and device cost is provided in the 120-mΩ $R_{DS(ON)}$ of the output MOSFETs.

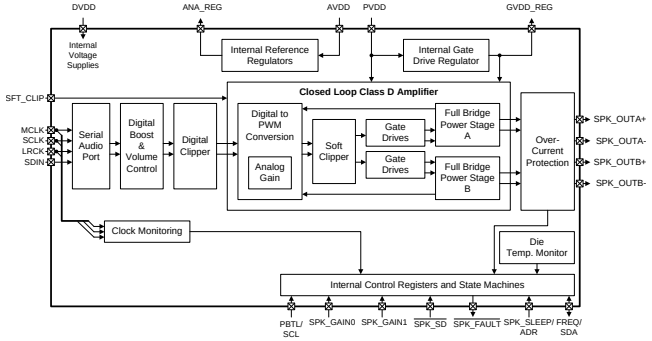
The device is offered in a thermally enhanced 32-Pin HTSSOP (DAP) package.

Device Information(1)

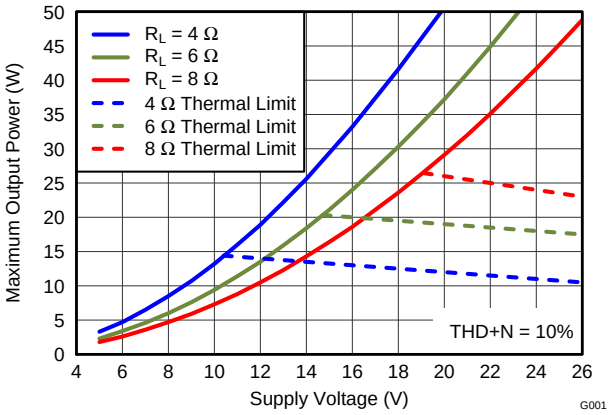
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TAS5760M-Q1	HTSSOP (32)	11 mm × 6.2 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Functional Block Diagram



Power at 10% THD+N vs PVDD



NOTE: Thermal Limits were determined via the TAS5760xxEVM

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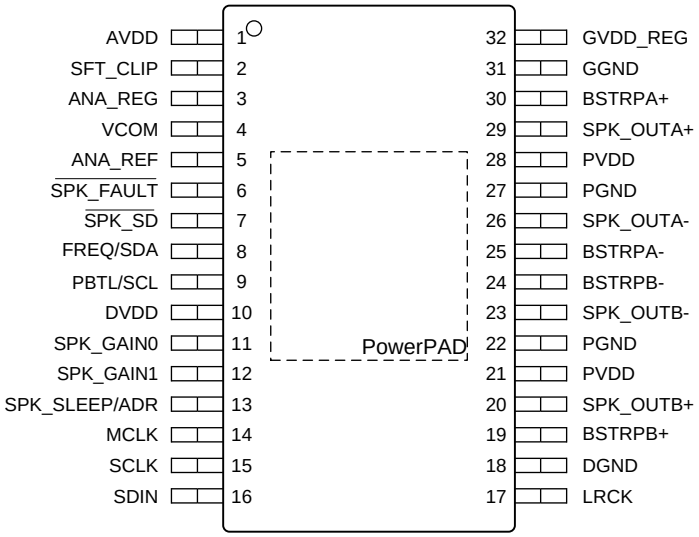
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2017) to Revision A	Page
• Released as Production Data	1

5 Pin Configuration and Functions

DAP PACKAGE
32-PIN TSSOP
TOP VIEW



Pin Functions

TAS5760M-Q1 NAME	NO.	TYPE (1)	INTERNAL TERMINATION	DESCRIPTION
AVDD	1	P	-	Power supply for internal analog circuitry
ANA_REF	5	P	-	Connection point for internal reference used by ANA_REG and VCOM filter capacitors
ANA_REG	3	P	-	Voltage regulator derived from AVDD supply (NOTE: This terminal is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry)
BSTRPA–	25	P	-	Connection point for the SPK_OUTA– bootstrap capacitor, which is used to create a power supply for the high-side gate drive for SPK_OUTA–
BSTRPA+	30	P	-	Connection point for the SPK_OUTA+ bootstrap capacitor, which is used to create a power supply for the high-side gate drive for SPK_OUTA
BSTRPB–	24	P	-	Connection point for the SPK_OUT bootstrap capacitor, which is used to create a power supply for the high-side gate drive for SPK_OUT
BSTRPB+	19	P	-	Connection point for the SPK_OUTB+ bootstrap capacitor, which is used to create a power supply for the high-side gate drive for SPK_OUTB+
DGND	18	G	-	Ground for digital circuitry (NOTE: This terminal should be connected to the system ground)
DVDD	10	P	-	Power supply for the internal digital circuitry
FREQ/SDA	8	DI	Weak Pull-Down	Dual function terminal that functions as an I²C data input terminal in I²C Control Mode or as a Frequency Select terminal when in Hardware Control Mode.
GGND	31	G	-	Ground for gate drive circuitry (this terminal should be connected to the system ground)
GVDD_REG	32	P	-	Voltage regulator derived from PVDD supply (NOTE: This terminal is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry)
LRCK	17	DI	Weak Pull-Down	Word select clock for the digital signal that is active on the serial port's input data line
MCLK	14	DI	Weak Pull-Down	Master Clock used for internal clock tree, sub-circuit/state machine, and Serial Audio Port clocking

(1) AI = Analog input, AO = Analog output, DI = Digital Input, DO = Digital Output, P = Power, G = Ground (0V)

Pin Functions (continued)

TAS5760M-Q1 NAME	NO.	TYPE(1)	INTERNAL TERMINATION	DESCRIPTION
PBTL/SCL	9	DI	Weak Pull-Down	Dual function terminal that functions as an I²C clock input terminal in I²C Control Mode or configures the device to operate in pre-filter Parallel Bridge Tied Load (PBTL) mode when in Hardware Control Mode
PGND	22, 27	G	-	Ground for power device circuitry (NOTE: This terminal should be connected to the system ground)
PVDD	21, 28	P	-	Power Supply for internal power circuitry
SCLK	15	DI	Weak Pull-Down	Bit clock for the digital signal that is active on the serial data port's input data line
SDIN	16	DI	Weak Pull-Down	Data line to the serial data port
SFT_CLIP	2	AI	-	Sets the maximum output voltage before clipping
$\overline{\text{SPK\_FAULT}}$	6	DO	Open Drain	Fault terminal, which is pulled LOW when an internal fault occurs
SPK_GAIN0	11	DI	Weak Pull-Down	Adjusts the LSB of the multi-bit gain of the speaker amplifier
SPK_GAIN1	12	DI	Weak Pull-Down	Adjusts the MSB of the multi-bit gain of the speaker amplifier
SPK_SLEEP/ ADR	13	DI	Weak Pull-Up	Places the speaker amplifier in mute
SPK_OUTA–	26	AO	-	Negative terminal for differential speaker amplifier output A
SPK_OUTA+	29	AO	-	Positive terminal for differential speaker amplifier output A
SPK_OUTB–	23	AO	-	Negative terminal for differential speaker amplifier output B
SPK_OUTB+	20	AO	-	Positive terminal for differential speaker amplifier output B
$\overline{\text{SPK\_SD}}$	7	DI	-	Places the device in shutdown when pulled LOW
VCOM	4	P	-	Bias voltage for internal PWM conversion block
PowerPAD™	-	G	-	Provides both electrical and thermal connection from the device to the board. A matching ground pad must be provided on the PCB and the device connected to it via solder

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Temperature	Ambient Operating Temperature, T_A	–40	105	°C
	Ambient Storage Temperature, T_S	–40	125	°C
Supply Voltage	AVDD Supply	–0.3	30	V
	PVDD Supply	–0.3	30	V
	DVDD Supply	–0.3	4	V
DVDD Referenced Digital Input Voltages	Digital Inputs referenced to DVDD supply	–0.5	DVDD + 0.5	V
Speaker Amplifier Output Voltage	V_{SPK_OUTxx}, measured at the output pin	–0.3	32	V
Storage temperature range, T_{stg}		–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Ambient Operating Temperature	–40		105	°C
AVDD	AVDD Supply	4.5		26.4	V
PVDD	PVDD Supply	4.5		26.4	V
DVDD	DVDD Supply	3		3.63	V
$VIH_{(DR)}$	Input Logic HIGH for DVDD Referenced Digital Inputs		DVDD		V
$VIL_{(DR)}$	Input Logic LOW for DVDD Referenced Digital Inputs		0		V
$R_{SPK\ (BTL)}$	Minimum Speaker Load in BTL Mode	4			Ω
$R_{SPK\ (PBTL)}$	Minimum Speaker Load in PBTL Mode	2			Ω

6.4 Thermal Information

THERMAL METRIC (1)		TAS5760M-Q1				UNIT
		DCA [HTSSOP]	DCA [HTSSOP]	DAP [HTSSOP]	DAP [HTSSOP]	
		32-PIN (2)	48-PIN (2)	32-PIN (3)	48-PIN (3)	
θ_{JA}	Junction-to-ambient thermal resistance	60.3	30.2	60.3	31.9	°C/W
$\theta_{JC(top)}$	Junction-to-case (top) thermal resistance	16	14.3	16	16	°C/W
θ_{JB}	Junction-to-board thermal resistance	12	12.7	12	17	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	0.6	0.4	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.9	12.7	11.9	16.8	°C/W
$\theta_{JC(bottom)}$	Junction-to-case (bottom) thermal resistance	0.8	0.7	0.8	0.81	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) JEDEC Standard 2 Layer Board
(3) JEDEC Standard 4 Layer Board

6.5 Digital I/O Pins

Test conditions (unless otherwise noted): T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH1}	Input Logic HIGH threshold for DVDD Referenced Digital Inputs	All digital pins	70			%DVDD
V_{IL1}	Input Logic LOW threshold for DVDD Referenced Digital Inputs	All digital pins			30	%DVDD
I_{IH1}	Input Logic HIGH Current Level	All digital pins			15	µA
I_{IL1}	Input Logic LOW Current Level	All digital pins			–15	µA
V_{OH}	Output Logic HIGH Voltage Level	I_{OH} = 2 mA	90			%DVDD
V_{OL}	Output Logic LOW Voltage Level	I_{OH} = -2 mA			10	%DVDD

6.6 Master Clock

Test conditions (unless otherwise noted): T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D_{MCLK}	Allowable MCLK Duty Cycle		45%	50%	55%	
f_{MCLK}	Supported MCLK Frequencies	Values include: 128, 192, 256, 384, 512.	128		512	f_S

6.7 Serial Audio Port

Test conditions (unless otherwise noted): T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D_{SCLK}	Allowable SCLK Duty Cycle		45%	50%	55%	
	Required LRCK to SCLK Rising Edge		15			ns
t_{HLD}	Required SDIN Hold Time after SCLK Rising Edge		15			ns
t_{su}	Required SDIN Setup Time before SCLK Rising Edge		15			ns
f_S	Supported Input Sample Rates	Sample rates above 48kHz supported by "double speed mode," which is activated through the I²C control port	32		96	kHz
f_{SCLK}	Supported SCLK Frequencies	Values include: 32, 48, 64	32		64	f_S

6.8 Protection Circuitry

Test conditions (unless otherwise noted): T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$OVE_{RTHRES(PVDD)}$	PVDD Overvoltage Error Threshold	PVDD Rising		28		V
$OVE_{FTHRES(PVDD)}$	PVDD Overvoltage Error Threshold	PVDD Falling		27.3		V
$UVE_{FTHRES(PVDD)}$	PVDD Undervoltage Error (UVE) Threshold	PVDD Falling		3.95		V
$UVE_{RTHRES(PVDD)}$	PVDD UVE Threshold (PVDD Rising)	PVDD Rising		4.15		V
OTE_{THRES}	Overtemperature Error (OTE) Threshold			150		°C
OTE_{HYST}	Overtemperature Error (OTE) Hysteresis			15		°C
OCE_{THRES}	Overcurrent Error (OCE) Threshold for each BTL Output	PVDD= 15V, T_A = 25 °C		7		A
DCE_{THRES}	DC Error (DCE) Threshold	PVDD= 12V, T_A = 25 °C		2.6		V
$T_{\overline{SPK\_FAULT}}$	Speaker Amplifier Fault Time Out period	DC Detect Error		650		ms
		OTE or OCP Fault		1.3		s

6.9 Speaker Amplifier in All Modes

Test conditions (unless otherwise noted): T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AV_{00}	Speaker Amplifier Gain with SPK_GAIN[1:0] Pins = 00	Hardware Control Mode (Additional gain settings available in Software Control Mode)(1)		25.2		dBV
AV_{01}	Speaker Amplifier Gain with SPK_GAIN[1:0] Pins = 01	Hardware Control Mode (Additional gain settings available in Software Control Mode)(1)		28.6		dBV
AV_{10}	Speaker Amplifier Gain with SPK_GAIN[1:0] Pins = 10	Hardware Control Mode (Additional gain settings available in Software Control Mode)(1)		31		dBV
AV_{11}	Speaker Amplifier Gain with SPK_GAIN[1:0] Pins = 11	(This setting places the device in Software Control Mode)		(Set via I²C)		
$\lvert VOS \rvert_{(SPK\_AMP)}$	Speaker Amplifier DC Offset	BTL, Worst case over voltage, gain settings			10	mV
		PBTL, Worst case over voltage, gain settings			15	mV
$f_{SPK\_AMP(0)}$	Speaker Amplifier Switching Frequency when PWM_FREQ Pin = 0	(Hardware Control Mode. Additional switching rates available in Software Control Mode.)		16		f_S
$f_{SPK\_AMP(1)}$	Speaker Amplifier Switching Frequency when PWM_FREQ Pin = 1	(Hardware Control Mode. Additional switching rates available in Software Control Mode.)		8		f_S
$R_{DS(ON)}$	On Resistance of Output MOSFET (both high-side and low-side)	PVDD = 15 V, TA = 25 °C, Die Only		120		mΩ
		PVDD= 15V, TA = 25 °C, Includes: Die, Bond Wires, Leadframe		150		mΩ
f_C	–3-dB Corner Frequency of High-Pass Filter	f_S = 44.1 kHz		3.7		Hz
		f_S = 48 kHz		4		
		f_S = 88.2 kHz		7.4		
		f_S = 96 kHz		8		

(1) The digital boost block contributes +6dB of gain to this value. The audio signal must be kept below -6dB to avoid clipping the digital audio path.

6.10 Speaker Amplifier in Stereo Bridge Tied Load (BTL) Mode

Test conditions (unless otherwise noted): T_C = 25°C, input signal is 1 kHz Sine

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ICN_{(SPK)}$	Idle Channel Noise	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8 Ω, A-Weighted		66		µVrms
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8 Ω, A-Weighted		75		
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8 Ω, A-Weighted		79		
		PVDD = 24 V, SPK_GAIN[1:0] Pins =10, R_{SPK} = 8 Ω, A-Weighted		120		
$Po_{(SPK)}$	Maximum Instantaneous Output Power Per. Ch.	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 4 Ω, THD+N = 0.1%,		14.2		W
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8 Ω, THD+N = 0.1%		8		
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 4 Ω, THD+N = 0.1%,		21.9		
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8 Ω, THD+N = 0.1%		12.5		
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 4 Ω, THD+N = 0.1%,		33.5		
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8 Ω, THD+N = 0.1%		20		
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, R_{SPK} = 4 Ω, THD+N = 0.1%,		55.2		
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, R_{SPK} = 8 Ω, THD+N = 0.1%		31.8		
$Po_{(SPK)}$	Maximum Continuous Output Power Per. Ch.(1)	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 4 Ω, THD+N = 0.1%,		14		W
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8 Ω, THD+N = 0.1%		8		
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 4 Ω, THD+N = 0.1%,		13.25		
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8 Ω, THD+N = 0.1%		12.5		
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 4 Ω, THD+N = 0.1%,		12.25		
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8 Ω, THD+N = 0.1%		20		
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, R_{SPK} = 4 Ω, THD+N = 0.1%,		11		
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, R_{SPK} = 8 Ω, THD+N = 0.1%		24		
$SNR_{(SPK)}$	Signal to Noise Ratio (Referenced to THD+N = 1%)	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8 Ω, A-Weighted, -60dBFS Input		99.7		dB
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8 Ω, A-Weighted, -60dBFS Input		98.2		
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8 Ω, A-Weighted, -60dBFS Input		100.4		
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, R_{SPK} = 8 Ω, A-Weighted, -60dBFS Input		98.8		

(1) The continuous power output of any amplifier is determined by the thermal performance of the amplifier as well as limitations placed on it by the system around it, such as the PCB configuration and the ambient operating temperature. The performance characteristics listed in this section are achievable on the TAS5760M-Q1's EVM, which is representative of the poplular "2 Layers / 1oz Copper" PCB configuration in a size that is representative of the amount of area often provided to the amplifier section of popular consumer audio electronics. As can be seen in the instantaneous power portion of this table, more power can be delivered from the TAS5760M-Q1 if steps are taken to pull more heat out of the device. For instance, using a board with more layers or adding a small heatsink will result in an increase of continuous power, up to and including the instantaneous power level. This behavior can also been seen in the POUT vs. PVDD plots shown in the *Typical Characteristics (Stereo BTL Mode): f_{SPK_AMP} = 384 kHz* section of this data sheet.

Speaker Amplifier in Stereo Bridge Tied Load (BTL) Mode (continued)

Test conditions (unless otherwise noted): T_C = 25°C, input signal is 1 kHz Sine

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$THD+N_{(SPK)}$	Total Harmonic Distortion and Noise	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 4 Ω, Po = 1 W		0.02%		
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8 Ω, Po = 1 W		0.03%		
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 4 Ω, Po = 1 W		0.03%		
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8 Ω, Po = 1 W		0.03%		
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 4 Ω, Po = 1 W		0.03%		
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8 Ω, Po = 1 W		0.04%		
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, R_{SPK} = 4 Ω, Po = 1 W		0.03%		
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, R_{SPK} = 8 Ω, Po = 1 W		0.04%		
$X\text{-}Talk_{(SPK)}$	Cross-talk (worst case between LtoR and RtoL coupling)	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8 Ω, Input Signal 250 mVrms, 1kHz Sine		–92		dB
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8 Ω, Input Signal 250 mVrms, 1kHz Sine		–93		
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8 Ω, Input Signal 250 mVrms, 1kHz Sine		–94		
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, R_{SPK} = 8 Ω, Input Signal 250 mVrms, 1kHz Sine		–93		

6.11 Speaker Amplifier in Mono Parallel Bridge Tied Load (PBTL) Mode

Test conditions (unless otherwise noted): T_C = 25°C, input signal is 1 kHz Sine

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ICN	Idle Channel Noise	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8Ω, A-Weighted		69		µVrms
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8Ω, A-Weighted		85		
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8Ω, A-Weighted		85		
		PVDD = 24 V, SPK_GAIN[1:0] Pins =10, R_{SPK} = 8Ω, A-Weighted		131		
$P_{O(SPK)}$	Maximum Instantaneous Output Power	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 2Ω, THD+N = 0.1%,		28.6		W
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 4Ω, THD+N = 0.1%,		15.9		
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8Ω, THD+N = 0.1%		8.4		
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 2Ω, THD+N = 0.1%,		43.2		
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 4Ω, THD+N = 0.1%,		25		
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8Ω, THD+N = 0.1%		13.3		
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 2Ω, THD+N = 0.1%,		68.3		
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 4Ω, THD+N = 0.1%,		40		
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8Ω, THD+N = 0.1%		21.3		
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, R_{SPK} = 2Ω, THD+N = 0.1%,		114.7		
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, R_{SPK} = 4Ω, THD+N = 0.1%,		63.5		
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, R_{SPK} = 8Ω, THD+N = 0.1%		34.1		

Speaker Amplifier in Mono Parallel Bridge Tied Load (PBTL) Mode (continued)

Test conditions (unless otherwise noted): T_C = 25°C, input signal is 1 kHz Sine

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_{O(SPK)}$	Maximum Continuous Output Power(1)	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 2Ω, THD+N = 0.1%,		30		W
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 4Ω, THD+N = 0.1%,		15.9		
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8Ω, THD+N = 0.1%		8.4		
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 2Ω, THD+N = 0.1%,		28.5		
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 4Ω, THD+N = 0.1%,		25		
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8Ω, THD+N = 0.1%		13.3		
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 2Ω, THD+N = 0.1%,		26.5		
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 4Ω, THD+N = 0.1%,		40		
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8Ω, THD+N = 0.1%		21.3		
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, R_{SPK} = 2Ω, THD+N = 0.1%,		24		
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, R_{SPK} = 4Ω, THD+N = 0.1%,		40		
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, R_{SPK} = 8Ω, THD+N = 0.1%		34.1		
SNR	Signal to Noise Ratio (Referenced to THD+N = 1%)	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8Ω, A-Weighted, -60dBFS Input		100.4		dB
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8Ω, A-Weighted, -60dBFS Input		99.5		
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8Ω, A-Weighted, -60dBFS Input		100.1		
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, R_{SPK} = 8Ω, A-Weighted, -60dBFS Input		99.5		

(1) The continuous power output of any amplifier is determined by the thermal performance of the amplifier as well as limitations placed on it by the system around it, such as the PCB configuration and the ambient operating temperature. The performance characteristics listed in this section are achievable on the TAS5760M-Q1's EVM, which is representative of the poplular "2 Layers / 1oz Copper" PCB configuration in a size that is representative of the amount of area often provided to the amplifier section of popular consumer audio electronics. As can be seen in the instantaneous power portion of this table, more power can be delivered from the TAS5760M-Q1 if steps are taken to pull more heat out of the device. For instance, using a board with more layers or adding a small heatsink will result in an increase of continuous power, up to and including the instantaneous power level. This behavior can also been seen in the POUT vs. PVDD plots shown in the *Typical Characteristics (Mono PBTL Mode): f_{SPK_AMP} = 384 kHz* section of this data sheet.

Speaker Amplifier in Mono Parallel Bridge Tied Load (PBTL) Mode (continued)

Test conditions (unless otherwise noted): T_C = 25°C, input signal is 1 kHz Sine

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$THD+N_{(SPK)}$	Total Harmonic Distortion and Noise	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 2Ω, Po = 1 W		0.03%		
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 4Ω, Po = 1 W		0.02%		
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8Ω, Po = 1 W		0.02%		
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 2Ω, Po = 1 W		0.03%		
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 4Ω, Po = 1 W		0.02%		
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8Ω, Po = 1 W		0.02%		
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 2Ω, Po = 1 W		0.03%		
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 4Ω, Po = 1 W		0.02%		
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8Ω, Po = 1 W		0.03%		
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, R_{SPK} = 2Ω, Po = 1 W		0.03%		
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, R_{SPK} = 4Ω, Po = 1 W		0.02%		
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, R_{SPK} = 8Ω, Po = 1 W		0.03%		

6.12 I²C Control Port

Test conditions (unless otherwise noted): T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{L(I^2C)}$	Allowable Load Capacitance for Each I²C Line				400	pF
f_{SCL}	Support SCL frequency	No Wait States			400	kHz
t_{buf}	Bus Free time between STOP and START conditions		1.3			µS
$t_{f(I^2C)}$	Rise Time, SCL and SDA				300	ns
$t_{h1(I^2C)}$	Hold Time, SCL to SDA		0			ns
$t_{h2(I^2C)}$	Hold Time, START condition to SCL		0.6			µs
$t_{I^2C(start)}$	I²C Startup Time				12	mS
$t_{r(I^2C)}$	Rise Time, SCL and SDA				300	ns
$t_{su1(I^2C)}$	Setup Time, SDA to SCL		100			ns
$t_{su2(I^2C)}$	Setup Time, SCL to START condition		0.6			µS
$t_{su3(I^2C)}$	Setup Time, SCL to STOP condition		0.6			µS
$T_{w(H)}$	Required Pulse Duration, SCL HIGH		0.6			µS
$T_{w(L)}$	Required Pulse Duration, SCL LOW		1.3			µS

6.13 Typical Idle, Mute, Shutdown, Operational Power Consumption

Test conditions (unless otherwise noted): T_C = 25°C, input signal is 1 kHz Sine

V_{PVDD} [V]	R_{SPK} [Ω]	SPEAKER AMPLIFIER STATE		$I_{PVDD+AVDD}$ [mA]	I_{DVDD} [mA]	P_{DISS} [W]
6	4	f_{SPK_AMP} = 384kHz	Idle	23.48	3.73	0.15
	8			23.44	3.72	0.15
	4		Mute	23.53	3.72	0.15
	8			23.46	3.72	0.15
	4		Sleep	13.26	0.48	0.08
	8			13.27	0.53	0.08
	4		Shutdown	0.046	0.04	0
	8			0.046	0.03	0
	4	f_{SPK_AMP} = 768kHz	Idle	30.94	3.71	0.2
	8			30.94	3.71	0.2
	4		Mute	29.37	3.71	0.19
	8			29.39	3.71	0.19
	4		Sleep	13.24	0.5	0.08
	8			13.23	0.52	0.08
	4		Shutdown	0.046	0.03	0
	8			0.046	0.03	0
	4	f_{SPK_AMP} = 1152kHz	Idle	39.39	3.7	0.25
	8			39.43	3.7	0.25
	4		Mute	36.91	3.7	0.23
	8			36.9	3.69	0.23
	4		Sleep	13.17	0.53	0.08
	8			13.13	0.45	0.08
	4		Shutdown	0.046	0.03	0
	8			0.046	0.03	0

Typical Idle, Mute, Shutdown, Operational Power Consumption (continued)

Test conditions (unless otherwise noted): T_C = 25°C, input signal is 1 kHz Sine

V_{PVDD} [V]	R_{SPK} [Ω]	SPEAKER AMPLIFIER STATE		$I_{PVDD+AVDD}$ [mA]	I_{DVDD} [mA]	P_{DISS} [W]
12	4	f_{SPK_AMP} = 384kHz	Idle	32.95	3.74	0.41
	8			32.93	3.73	0.41
	4		Mute	32.98	3.73	0.41
	8			32.97	3.73	0.41
	4		Sleep	12.71	0.47	0.15
	8			12.75	0.5	0.15
	4		Shutdown	0.053	0.04	0
	8			0.053	0.04	0
	4	f_{SPK_AMP} = 768kHz	Idle	44.84	3.73	0.55
	8			44.82	3.73	0.55
	4		Mute	42.71	3.72	0.52
	8			42.66	3.72	0.52
	4		Sleep	12.71	0.49	0.15
	8			12.73	0.52	0.15
	4		Shutdown	0.063	0.03	0
	8			0.053	0.03	0
	4	f_{SPK_AMP} = 1152kHz	Idle	59.3	3.73	0.72
	8			59.3	3.73	0.72
	4		Mute	55.74	3.72	0.68
	8			55.74	3.72	0.68
	4		Sleep	12.67	0.49	0.15
	8			12.61	0.43	0.15
	4		Shutdown	0.053	0.02	0
	8			0.053	0.03	0

Typical Idle, Mute, Shutdown, Operational Power Consumption (continued)

Test conditions (unless otherwise noted): T_C = 25°C, input signal is 1 kHz Sine

V_{PVDD} [V]	R_{SPK} [Ω]	SPEAKER AMPLIFIER STATE		$I_{PVDD+AVDD}$ [mA]	I_{DVDD} [mA]	P_{DISS} [W]
19	4	f_{SPK_AMP} = 384kHz	Idle	42	3.73	0.81
	8			41.92	3.73	0.81
	4		Mute	41.93	3.73	0.81
	8			41.97	3.72	0.81
	4		Sleep	12.95	0.47	0.25
	8			13	0.52	0.25
	4		Shutdown	0.072	0.04	0
	8			0.072	0.03	0
	4	f_{SPK_AMP} = 768kHz	Idle	55.86	3.73	1.07
	8			55.82	3.73	1.07
	4		Mute	51.72	3.72	0.99
	8			51.69	3.72	0.99
	4		Sleep	12.96	0.47	0.25
	8			12.95	0.51	0.25
	4		Shutdown	0.072	0.03	0
	8			0.062	0.03	0
	4	f_{SPK_AMP} = 1152kHz	Idle	74.87	3.72	1.43
	8			74.81	3.72	1.43
	4		Mute	67.96	3.71	1.3
	8			67.91	3.71	1.3
	4		Sleep	12.94	0.51	0.25
	8			12.84	0.42	0.25
	4		Shudown	0.062	0.03	0
	8			0.062	0.03	0

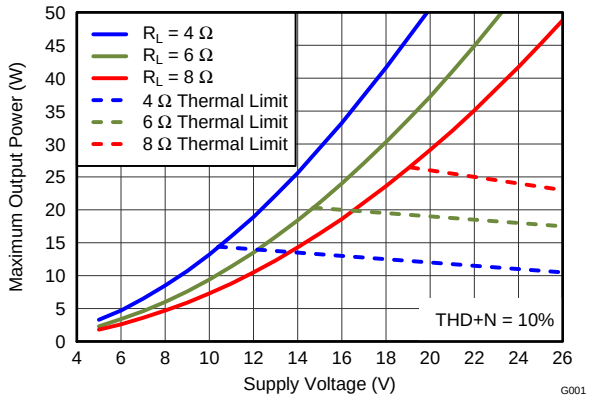
Typical Idle, Mute, Shutdown, Operational Power Consumption (continued)

Test conditions (unless otherwise noted): T_C = 25°C, input signal is 1 kHz Sine

V_{PVDD} [V]	R_{SPK} [Ω]	SPEAKER AMPLIFIER STATE		$I_{PVDD+AVDD}$ [mA]	I_{DVDD} [mA]	P_{DISS} [W]
24	4	f_{SPK_AMP} = 384kHz	Idle	48.03	3.73	1.17
	8			47.98	3.73	1.16
	4		Mute	47.99	3.72	1.16
	8			48	3.72	1.16
	4		Sleep	13.12	0.49	0.32
	8			13.14	0.48	0.32
	4		Shutdown	0.088	0.03	0
	8			0.088	0.03	0
	4	f_{SPK_AMP} = 768kHz	Idle	62.84	3.72	1.52
	8			62.84	3.72	1.52
	4		Mute	57.12	3.71	1.38
	8			57.07	3.71	1.38
	4		Sleep	13.19	0.47	0.32
	8			13.14	0.49	0.32
	4		Shutdown	0.078	0.03	0
	8			0.078	0.03	0
	4	f_{SPK_AMP} = 1152kHz	Idle	84.86	3.71	2.05
	8			84.83	3.71	2.05
	4		Mute	75.07	3.7	1.81
	8			75.01	3.71	1.81
	4		Sleep	13.11	0.51	0.32
	8			13.03	0.43	0.31
	4		Shutdown	0.078	0.03	0
	8			0.078	0.03	0

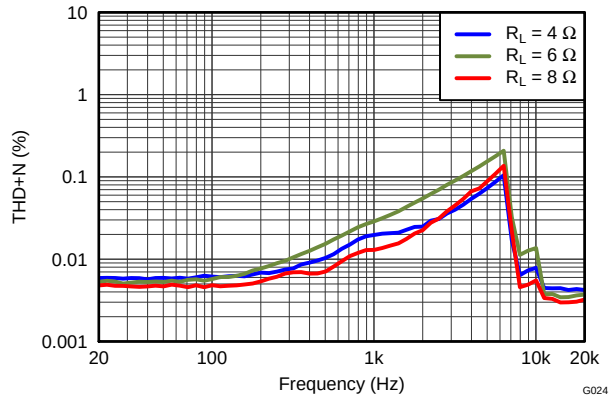
6.14 Typical Characteristics (Stereo BTL Mode): f_{SPK_AMP} = 384 kHz

At T_A = 25°C, f_{SPK_AMP} = 384 kHz, input signal is 1 kHz Sine, unless otherwise noted. Filter used for 8 Ω = 22 µH + 0.68 µF, Filter used for 6 Ω = 15 µH + 0.68 µF, Filter used for 4 Ω = 10 µH + 0.68 µF unless otherwise noted.



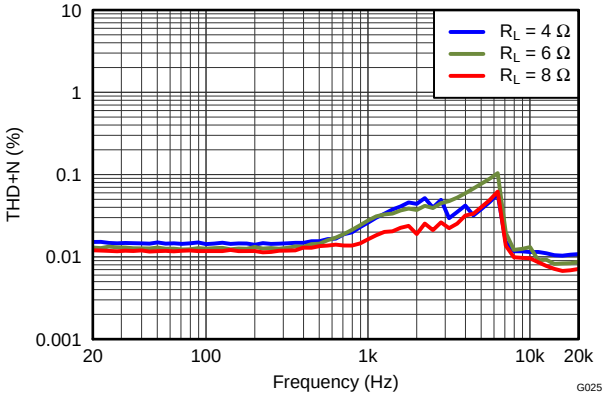
Thermal Limits are referenced to TAS5760xxEVM Rev D

Figure 1. Output Power vs PVDD



PVDD = 12 V, P_{OSPK} = 1 W

Figure 2. THD+N vs Frequency



PVDD = 24 V, P_{OSPK} = 1 W

Figure 3. THD+N vs Frequency

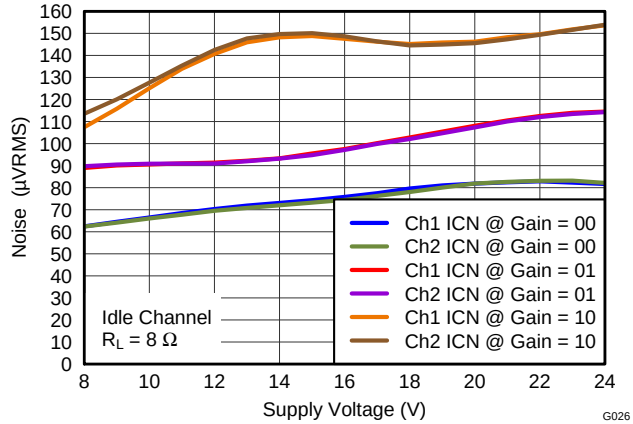
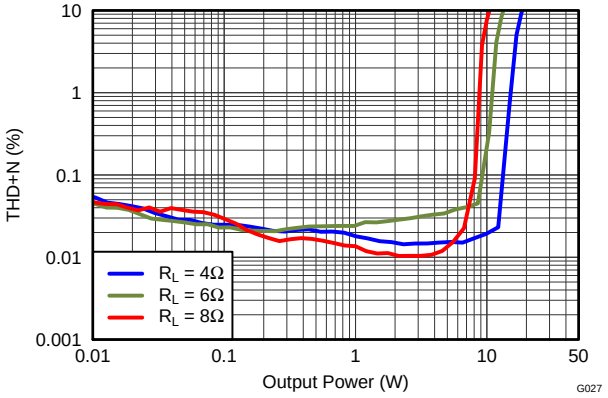
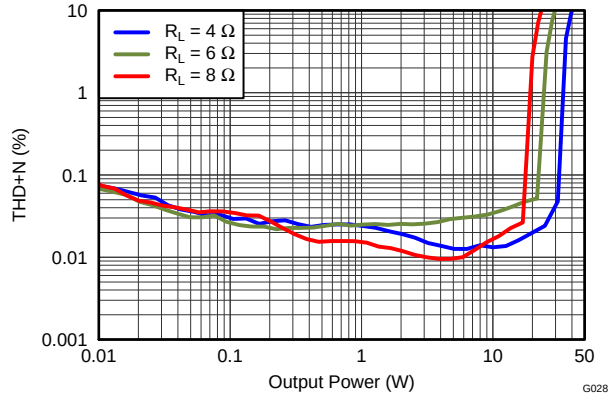


Figure 4. Idle Channel Noise vs PVDD



PVDD = 12 V, Both Channels Driven

Figure 5. THD+N vs Output Power

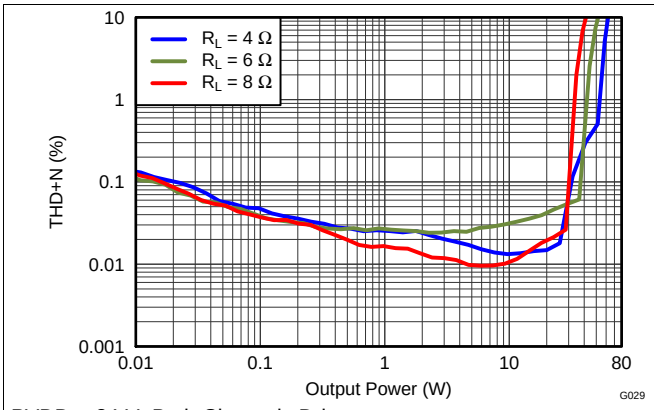


PVDD = 18 V, Both Channels Driven

Figure 6. THD+N vs Output Power

Typical Characteristics (Stereo BTL Mode): f_{SPK_AMP} = 384 kHz (continued)

At T_A = 25°C, f_{SPK_AMP} = 384 kHz, input signal is 1 kHz Sine, unless otherwise noted. Filter used for 8 Ω = 22 µH + 0.68 µF, Filter used for 6 Ω = 15 µH + 0.68 µF, Filter used for 4 Ω = 10 µH + 0.68 µF unless otherwise noted.



PVDD = 24 V, Both Channels Driven

Figure 7. THD+N vs Output Power

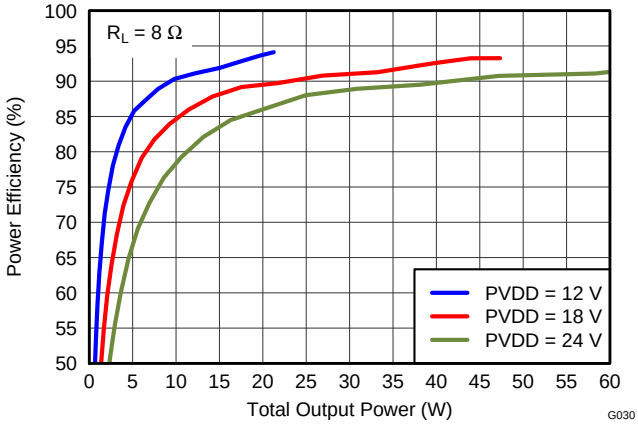


Figure 8. Efficiency vs Output Power

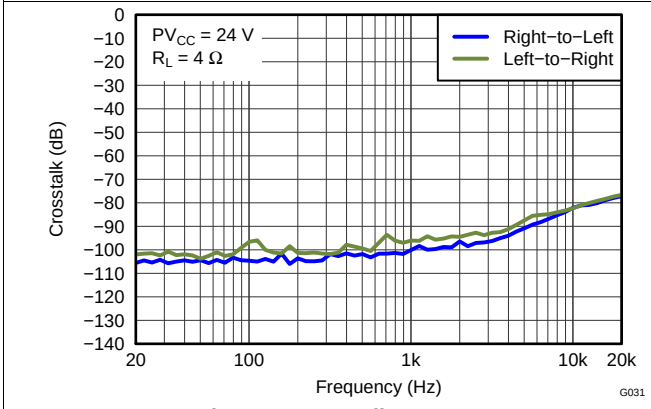


Figure 9. Crosstalk vs Frequency

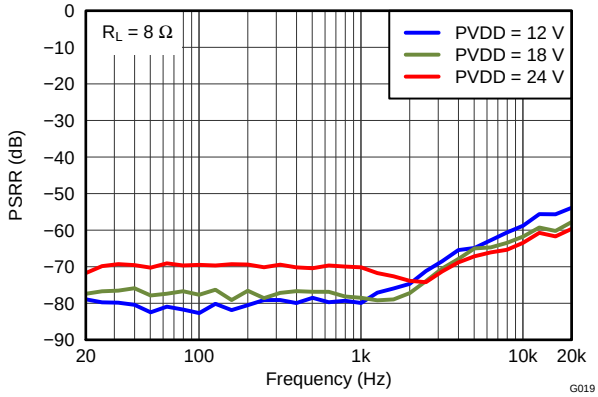


Figure 10. PVDD PSRR vs Frequency

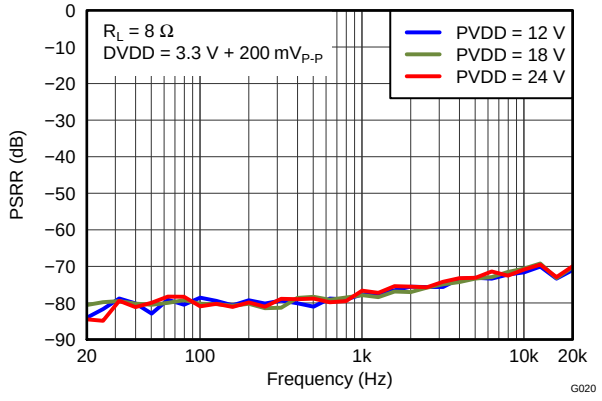


Figure 11. DVDD PSRR vs Frequency

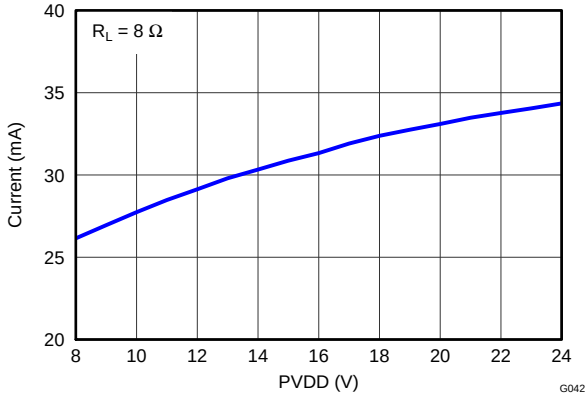
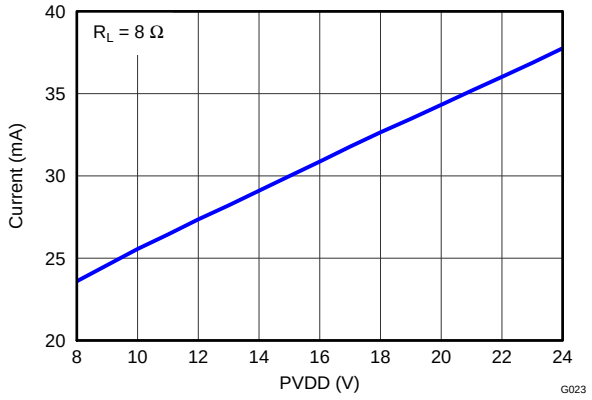


Figure 12. Idle Current Draw vs PVDD (Filterless)

Typical Characteristics (Stereo BTL Mode): f_{SPK_AMP} = 384 kHz (continued)

At T_A = 25°C, f_{SPK_AMP} = 384 kHz, input signal is 1 kHz Sine, unless otherwise noted. Filter used for 8 Ω = 22 µH + 0.68 µF, Filter used for 6 Ω = 15 µH + 0.68 µF, Filter used for 4 Ω = 10 µH + 0.68 µF unless otherwise noted.



With LC Filter as Shown on the EVM

Figure 13. Idle Current Draw vs PVDD

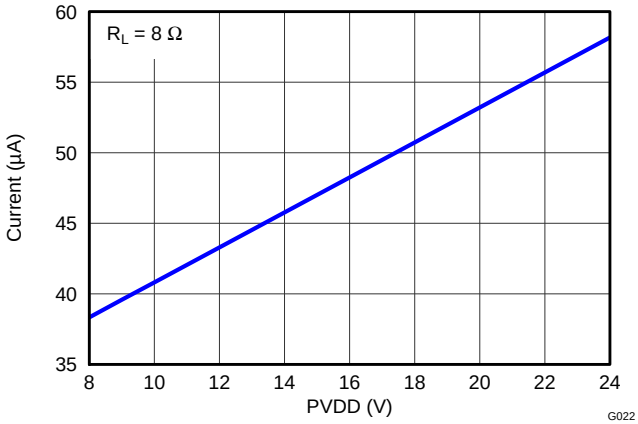
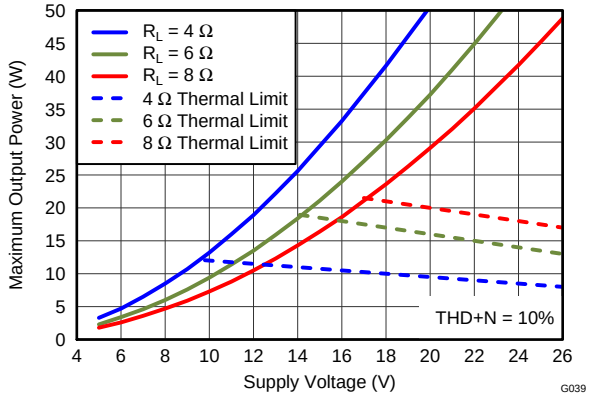


Figure 14. Shutdown Current Draw vs PVDD (Filterless)

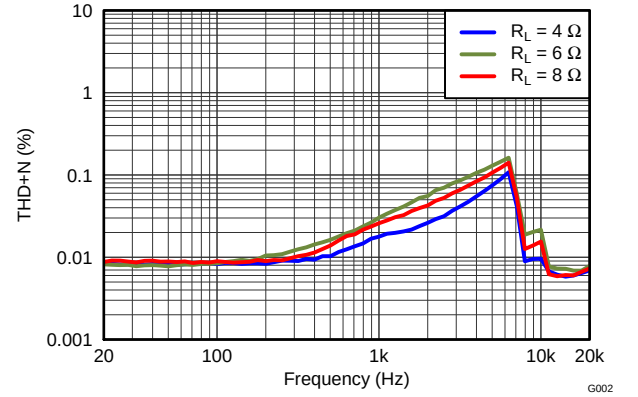
6.15 Typical Characteristics (Stereo BTL Mode): f_{SPK_AMP} = 768 kHz

At T_A = 25°C, f_{SPK_AMP} = 768 kHz, input signal is 1 kHz Sine, unless otherwise noted. Filter used for 8 Ω = 22 µH + 0.68 µF, Filter used for 6 Ω = 15 µH + 0.68 µF, Filter used for 4 Ω = 10 µH + 0.68 µF unless otherwise noted.



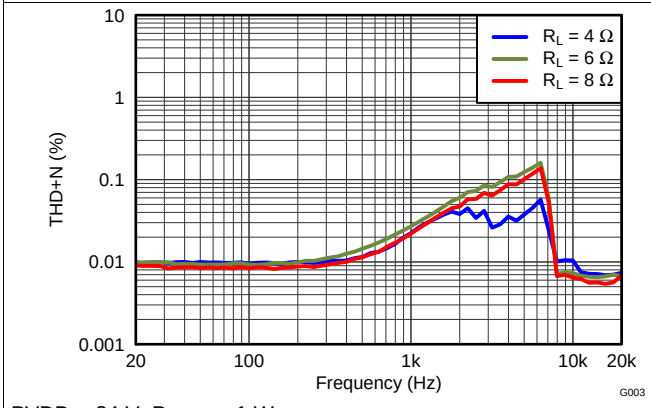
Thermal Limits are referenced to TAS5760xxEVM Rev D

Figure 15. Output Power vs PVDD



PVDD = 12 V, P_{OSPK} = 1 W

Figure 16. THD+N vs Frequency



PVDD = 24 V, P_{OSPK} = 1 W

Figure 17. THD+N vs Frequency

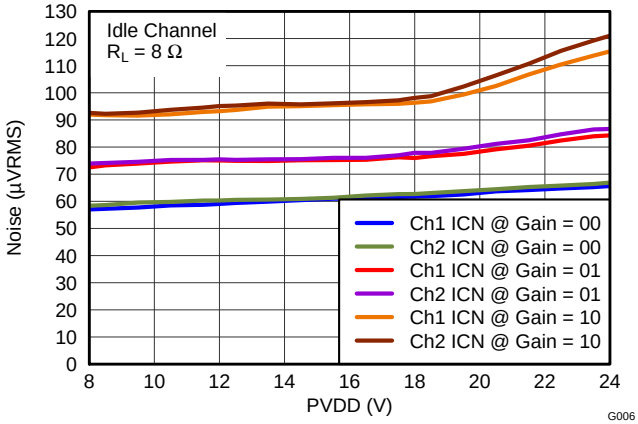
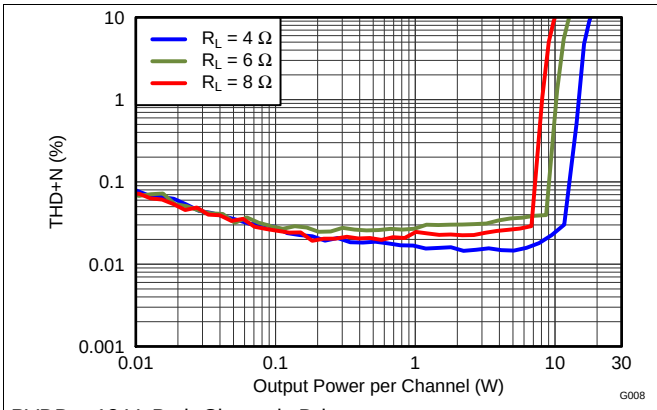


Figure 18. Idle Channel Noise vs PVDD

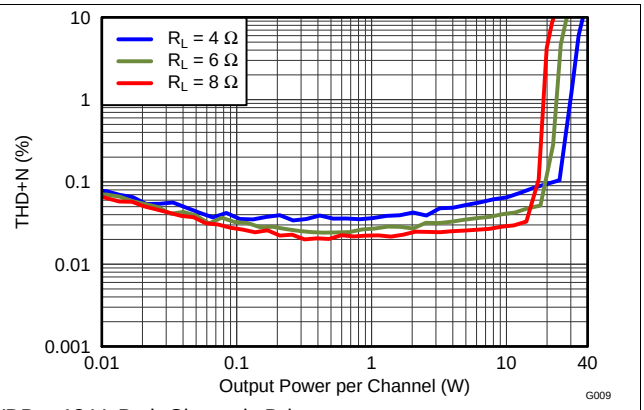
Typical Characteristics (Stereo BTL Mode): f_{SPK_AMP} = 768 kHz (continued)

At T_A = 25°C, f_{SPK_AMP} = 768 kHz, input signal is 1 kHz Sine, unless otherwise noted. Filter used for 8 Ω = 22 µH + 0.68 µF, Filter used for 6 Ω = 15 µH + 0.68 µF, Filter used for 4 Ω = 10 µH + 0.68 µF unless otherwise noted.



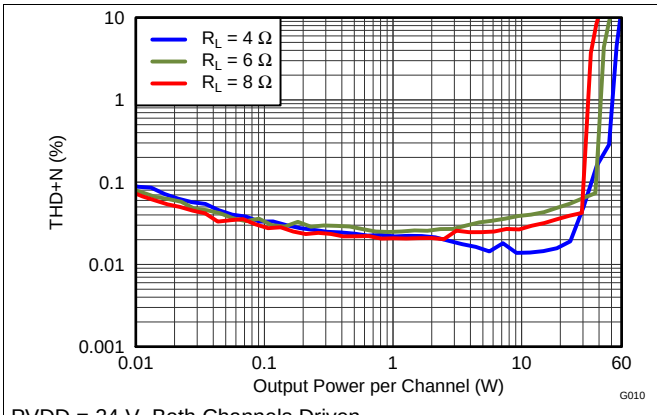
PVDD = 12 V, Both Channels Driven

Figure 19. THD+N vs Output Power



PVDD = 18 V, Both Channels Driven

Figure 20. THD+N vs Output Power



PVDD = 24 V, Both Channels Driven

Figure 21. THD+N vs Output Power

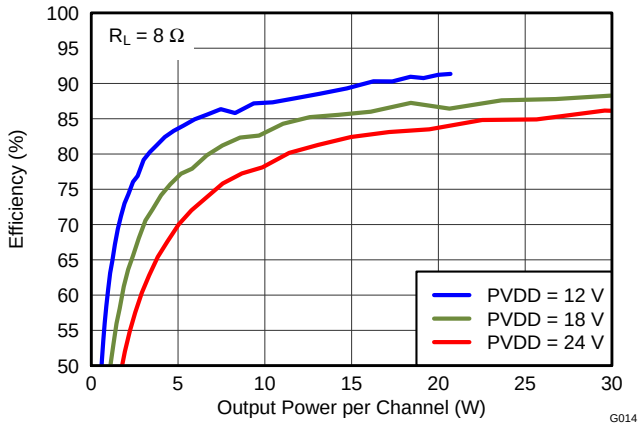


Figure 22. Efficiency vs Output Power

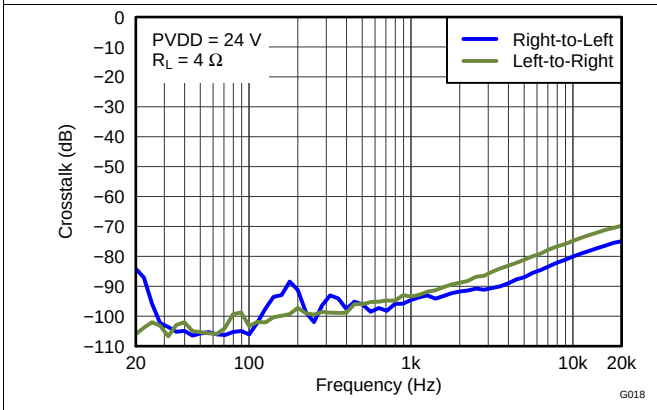


Figure 23. Crosstalk vs Frequency

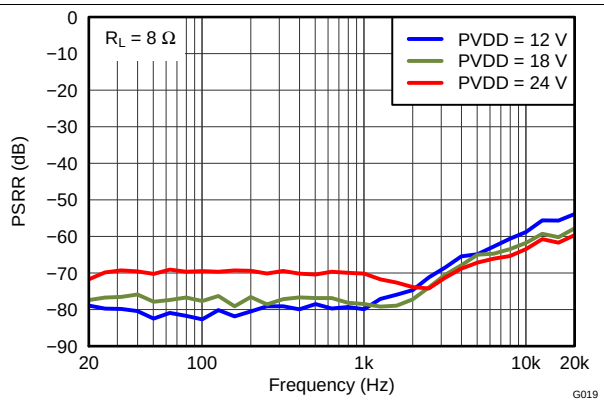


Figure 24. PVDD PSRR vs Frequency

Typical Characteristics (Stereo BTL Mode): f_{SPK_AMP} = 768 kHz (continued)

At T_A = 25°C, f_{SPK_AMP} = 768 kHz, input signal is 1 kHz Sine, unless otherwise noted. Filter used for 8 Ω = 22 µH + 0.68 µF, Filter used for 6 Ω = 15 µH + 0.68 µF, Filter used for 4 Ω = 10 µH + 0.68 µF unless otherwise noted.

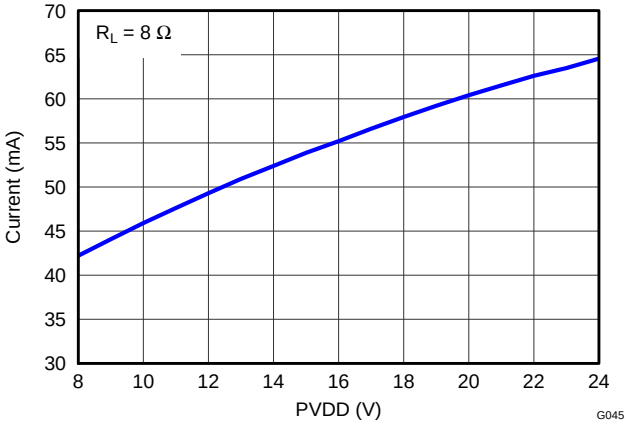
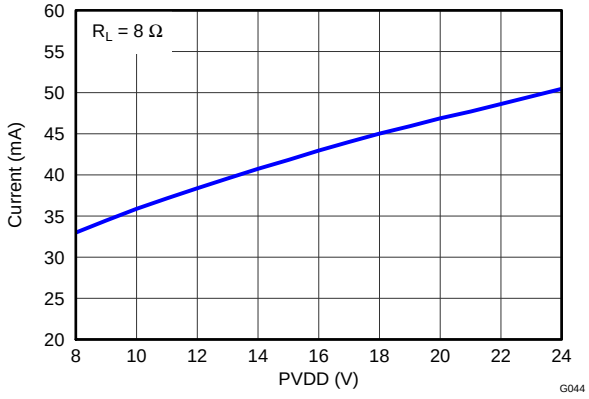


Figure 25. Idle Current Draw vs PVDD (Filterless)



With LC Filter as Shown on EVM

Figure 26. Idle Current Draw vs PVDD

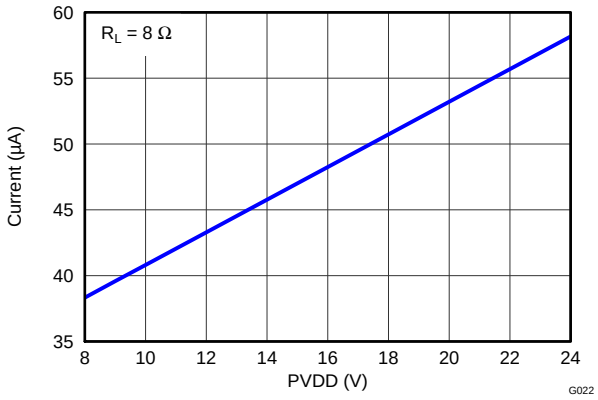
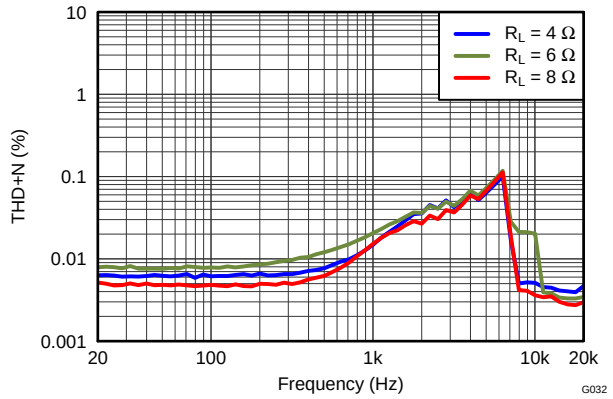


Figure 27. Shutdown Current Draw vs PVDD (Filterless)

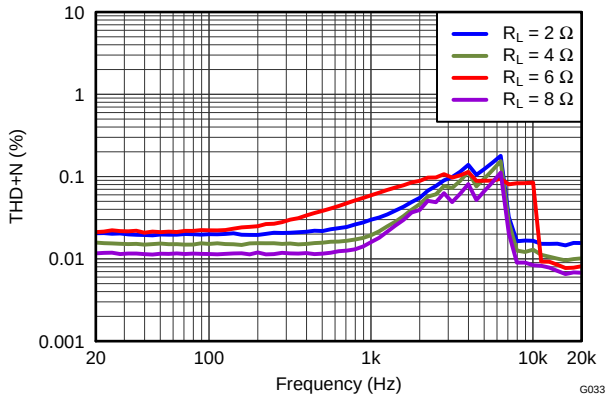
6.16 Typical Characteristics (Mono PBTL Mode): f_{SPK_AMP} = 384 kHz

At T_A = 25°C, f_{SPK_AMP} = 384 kHz, input signal is 1 kHz Sine unless otherwise noted.



PVDD = 12 V, P_{OSPK} = 1 W

Figure 28. THD+N vs Frequency



PVDD = 24 V, P_{OSPK} = 1 W

Figure 29. THD+N vs Frequency

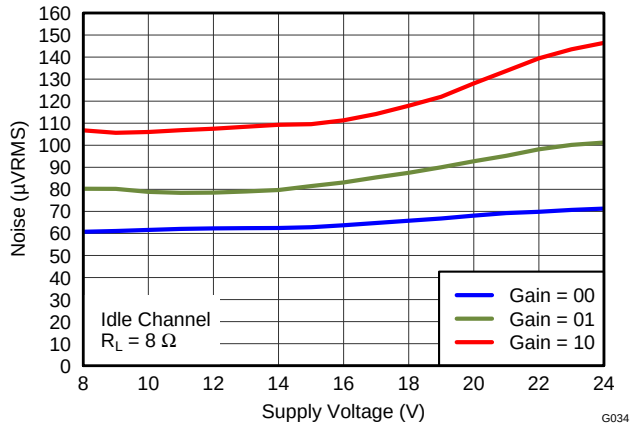
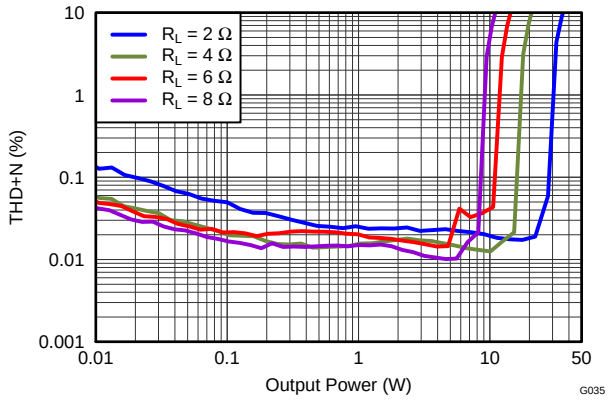
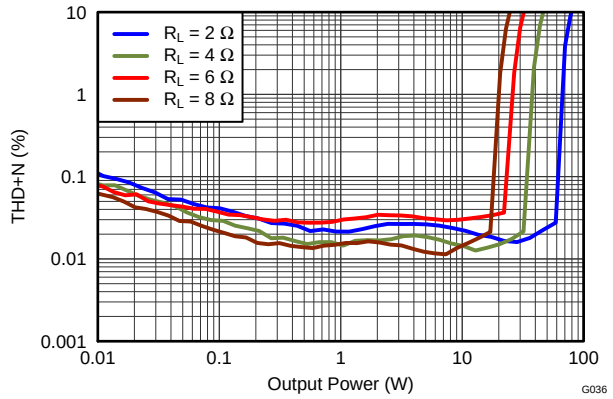


Figure 30. Idle Channel Noise vs PVDD



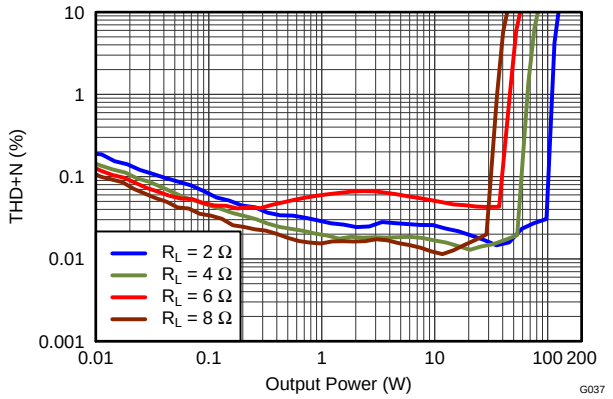
PVDD = 12 V With 1 kHz Sine Input

Figure 31. THD+N vs Output Power



PVDD = 18 V With 1 kHz Sine Input

Figure 32. THD+N vs Output Power



PVDD = 24 V With 1 kHz Sine Input

Figure 33. THD+N vs Output Power

Typical Characteristics (Mono PBTL Mode): f_{SPK_AMP} = 384 kHz (continued)

At T_A = 25°C, f_{SPK_AMP} = 384 kHz, input signal is 1 kHz Sine unless otherwise noted.

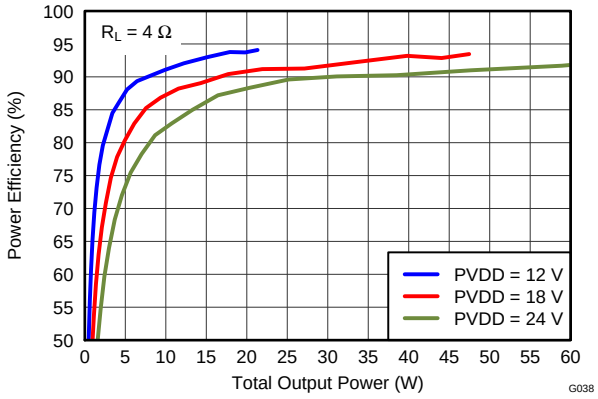
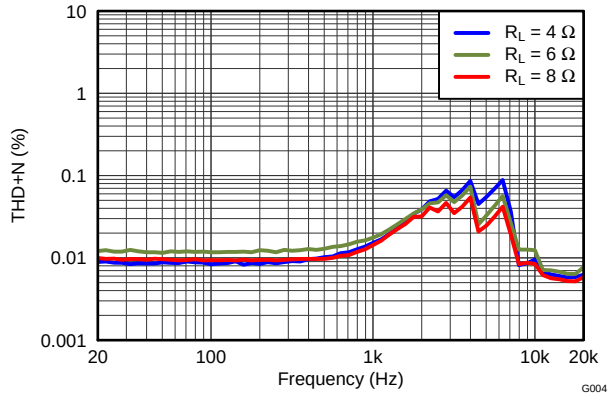


Figure 34. Efficiency vs Output Power

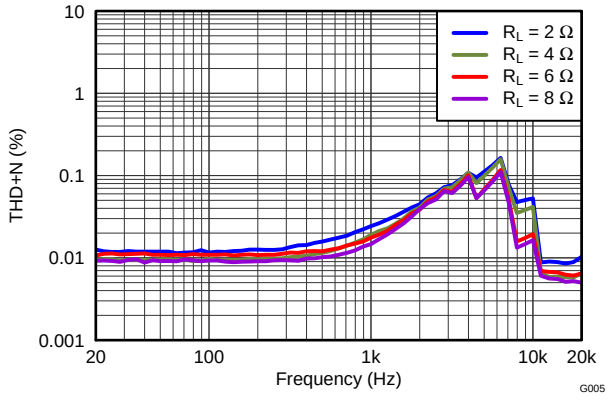
6.17 Typical Characteristics (Mono PBTL Mode): f_{SPK_AMP} = 768 kHz

At T_A = 25°C, f_{SPK_AMP} = 768 kHz, input signal is 1 kHz Sine unless otherwise noted.



PVDD = 12 V, P_{OSPK} = 1 W

Figure 35. THD+N vs Frequency



PVDD = 24 V, P_{OSPK} = 1 W

Figure 36. THD+N vs Frequency

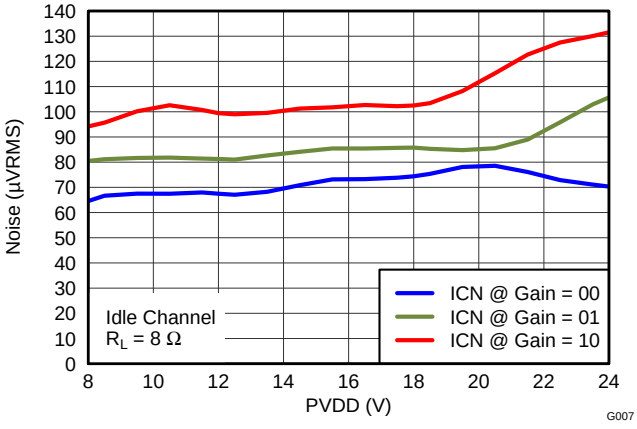


Figure 37. Idle Channel Noise vs PVDD

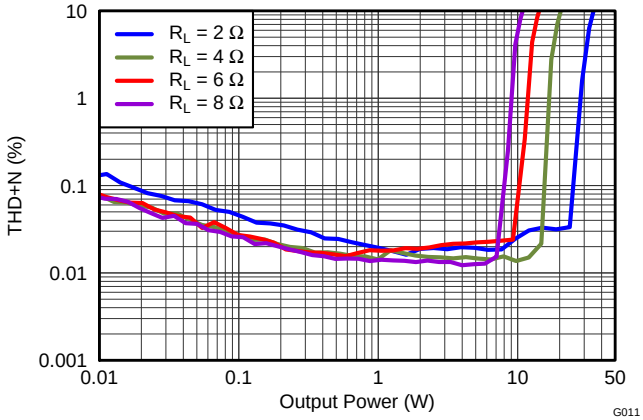


Figure 38. THD+N vs Output Power With PVDD = 12 V

Typical Characteristics (Mono PBTL Mode): f_{SPK_AMP} = 768 kHz (continued)

At T_A = 25°C, f_{SPK_AMP} = 768 kHz, input signal is 1 kHz Sine unless otherwise noted.

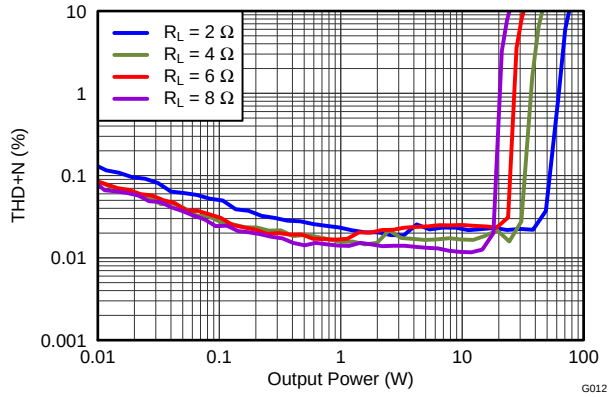


Figure 39. THD+N vs Output Power With PVDD = 18 V

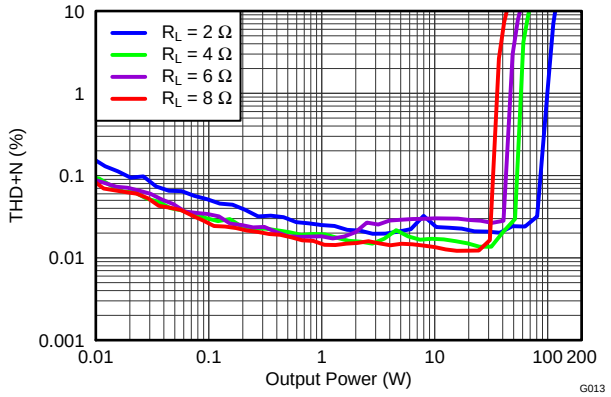


Figure 40. THD+N vs Output Power With PVDD = 24 V

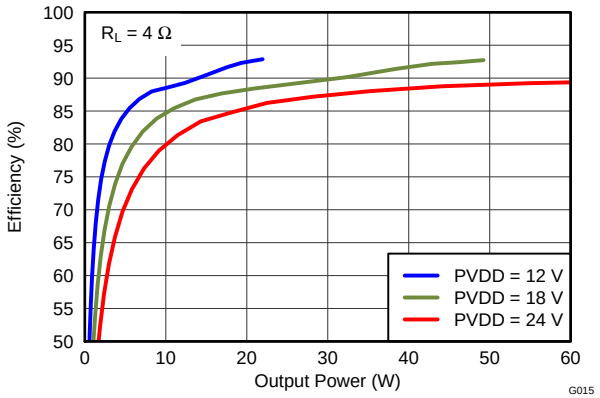


Figure 41. Efficiency vs Output Power

7 Parameter Measurement Information

All parameters are measured according to the conditions described in *Specifications*.

8 Detailed Description

8.1 Overview

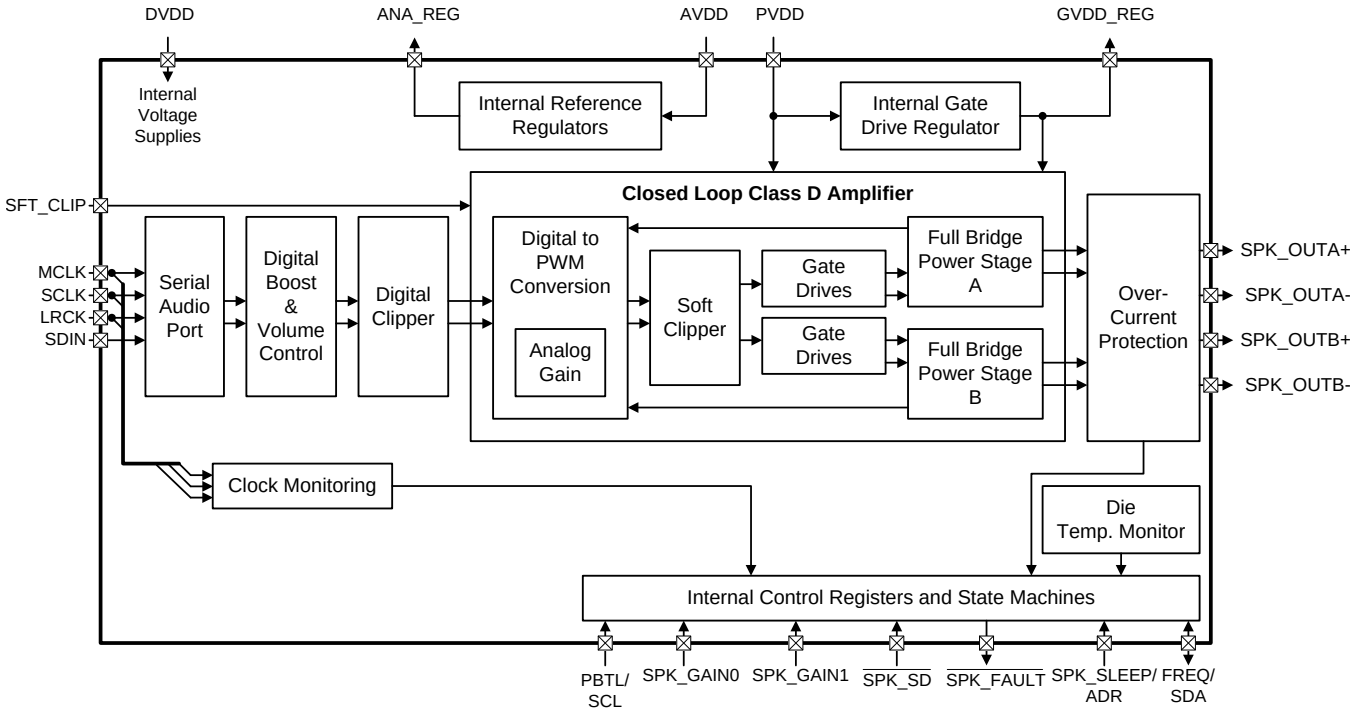
The TAS5760M-Q1 is a flexible and easy-to-use stereo class-D speaker amplifier with an I²S input serial audio port. The TAS5760M-Q1 supports a variety of audio clock configurations via two speed modes. In Hardware Control mode, the device only operates in single-speed mode. When used in Software Control mode, the device can be placed into double speed mode to support higher sample rates, such as 88.2 kHz and 96 kHz. The outputs of the TAS5760M-Q1 can be configured to drive two speakers in stereo Bridge Tied Load (BTL) mode or a single speaker in Parallel Bridge Tied Load (PBTL) mode.

Only two power supplies are required for the TAS5760M-Q1. They are a 3.3-V power supply, called VDD, for the small signal analog and digital and a higher voltage power supply, called PVDD, for the output stage of the speaker amplifier. To enable use in a variety of applications, PVDD can be operated over a large range of voltages, as specified in the *Recommended Operating Conditions*.

To configure and control the TAS5760M-Q1, two methods of control are available. In Hardware Control Mode, the configuration and real-time control of the device is accomplished through hardware control pins. In Software Control mode, the I²C control port is used both to configure the device and for real-time control. In Software Control Mode, several of the hardware control pins remain functional, such as the $\overline{\text{SPK\_SD}}$, $\overline{\text{SPK\_FAULT}}$, and SFT_CLIP pins.

8.2 Functional Block Diagram

Functional Block Diagram



8.3 Feature Description

8.3.1 Power Supplies

The power supply requirements for the TAS5760M-Q1 consist of one 3.3-V supply to power the low voltage analog and digital circuitry and one higher-voltage supply to power the output stage of the speaker amplifier. Several on-chip regulators are included on the TAS5760M-Q1 to generate the voltages necessary for the internal circuitry of the audio path. It is important to note that the voltage regulators which have been integrated are sized only to provide the current necessary to power the internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. Connecting external circuitry to these regulator outputs may result in reduced performance and damage to the device.

8.3.2 Speaker Amplifier Audio Signal Path

Figure 42 shows a block diagram of the speaker amplifier of the TAS5760M-Q1. In Hardware Control mode, a limited subset of audio path controls are made available via external pins, which are pulled HIGH or LOW to configure the device. In Software Control Mode, the additional features and configurations are available. All of the available controls are discussed in this section, and the subset of controls that available in Hardware Control Mode are discussed in the respective section below.

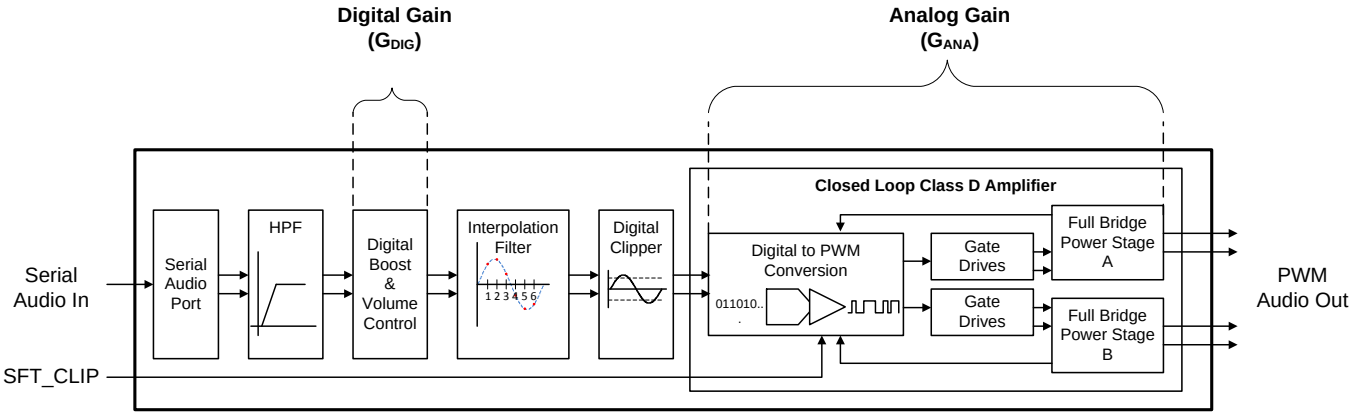


Figure 42. Speaker Amplifier Audio Signal Path

8.3.2.1 Serial Audio Port (SAP)

The serial audio port (SAP) receives audio in either I²S, Left Justified, or Right Justified formats. In Hardware Control mode, the device operates only in 32, 48 or 64 x f_S I²S mode. In Software Control mode, additional options for left-justified and right justified audio formats are available. The supported clock rates and ratios for Hardware Control Mode and Software Control Mode are detailed in their respective sections below.

8.3.2.1.1 I²S Timing

I²S timing uses LRCK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCK is LOW for the left channel and HIGH for the right channel. A bit clock, called SCLK, runs at 32, 48, or 64 × f_S and is used to clock in the data. There is a delay of one bit clock from the time the LRCK signal changes state to the first bit of data on the data lines. The data is presented in 2's-complement form (MSB-first) and is valid on the rising edge of bit clock.

8.3.2.1.2 Left-Justified

Left-justified (LJ) timing also uses LRCK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCK is HIGH for the left channel and LOW for the right channel. A bit clock running at 32, 48, or 64 × f_S is used to clock in the data. The first bit of data appears on the data lines at the same time LRCK toggles. The data is written MSB-first and is valid on the rising edge of the bit clock. The TAS5760M-Q1 can accept digital words from 16 to 24 bits wide and pads any unused trailing data-bit positions in the L/R frame with zeros before presenting the digital word to the audio signal path.

Feature Description (continued)

8.3.2.1.3 Right-Justified

Right-justified (RJ) timing also uses LRCK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCK is HIGH for the left channel and LOW for the right channel. A bit clock running at 32, 48, or 64 × f_S is used to clock in the data. The first bit of data appears on the data 8 bit-clock periods (for 24-bit data) after LRCK toggles. In RJ mode the LSB of data is always clocked by the last bit clock before LRCK transitions. The data is written MSB-first and is valid on the rising edge of bit clock. The TAS5760M-Q1 pads unused leading data-bit positions in the left/right frame with zeros before presenting the digital word to the audio signal path.

8.3.2.2 DC Blocking Filter

Excessive DC content in the audio signal can damage loudspeakers and even small amounts of DC offset in the signal path cause cause audible artifacts when muting and unmuting the speaker amplifier. For these reasons, the amplifier employs two separate DC blocking methods for the speaker amplifier. The first is a high-pass filter provided at the front of the data path to remove any DC from incoming audio data before it is presented to the audio path. The –3 dB corner frequencies for the filter are specified in the speaker amplifier electrical characteristics table. In Hardware Control mode, the DC blocking filter is active and cannot be disabled. In Software Control mode, the filter can be bypassed by writing a 1 to bit 7 of register 0x02. The second method is a DC detection circuit that will shutdown the power stage and issue a latching fault if DC is found to be present on the output due to some internal error of the device. This DC Error (DCE) protection is discussed in the Protection Circuitry section below.

8.3.2.3 Digital Boost and Volume Control

Following the high-pass filter, a digital boost block is included to provide additional digital gain if required for a given application as well as to set an appropriate clipping point for a given GAIN[1:0] pin configuration when in Hardware Control mode. The digital boost block defaults to +6dB when the device is in Hardware Mode. In most use cases, the digital boost block will remain unchanged when operating the device in Software Control mode, as the volume control offers sufficient digital gain for most applications. The TAS5760M-Q1's digital volume control operates from Mute to 24 dB, in steps of 0.5 dB. The equation below illustrates how to set the 8-bit volume control register at address 0x04:

DVC [Hex Value] = 0xCF + (DVC [dB] / 0.5 [dB]) (1)

Transitions between volume settings will occur at a rate of 0.5 dB every 8 LRCK cycles to ensure no audible artifacts occur during volume changes. This volume fade feature can be disabled via Bit 7 of the Volume Control Configuration Register.

8.3.2.4 Digital Clipper

A digital clipper is integrated in the oversampled domain to provide a component-free method to set the clip point of the speaker amplifier. Through the "Digital Clipper Level x" controls in the I²C control port, the point at which the oversampled digital path clips can be set directly, which in turns sets the 10% THD+N operating point of the amplifier. This is useful for applications in which a single system is designed for use in several end applications that have different power rating specifications. Its place in the oversampled domain ensures that the digital clipper is acoustically appealing and reduces or eliminates tones which would otherwise foldback into the audio band during clipping events. Figure 43 shows a block diagram of the digital clipper.

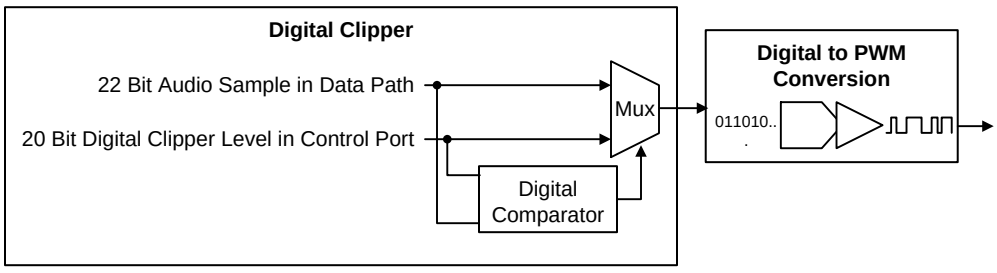


Figure 43. Digital Clipper Simplified Block Diagram

Feature Description (continued)

As mentioned previously, the audio signature of the amplifier when the digital clipper is active is very smooth, owing to its place in the signal chain. Figure 44 shows the typical behavior of the clipping events.

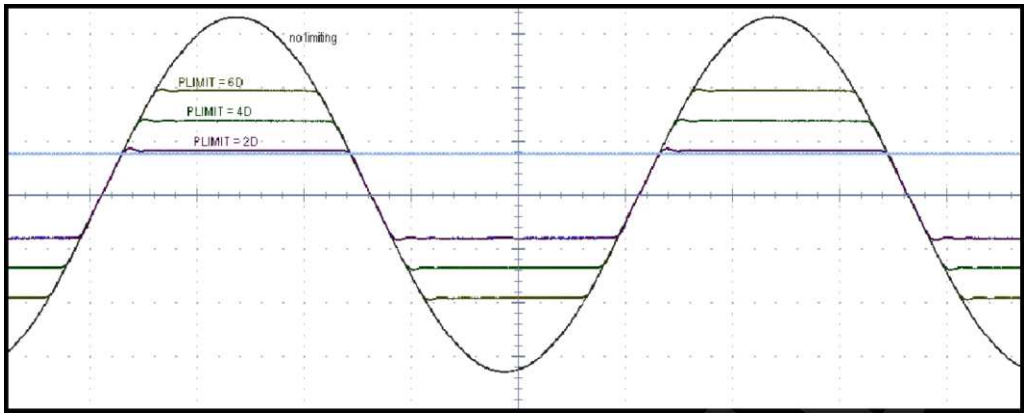


Figure 44. Digital Clipper Example Waveform for Various Settings of Digital Clip Level [19:0]

It is important to note that the actual signal developed across the speaker will be determined not only by the digital clipper, but also the analog gain of the amplifier. Depending on the analog gain settings and the PVDD level applied, clipping could occur as a result of the voltage swing that is determined by the gain being larger than the available PVDD supply rail. The gain structures are discussed in detail below for both Hardware Control Mode and Software Control Mode.

8.3.2.5 Closed-Loop Class-D Amplifier

Following the digital clipper, the interpolated audio data is next sent to the Closed-Loop Class-D amplifier, whose first stage is Digital to PWM Conversion (DPC) block. In this block, the stereo audio data is translated into two pairs of complimentary pulse width modulated (PWM) signals which are used to drive the outputs of the speaker amplifer. Feedback loops around the DPC ensure constant gain across supply voltages, reduce distortion, and increase immunity to power supply injected noise and distortion. The analog gain is also applied in the Class-D amplifier section of the device. The gain structures are discussed in detail below for both Hardware Control Mode and Software Control Mode.

The switching rate of the amplifier is configurable in both Hardware Control Mode and Software Control Mode. In both cases, the PWM switching frequency is a multiple of the sample rate. This behavior is described in the respective *Hardware Control Mode* and *Software Control Mode* sections below.

8.3.3 Speaker Amplifier Protection Suite

The speaker amplifier in the TAS5760M-Q1 includes a robust suite of error handling and protection features. It is protected against Over-Current, Under-Voltage, Over-Voltage, Over-Temperature, DC, and Clock Errors. The status of these errors is reported via the $\overline{\text{SPK\_FAULT}}$ pin and the appropriate error status register in the I²C Control Port. The error or handling behavior of the device is characterized as being either "Latching" or "Non-Latching" depending on what is required to clear the fault and resume normal operation (that is playback of audio).

For latching errors, the $\overline{\text{SPK\_SD}}$ pin or the $\overline{\text{SPK\_SD}}$ bit in the control port must be toggled in order to clear the error and resume normal operation. If the error is still present when the $\overline{\text{SPK\_SD}}$ pin or bit transitions from LOW back to HIGH, the device will again detect the error and enter into a fault state resulting in the error status bit being set in the control port and the $\overline{\text{SPK\_FAULT}}$ line being pulled LOW. If the error has been cleared (for example, the temperature of the device has decreased below the error threshold) the device will attempt to resume normal operation after the $\overline{\text{SPK\_SD}}$ pin or bit is toggled and the required fault time out period ($T_{\overline{\text{SPK\_FAULT}}}$) has passed. If the error is still present, the device will once again enter a fault state and must be placed into and brought back out of shutdown in order to attempt to clear the error.

Feature Description (continued)

For non-latching errors, the device will automatically resume normal operation (that is playback) once the error has been cleared. The non-latching errors, with the exception of clock errors will not cause the $\overline{\text{SPK\_FAULT}}$ line to be pulled LOW. It is not necessary to toggle the $\overline{\text{SPK\_SD}}$ pin or bit in order to clear the error and resume normal operation for non-latching errors. Table 1 details the types of errors protected by the TAS5760M-Q1's Protection Suite and how each are handled.

8.3.3.1 Speaker Amplifier Fault Notification ($\overline{\text{SPK\_FAULT}}$ Pin)

In both hardware and Software Control mode, the $\overline{\text{SPK\_FAULT}}$ pin of the TAS5760M-Q1 serves as a fault indicator to notify the system that a fault has occurred with the speaker amplifier by being actively pulled LOW. This pin is an open-drain output pin and, unless one is provided internal to the receiver, requires an external pullup to set the net to a known value. The behavior of this pin varies based upon the type of error which has occurred.

In the case of a latching error, the fault line will remain LOW until such time that the TAS5760M-Q1 has resumed normal operation (that is the $\overline{\text{SPK\_SD}}$ pin has been toggled and $T_{\overline{\text{SPK\_FAULT}}}$ has passed).

With the exception of clock errors, non-latching errors will not cause the $\overline{\text{SPK\_FAULT}}$ pin to be pulled LOW. Once a non-latching error has been cleared, normal operation will resume. For clocking errors, the SPK_FAULT line will be pulled LOW, but upon clearing of the clock error normal operation will resume automatically, that is, with no $T_{\overline{\text{SPK\_FAULT}}}$ delay.

One method which can be used to convert a latching error into an auto-recovered, non-latching error is to connect the $\overline{\text{SPK\_FAULT}}$ pin to the $\overline{\text{SPK\_SD}}$ pin. In this way, a fault condition will automatically toggle the $\overline{\text{SPK\_SD}}$ pin when the $\overline{\text{SPK\_FAULT}}$ pin goes LOW and returns HIGH after the $T_{\overline{\text{SPK\_FAULT}}}$ period has passed.

Table 1. Protection Suite Error Handling Summary

ERROR	CAUSE	FAULT TYPE	ERROR IS CLEARED BY:
Overvoltage Error (OVE)	PVDD level rises above that specified by OVE_{RTHRES}(PVDD)	Non-Latching ($\overline{\text{SPK\_FAULT}}$ Pin is not pulled LOW)	PVDD level returning below $OVE_{THRES(PVDD)}$
Undervoltage Error (UVE)	PVDD voltage level drops below that specified by $UVE_{FTHRES(SPK)}$	Non-Latching ($\overline{\text{SPK\_FAULT}}$ Pin is not pulled LOW)	PVDD level returning above $UVE_{THRES(PVDD)}$
Clock Error (CLKE)	One or more of the following errors has occured: 1. Non-Supported MCLK to LRCK and/or SCLK to LRCK Ratio 2. Non-Supported MCLK or LRCK rate 3. MCLK, SCLK, or LRCK has stopped	Non-Latching ($\overline{\text{SPK\_FAULT}}$ Pin is pulled LOW)	Clocks returning to valid state
Overcurrent Error (OCE)	Speaker Amplifier output current has increased above the level specified by OCE_{THRES}	Latching	$T_{\overline{\text{SPK\_FAULT}}}$ has passed **AND** $\overline{\text{SPK\_SD}}$ Pin or Bit Toggle
DC Detect Error (DCE)	DC offset voltage on the speaker amplifier output has increased above the level specified by the DCE_{THRES}	Latching	$T_{\overline{\text{SPK\_FAULT}}}$ has passed **AND** $\overline{\text{SPK\_SD}}$ Pin or Bit Toggle
Overtemperature Error (OTE)	The temperature of the die has increased above the level specified by the OTE_{THRES}	Latching	$T_{\overline{\text{SPK\_FAULT}}}$ has passed **AND** $\overline{\text{SPK\_SD}}$ Pin or Bit Toggle **AND** the temperature of the device has reached a level below that which is dictated by the OTE_{HYST} specification

8.3.3.2 DC Detect Protection

The TAS5760M-Q1 has circuitry which will protect the speakers from DC current which might occur due to an internal amplifier error. The device behavior in response to a DCE event is detailed in the table in the previous section.

A DCE event occurs when the output differential duty-cycle of either channel exceeds 60% for more than 420 msec at the same polarity. The table below shows some examples of the typical DCE Protection threshold for several values of the supply voltage. This feature protects the speaker from large DC currents or AC currents less than 2 Hz.

The minimum output offset voltages required to trigger the DC detect are listed in Table 2. The outputs must remain at or above the voltage listed in the table for more than 420 msec to trigger the DC detect.

Table 2. DC Detect Threshold

PVDD [V]	$\|V_{OS}\|$- OUTPUT OFFSET VOLTAGE [V]
4.5	0.96
6	1.30
12	2.60
18	3.90

8.4 Device Functional Modes

8.4.1 Hardware Control Mode

For systems which do not require the added flexibility of the I²C control port or do not have an I²C host controller, the TAS5760M-Q1 can be used in Hardware Control Mode. In this mode of operation, the device operates in its default configuration and any changes to the device are accomplished via the hardware control pins, described below. The audio performance between Hardware and Software Control mode is identical, however more features and functionality are available when the device is operated in Software Control mode. The behavior of these Hardware Control Mode pins is described in the sections below.

Several static I/O's are present on the TAS5760M-Q1 which are meant to be configured during PCB design and not changed during normal operation. Some examples of these are the GAIN[1:0] and PBTL/SCL pins. These pins are often referred to as being tied or pulled LOW or tied or pulled HIGH. A pin which is tied or pulled LOW has been connected directly to the system ground. The TAS5760M-Q1 is configured such that the most popular use cases for the device (that is BTL mode, 768-kHz switching frequency, and so forth) require the static I/O lines to be tied LOW. This ensures optimum thermal performance as well as BOM reduction.

Device pins that need to be tied or pulled HIGH should be connected to DVDD. For these pins, a pull-up resistor is recommended to limit the slew rate of the voltage which is presented to the pin during power up. Depending on the output impedance of the supply, and the capacitance connected to the DVDD net on the board, slew rates of this node could be high enough to trigger the integrated ESD protection circuitry at high current levels, causing damage to the device. It is not necessary to have a separate pull-up resistor for each static digital I/O pin. Instead, a single resistor can be connected to DVDD and all static I/O lines which are to be tied HIGH can be connected to that pull-up resistor. This connectivity is shown in the Typical Application Circuits. These pullup resistors are not required when the digital I/O pins are driven by a controlled driver, such as a digital control line from a systems processor, as the output buffer in the system processor will ensure a controlled slew rate.

8.4.1.1 Speaker Amplifier Shut Down ($\overline{\text{SPK\_SD}}$ Pin)

In both Hardware and Software Control mode, the $\overline{\text{SPK\_SD}}$ pin is provided to place the speaker amplifier into shutdown. Driving this pin LOW will place the device into shutdown, while pulling it HIGH (to DVDD) will bring the device out of shutdown. This is the lowest power consumption mode that the device can be placed in while the power supplies are up. If the device is placed into shutdown while in normal operation, an audible artifact may occur on the output. To avoid this, the device should first be placed into sleep mode, by pulling the SPK_SLEEP/ADR pin HIGH before pulling the $\overline{\text{SPK\_SD}}$ low.

8.4.1.2 Serial Audio Port in Hardware Control Mode

When used in Hardware Control Mode, the Serial Audio Port (SAP) accepts only I^2S formatted data. Additionally, the device operates in Single-Speed Mode (SSM), which means that supported sample rates, MCLK rates, and SCLK rates are limited to those shown in the table below. Additional clocking options, including higher sample rates, are available when operating the device in Software Control Mode.

Device Functional Modes (continued)

Table 3 details the supported SCLK rates for each of the available sample rate and MCLK rate configurations. For each f_S and MCLK rate, the supported SCLK rates are shown and are represented in multiples of the sample rate, which is written as "x f_S".

Table 3. Supported SCLK Rates in Hardware Control Mode (Single Speed Mode)

		MCLK Rate [x f_S]				
		128	**192**	**256**	**384**	**512**
Sample Rate [kHz]	**12**	N/S	N/S	N/S	N/S	32, 48, 64
	16	N/S	N/S	32, 48, 64	32, 48, 64	32, 48, 64
	24	N/S	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
	32	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
	38	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
	44.1	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
	48	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64

8.4.1.3 Soft Clipper Control (SFT_CLIP Pin)

The TAS5760M-Q1 has a soft clipper that can be used to clip the output voltage level below the supply rail. When this circuit is active, the amplifier operates as if it was powered by a lower supply voltage, and thereby enters into clipping sooner than if the circuit was not active. The result is clipping behavior very similar to that of clipping at the PVDD rail, in contrast to the digital clipper behavior which occurs in the oversampled domain of the digital path. The point at which clipping begins is controlled by a resistor divider from GVDD_REG to ground, which sets the voltage at the SFT_CLIP pin. The precision of the threshold at which clipping occurs is dependent upon the voltage level at the SFT_CLIP pin. Because of this, increasing the precision of the resistors used to create the voltage divider, or using an external reference will increase the precision of the point at which the device enters into clipping. To ensure stability, and soften the edges of the clipping event, a capacitor should be connected from pin SFT_CLIP to ground.

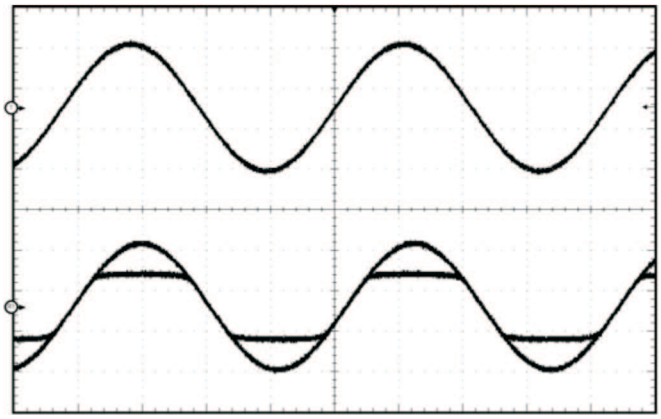


Figure 45. Soft Clipper Example Wave Form

To move the output stage into clipping, the soft clipper circuit limits the duty cycle of the output PWM pulses to a fixed maximum value. After filtering this limit applied to the duty cycle resembles a clipping event at a voltage below that of the PVDD level. The peak voltage level attainable when the soft clipper circuit is active, called V_P in the example below, is approximately 4 times the voltage at the SFT_CLIP pin, noted as V_{SFT_CLIP}. This voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance, as shown in the equation below.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \quad \text{for unclipped power} \tag{2}$$

Where:

R_S is the total series resistance including $R_{DS(on)}$, and output filter resistance.
R_L is the load resistance.
V_P is the peak amplitude achievable when the soft clipper circuit is active (As mentioned previously, V_P = [4 x V_{SFT_CLIP}], provided that [4 x V_{SFT_CLIP}] < PVDD.)
P_{OUT} (10%THD) ≈ 1.25 × P_{OUT} (unclipped)

If the PVDD level is below (4 x V_{SFT_CLIP}) clipping will occur due to clipping at PVDD before the clipping due to the soft clipper circuit becomes active.

Table 4. Soft Clipper Example

PVDD [V]	SFT_CLIP Pin Voltage [V](1)	Resistor to GND [kΩ]	Resistor to GVDD [kΩ]	Output Voltage [V_{rms}]
24	GVDD	(Open)	0	17.90
24	3.3	45	51	12.67
24	2.25	24	51	9.00
12	GVDD	(Open)	0	10.33
12	2.25	24	51	9.00
12	1.5	18	68	6.30

(1) Output voltage measurements are dependent upon gain settings.

8.4.1.4 Speaker Amplifier Switching Frequency Select (FREQ/SDA Pin)

In Hardware Control mode, the PWM switching frequency of the TAS5760M-Q1 is configurable via the FREQ/SDA pin. When connected to the system ground, the pin sets the output switching frequency to 16 × f_S. When connected to DVDD through a pull-up resistor, as shown in the Typical Application Circuits, the pin sets the output switching frequency to 8 × f_S. More switching frequencies are available when the TAS5760M-Q1 is used in Software Control Mode.

8.4.1.5 Parallel Bridge Tied Load Mode Select (PBTL/SCL Pin)

The TAS5760M-Q1 can be configured to drive a single speaker with the two output channels connected in parallel. This mode of operation is called Parallel Bridge Tied Load (PBTL) mode. This mode of operation effectively reduces the output impedance of the amplifier in half, which in turn reduces the power dissipated in the device due to conduction losses through the output FETs. Additionally, since the output channels are working in parallel, it also doubles the amount of current the speaker amplifier can source before hitting the over-current error threshold.

The device can be placed operated in PBTL mode in either Hardware Control Mode or in Software Control Mode, via the I²C Control Port. For instructions on placing the device in PBTL via the I²C Control Port, see *Software Control Mode*.

To place the TAS5760M-Q1 into PBTL Mode when operating in Hardware Control Mode, the PBTL/SCL pin should be pulled HIGH (that is, connected to the DVDD supply through a pull-up resistor). If the device is to operate in BTL mode instead, the PBTL/SCL pin should be pulled LOW, that is connected to the system supply ground. When operated in PBTL mode, the output pins should be connected as shown in the Typical Application Circuit Diagrams.

In PBTL mode, the amplifier selects its source signal from the right channel of the stereo signal presented on the SDIN line of the Serial Audio Port. To select the right channel of the stereo signal, the LRCK can be inverted in the processor that is sending the serial audio data to the TAS5760M-Q1.

8.4.1.6 Speaker Amplifier Sleep Enable (SPK_SLEEP/ADR Pin)

In Hardware Control mode, pulling the SPK_SLEEP/ADR pin HIGH gracefully transitions the switching of the output devices to a non-switching state or "High-Z" state. This mode of operation is similar to mute in that no audio is present on the outputs of the device. However, unlike the 50/50 mute available in the I²C Control Port, sleep mode saves quiescent power dissipation by stopping the speaker amplifier output transitors from switching. This mode of operation saves quiescent current operation but keeps signal path blocks active so that normal operation can resume more quickly than if the device were placed into shutdown. It is recommended to place the device into sleep mode before stopping the audio signal coming in on the SDIN line or before bringing down the power supplies connected to the TAS5760M-Q1 in order to avoid audible artifacts.

8.4.1.7 Speaker Amplifier Gain Select (SPK_GAIN [1:0] Pins)

In Hardware Control Mode, a combination of digital gain and analog gain is used to provide the overall gain of the speaker amplifier. The decode of the two pins "SPK_GAIN1" and "SPK_GAIN0" sets the gain of the speaker amplifier. Additionally, pulling both of the SPK_SPK_GAIN[1:0] pins HIGH places the device into software control mode.

As seen in Figure 46, the audio path of the TAS5760M-Q1 consists of a digital audio input port, a digital audio path, a digital to PWM converter (DPC), a gate driver stage, a Class D power stage, and a feedback loop which feeds the output information back into the DPC block to correct for distortion sensed on the output pins. The total amplifier gain is comprised of digital gain, shown as G_{DIG} in the digital audio path and the analog gain from the input of the analog modulator G_{ANA} to the output of the speaker amplifier power stage.

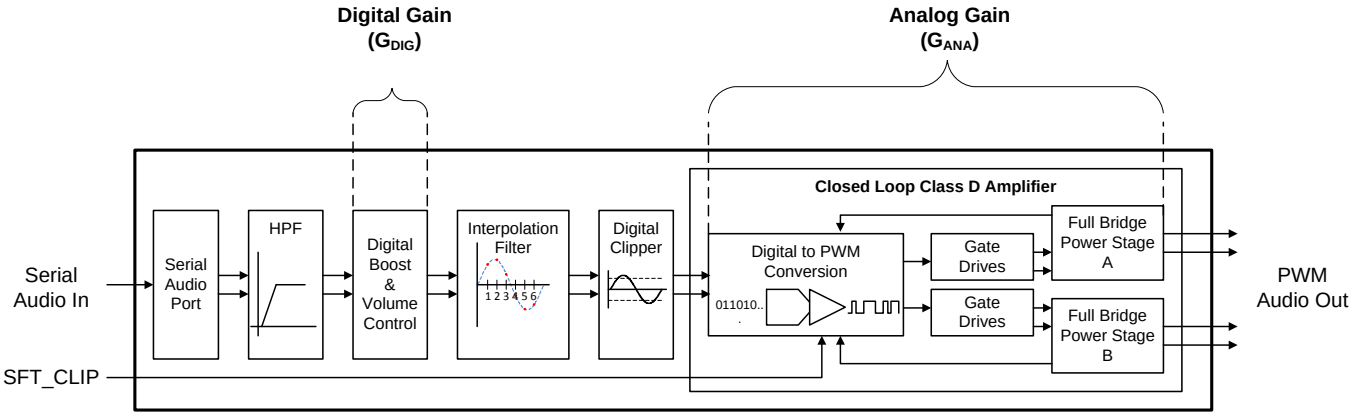


Figure 46. Speaker Amplifier Gain Select (SPK_GAIN [1:0] Pins)

As shown in Figure 46, the first gain stage for the speaker amplifier is present in the digital audio path. It consists of the volume control and the digital boost block. The volume control is set to 0dB by default and, in Hardware Control mode, it does not change. For all settings of the SPK_GAIN[1:0] pins, the digital boost block remains at +6 dB as analog gain block is transitioned through 19.2, 22.6, and 25 dBV.

The gain configurations provided in Hardware Control mode were chosen to align with popular power supply levels found in many consumer electronics and to balance the trade-off between maximum power output before clipping and noise performance. These gain settings ensure that the output signal can be driven into clipping at those popular PVDD levels. If the power level required is lower than that which is possible with the PVDD level, a lower gain setting can be used. Additionally, if clipping at a level lower than the PVDD supply is desired, the digital clipper or soft clipper can be used.

The values of G_{DIG} and G_{ANA} for each of the SPK_GAIN[1:0] settings are shown in the table below. Additionally, the recommended PVDD level for each gain setting, along with the typical unclipped peak to peak output voltage swing for a 0dBFS input signal is provided. The peak voltage levels in the table below should only be used to understand the peak target output voltage swing of the amplifier if it had not been limited by clipping at the PVDD rail.

Table 5. Gain Structure for Hardware Control Mode

PVDD Level	Recommended SPK_GAIN[1:0] Pins Setting	Digital Boost [dB]	A_GAIN [dBV]	V_{Pk} Acheivable Voltage Swing (If output is not clipped at PVDD)
12	00	6	19.2	12.90
19	01	6	22.6	19.08
24	10	6	25	25.15
-	11	(Gain is controlled via I²C Port)		

8.4.1.8 Considerations for Setting the Speaker Amplifier Gain Structure

Configuration of the gain of the amplifier is important to the overall noise and output power performance of the TAS5760M-Q1. Higher gain settings mean that more power can be driven from an amplifier before it becomes voltage limited. Moreover, when output clipping "at the rail" is desired, it becomes important that there be enough voltage gain in the signal path to drive the output signal above the PVDD level in order to "clip" the output signal at the PVDD level in the output stage. Another desirable aspect of higher gain settings is that the dynamic headroom of an amplifier is increased with higher gain settings, which increases the overall dynamic audio quality of the signal being amplified.

With these advantages in mind, it may seem that setting the gain at the highest setting available would be appropriate. However, there are some drawbacks to having a gain that is set arbitrarily high. The first drawback is that a higher gain setting results in increased amplification of any noise that is present in the signal path. If the gain is set too high, and the speaker is sensitive enough, this may result in an audible "hiss" at the speakers when no audio is playing. Another consideration is that the speakers used in the system may not be rated for operation at the power levels which would be possible for the given PVDD supply that is present in the system. For this reason, it may be necessary to limit the voltage swing of the amplifier via a lower gain setting to reduce the voltage presented, and therefore, the power delivered, to the speaker.

8.4.1.8.1 Recommendations for Setting the Speaker Amplifier Gain Structure in Hardware Control Mode

1. Determine the maximum power target and the speaker impedance which is required for the application.
2. Calculate the required output voltage swing for the given speaker impedance which will deliver the target maximum power.
3. Chose the lowest gain setting via the SPK_GAIN[1:0] pins that produces an output voltage swing higher than the required output voltage swing for the target maximum power.

NOTE

A higher gain setting can be used, provided the noise performance is acceptable and the power delivered to the speaker remains within the safe operating area (SOA) of the speaker, using the soft clipper if necessary to set the clip point within the SOA of the speaker.

4. Characterize the clipping behavior of the system at the rated power.
   - If the system does not produce the target power before clipping that is required, increase the gain setting.
   - If the system meets the power requirements, but clipping is preferred at the rated power, use the soft clipper to set the clip point
   - If the system makes more power than is required but the noise performance is too high, consider reducing the gain.
5. Repeat Step 4 until the optimum balance of power, noise, and clipping behavior is achieved.

8.4.2 Software Control Mode

The TAS5760M-Q1 can be used in Hardware Control Mode or Software Control Mode. In order to place the device in software control mode, the two gain pins (GAIN[1:0]) should be pulled HIGH. When this is done, the PBTL/SCL and FREQ/SDA pins are allocated to serve as the clock and data lines for the I²C Control Port.

8.4.2.1 Speaker Amplifier Shut Down ($\overline{\text{SPK\_SD}}$ Pin)

In both hardware and Software Control mode, the $\overline{\text{SPK\_SD}}$ pin is provided to place the speaker amplifier into shutdown. Driving this pin LOW will place the device into shutdown, while driving it HIGH (DVDD) will bring the device out of shutdown. This is the lowest power consumption mode that the device can be placed in while the power supplies are up. If the device is placed into shutdown while in normal operation, an audible artifact may occur on the output. To avoid this, the device should first be placed into sleep mode, by pulling the SPK_SLEEP/ADR pin HIGH before pulling the $\overline{\text{SPK\_SD}}$ low.

8.4.2.2 Serial Audio Port Controls

In Software Control mode, additional digital audio data formats and clock rates are made available via the I²C control port. With these controls, the audio format can be set to left justified, right justified, or I²S formatted data.

8.4.2.2.1 Serial Audio Port (SAP) Clocking

When used in Software Control mode, the device can be placed into double speed mode to support higher sample rates, such as 88.2 kHz and 96 kHz. The tables below detail the supported SCLK rates for each of the available sample rate and MCLK rate configurations. For each f_S and MCLK Rate the support SCLK rates are shown and are represented in multiples of the sample rate, which is written as "x f_S".

Table 6. Supported SCLK Rates in Single-Speed Mode

		MCLK Rate [x f_S]				
		128	**192**	**256**	**384**	**512**
Sample Rate [kHz]	**12**	N/S	N/S	N/S	N/S	32, 48, 64
	16	N/S	N/S	32, 48, 64	32, 48, 64	32, 48, 64
	24	N/S	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
	32	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
	38	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
	44.1	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
	48	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64

Table 7. Supported SCLK Rates in Double-Speed Mode

		MCLK Rate [x f_S]		
		128	**192**	**256**
Sample Rate [kHz]	**88.2**	32, 48, 64	32, 48, 64	32, 48, 64
	96	32, 48, 64	32, 48, 64	32, 48, 64

8.4.2.3 Parallel Bridge Tied Load Mode via Software Control

The TAS5760M-Q1 can be configured to drive a single speaker with the two output channels connected in parallel. This mode of operation is called Parallel Bridge Tied Load (PBTL) mode. This mode of operation effectively reduces the on resistance of the amplifier in half, which in turn reduces the power dissipated in the device due to conduction losses through the output FETs. Additionally, since the output channels are working in parallel, it also doubles the amount of current the speaker amplifier can source before hitting the over-current error threshold.

It should be noted that the device can be placed operated in PBTL mode in either Hardware Control Mode or in Software Control Mode, via the I²C Control Port. For instructions on placing the device in PBTL via the PBTL/SCL Pin, see *Hardware Control Mode*.

To place the TAS5760M-Q1 into PBTL Mode when operating in Software Control Mode, the Bit 7 of the Analog Control Register (0x06) should be set in the control port. This bit is cleared by default to configure the device for BTL mode operation. An additional control available in software mode control is PBTL Channel Select, which selects which of the two channels presented on the SDIN line will be used for the input signal for the amplifier. This is found at Bit 1 of the Analog Control Register (0x06).

8.4.2.4 Speaker Amplifier Gain Structure

As shown in Figure 47, the audio path of the TAS5760M-Q1 consists of a digital audio input port, a digital audio path, a digital to analog converter, an analog modulator, a gate driver stage, a Class D power stage, and a feedback loop which feeds the output information back into the analog modulator to correct for distortion sensed on the output pins. The total amplifier gain is comprised of digital gain, shown as G_{DIG} in the digital audio path and the analog gain from the input of the analog modulator G_{ANA} to the output of the speaker amplifier power stage.

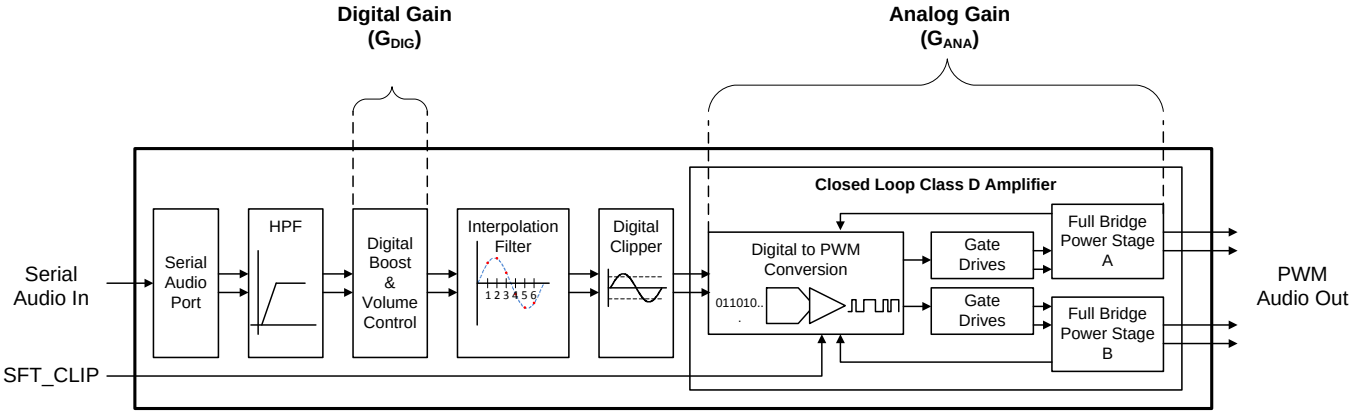


Figure 47. Speaker Amplifier Gain Structure

8.4.2.4.1 Speaker Amplifier Gain in Software Control Mode

The analog and digital gain are configured directly when operating in Software Control mode. It is important to note that the digital boost block is separate from the volume control. The digital boost block should be set before the speaker amplifier is brought out of mute and not changed during normal operation. In most cases, the digital boost can be left in its default configuration, and no further adjustment is necessary. As mentioned previously, the analog gain is directly set via the I²C control port in software control mode.

8.4.2.4.2 Considerations for Setting the Speaker Amplifier Gain Structure

Configuration of the gain of the amplifier is important to the overall noise and output power performance of the TAS5760M-Q1. Higher gain settings mean that more power can be driven from an amplifier before it becomes voltage limited. Moreover, when output clipping "at the rail" is desired, it becomes important that there be enough voltage gain in the signal path to drive the output signal above the PVDD level in order to "clip" the output signal at the PVDD level in the output stage. Another desirable aspect of higher gain settings is that the dynamic headroom of an amplifier is increased with higher gain settings, which increases the overall dynamic audio quality of the signal being amplified.

With these advantages in mind, it may seem that setting the gain at the highest setting available would be appropriate. However, there are some drawbacks to having a gain that is set arbitrarily high. The first drawback is that a higher gain setting results in increased amplification of any noise that is present in the signal path. If the gain is set too high, and the speaker is sensitive enough, this may result in an audible "hiss" at the speakers when no audio is playing. Another consideration is that the speakers used in the system may not be rated for operation at the power levels which would be possible for the given PVDD supply that is present in the system. For this reason it may be necessary to limit the voltage swing of the amplifier via a lower gain setting to reduce the voltage presented, and therefore the power delivered, to the speaker.

8.4.2.4.3 Recommendations for Setting the Speaker Amplifier Gain Structure in Software Control Mode

1. Determine the maximum power target and the speaker impedance which is required for the application.
2. Calculate the required output voltage swing for the given speaker impedance which will deliver the target maximum power.
3. Chose the lowest analog gain setting via the A_GAIN[3:2] bits in the control port which will produce an output voltage swing higher than the required output voltage swing for the target maximum power.

NOTE

A higher gain setting can be used, provided the noise performance is acceptable and the power delivered to the speaker remains within the safe operating area (SOA) of the speaker, using the soft clipper if necessary to set the clip point within the SOA of the speaker.

4. Characterize the clipping behavior of the system at the rated power.
   - If the system does not produce the target power before clipping that is required, increase the analog gain.
   - If the system meets the power requirements, but clipping is preferred at the rated power, use the soft clipper or the digital clipper to set the clip point
   - If the system makes more power than is required but the noise performance is too high, consider reducing the analog gain.
5. Repeat Step 4 until the optimum balance of power, noise, and clipping behavior is achieved.

8.4.2.5 I²C Software Control Port

The TAS5760M-Q1 includes an I²C control port for increased flexibility and extended feature set.

8.4.2.5.1 Setting the I²C Device Address

Each device on the I²C bus has a unique address that allows it to appropriately transmit and receive data to and from the I²C master controller. As part of the I²C protocol, the I²C master broadcast an 8-bit word on the bus that contains a 7-bit device address in the upper 7 bits and a read or write bit for the LSB. The TAS5760M-Q1 has a configurable I²C address. The SPK_SLEEP/ADR can be used to set the device address of the TAS5760M-Q1. In Software Control mode, the seven bit I²C device address is configured as "110110x[$^{R}/_{W}$]", where "x" corresponds to the state of the SPK_SLEEP/ADR pin at first power up sequence of the device. Upon application of the power supplies, the device latches in the value of the SPK_SLEEP/ADR pin for use in determining the I²C address of the device. If the SPK_SLEEP/ADR pin is tied LOW at power up (that is connected to the system ground), the device address will be set to 1101100[$^{R}/_{W}$]. If it is pulled HIGH (that is connected to the DVDD supply), the address will be set to 1101101[$^{R}/_{W}$] at power up.

8.4.2.5.2 General Operation of the I²C Control Port

The TAS5760M-Q1 device has a bidirectional I²C interface that is compatible with the Inter IC (I²C) bus protocol and supports both 100-kHz and 400-kHz data transfer rates. This is a slave-only device that does not support a multimaster bus environment or wait-state insertion. The control interface is used to program the registers of the device and to read device status.

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially, one bit at a time. The address and data can be transferred in byte (8-bit) format, with the most significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a START condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is HIGH to indicate START and STOP conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 48. The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The TAS5760M-Q1 holds SDA LOW during the acknowledge clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence. All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pullup resistor must be used for the SDA and SCL signals to set the HIGH level for the bus.

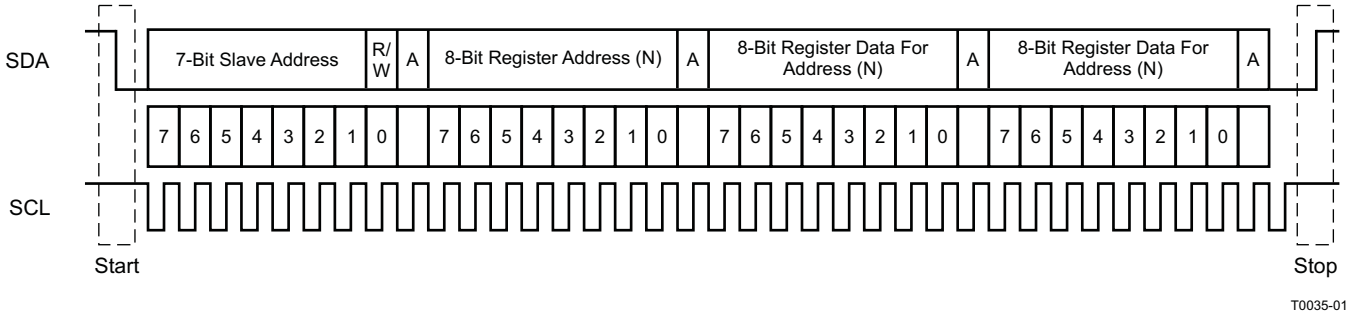


Figure 48. Typical I²C Sequence

There is no limit on the number of bytes that can be transmitted between START and STOP conditions. When the last word transfers, the master generates a STOP condition to release the bus. A generic data transfer sequence is shown in Figure 48.

8.4.2.5.3 Writing to the I²C Control Port

As shown in Figure 49, a single-byte data-write transfer begins with the master device transmitting a START condition followed by the I²C and the read/write bit. The read/write bit determines the direction of the data transfer. For a data-write transfer, the read/write bit is a 0. After receiving the correct I²C and the read/write bit, the TAS5760M-Q1 responds with an acknowledge bit. Next, the master transmits the address byte corresponding to the TAS5760M-Q1 register being accessed. After receiving the address byte, the TAS5760M-Q1 again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TAS5760M-Q1 again responds with an acknowledge bit. Finally, the master device transmits a STOP condition to complete the single-byte data-write transfer.

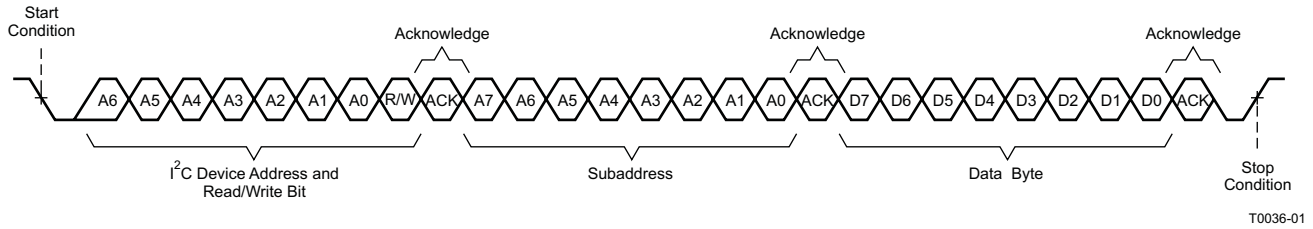


Figure 49. Write Transfer

8.4.2.5.4 Reading from the I²C Control Port

As shown in Figure 50, a data-read transfer begins with the master device transmitting a START condition, followed by the I²C device address and the read/write bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal register to be read. As a result, the read/write bit becomes a 0. After receiving the TAS5760M-Q1 address and the read/write bit, TAS5760M-Q1 responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another START condition followed by the TAS5760M-Q1 address and the read/write bit again. This time, the read/write bit becomes a 1, indicating a read transfer. After receiving the address and the read/write bit, the TAS5760M-Q1 again responds with an acknowledge bit. Next, the TAS5760M-Q1 transmits the data byte from the register being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a STOP condition to complete the data-read transfer.

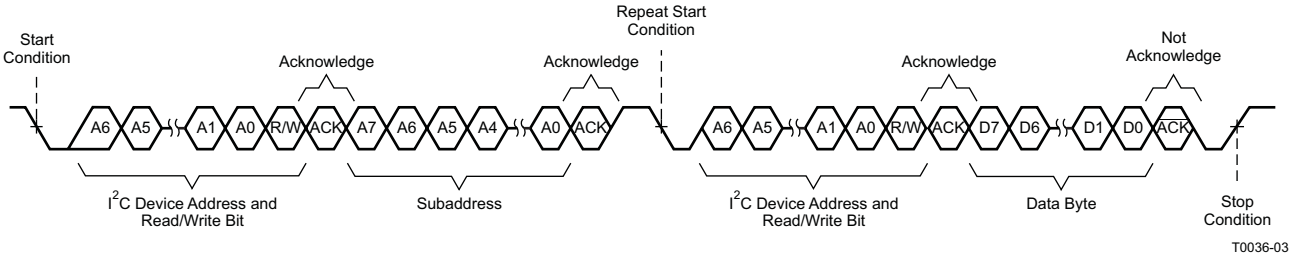


Figure 50. Read Transfer

8.5 Register Maps

8.5.1 Control Port Registers - Quick Reference

Table 8. Control Port Quick Reference Table

Adr. (Dec)	Adr. (Hex)	Register Name	Default (Binary)								Default (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
0	0	Device Identification	Device Identification								0x00
			0	0	0	0	0	0	0	0	
1	1	Power Control	DigClipLev[19:14]						SPK_SLEEP	$\overline{\text{SPK\_SD}}$	0xFD
			1	1	1	1	1	1	0	1	
2	2	Digital Control	HPF Bypass	Reserved	Digital Boost		$\overline{\text{SS}}$/DS	Serial Audio Input Format			0x14
			0	0	0	1	0	1	0	0	
3	3	Volume Control Configuration	Fade	Reserved	Reserved	Reserved	Reserved	Reserved	Mute R	Mute L	0x80
			1	0	0	0	0	0	0	0	
4	4	Left Channel Volume Control	Volume Left								0xCF
			1	1	0	0	1	1	1	1	
5	5	Right Channel Volume Control	Volume Right								0xCF
			1	1	0	0	1	1	1	1	
6	6	Analog Control	PBTL Enable	PWM Rate Select			A_GAIN		PBTL Ch Sel	Reserved	0x51
			0	1	0	1	0	0	0	1	
7	7	Reserved	Reserved	Reserved	Reserved		Reserved	Reserved	Reserved	Reserved	0x00
			0	0	0	0	0	0	0	0	
8	8	Fault Configuration and Error Status	Reserved		OCE Thres		CLKE	OCE	DCE	OTE	0x00
			0	0	0	0	0	0	0	0	
9	9	Reserved	-	-	-	-	-	-	-	-	-
...		Reserved	-	-	-	-	-	-	-	-	-
15	F	Reserved	-	-	-	-	-	-	-	-	-
16	10	Digital Clipper 2	DigClipLev[13:6]								0xFF
			1	1	1	1	1	1	1	1	
17	11	Digital Clipper 1	DigClipLev[5:0]								0xFC
			1	1	1	1	1	1	0	0	

8.5.2 Control Port Registers - Detailed Description

8.5.2.1 Device Identification Register (0x00)

Figure 51. Device Identification Register

7	6	5	4	3	2	1	0
Device Identification							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. Device Identification Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Device Identification	R	0	Device Identification - TAS5760Mx

8.5.2.2 Power Control Register (0x01)

Figure 52. Power Control Register

7	6	5	4	3	2	1	0
DigClipLev[19:14]						SPK_SLEEP	$\overline{\text{SPK\_SD}}$
R/W						R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. Power Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	DigClipLev[19:14]	R/W	1	The digital clipper is decoded from 3 registers- DigClipLev[19:14], DigClipLev[13:6], and DigClipLev[5:0]. DigClipLev[19:14], shown here, represents the upper 6 bits of the total of 20 bits that are used to set the Digital Clipping Threshold.
1	SPK_SLEEP	R/W	0	Sleep Mode 0: Device is not in sleep mode. 1: Device is placed in sleep mode (In this mode, the power stage is disabled to reduce quiescent power consumption over a 50/50 duty cycle mute, while low-voltage blocks remain on standby. This reduces the time required to resume playback when compared with entering and exiting full shut down.).
0	$\overline{\text{SPK\_SD}}$	R/W	1	Speaker Shutdown 0: Speaker amplifier is shut down (This is the lowest power mode available when the device is connected to power supplies. In this mode, circuitry in both the DVDD and PVDD domain are powered down to minimize power consumption.). 1: Speaker amplifier is not shut down.

8.5.2.3 Digital Control Register (0x02)

Figure 53. Digital Control Register

7	6	5	4	3	2	1	0
HPF Bypass	Reserved	Digital Boost		SS/DS	Serial Audio Input Format		
R/W	R	R/W		R/W	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. Digital Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HPF Bypass	R/W	0	High-Pass Filter Bypass 0: The internal high-pass filter in the digital path is not bypassed. 1: The internal high-pass filter in the digital path is bypassed.
6	Reserved	R	0	This control is reserved and must not be changed from its default setting.

Table 11. Digital Control Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	Digital Boost	R/W	01	Digital Boost 00: +0 dB is added to the signal in the digital path. 01: +6 dB is added to the signal in the digital path. (Default) 10: +12 dB is added to the signal in the digital path. 11: +18 dB is added to the signal in the digital path.
3	SS/DS	R/W	0	Single Speed / Double Speed Mode Select 0: Serial Audio Port will accept single speed sample rates (that is 32 kHz, 44.1 kHz, 48 kHz) 1: Serial Audio Port will accept double speed sample rates (that is 88.2 kHz, 96 kHz)
2:0	Serial Audio Input Format	R/W	100	Serial Audio Input Format 000: Serial Audio Input Format is 24 Bits, Right Justified 001: Serial Audio Input Format is 20 Bits, Right Justified 010: Serial Audio Input Format is 18 Bits, Right Justified 011: Serial Audio Input Format is 16 Bits, Right Justified 100: Serial Audio Input Format is I²S (Default) 101: Serial Audio Input Format is 16-24 Bits, Left Justified Settings above 101 are reserved and must not be used

8.5.2.4 Volume Control Configuration Register (0x03)

Figure 54. Volume Control Configuration Register

7	6	5	4	3	2	1	0
Fade	Reserved					Mute R	Mute L
R/W	R					R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. Volume Control Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Fade	R/W	1	Volume Fade Enable 0: Volume fading is disabled. 1: Volume fading is enabled.
6:2	Reserved	R	0	This control is reserved and must not be changed from its default setting.
1	Mute R	R/W	0	Mute Right Channel 0: The right channel is not muted 1: The right channel is muted (In software mute, most analog and digital blocks remain active and the speaker amplifier outputs transition to a 50/50 duty cycle.)
0	Mute L	R/W	0	Mute Left Channel 0: The left channel is not muted 1: The left channel is muted (In software mute, most analog and digital blocks remain active and the speaker amplifier outputs transition to a 50/50 duty cycle.)

8.5.2.5 Left Channel Volume Control Register (0x04)

Figure 55. Left Channel Volume Control Register

7	6	5	4	3	2	1	0
Volume Left							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. Left Channel Volume Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Volume Left	R/W	11001111	Left Channel Volume Control 11111111: Channel Volume is +24 dB 11111110: Channel Volume is +23.5 dB 11111101: Channel Volume is +23.0 dB ... 11001111: Channel Volume is 0 dB (Default) ... 00000111: Channel Volume is -100 dB Any setting less than 00000111 places the channel in Mute

8.5.2.6 Right Channel Volume Control Register (0x05)

Figure 56. Right Channel Volume Control Register

7	6	5	4	3	2	1	0
Volume Right							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. Right Channel Volume Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Volume Right	R/W	11001111	Right Channel Volume Control 11111111: Channel Volume is +24 dB 11111110: Channel Volume is +23.5 dB 11111101: Channel Volume is +23.0 dB ... 11001111: Channel Volume is 0 dB (Default) ... 00000111: Channel Volume is -100 dB Any setting less than 00000111 places the channel in Mute

8.5.2.7 Analog Control Register (0x06)

Figure 57. Analog Control Register

7	6	5	4	3	2	1	0
PBTL Enable	PWM Rate Select			A_GAIN		PBTL Ch Sel	Reserved
R/W	R/W			R/W		R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. Analog Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PBTL Enable	R/W	0	PBTL Enable 0: Device is placed in BTL mode. 1: Device is placed in PBTL mode.
6:4	PWM Rate Select	R/W	101	PWM Rate Select 000: Output switching rate of the Speaker Amplifier is 6 * LRCK. 001: Output switching rate of the Speaker Amplifier is 8 * LRCK. 010: Output switching rate of the Speaker Amplifier is 10 * LRCK. 011: Output switching rate of the Speaker Amplifier is 12 * LRCK. 100: Output switching rate of the Speaker Amplifier is 14 * LRCK. 101: Output switching rate of the Speaker Amplifier is 16 * LRCK. (Default) 110: Output switching rate of the Speaker Amplifier is 20 * LRCK. 111: Output switching rate of the Speaker Amplifier is 24 * LRCK. Note that all rates listed above are valid for single speed mode. For double speed mode, switching frequency is half of that represented above.
3:2	A_GAIN	R/W	00	00: Analog Gain Setting is 19.2 dBV.(Default) 01: Analog Gain Setting is 22.6 dBV. 10: Analog Gain Setting is 25 dBV. 11: This setting is reserved and must not be used.
1	PBTL Ch Sel	R/W	0	Channel Selection for PBTL Mode 0: When placed in PBTL mode, the audio information from the Right channel of the serial audio input stream is used by the speaker amplifier. 1: When placed in PBTL mode, the audio information from the Left channel of the serial audio input stream is used by the speaker amplifier.
0	Reserved	R/W	1	This control is reserved and must not be changed from its default setting.

8.5.2.8 Reserved Register (0x07)

The controls in this section of the control port are reserved and must not be used.

8.5.2.9 Fault Configuration and Error Status Register (0x08)

Figure 58. Fault Configuration and Error Status Register

7	6	5	4	3	2	1	0
Reserved		OCE Thres		CLKE	OCE	DCE	OTE
R		R/W		R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. Fault Configuration and Error Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	Reserved	R	0	This control is reserved and must not be changed from its default setting.
5:4	OCE Thres	R/W	00	OCE Threshold 00: Threshold is set to the default level specified in the electrical characteristics table. (Default) 01: Threshold is reduced to 75% of the evel specified in the electrical characteristics table. 10: Threshold is reduced to 50% of the evel specified in the electrical characteristics table. 11: Threshold is reduced to 25% of the evel specified in the electrical characteristics table.
3	CLKE	R	0	Clock Error Status 0: Clocks are valid and no error is currently detected. 1: A clock error is occuring (This error is non-latching, so intermittent clock errors will be cleared when clocks re-enter valid state and the device will resume normal operation automatically. This bit will likewise be cleared once normal operation resumes.).
2	OCE	R	0	Over Current Error Status 0: The output current levels of the speaker amplifier outputs are below the OCE threshold. 1: The DC offset level of the outputs has exceeded the OCE threshold, causing an error (This is a latching error and $\overline{\text{SPK\_SD}}$ must be toggled after an OCE event for the device to resume normal operation. This bit will remain HIGH until $\overline{\text{SPK\_SD}}$ is toggled.).
1	DCE	R	0	Output DC Error Status 0: The DC offset level of the speaker amplifier outputs are below the DCE threshold. 1: The DC offset level of the speaker amplifier outputs has exceeded the DCE threshold, causing an error (This is a latching error and $\overline{\text{SPK\_SD}}$ must be toggled after an DCE event for the device to resume normal operation. This bit will remain HIGH until $\overline{\text{SPK\_SD}}$ is toggled.).
0	OTE	R	0	Over-Temperature Error Status 0: The temperature of the die is below the OTE threshold. 1: The temperature of the die has exceeded the level specified in the electrical characteristics table. (This is a latching error and $\overline{\text{SPK\_SD}}$ must be toggled for the device to resume normal operation. This bit will remain HIGH until $\overline{\text{SPK\_SD}}$ is toggled.).

8.5.2.10 Reserved Controls (9 / 0x09) - (15 / 0x0F)

The controls in this section of the control port are reserved and must not be used.

8.5.2.11 Digital Clipper Control 2 Register (0x10)

Figure 59. Digital Clipper Control 2 Register

7	6	5	4	3	2	1	0
DigClipLev[13:6]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. Digital Clipper Control 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DigClipLev[13:6]	R/W	1	The digital clipper is decoded from 3 registers- DigClipLev[19:14], DigClipLev[13:6], and DigClipLev[5:0]. DigClipLev[13:6], shown here, represents the [13:6] bits of the total of 20 bits that are used to set the Digital Clipping Threshold.

8.5.2.12 Digital Clipper Control 1 Register (0x11)

Figure 60. Digital Clipper Control 1 Register

7	6	5	4	3	2	1	0
DigClipLev[5:0]						Reserved	
R/W						R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. Digital Clipper Control 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	DigClipLev[5:0]	R/W	1	The digital clipper is decoded from 3 registers- DigClipLev[19:14], DigClipLev[13:6], and DigClipLev[5:0]. DigClipLev[5:0], shown here, represents the [5:0] bits of the total of 20 bits that are used to set the Digital Clipping Threshold.
1:0	Reserved	R/W	0	These controls are reserved and should not be changed from there default values.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

These typical connection diagrams highlight the required external components and system level connections for proper operation of the device in several popular use cases.

Each of these configurations can be realized using the Evaluation Modules (EVMs) for the device. These flexible modules allow full evaluation of the device in all available modes of operation. Additionally, some of the application circuits are available as reference designs and can be found on the TI website. Also see the TAS5760M-Q1's product page for information on ordering the EVM. Not all configurations are available as reference designs; however, any design variation can be supported by TI through schematic and layout reviews. Visit support.ti.com for additional design assistance. Also, join the audio amplifier discussion forum at http://e2e.ti.com.

9.2 Typical Applications

These application circuits detail the recommended component selection and board configurations for the TAS5760M-Q1 device. Note that in Software Control mode, the clipping point of the amplifier and thus the *rated power* of the end equipment can be set using the digital clipper if desired. Additionally, if the sonic signature of the soft clipper is preferred, it can be used in addition to or in lieu of the digital clipper. The software control application circuit detailed in this section shows the soft clipper in its bypassed state, which results in a lower BOM count than when using the soft clipper. The trade-off between the sonic characteristics of the clipping events in the amplifier and BOM minimization can be chosen based upon the design goals related to the end product.

9.2.1 Stereo BTL Using Software Control

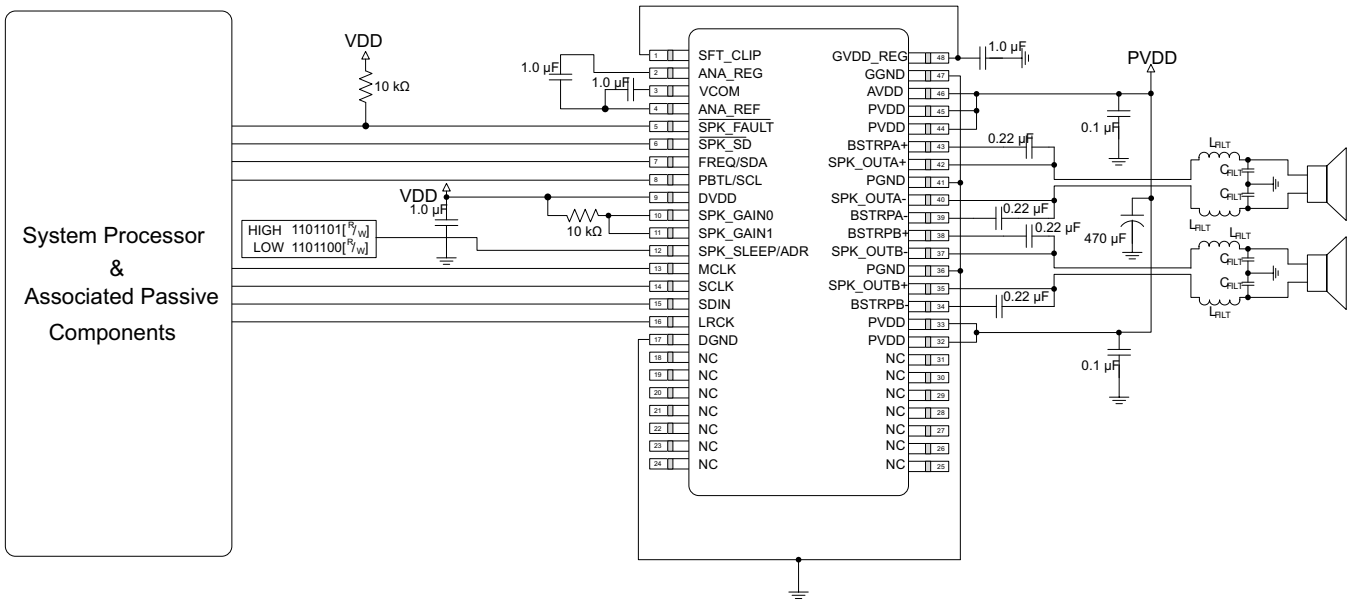


Figure 61. Stereo BTL Using Software Control

9.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 19 as the input parameters.

Typical Applications (continued)

Table 19. Design Parameters

PARAMETER	EXAMPLE
Low Power Supply	3.3 V
High Power Supply	5 V to 24 V
Host Processor	I2S Compliant Master
	I2C Compliant Master
	GPIO Control
Output Filters	Inductor-Capacitor Low Pass Filter
Speakers	4 Ω to 8 Ω

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Startup Procedures- Software Control Mode

1. Configure all digital I/O pins as required by the application using PCB connections (that is SPK_GAIN[1:0] = 11, ADR, etc.)
2. Start with $\overline{\text{SPK\_SD}}$ Pin = LOW
3. Bring up power supplies (it does not matter if PVDD/AVDD or DVDD comes up first, provided the device is held in shutdown.)
4. Once power supplies are stable, start MCLK, SCLK, LRCK
5. Configure the device via the control port in the manner required by the use case, making sure to mute the device via the control port
6. Once power supplies and clocks are stable and the control port has been programmed, bring $\overline{\text{SPK\_SD}}$ HIGH
7. Unmute the device via the control port
8. The device is now in normal operation

NOTE

Control port register changes should only occur when the device is placed into shutdown. This can be accomplished either by pulling the $\overline{\text{SPK\_SD}}$ pin LOW or clearing the $\overline{\text{SPK\_SD}}$ bit in the control port.

9.2.1.2.2 Shutdown Procedures- Software Control Mode

1. The device is in normal operation
2. Mute via the control port
3. Pull $\overline{\text{SPK\_SD}}$ LOW
4. The clocks can now be stopped and the power supplies brought down
5. The device is now fully shutdown and powered off

NOTE

Any control port register changes excluding volume control changes should only occur when the device is placed into shutdown. This can be accomplished either by pulling the $\overline{\text{SPK\_SD}}$ pin LOW or clearing the $\overline{\text{SPK\_SD}}$ bit in the control port.

9.2.1.2.3 Component Selection and Hardware Connections

Figure 61 details the typical connections required for proper operation of the device. It is with this list of components that the device was simulated, tested, and characterized. Deviation from this typical application circuit unless recommended by this document may produce unwanted results, which could range from degradation of audio performance to destructive failure of the device.

9.2.1.2.3.1 I²C Pullup Resistors

It is important to note that when the device is operated in Software Control Mode, the customary pullup resistors are required on the SCL and SDA signal lines. They are not shown in the Typical Application Circuits, because they are shared by all of the devices on the I²C bus and are considered to be part of the associated passive components for the System Processor. These resistor values should be chosen per the guidance provided in the I²C Specification.

9.2.1.2.3.2 Digital I/O Connectivity

The digital I/O lines of the TAS5760M-Q1 are described in previous sections. As discussed, whenever a static digital pin (that is a pin that is hardwired to be HIGH or LOW) is required to be pulled HIGH, it should be connected to DVDD through a pullup resistor to control the slew rate of the voltage presented to the digital I/O pins. It is not, however, necessary to have a separate pullup resistor for each static digital I/O line. Instead, a single resistor can be used to tie all static I/O lines HIGH to reduce BOM count. For instance, if Software Control Mode is desired both the GAIN[1:0] and the PBTL/SCL pins can both be pulled HIGH through a single pullup resistor.

9.2.1.2.4 Recommended Startup and Shutdown Procedures

The start up and shutdown procedures for both Hardware Control Mode and Software Control Mode are shown below.

9.2.1.3 Application Curves

Table 20. Relevant Performance Plots

PLOT TITLE	PLOT NUMBER
Figure 1. Output Power vs PVDD	G001
Figure 2. THD+N vs Frequency With PVDD = 12 V, POSPK = 1 W	G024
Figure 3. THD+N vs Frequency With PVDD = 24 V, POSPK = 1 W	G025
Figure 5. THD+N vs Output Power With PVDD = 12 V, Both Channels Driven	G027
Figure 6. THD+N vs Output Power With PVDD = 18 V, Both Channels Driven	G028
Figure 7. THD+N vs Output Power With PVDD = 24 V, Both Channels Driven	G029
Figure 8. Efficiency vs Output Power	G030
Figure 9. Crosstalk vs Frequency	G031
Figure 10. PVDD PSRR vs Frequency	G019
Figure 11. DVDD PSRR vs Frequency	G020
Figure 12. Idle Current Draw vs PVDD (Filterless)	G042
Figure 13. Idle Current Draw vs PVDD (With LC Filter as Shown on the EVM)	G023
Figure 14. Shutdown Current Draw vs PVDD (Filterless)	G022
Figure 15. Output Power vs PVDD	G039
Figure 16. THD+N vs Frequency With PVDD = 12 V, P_{OSPK} = 1 W	G002
Figure 17. THD+N vs Frequency With PVDD = 24 V, P_{OSPK} = 1 W	G003
Figure 19. THD+N vs Output Power With PVDD = 12 V, Both Channels Driven	G008
Figure 20. THD+N vs Output Power With PVDD = 18 V, Both Channels Driven	G009
Figure 21. THD+N vs Output Power With PVDD = 24 V, Both Channels Driven	G010
Figure 22. Efficiency vs Output Power	G014
Figure 23. Crosstalk vs Frequency	G018
Figure 24. PVDD PSRR vs Frequency	G019
Figure 25. Idle Current Draw vs PVDD (Filterless)	G045
Figure 26. Idle Current Draw vs PVDD (With LC Filter as Shown on EVM)	G044
Figure 27. Shutdown Current Draw vs PVDD (Filterless)	G022

9.2.2 Stereo BTL Using Hardware Control

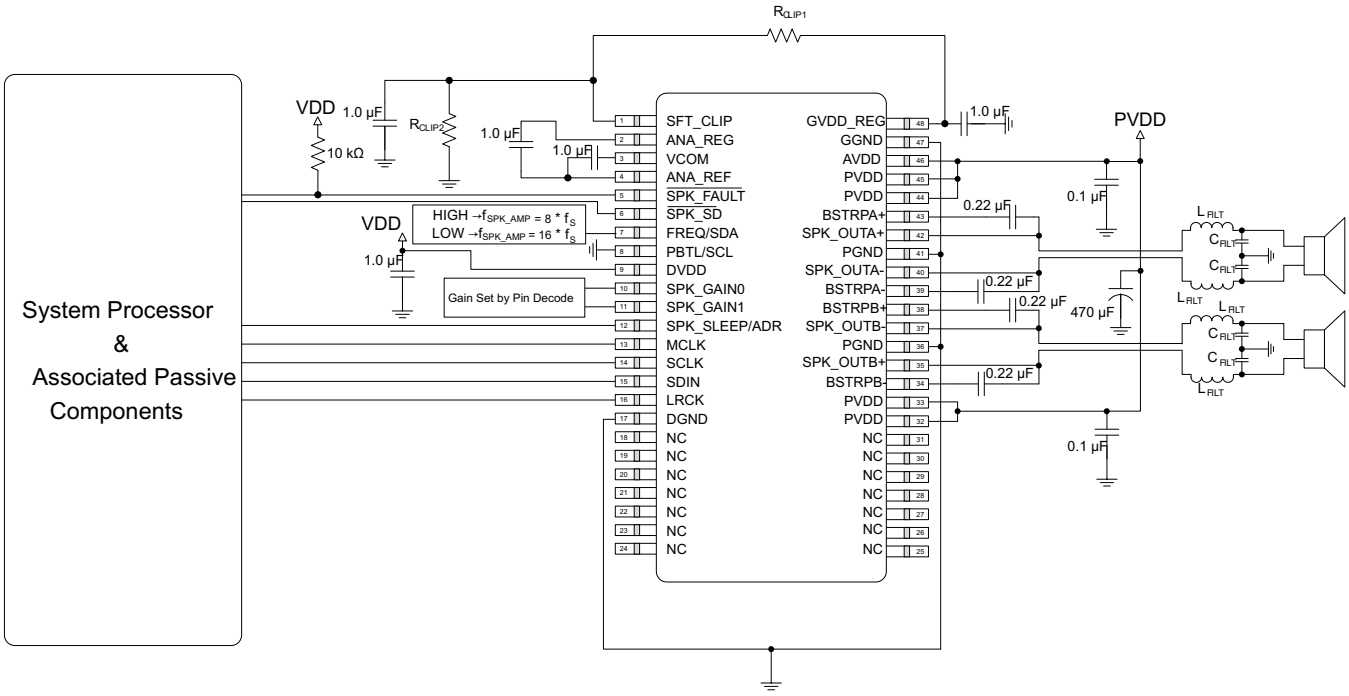


Figure 62. Stereo BTL Using Hardware Control

9.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 21 as the input parameters.

Table 21. Design Parameters

PARAMETER	EXAMPLE
Low Power Supply	3.3 V
High Power Supply	5 V to 24 V
Host Processor	I2S Compliant Master
	GPIO Control
Output Filters	Inductor-Capacitor Low Pass Filter
Speakers	4 Ω to 8 Ω

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Startup Procedures- Hardware Control Mode

1. Configure all hardware pins as required by the application using PCB connections (that is PBTL, FREQ, GAIN, etc.)
2. Start with $\overline{\text{SPK\_SD}}$ pin pulled LOW and SPK_SLEEP/ADR pin pulled HIGH
3. Bring up power supplies (it does not matter if PVDD/AVDD or DVDD comes up first, provided the device is held in shutdown.)
4. Once power supplies are stable, start MCLK, SCLK, LRCK
5. Once power supplies and clocks are stable and all hardware control pins have been configured, bring $\overline{\text{SPK\_SD}}$ HIGH
6. Once the device is out of shutdown mode, bring SPK_SLEEP/ADR LOW
7. The device is now in normal operation

9.2.2.2.2 Shutdown Procedures- Hardware Control Mode

1. The device is in normal operation
2. Pull SPK_SLEEP/ADR HIGH
3. Pull $\overline{\text{SPK\_SD}}$ LOW
4. The clocks can now be stopped and the power supplies brought down
5. The device is now fully shutdown and powered off

9.2.2.2.3 Digital I/O Connectivity

The digital I/O lines of the TAS5760M-Q1 are described in previous sections. As discussed, whenever a static digital pin (that is a pin that is hardwired to be HIGH or LOW) is required to be pulled HIGH, it should be connected to DVDD through a pullup resistor in order to control the slew rate of the voltage presented to the digital I/O pins. It is not, however, necessary to have a separate pullup resistor for each static digital I/O line. Instead, a single resistor can be used to tie all static I/O lines HIGH to reduce BOM count. For instance, if Software Control Mode is desired both the GAIN[1:0] and the PBTL/SCL pins can both be pulled HIGH through a single pullup resistor.

9.2.2.3 Application Curves

Table 22. Relevant Performance Plots

PLOT TITLE	PLOT NUMBER
Figure 1. Output Power vs PVDD	G001
Figure 2. THD+N vs Frequency With PVDD = 12 V, P_{OSPK} = 1 W	G024
Figure 3. THD+N vs Frequency With PVDD = 24 V, P_{OSPK} = 1 W	G025
Figure 4. Idle Channel Noise vs PVDD	G026
Figure 5. THD+N vs Output Power With PVDD = 12 V, Both Channels Driven	G027
Figure 6. THD+N vs Output Power With PVDD = 18 V, Both Channels Driven	G028
Figure 7. THD+N vs Output Power With PVDD = 24 V, Both Channels Driven	G029
Figure 8. Efficiency vs Output Power	G030
Figure 9. Crosstalk vs Frequency	G031
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Figure 11. DVDD PSRR vs Frequency	G020
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Figure 13. Idle Current Draw vs PVDD (With LC Filter as Shown on the EVM)	G023
Figure 14. Shutdown Current Draw vs PVDD (Filterless)	G022
Figure 15. Output Power vs PVDD	G039
Figure 16. THD+N vs Frequency With PVDD = 12 V, P_{OSPK} = 1 W	G002
Figure 17. THD+N vs Frequency With PVDD = 24 V, P_{OSPK} = 1 W	G003
Figure 18. Idle Channel Noise vs PVDD	G006
Figure 19. THD+N vs Output Power With PVDD = 12 V, Both Channels Driven	G008
Figure 20. THD+N vs Output Power With PVDD = 18 V, Both Channels Driven	G009
Figure 21. THD+N vs Output Power With PVDD = 24 V, Both Channels Driven	G010
Figure 22. Efficiency vs Output Power	G014
Figure 23. Crosstalk vs Frequency	G018
Figure 24. PVDD PSRR vs Frequency	G019
Figure 25. Idle Current Draw vs PVDD (Filterless)	G045
Figure 26. Idle Current Draw vs PVDD (With LC Filter as Shown on EVM)	G044
Figure 27. Shutdown Current Draw vs PVDD (Filterless)	G022

9.2.3 Mono PBTL Using Software Control

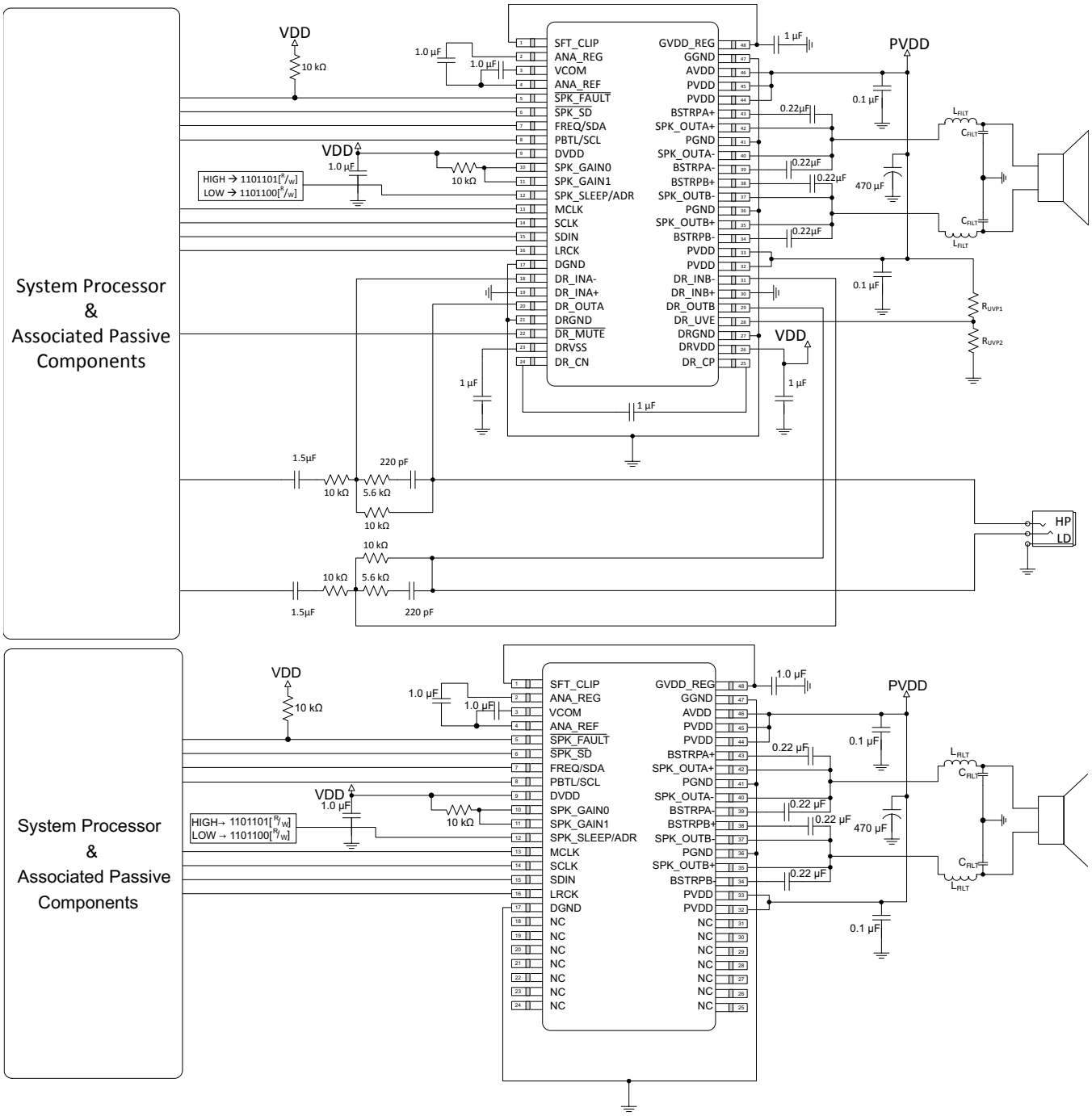


Figure 63. Mono PBTL Using Software Control

9.2.3.1 Design Requirements

For this design example, use the parameters listed in Table 23 as the input parameters.

Table 23. Design Parameters

PARAMETER	EXAMPLE
Low Power Supply	3.3 V
High Power Supply	5 V to 24 V
Host Processor	I2S Compliant Master
	I2C Compliant Master
	GPIO Control
Output Filters	Inductor-Capacitor Low Pass Filter
Speakers	4 Ω to 8 Ω

9.2.3.2 Detailed Design Procedure

9.2.3.2.1 Startup Procedures- Software Control Mode

1. Configure all digital I/O pins as required by the application using PCB connections (that is SPK_GAIN[1:0] = 11, ADR, etc.)
2. Start with $\overline{\text{SPK\_SD}}$ Pin = LOW
3. Bring up power supplies (it does not matter if PVDD/AVDD or DVDD comes up first, provided the device is held in shutdown.)
4. Once power supplies are stable, start MCLK, SCLK, LRCK
5. Configure the device via the control port in the manner required by the use case, making sure to mute the device via the control port
6. Once power supplies and clocks are stable and the control port has been programmed, bring $\overline{\text{SPK\_SD}}$ HIGH
7. Unmute the device via the control port
8. The device is now in normal operation

NOTE

Control port register changes should only occur when the device is placed into shutdown. This can be accomplished either by pulling the $\overline{\text{SPK\_SD}}$ pin LOW or clearing the $\overline{\text{SPK\_SD}}$ bit in the control port.

9.2.3.2.2 Shutdown Procedures- Software Control Mode

1. The device is in normal operation
2. Mute via the control port
3. Pull $\overline{\text{SPK\_SD}}$ LOW
4. The clocks can now be stopped and the power supplies brought down
5. The device is now fully shutdown and powered off

NOTE

Any control port register changes excluding volume control changes should only occur when the device is placed into shutdown. This can be accomplished either by pulling the $\overline{\text{SPK\_SD}}$ pin LOW or clearing the $\overline{\text{SPK\_SD}}$ bit in the control port.

9.2.3.2.3 Component Selection and Hardware Connections

Figure 63 above details the typical connections required for proper operation of the device. It is with this list of components that the device was simulated, tested, and characterized. Deviation from this typical application circuit unless recommended by this document may produce unwanted results, which could range from degradation of audio performance to destructive failure of the device.

9.2.3.2.3.1 I²C Pull-Up Resistors

It is important to note that when the device is operated in Software Control Mode, the customary pull-up resistors are required on the SCL and SDA signal lines. They are not shown in the Typical Application Circuits, since they are shared by all of the devices on the I²C bus and are considered to be part of the associated passive components for the System Processor. These resistor values should be chosen per the guidance provided in the I²C Specification.

9.2.3.2.3.2 Digital I/O Connectivity

The digital I/O lines of the TAS5760M-Q1 are described in previous sections. As discussed, whenever a static digital pin (that is a pin that is hardwired to be HIGH or LOW) is required to be pulled HIGH, it should be connected to DVDD through a pullup resistor in order to control the slew rate of the voltage presented to the digital I/O pins. It is not, however, necessary to have a separate pullup resistor for each static digital I/O line. Instead, a single resistor can be used to tie all static I/O lines HIGH to reduce BOM count. For instance, if Software Control Mode is desired both the GAIN[1:0] and the PBTL/SCL pins can both be pulled HIGH through a single pullup resistor.

9.2.3.3 Application Curves

Table 24. Relevant Performance Plots

PLOT TITLE	PLOT NUMBER
Figure 28. THD+N vs Frequency With PVDD = 12 V, P_{OSPK} = 1 W	G032
Figure 29. THD+N vs Frequency With PVDD = 24 V, P_{OSPK} = 1 W	G033
Figure 31. THD+N vs Output Power With PVDD = 12 V With 1 kHz Sine Input	G035
Figure 32. THD+N vs Output Power With PVDD = 18 V With 1 kHz Sine Input	G036
Figure 33. THD+N vs Output Power With PVDD = 24 V With 1 kHz Sine Input	G037
Figure 34. Efficiency vs Output Power	G038
Figure 35. THD+N vs Frequency With PVDD = 12 V, P_{OSPK} = 1 W	G004
Figure 36. THD+N vs Frequency With PVDD = 24 V, P_{OSPK} = 1 W	G005
Figure 38. THD+N vs Output Power With PVDD = 12 V	G011
Figure 39. THD+N vs Output Power With PVDD = 18 V	G012
Figure 40. THD+N vs Output Power With PVDD = 24 V	G013
Figure 41. Efficiency vs Output Power	G015

9.2.4 Mono PBTL Using Hardware Control

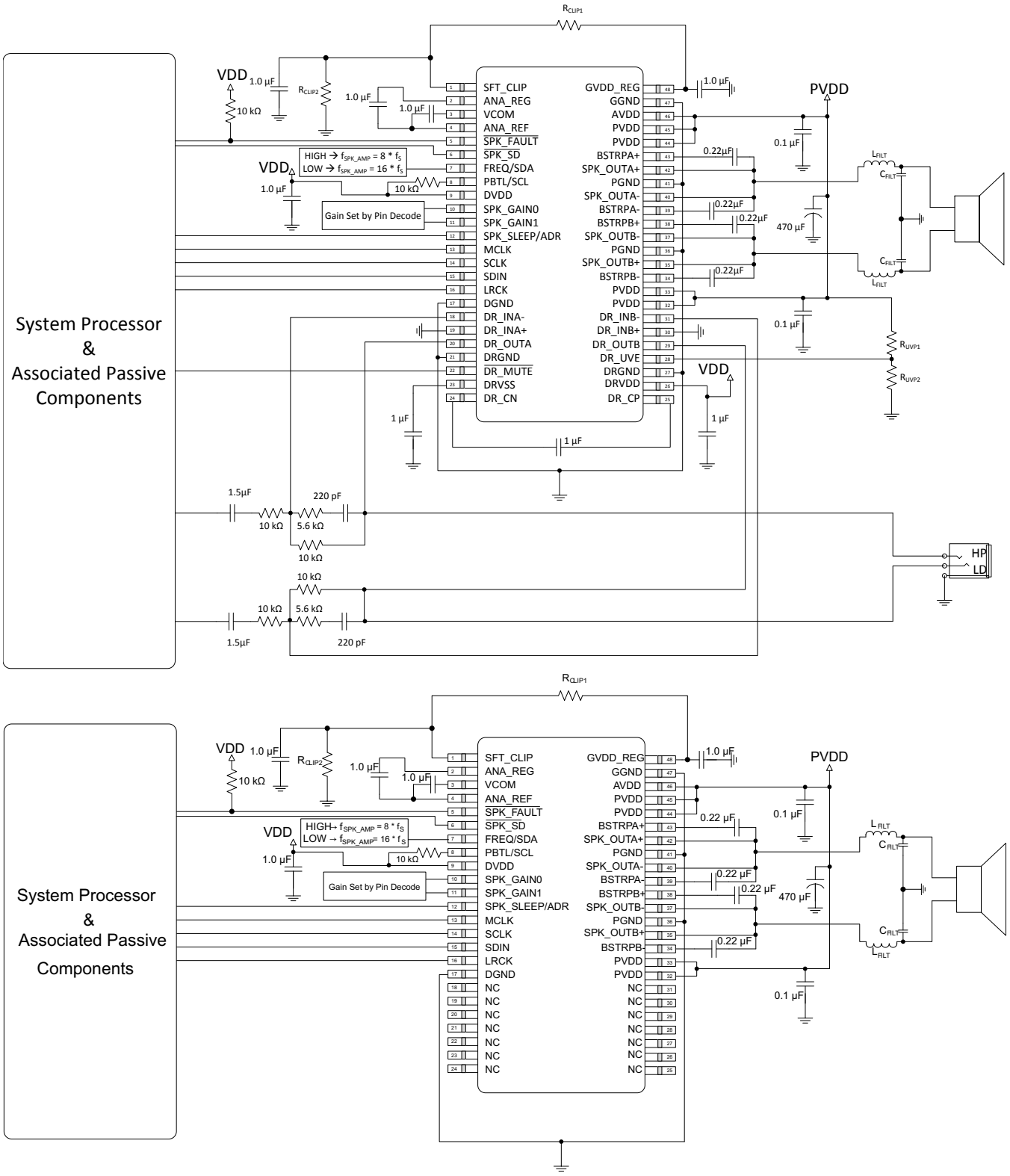


Figure 64. Mono PBTL Using Hardware Control

9.2.4.1 Design Requirements

For this design example, use the parameters listed in Table 25 as the input parameters.

Table 25. Design Parameters

PARAMETER	EXAMPLE
Low Power Supply	3.3 V
High Power Supply	5 V to 24 V
Host Processor	I2S Compliant Master
	GPIO Control
Output Filters	Inductor-Capacitor Low Pass Filter
Speakers	4 Ω to 8 Ω

9.2.4.2 Detailed Design Procedure

9.2.4.2.1 Startup Procedures- Hardware Control Mode

1. Configure all hardware pins as required by the application using PCB connections (that is PBTL, FREQ, GAIN, etc.)
2. Start with $\overline{\text{SPK\_SD}}$ pin pulled LOW and SPK_SLEEP/ADR pin pulled HIGH
3. Bring up power supplies (it does not matter if PVDD/AVDD or DVDD comes up first, provided the device is held in shutdown.)
4. Once power supplies are stable, start MCLK, SCLK, LRCK
5. Once power supplies and clocks are stable and all hardware control pins have been configured, bring $\overline{\text{SPK\_SD}}$ HIGH
6. Once the device is out of shutdown mode, bring SPK_SLEEP/ADR LOW
7. The device is now in normal operation

9.2.4.2.2 Shutdown Procedures- Hardware Control Mode

1. The device is in normal operation
2. Pull SPK_SLEEP/ADR HIGH
3. Pull $\overline{\text{SPK\_SD}}$ LOW
4. The clocks can now be stopped and the power supplies brought down
5. The device is now fully shutdown and powered off

9.2.4.2.3 Component Selection and Hardware Connections

Figure 64 details the typical connections required for proper operation of the device. It is with this list of components that the device was simulated, tested, and characterized. Deviation from this typical application circuit unless recommended by this document may produce unwanted results, which could range from degradation of audio performance to destructive failure of the device.

9.2.4.2.4 Digital I/O Connectivity

The digital I/O lines of the TAS5760M-Q1 are described in previous sections. As discussed, whenever a static digital pin (that is a pin that is hardwired to be HIGH or LOW) is required to be pulled HIGH, it should be connected to DVDD through a pullup resistor in order to control the slew rate of the voltage presented to the digital I/O pins. It is not, however, necessary to have a separate pullup resistor for each static digital I/O line. Instead, a single resistor can be used to tie all static I/O lines HIGH to reduce BOM count. For instance, if Software Control Mode is desired both the GAIN[1:0] and the PBTL/SCL pins can both be pulled HIGH through a single pullup resistor.

9.2.4.3 Application Curve

Table 26. Relevant Performance Plots

PLOT TITLE	PLOT NUMBER
Figure 28. THD+N vs Frequency With PVDD = 12 V, P_{OSPK} = 1 W	G032
Figure 29. THD+N vs Frequency With PVDD = 24 V, P_{OSPK} = 1 W	G033
Figure 30. Idle Channel Noise vs PVDD	G034
Figure 31. THD+N vs Output Power With PVDD = 12 V With 1 kHz Sine Input	G035
Figure 32. THD+N vs Output Power With PVDD = 18 V With 1 kHz Sine Input	G036
Figure 33. THD+N vs Output Power With PVDD = 24 V With 1 kHz Sine Input	G037
Figure 34. Efficiency vs Output Power	G038
Figure 35. THD+N vs Frequency With PVDD = 12 V, P_{OSPK} = 1 W	G004
Figure 36. THD+N vs Frequency With PVDD = 24 V, P_{OSPK} = 1 W	G005
Figure 37. Idle Channel Noise vs PVDD	G007
Figure 38. THD+N vs Output Power With PVDD = 12 V	G011
Figure 39. THD+N vs Output Power With PVDD = 18 V	G012
Figure 40. THD+N vs Output Power With PVDD = 24 V	G013
Figure 41. Efficiency vs Output Power	G015

9.2.5 Stereo BTL Using Software Control, 32-Pin DAP Package Option

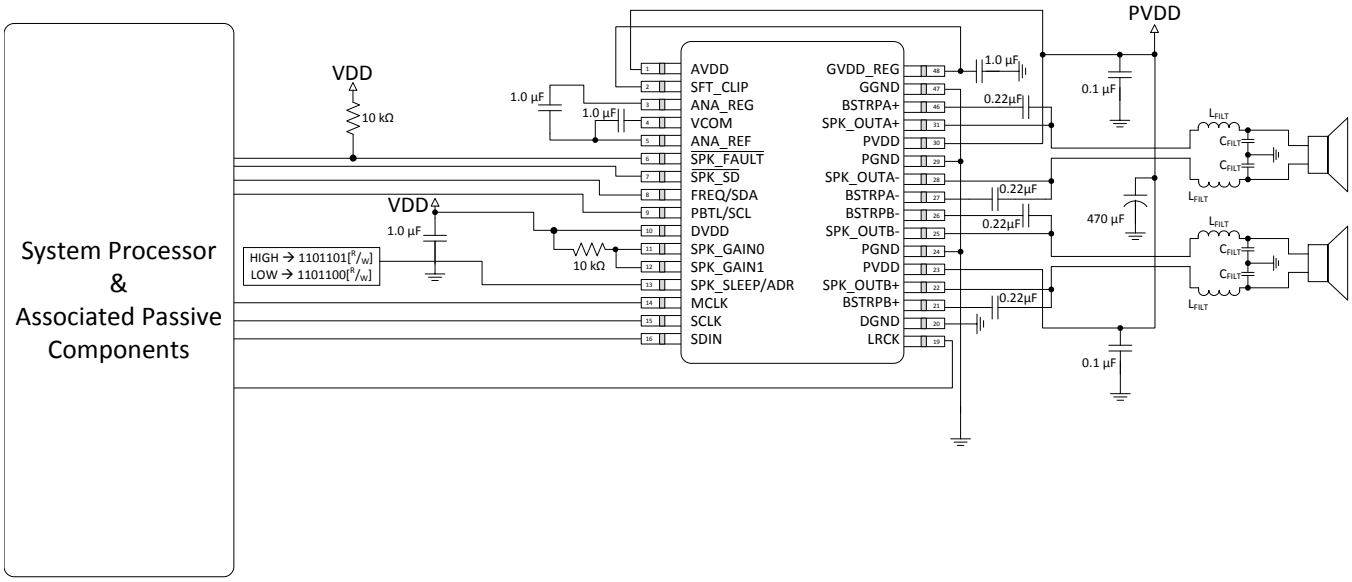


Figure 65. Stereo BTL using Software Control, 32-Pin DAP Package Option

9.2.5.1 Design Requirements

For this design example, use the parameters listed in Table 27 as the input parameters.

Table 27. Design Parameters

PARAMETER	EXAMPLE
Low Power Supply	3.3 V
High Power Supply	5 V to 24 V
Host Processor	I2S Compliant Master
	I2C Compliant Master
	GPIO Control
Output Filters	Inductor-Capacitor Low Pass Filter
Speakers	4 Ω to 8 Ω

9.2.5.2 Detailed Design Procedure

9.2.5.2.1 Startup Procedures- Software Control Mode

1. Configure all digital I/O pins as required by the application using PCB connections (that is SPK_GAIN[1:0] = 11, ADR, etc.)
2. Start with $\overline{\text{SPK\_SD}}$ Pin = LOW
3. Bring up power supplies (it does not matter if PVDD/AVDD or DVDD comes up first, provided the device is held in shutdown.)
4. Once power supplies are stable, start MCLK, SCLK, LRCK
5. Configure the device via the control port in the manner required by the use case, making sure to mute the device via the control port
6. Once power supplies and clocks are stable and the control port has been programmed, bring $\overline{\text{SPK\_SD}}$ HIGH
7. Unmute the device via the control port
8. The device is now in normal operation

NOTE

Control port register changes should only occur when the device is placed into shutdown. This can be accomplished either by pulling the SPK_SD pin LOW or clearing the SPK_SD bit in the control port.

9.2.5.2.2 Shutdown Procedures- Software Control Mode

1. The device is in normal operation
2. Mute via the control port
3. Pull SPK_SD LOW
4. The clocks can now be stopped and the power supplies brought down
5. The device is now fully shutdown and powered off

NOTE

Any control port register changes excluding volume control changes should only occur when the device is placed into shutdown. This can be accomplished either by pulling the SPK_SD pin LOW or clearing the SPK_SD bit in the control port.

9.2.5.2.3 Component Selection and Hardware Connections

Figure 65 details the typical connections required for proper operation of the device. It is with this list of components that the device was simulated, tested, and characterized. Deviation from this typical application circuit unless recommended by this document may produce unwanted results, which could range from degradation of audio performance to destructive failure of the device.

9.2.5.2.3.1 I²C Pullup Resistors

It is important to note that when the device is operated in Software Control Mode, the customary pullup resistors are required on the SCL and SDA signal lines. They are not shown in the Typical Application Circuits, because they are shared by all of the devices on the I²C bus and are considered to be part of the associated passive components for the System Processor. These resistor values should be chosen per the guidance provided in the I²C Specification.

9.2.5.2.3.2 Digital I/O Connectivity

The digital I/O lines of the TAS5760M-Q1 are described in previous sections. As discussed, whenever a static digital pin (that is a pin that is hardwired to be HIGH or LOW) is required to be pulled HIGH, it should be connected to DVDD through a pullup resistor to control the slew rate of the voltage presented to the digital I/O pins. It is not, however, necessary to have a separate pullup resistor for each static digital I/O line. Instead, a single resistor can be used to tie all static I/O lines HIGH to reduce BOM count. For instance, if Software Control Mode is desired both the GAIN[1:0] and the PBTL/SCL pins can both be pulled HIGH through a single pullup resistor.

9.2.5.2.4 Recommended Startup and Shutdown Procedures

The start up and shutdown procedures for both Hardware Control Mode and Software Control Mode are shown below.

9.2.5.3 Application Curve

Table 28. Relevant Performance Plots

PLOT TITLE	PLOT NUMBER
Figure 1. Output Power vs PVDD	G001
Figure 2. THD+N vs Frequency With PVDD = 12 V, POSPK = 1 W	G024
Figure 3. THD+N vs Frequency With PVDD = 24 V, POSPK = 1 W	G025
Figure 5. THD+N vs Output Power With PVDD = 12 V, Both Channels Driven	G027
Figure 6. THD+N vs Output Power With PVDD = 18 V, Both Channels Driven	G028

Table 28. Relevant Performance Plots (continued)

PLOT TITLE	PLOT NUMBER
Figure 7. THD+N vs Output Power With PVDD = 24 V, Both Channels Driven	G029
Figure 8. Efficiency vs Output Power	G030
Figure 9. Crosstalk vs Frequency	G031
Figure 10. PVDD PSRR vs Frequency	G019
Figure 11. DVDD PSRR vs Frequency	G020
Figure 12. Idle Current Draw vs PVDD (Filterless)	G042
Figure 13. Idle Current Draw vs PVDD (With LC Filter as Shown on the EVM)	G023
Figure 14. Shutdown Current Draw vs PVDD (Filterless)	G022
Figure 15. Output Power vs PVDD	G039
Figure 16. THD+N vs Frequency With PVDD = 12 V, P_{OSPK} = 1 W	G002
Figure 17. THD+N vs Frequency With PVDD = 24 V, P_{OSPK} = 1 W	G003
Figure 19. THD+N vs Output Power With PVDD = 12 V, Both Channels Driven	G008
Figure 20. THD+N vs Output Power With PVDD = 18 V, Both Channels Driven	G009
Figure 21. THD+N vs Output Power With PVDD = 24 V, Both Channels Driven	G010
Figure 22. Efficiency vs Output Power	G014
Figure 23. Crosstalk vs Frequency	G018
Figure 24. PVDD PSRR vs Frequency	G019
Figure 25. Idle Current Draw vs PVDD (Filterless)	G045
Figure 26. Idle Current Draw vs PVDD (With LC Filter as Shown on EVM)	G044
Figure 27. Shutdown Current Draw vs PVDD (Filterless)	G022

9.2.6 Stereo BTL Using Hardware Control, 32-Pin DAP Package Option

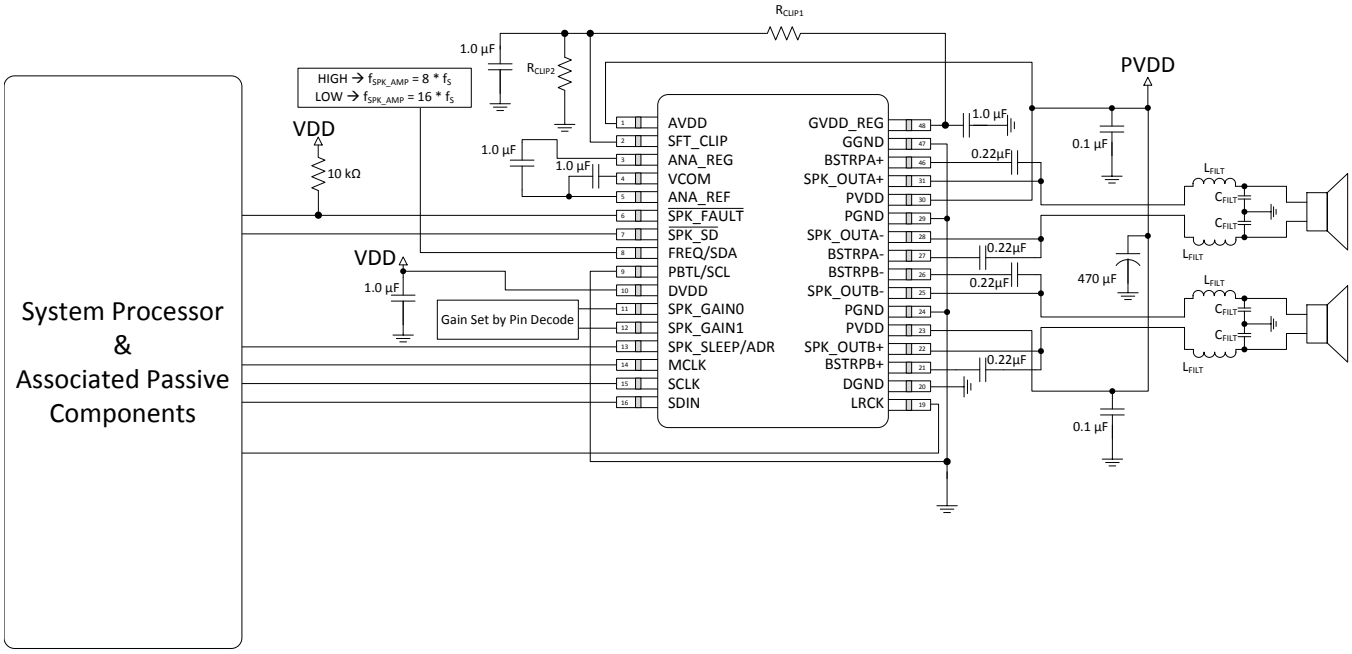


Figure 66. Stereo BTL using Hardware Control, 32-Pin DAP Package Option

9.2.6.1 Design Requirements

For this design example, use the parameters listed in Table 29 as the input parameters.

Table 29. Design Parameters

PARAMETER	EXAMPLE
Low Power Supply	3.3 V
High Power Supply	5 V to 24 V
Host Processor	I2S Compliant Master
	GPIO Control
Output Filters	Inductor-Capacitor Low Pass Filter
Speakers	4 Ω to 8 Ω

9.2.6.2 Detailed Design Procedure

9.2.6.2.1 Startup Procedures- Hardware Control Mode

1. Configure all hardware pins as required by the application using PCB connections (that is PBTL, FREQ, GAIN, etc.)
2. Start with $\overline{\text{SPK\_SD}}$ pin pulled LOW and SPK_SLEEP/ADR pin pulled HIGH
3. Bring up power supplies (it does not matter if PVDD/AVDD or DVDD comes up first, provided the device is held in shutdown.)
4. Once power supplies are stable, start MCLK, SCLK, LRCK
5. Once power supplies and clocks are stable and all hardware control pins have been configured, bring $\overline{\text{SPK\_SD}}$ HIGH
6. Once the device is out of shutdown mode, bring SPK_SLEEP/ADR LOW
7. The device is now in normal operation

9.2.6.2.2 Shutdown Procedures- Hardware Control Mode

1. The device is in normal operation

2. Pull SPK_SLEEP/ADR HIGH
3. Pull $\overline{\text{SPK\_SD}}$ LOW
4. The clocks can now be stopped and the power supplies brought down
5. The device is now fully shutdown and powered off

9.2.6.2.3 Digital I/O Connectivity

The digital I/O lines of the TAS5760M-Q1 are described in previous sections. As discussed, whenever a static digital pin (that is a pin that is hardwired to be HIGH or LOW) is required to be pulled HIGH, it should be connected to DVDD through a pullup resistor in order to control the slew rate of the voltage presented to the digital I/O pins. It is not, however, necessary to have a separate pullup resistor for each static digital I/O line. Instead, a single resistor can be used to tie all static I/O lines HIGH to reduce BOM count. For instance, if Software Control Mode is desired both the GAIN[1:0] and the PBTL/SCL pins can both be pulled HIGH through a single pullup resistor.

9.2.6.3 Application Curve

Table 30. Relevant Performance Plots

PLOT TITLE	PLOT NUMBER
Figure 1. Output Power vs PVDD	G001
Figure 2. THD+N vs Frequency With PVDD = 12 V, P_{OSPK} = 1 W	G024
Figure 3. THD+N vs Frequency With PVDD = 24 V, P_{OSPK} = 1 W	G025
Figure 4. Idle Channel Noise vs PVDD	G026
Figure 5. THD+N vs Output Power With PVDD = 12 V, Both Channels Driven	G027
Figure 6. THD+N vs Output Power With PVDD = 18 V, Both Channels Driven	G028
Figure 7. THD+N vs Output Power With PVDD = 24 V, Both Channels Driven	G029
Figure 8. Efficiency vs Output Power	G030
Figure 9. Crosstalk vs Frequency	G031
Figure 10. PVDD PSRR vs Frequency	G019
Figure 11. DVDD PSRR vs Frequency	G020
Figure 12. Idle Current Draw vs PVDD (Filterless)	G042
Figure 13. Idle Current Draw vs PVDD (With LC Filter as Shown on the EVM)	G023
Figure 14. Shutdown Current Draw vs PVDD (Filterless)	G022
Figure 15. Output Power vs PVDD	G039
Figure 16. THD+N vs Frequency With PVDD = 12 V, P_{OSPK} = 1 W	G002
Figure 17. THD+N vs Frequency With PVDD = 24 V, P_{OSPK} = 1 W	G003
Figure 18. Idle Channel Noise vs PVDD	G006
Figure 19. THD+N vs Output Power With PVDD = 12 V, Both Channels Driven	G008
Figure 20. THD+N vs Output Power With PVDD = 18 V, Both Channels Driven	G009
Figure 21. THD+N vs Output Power With PVDD = 24 V, Both Channels Driven	G010
Figure 22. Efficiency vs Output Power	G014
Figure 23. Crosstalk vs Frequency	G018
Figure 24. PVDD PSRR vs Frequency	G019
Figure 25. Idle Current Draw vs PVDD (Filterless)	G045
Figure 26. Idle Current Draw vs PVDD (With LC Filter as Shown on EVM)	G044
Figure 27. Shutdown Current Draw vs PVDD (Filterless)	G022

9.2.7 Mono PBTL Using Software Control, 32-Pin DAP Package Option

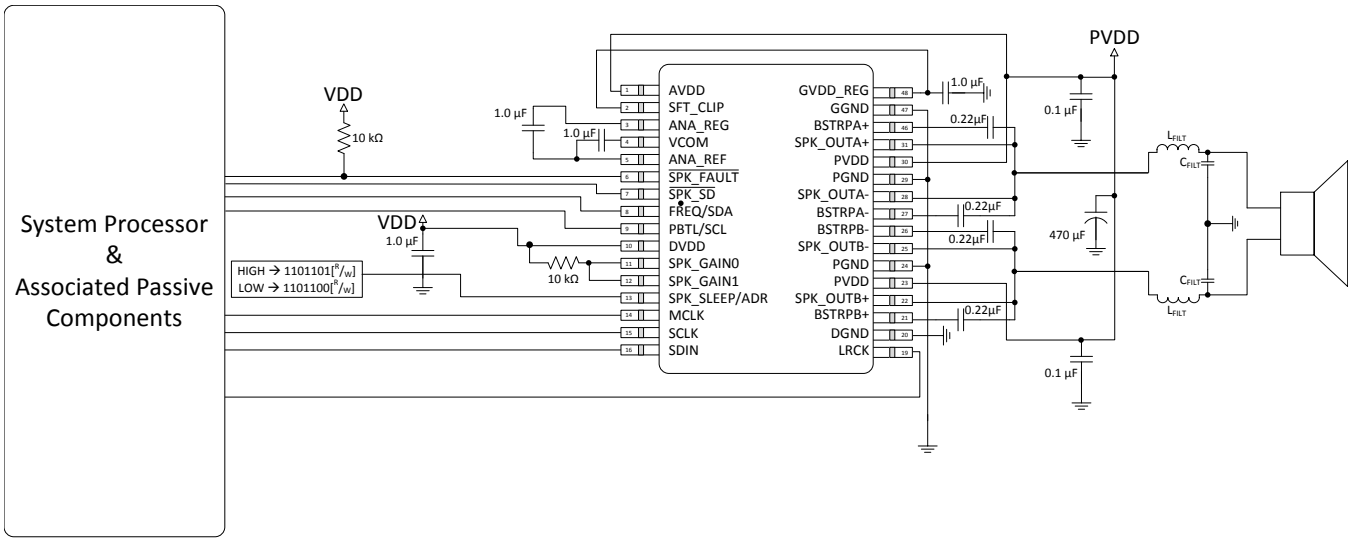


Figure 67. Mono PBTL using Software Control, 32-Pin DAP Package Option

9.2.7.1 Design Requirements

For this design example, use the parameters listed in Table 31 as the input parameters.

Table 31. Design Parameters

PARAMETER	EXAMPLE
Low Power Supply	3.3 V
High Power Supply	5 V to 24 V
Host Processor	I2S Compliant Master
	I2C Compliant Master
	GPIO Control
Output Filters	Inductor-Capacitor Low Pass Filter
Speakers	4 Ω to 8 Ω

9.2.7.2 Detailed Design Procedure

9.2.7.2.1 Startup Procedures- Software Control Mode

1. Configure all digital I/O pins as required by the application using PCB connections (that is SPK_GAIN[1:0] = 11, ADR, etc.)
2. Start with $\overline{\text{SPK\_SD}}$ Pin = LOW
3. Bring up power supplies (it does not matter if PVDD/AVDD or DVDD comes up first, provided the device is held in shutdown.)
4. Once power supplies are stable, start MCLK, SCLK, LRCK
5. Configure the device via the control port in the manner required by the use case, making sure to mute the device via the control port
6. Once power supplies and clocks are stable and the control port has been programmed, bring $\overline{\text{SPK\_SD}}$ HIGH
7. Unmute the device via the control port
8. The device is now in normal operation

NOTE

Control port register changes should only occur when the device is placed into shutdown. This can be accomplished either by pulling the SPK_SD pin LOW or clearing the SPK_SD bit in the control port.

9.2.7.2.2 Shutdown Procedures- Software Control Mode

1. The device is in normal operation
2. Mute via the control port
3. Pull SPK_SD LOW
4. The clocks can now be stopped and the power supplies brought down
5. The device is now fully shutdown and powered off

NOTE

Any control port register changes excluding volume control changes should only occur when the device is placed into shutdown. This can be accomplished either by pulling the SPK_SD pin LOW or clearing the SPK_SD bit in the control port.

9.2.7.2.3 Component Selection and Hardware Connections

Figure 67 above details the typical connections required for proper operation of the device. It is with this list of components that the device was simulated, tested, and characterized. Deviation from this typical application circuit unless recommended by this document may produce unwanted results, which could range from degradation of audio performance to destructive failure of the device.

9.2.7.2.3.1 I²C Pull-Up Resistors

It is important to note that when the device is operated in Software Control Mode, the customary pull-up resistors are required on the SCL and SDA signal lines. They are not shown in the Typical Application Circuits, since they are shared by all of the devices on the I²C bus and are considered to be part of the associated passive components for the System Processor. These resistor values should be chosen per the guidance provided in the I²C Specification.

9.2.7.2.3.2 Digital I/O Connectivity

The digital I/O lines of the TAS5760M-Q1 are described in previous sections. As discussed, whenever a static digital pin (that is a pin that is hardwired to be HIGH or LOW) is required to be pulled HIGH, it should be connected to DVDD through a pullup resistor in order to control the slew rate of the voltage presented to the digital I/O pins. It is not, however, necessary to have a separate pullup resistor for each static digital I/O line. Instead, a single resistor can be used to tie all static I/O lines HIGH to reduce BOM count. For instance, if Software Control Mode is desired both the GAIN[1:0] and the PBTL/SCL pins can both be pulled HIGH through a single pullup resistor.

9.2.7.3 Application Curves

Table 32. Relevant Performance Plots

PLOT TITLE	PLOT NUMBER
Figure 28. THD+N vs Frequency With PVDD = 12 V, P_{OSPK} = 1 W	G032
Figure 29. THD+N vs Frequency With PVDD = 24 V, P_{OSPK} = 1 W	G033
Figure 31. THD+N vs Output Power With PVDD = 12 V With 1 kHz Sine Input	G035
Figure 32. THD+N vs Output Power With PVDD = 18 V With 1 kHz Sine Input	G036
Figure 33. THD+N vs Output Power With PVDD = 24 V With 1 kHz Sine Input	G037
Figure 34. Efficiency vs Output Power	G038
Figure 35. THD+N vs Frequency With PVDD = 12 V, P_{OSPK} = 1 W	G004
Figure 36. THD+N vs Frequency With PVDD = 24 V, P_{OSPK} = 1 W	G005
Figure 38. THD+N vs Output Power With PVDD = 12 V	G011
Figure 39. THD+N vs Output Power With PVDD = 18 V	G012
Figure 40. THD+N vs Output Power With PVDD = 24 V	G013
Figure 41. Efficiency vs Output Power	G015

9.2.8 Mono PBTL Using Hardware Control, 32-Pin DAP Package Option

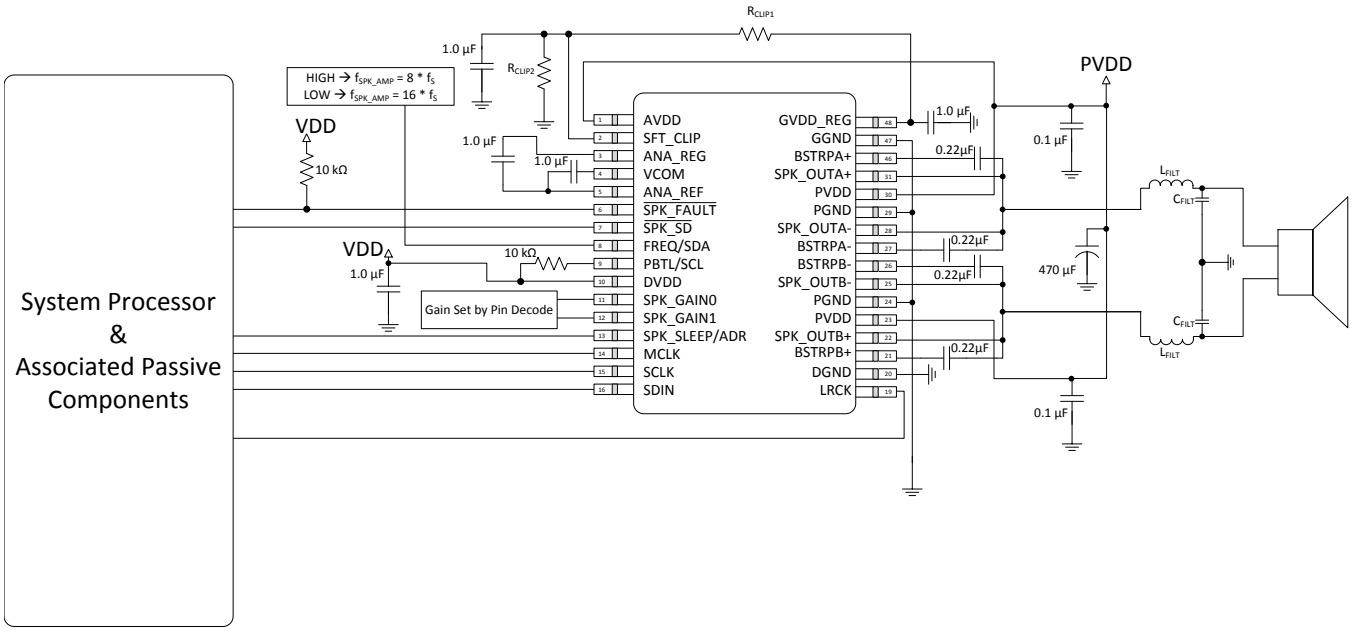


Figure 68. Mono PBTL using Hardware Control, 32 Pin DAP Package Option

9.2.8.1 Design Requirements

For this design example, use the parameters listed in Table 33 as the input parameters.

Table 33. Design Parameters

PARAMETER	EXAMPLE
Low Power Supply	3.3 V
High Power Supply	5 V to 24 V
Host Processor	I2S Compliant Master
	GPIO Control
Output Filters	Inductor-Capacitor Low Pass Filter
Speakers	4 Ω to 8 Ω

9.2.8.2 Detailed Design Procedure

9.2.8.2.1 Startup Procedures- Hardware Control Mode

1. Configure all hardware pins as required by the application using PCB connections (that is PBTL, FREQ, GAIN, etc.)
2. Start with $\overline{\text{SPK\_SD}}$ pin pulled LOW and SPK_SLEEP/ADR pin pulled HIGH
3. Bring up power supplies (it does not matter if PVDD/AVDD or DVDD comes up first, provided the device is held in shutdown.)
4. Once power supplies are stable, start MCLK, SCLK, LRCK
5. Once power supplies and clocks are stable and all hardware control pins have been configured, bring $\overline{\text{SPK\_SD}}$ HIGH
6. Once the device is out of shutdown mode, bring SPK_SLEEP/ADR LOW
7. The device is now in normal operation

9.2.8.2.2 Shutdown Procedures- Hardware Control Mode

1. The device is in normal operation
2. Pull SPK_SLEEP/ADR HIGH

3. Pull $\overline{\text{SPK\_SD}}$ LOW
4. The clocks can now be stopped and the power supplies brought down
5. The device is now fully shutdown and powered off

9.2.8.2.3 Digital I/O Connectivity

The digital I/O lines of the TAS5760M-Q1 are described in previous sections. As discussed, whenever a static digital pin (that is a pin that is hardwired to be HIGH or LOW) is required to be pulled HIGH, it should be connected to DVDD through a pullup resistor in order to control the slew rate of the voltage presented to the digital I/O pins. It is not, however, necessary to have a separate pullup resistor for each static digital I/O line. Instead, a single resistor can be used to tie all static I/O lines HIGH to reduce BOM count. For instance, if Software Control Mode is desired both the GAIN[1:0] and the PBTL/SCL pins can both be pulled HIGH through a single pullup resistor.

9.2.8.3 Application Curves

Table 34. Relevant Performance Plots

PLOT TITLE	PLOT NUMBER
Figure 28. THD+N vs Frequency With PVDD = 12 V, P_{OSPK} = 1 W	G032
Figure 29. THD+N vs Frequency With PVDD = 24 V, P_{OSPK} = 1 W	G033
Figure 30. Idle Channel Noise vs PVDD	G034
Figure 31. THD+N vs Output Power With PVDD = 12 V With 1 kHz Sine Input	G035
Figure 32. THD+N vs Output Power With PVDD = 18 V With 1 kHz Sine Input	G036
Figure 33. THD+N vs Output Power With PVDD = 24 V With 1 kHz Sine Input	G037
Figure 34. Efficiency vs Output Power	G038
Figure 35. THD+N vs Frequency With PVDD = 12 V, P_{OSPK} = 1 W	G004
Figure 36. THD+N vs Frequency With PVDD = 24 V, P_{OSPK} = 1 W	G005
Figure 37. Idle Channel Noise vs PVDD	G007
Figure 38. THD+N vs Output Power With PVDD = 12 V	G011
Figure 39. THD+N vs Output Power With PVDD = 18 V	G012
Figure 40. THD+N vs Output Power With PVDD = 24 V	G013
Figure 41. Efficiency vs Output Power	G015

10 Power Supply Recommendations

The TAS5760M-Q1 device requires two power supplies for proper operation. A high-voltage supply called PVDD is required to power the output stage of the speaker amplifier and its associated circuitry. Additionally, one low voltage power supply called DVDD is required to power the various low-power portions of the device. The allowable voltage range for both the PVDD and the DVDD supply are listed in the *Recommended Operating Conditions* table.

10.1 DVDD Supply

The DVDD supply required from the system is used to power several portions of the device it provides power to the DVDD pin and the DRVDD pin. Proper connection, routing, and decoupling techniques are highlighted in the *TAS5760xx EVM User's Guide*, SLOU371 (as well as the *Application and Implementation* section and *Layout Example* section) and must be followed as closely as possible for proper operation and performance. Deviation from the guidance offered in the TAS5760xx EVM User's Guide, which followed the same techniques as those shown in the *Application and Implementation* section, may result in reduced performance, errant functionality, or even damage to the TTAS5760M-Q1 device. Some portions of the device also require a separate power supply which is a lower voltage than the DVDD supply. To simplify the power supply requirements for the system, the TAS5760M-Q1 device includes an integrated low-dropout (LDO) linear regulator to create this supply. This linear regulator is internally connected to the DVDD supply and its output is presented on the ANA_REG pin, providing a connection point for an external bypass capacitor. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

10.2 PVDD Supply

The output stage of the speaker amplifier drives the load using the PVDD supply. This is the power supply which provides the drive current to the load during playback. Proper connection, routing, and decoupling techniques are highlighted in the TAS5760xx EVM and must be followed as closely as possible for proper operation and performance. Due the high-voltage switching of the output stage, it is particularly important to properly decouple the output power stages in the manner described in the *TaS5760xx EVM User's Guide*, SLOU371. The lack of proper decoupling, like that shown in the *EVM User's Guide*, can results in voltage spikes which can damage the device. A separate power supply is required to drive the gates of the MOSFETs used in the output stage of the speaker amplifier. This power supply is derived from the PVDD supply via an integrated linear regulator. A GVDD_REG pin is provided for the attachment of decoupling capacitor for the gate drive voltage regulator. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

11 Layout

11.1 Layout Guidelines

11.1.1 General Guidelines for Audio Amplifiers

Audio amplifiers which incorporate switching output stages must have special attention paid to their layout and the layout of the supporting components used around them. The system level performance metrics, including thermal performance, electromagnetic compliance (EMC), device reliability, and audio performance are all affected by the device and supporting component layout. Ideally, the guidance provided in the applications section with regard to device and component selection can be followed by precise adherence to the layout guidance shown in *Layout Example*. These examples represent exemplary baseline balance of the engineering trade-offs involved with laying out the device. These designs can be modified slightly as needed to meet the needs of a given application. In some applications, for instance, solution size can be compromised in order to improve thermal performance through the use of additional contiguous copper near the device. Conversely, EMI performance can be prioritized over thermal performance by routing on internal traces and incorporating a via picket-fence and additional filtering components. In all cases, it is recommended to start from the guidance shown in the *Layout Example* section and the TAS5760xx EVM, and work with TI field application engineers or through the E2E community in order to modify it based upon the application specific goals.

Layout Guidelines (continued)

11.1.2 Importance of PVDD Bypass Capacitor Placement on PVDD Network

Placing the bypassing and decoupling capacitors close to supply has been long understood in the industry. This applies to DVDD, DRVDD, and PVDD. However, the capacitors on the PVDD net for the TAS5760M-Q1 device deserve special attention. It is imperative that the small bypass capacitors on the PVDD lines of the DUT be placed as close the PVDD pins as possible. Not only does placing these devices far away from the pins increase the electromagnetic interference in the system, but doing so can also negatively affect the reliability of the device. Placement of these components too far from the TAS5760M-Q1device may cause ringing on the output pins that can cause the voltage on the output pin to exceed the maximum allowable ratings shown in the *Absolute Maximum Ratings* table, damaging the device. For that reason, the capacitors on the PVDD net must be no further away from their associated PVDD pins than what is shown in the example layouts in the *Layout Example* section.

11.1.3 Optimizing Thermal Performance

Follow the layout examples shown in the *Layout Example* section of this document to achieve the best balance of solution size, thermal, audio, and electromagnetic performance. In some cases, deviation from this guidance may be required due to design constraints which cannot be avoided. In these instances, the system designer should ensure that the heat can get out of the device and into the ambient air surrounding the device. Fortunately, the heat created in the device would prefer to travel away from the device and into the lower temperature structures around the device.

11.1.3.1 Device, Copper, and Component Layout

Primarily, the goal of the PCB design is to minimize the thermal impedance in the path to those cooler structures. These tips should be followed to achieve that goal:

- Avoid placing other heat producing components or structures near the amplifier (including above or below in the end equipment).
- If possible, use a higher layer count PCB to provide more heat sinking capability for the TAS5760M-Q1device and to prevent traces and copper signal and power planes from breaking up the contiguous copper on the top and bottom layer.
- Place the TTAS5760M-Q1 device away from the edge of the PCB when possible to ensure that heat can travel away from the device on all four sides.
- Avoid cutting off the flow of heat from the TAS5760M-Q1device to the surrounding areas with traces or via strings. Instead, route traces perpendicular to the device and line up vias in columns which are perpendicular to the device.
- Unless the area between two pads of a passive component is large enough to allow copper to flow in between the two pads, orient it so that the narrow end of the passive component is facing the TAS5760M-Q1 device.
- Because the ground pins are the best conductors of heat in the package, maintain a contiguous ground plane from the ground pins to the PCB area surrounding the device for as many of the ground pins as possible.

11.1.3.2 Stencil Pattern

The recommended drawings for the TAS5760M-Q1 device PCB foot print and associated stencil pattern are shown at the end of this document in the package addendum. Additionally, baseline recommendations for the via arrangement under and around the device are given as a starting point for the PCB design. This guidance is provided to suit the majority of manufacturing capabilities in the industry and prioritizes manufacturability over all other performance criteria. In elevated ambient temperatures or under high-power dissipation use-cases, this guidance may be too conservative and advanced PCB design techniques may be used to improve thermal performance of the system. It is important to note that the customer must verify that deviation from the guidance shown in the package addendum, including the deviation explained in this section, meets the customer's quality, reliability, and manufacturability goals.

Layout Guidelines (continued)

11.1.3.2.1 PCB Footprint and Via Arrangement

The PCB footprint (also known as a symbol or land pattern) communicates to the PCB fabrication vendor the shape and position of the copper patterns to which the TAS5760M-Q1device will be soldered to. This footprint can be followed directly from the guidance in the package addendum at the end of this data sheet. It is important to make sure that the thermal pad, which connects electrically and thermally to the PowerPAD of the TAS5760M-Q1device, be made no smaller than what is specified in the package addendum. This ensures that the TAS5760M-Q1 device has the largest interface possible to move heat from the device to the board. The via pattern shown in the package addendum provides an improved interface to carry the heat from the device through to the layers of the PCB, because small diameter plated vias (with minimally-sized annular rings) present a low thermal-impedance path from the device into the PCB. Once into the PCB, the heat travels away from the device and into the surrounding structures and air. By increasing the number of vias, as shown in *Layout Example*, this interface can benefit from improved thermal performance.

NOTE

Vias can obstruct heat flow if they are not constructed properly.

- Remove thermal reliefs on thermal vias, because they impede the flow of heat through the via.
- Vias filled with thermally conductive material are best, but a simple plated via can be used to avoid the additional cost of filled vias.
- The drill diameter should be no more than 8mils in diameter. Also, the distance between the via barrel and the surrounding planes should be minimized to help heat flow from the via into the surrounding copper material. In all cases, minimum spacing should be determined by the voltages present on the planes surrounding the via and minimized wherever possible.
- Vias should be arranged in columns, which extend in a line radially from the heat source to the surrounding area. This arrangement is shown in the *Layout Example* section.
- Ensure that vias do not cut-off power current flow from the power supply through the planes on internal layers. If needed, remove some vias which are farthest from the TAS5760M-Q1 device to open up the current path to and from the device.

11.1.3.2.1.1 Solder Stencil

During the PCB assembly process, a piece of metal called a stencil on top of the PCB and deposits solder paste on the PCB wherever there is an opening (called an aperture) in the stencil. The stencil determines the quantity and the location of solder paste that is applied to the PCB in the electronic manufacturing process. In most cases, the aperture for each of the component pads is almost the same size as the pad itself.

However, the thermal pad on the PCB is quite large and depositing a large, single deposition of solder paste would lead to manufacturing issues. Instead, the solder is applied to the board in multiple apertures, to allow the solder paste to outgas during the assembly process and reduce the risk of solder bridging under the device. This structure is called an aperture array, and is shown in the *Layout Example* section. It is important that the total area of the aperture array (the area of all of the small apertures combined) covers between 70% and 80% of the area of the thermal pad itself.

11.2 Layout Example

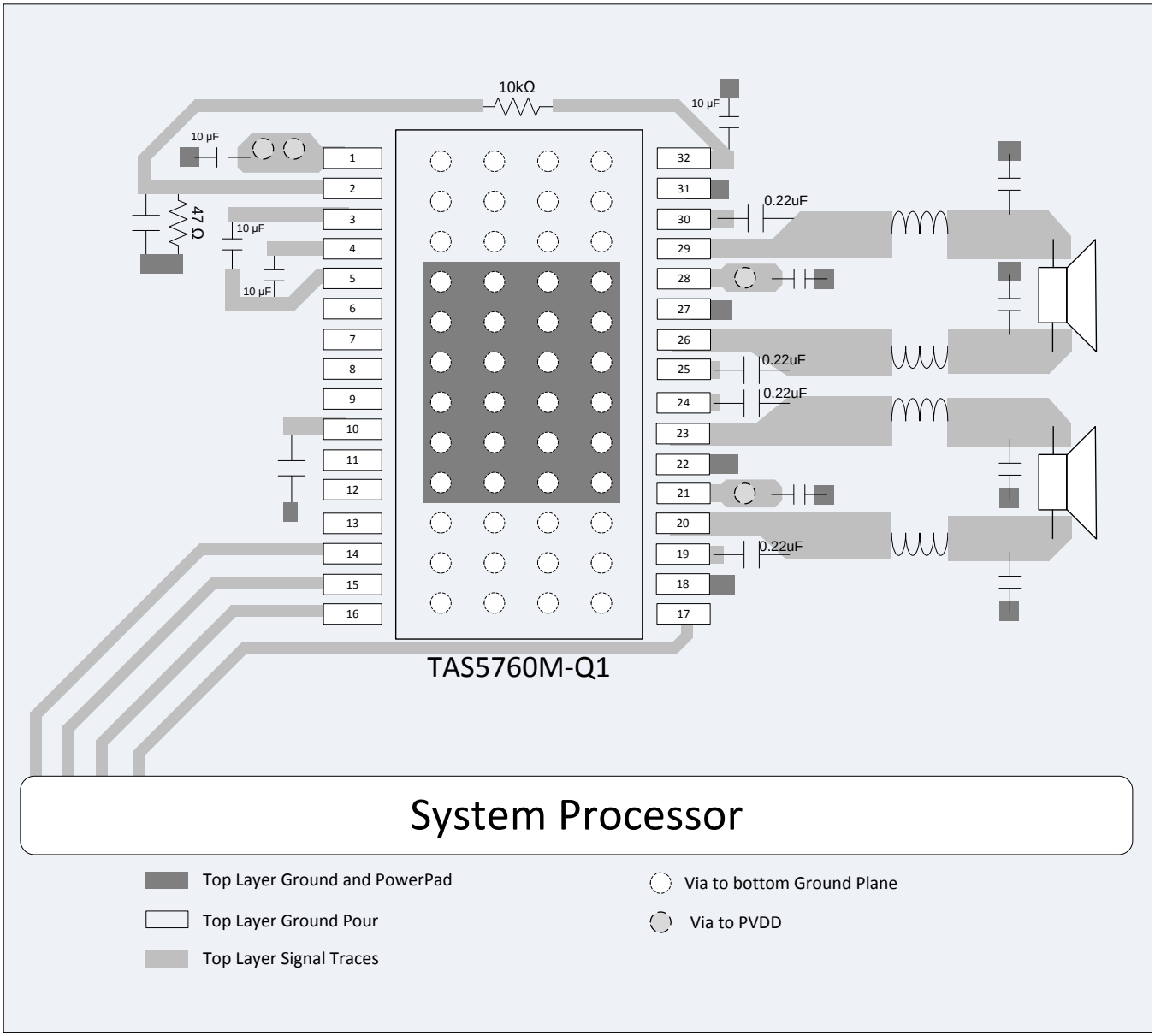


Figure 69. DAP Package BTL Configuration

Layout Example (continued)

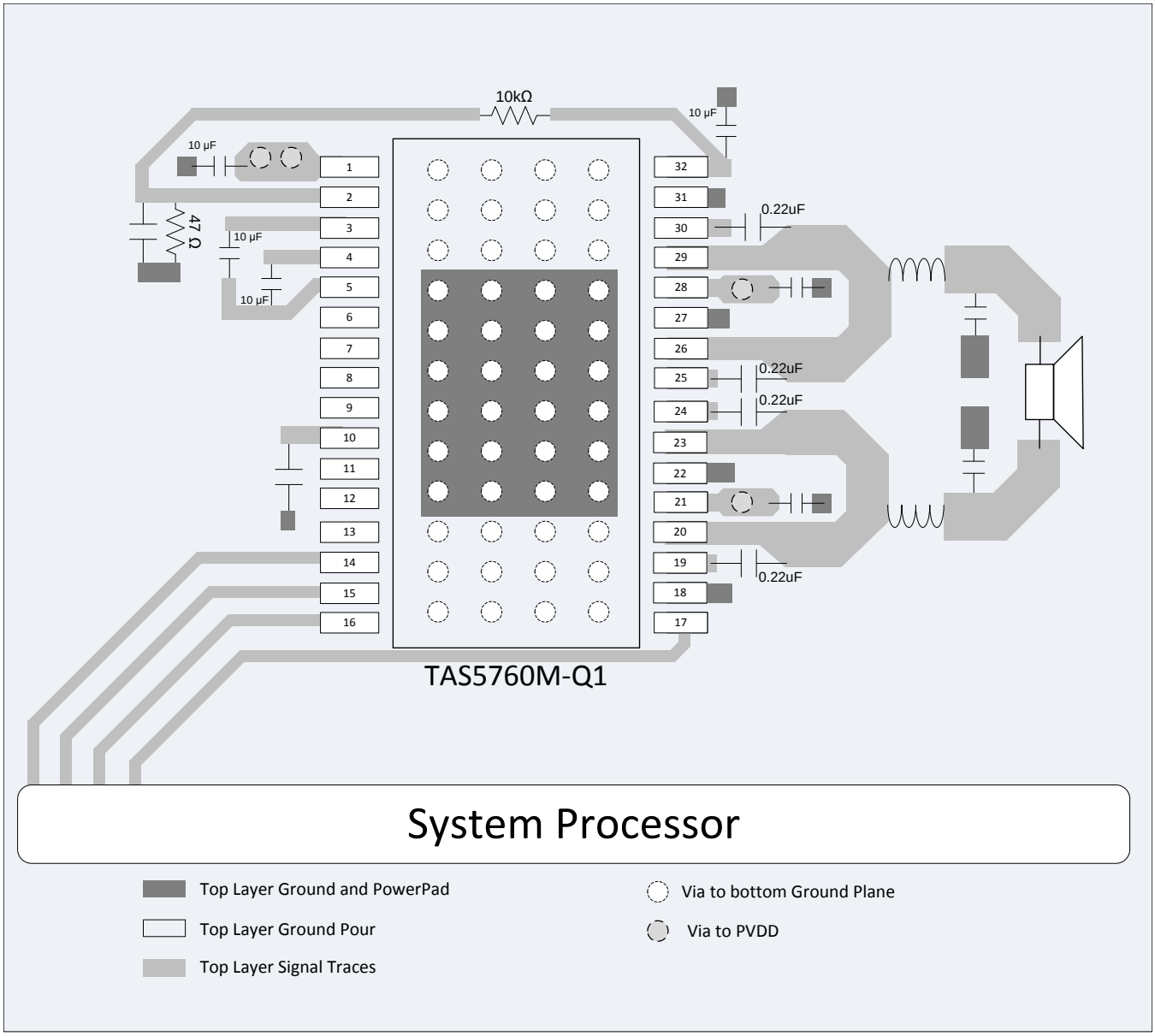


Figure 70. DAP Package PBTL Configuration

Layout Example (continued)

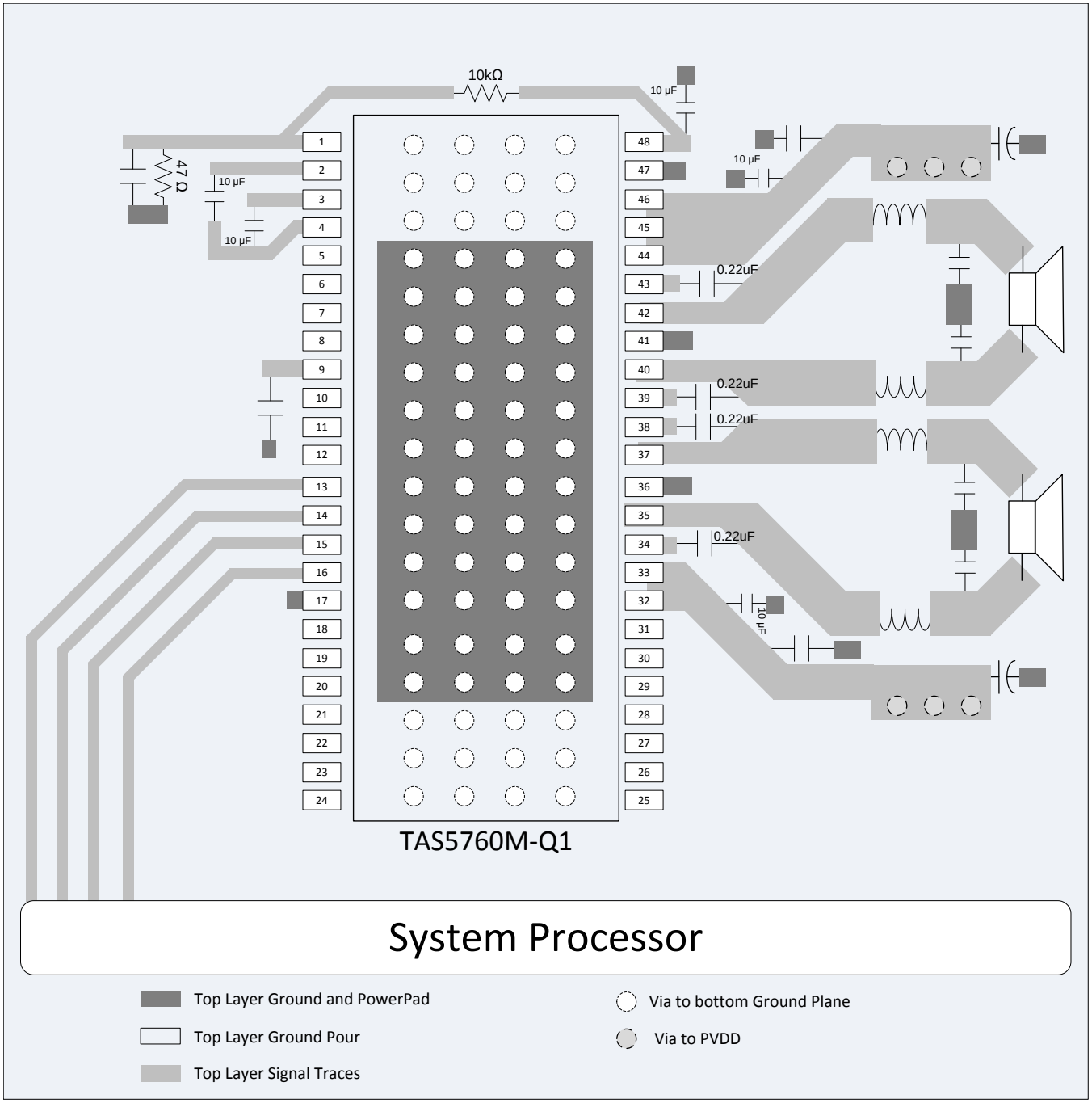


Figure 71. DCA Package BTL Configuration

Layout Example (continued)

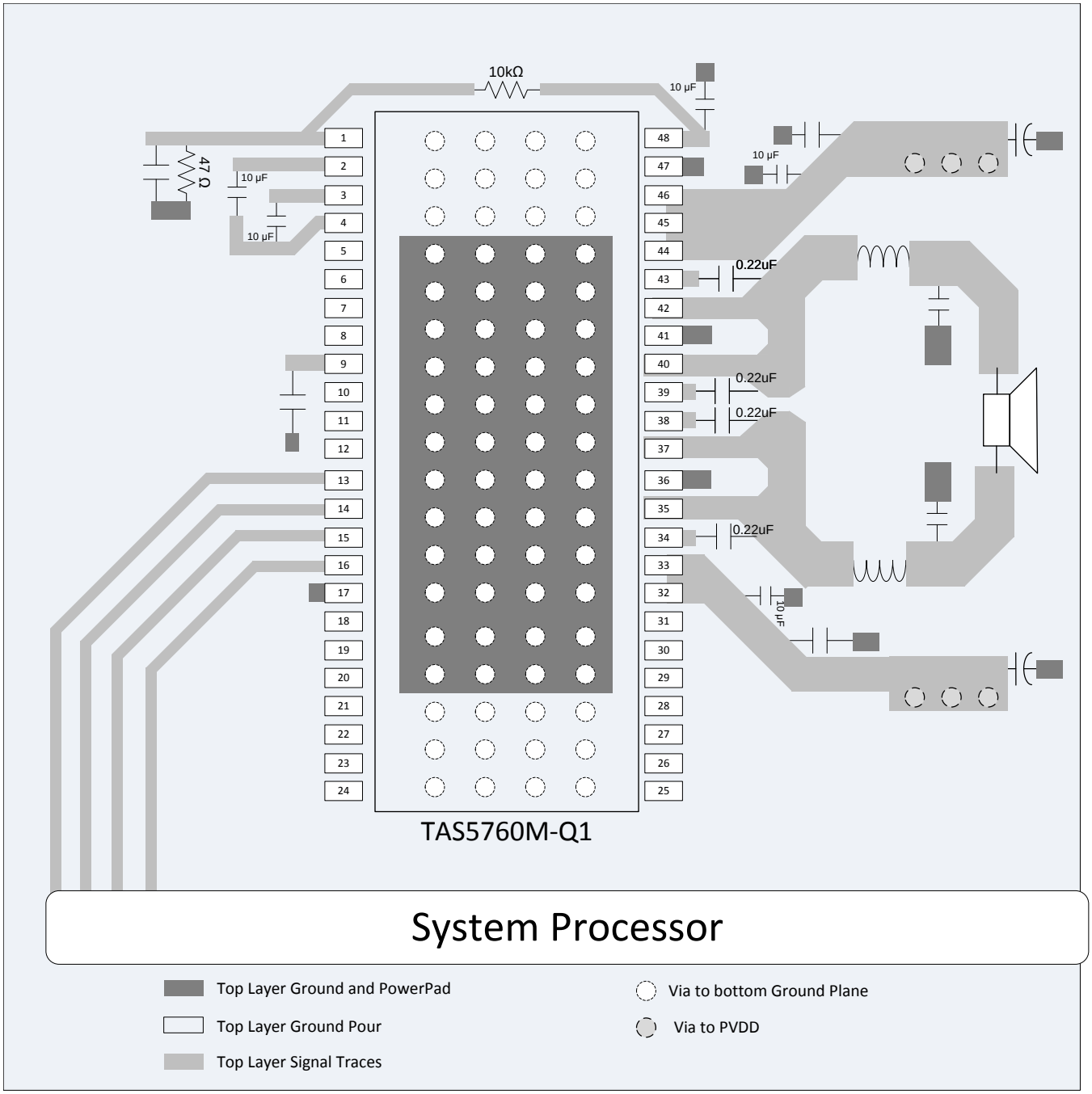


Figure 72. DCA Package PBTL Configuration

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

- TI FilterPro program available at: http://focus.ti.com/docs/toolsw/folders/print/filterpro.html
- *TAS5760xx EVM User's Guide*, SLOU371

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided *AS IS* by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTAS5760MTDAPRQ1	ACTIVE	HTSSOP	DAP	32	2000	TBD	Call TI	Call TI	-40 to 105		Samples
TAS5760MTDAPQ1	ACTIVE	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	5760MQ1	Samples
TAS5760MTDAPRQ1	ACTIVE	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 105	5760MQ1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TAS5760M-Q1 :

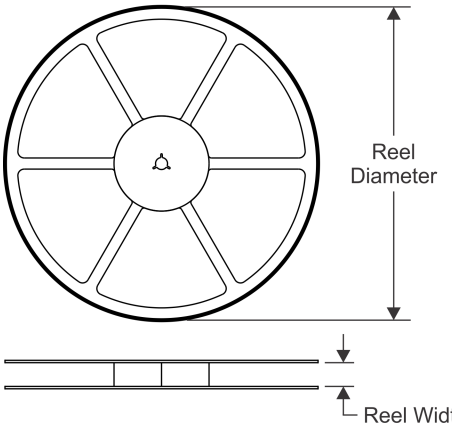
- Catalog: TAS5760M

NOTE: Qualified Version Definitions:

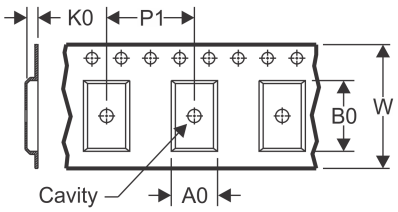
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

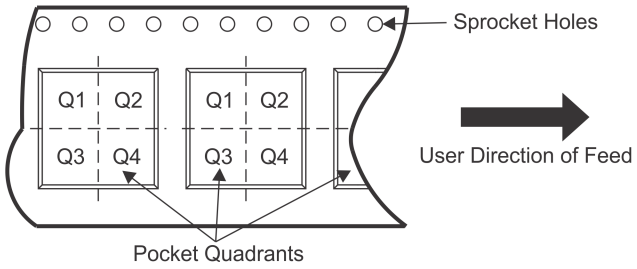


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

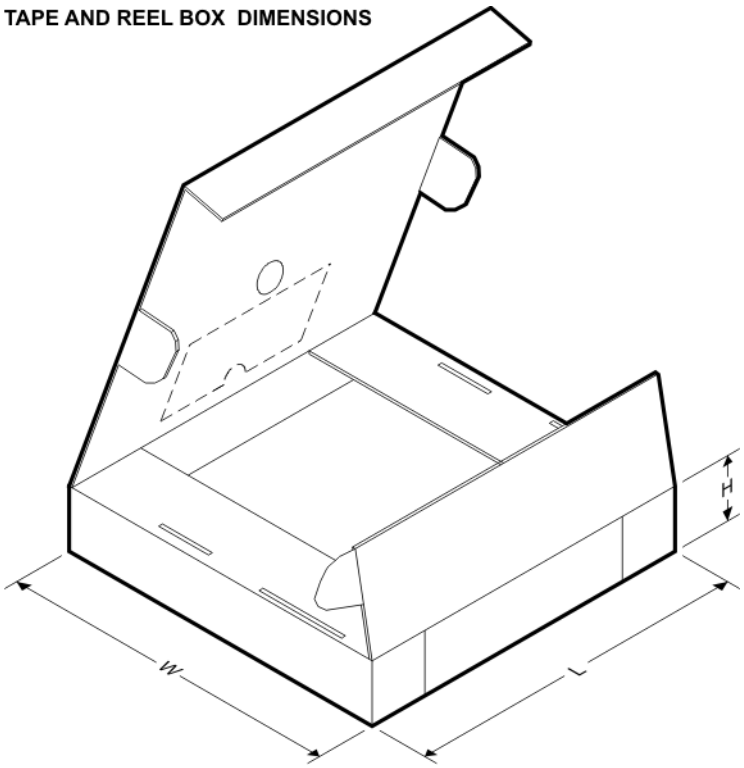
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5760MTDAPRQ1	HTSSOP	DAP	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1

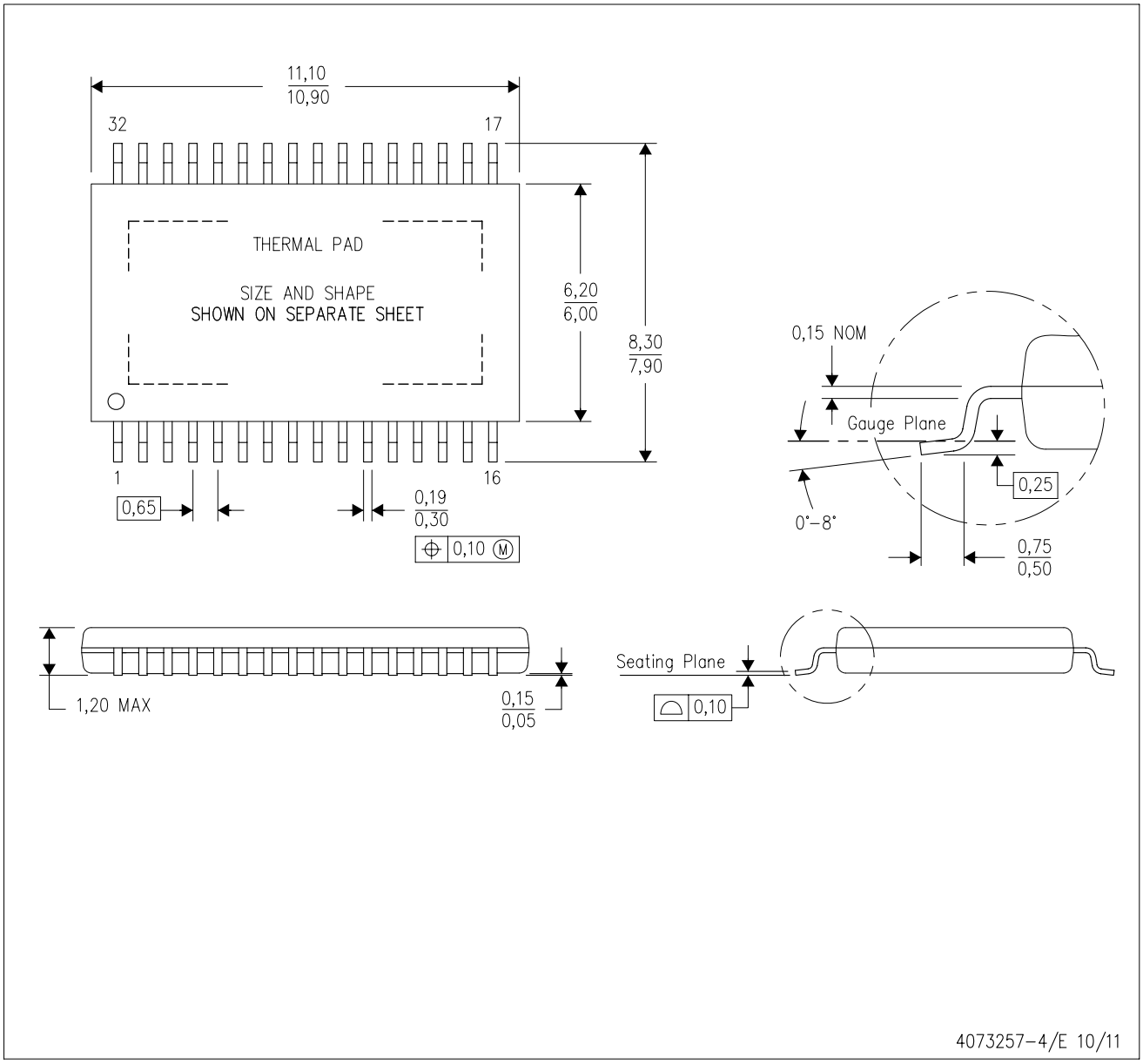
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5760MTDAPRQ1	HTSSOP	DAP	32	2000	367.0	367.0	45.0

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
F. Falls within JEDEC MO–153 Variation DCT.

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