Ordering number : EN4345A

Thick Film Hybrid IC

SANYO

STK6105

DC 3-phase Brushless Motor Driver (Output Current 5A)

Overview

The STK6105 is a hybrid IC incorporating a 3-phase brushless motor controller and driver into a single package, on the Sanyo IMST (Insulated Metal Substrate Technology) substrate. Revolution speed is controlled through the DC voltage level ($Vref_1$) external input and PWM control of motor phase winding current. The driver is MOSFET to minimize circuit loss and handle high-output current (rush current) demands.

Applications

- PPC and LBP drum motors
- Air conditioner fan motors

Features

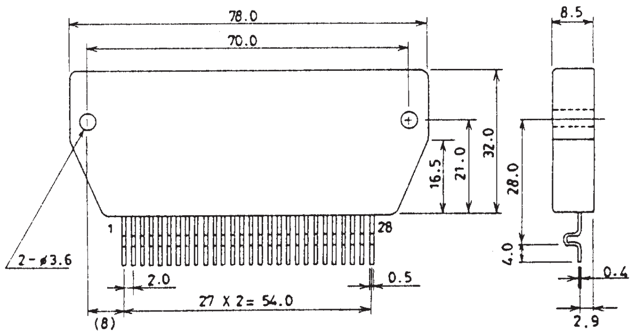
- The output driver transistor is MOSFET for low power loss (half that of a bipolar transistor) and reliable handling of high-output current (rush current).
- Variation in $Vref_1$ level causes the driver transistor to switch to PWM drive for high-efficiency motor speed variation.
- Normal and reverse revolution select function.
- Start/stop and brake functions.
- Current limiter function.

Package Dimensions

unit: mm

4130

[STK6105]



Specifications

Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage 1	$V_{CC}1$ max	No input signal	50	V
Maximum supply voltage 2	$V_{CC}2$ max	No input signal	7	V
Maximum output current	Io max	Position detect input signal cycle = 30 ms, PWM duty = 50%, operation time 1s	8	A
Operating substrate temperature	Tc max		105	°C
Junction temperature	Tj max		150	°C
Storage temperature	Tstg		-40 to +125	°C

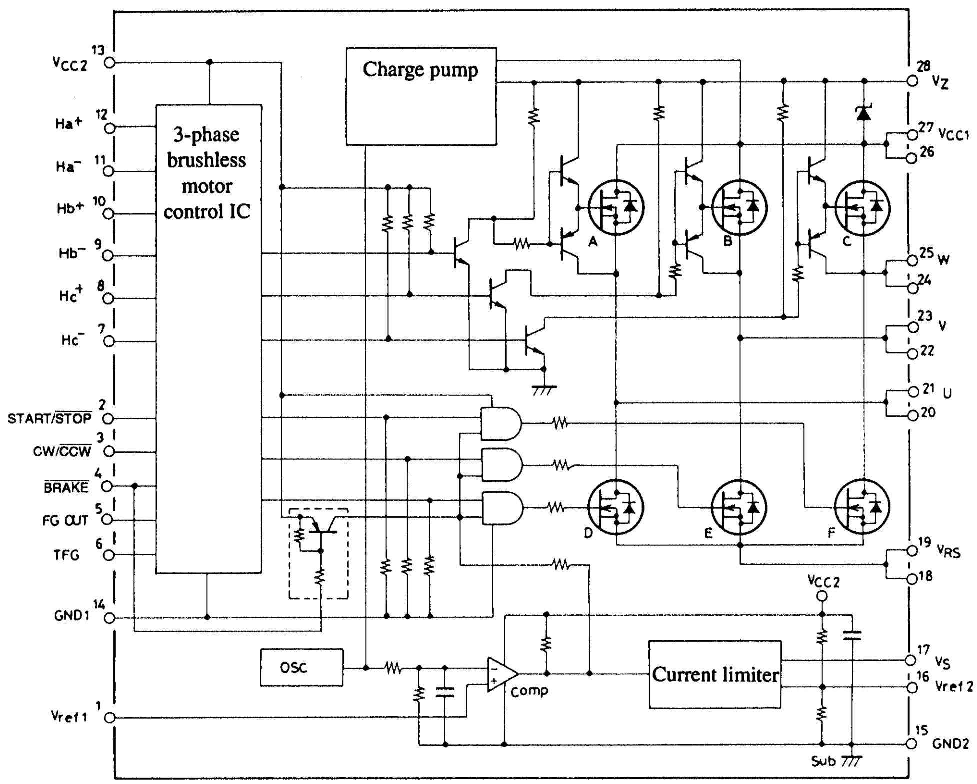
Allowable Operating Ranges at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	$V_{CC}1$	With input signal	16 to 42	V
Output current	Io ave	DC phases present	5	A
Supply voltage 2	$V_{CC}2$	With input signal	4.75 to 6.00	V
Brake current	I_{OB}	80 Hz full sine waves (all phases). Operating time 0.1 s, duty = 5% (see Note 1).	11	A

Electrical Characteristics at Tc=25°C, $V_{CC}1$ = 24V, $V_{CC}2$ = 5.0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current 1 (pin 13)	$I_{CCO}1$	CW revolution		12	20	mA
Supply current 2 (pin 13)	$I_{CCO}2$	Braking		26	38	mA
Output saturation voltage 1	Vst1	$V_{CC}1$ sideTR, Io = 5A		0.70	0.91	V
Output saturation voltage 2	Vst2	GND sideTR, Io = 5A		0.85	1.11	V
Internal MOSFET diode forward voltage	V_F	I_F = 5A		1.0	1.5	V
PWM oscillation frequency	f_C		20	25	30	kHz
Current limiter reference voltage	Vref2		0.78	0.83	0.88	V
Position detect input sensitivity	V_H		20		500	mV
Position detect common mode range	CMRH		2.0		4.5	V
Input “L” current 1 (pins 2,3)	I_{IL1}	V_{IL1} = GND		130	200	µA
Input “L” voltage 1 (pins 2,3)	V_{IL1}				1.0	V
Input “L” current 2 (pin 4)	I_{IL2}	V_{IL2} = GND		570	910	µA
Input “L” voltage 2 (pin 4)	V_{IL2}				1.0	V
$Vref_1$ “H” voltage	$Vref_{1H}$	GND side transistor not in PWM		2.82	3.20	V
$Vref_1$ “L” voltage	$Vref_{1L}$	GND side transistor off	0.15	0.35		V
Zener voltage	V_Z		5.7	6.2	6.7	V
FG output current	I_{FGH}	V_{FG} = 1.6V	80			µA
FG output “L” voltage	V_{FGL}	I_{FG} = 0.3mA			0.4	V
FG output pulse width	t_{FG}	C_F = 0.1µF, R_F = 10kΩ	0.9	1.0	1.1	ms

Equivalent Circuit



Pin Functions

Pin No.	Symbol	Function
1	$Vref_1$	GND-side driver transistor PWM control pin; range 0.15 to 3.2V
2	START/$\overline{\text{STOP}}$	"H" = start, "L" = stop (all transistors off)
3	CW/$\overline{\text{CCW}}$	"H" = CW, "L" = CCW
4	$\overline{\text{BRAKE}}$	"H" = rotate, "L" = Only GND-side transistor on
5	FG OUT	Position detect signal: output 6 pulses per cycle
6	TFG	For setting FG OUT "L" level pulse width. R_F and C_F pins.
7	H_{C-}	Motor position detect signal input pin (to Hall device)
8	H_{C+}	Motor position detect signal input pin (to Hall device)
9	H_{b-}	Motor position detect signal input pin (to Hall device)
10	H_{b+}	Motor position detect signal input pin (to Hall device)
11	H_{a-}	Motor position detect signal input pin (to Hall device)
12	H_{a+}	Motor position detect signal input pin (to Hall device)
13	$V_{CC}2$	Motor controller supply voltage pin
14	GND1	Motor controller IC GND pin; signal gnd (SG)
15	GND2	External R_S GND-side connection pin; power gnd (PG)
16	$Vref_2$	Current limiter set pin; $0.167V_{CC}2$ when open.
17	V_S	External R_S current limiter detect pin
18, 19	V_{RS}	External R_S connect pin
20, 21	U	Output pin (to motor winding)
22, 23	V	Output pin (to motor winding)
24, 25	W	Output pin (to motor winding)
26, 27	$V_{CC}1$	Supply voltage pin (to motor)
28	V_Z	Zener voltage (6.2V typ) for $V_{CC}1$ driver transistor date source supply

Input Type

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<tr><th>Input pin No.</th><th>Type</th></tr>
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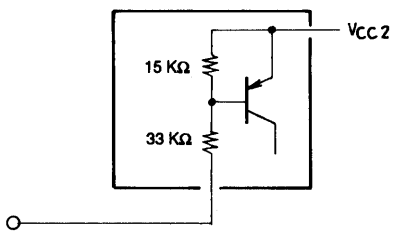
③</td><td>
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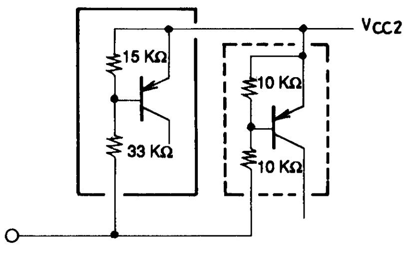
<tr><td>④</td><td>
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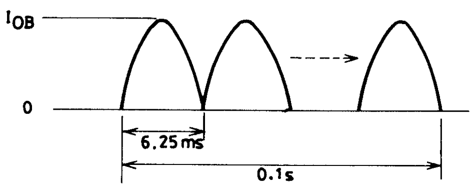
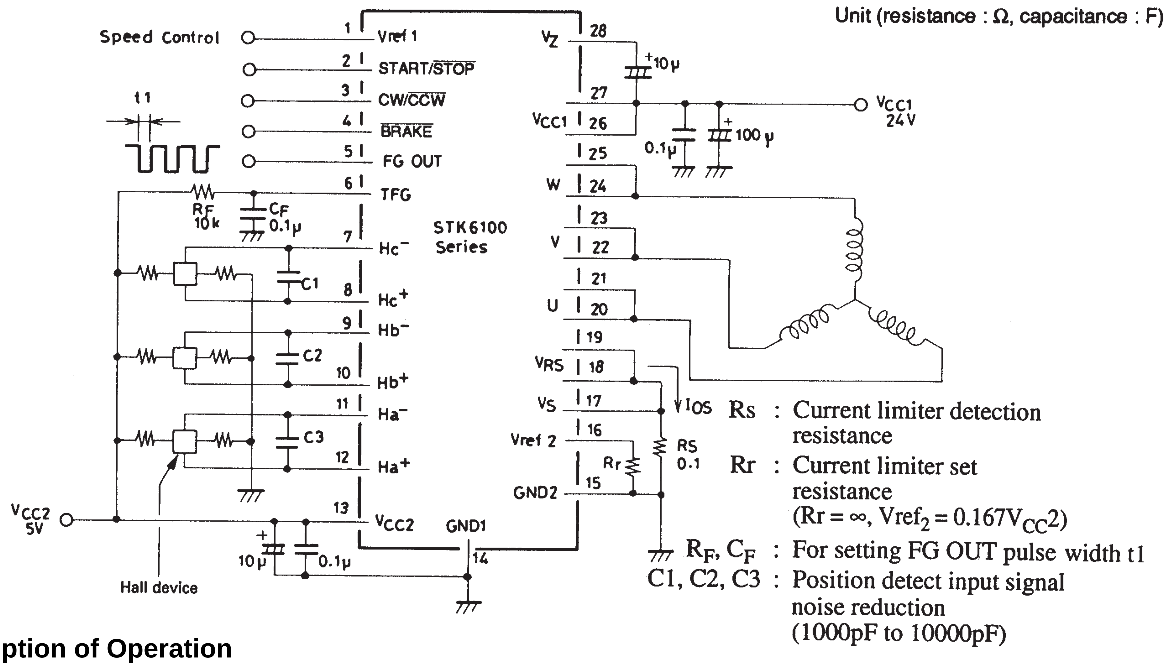
Note 1: I_{OB} indicates the operating current waveform peak as shown below.



Sample Application Circuit



Description of Operation

The DC 3-phase brushless motor generally uses a permanent magnet for the rotor and places the stator coil around it. When the rotor and stator coil are excited, magnetic force is generated between the poles, which is used for revolution torque. For efficient revolution it is necessary to know precisely where the rotor pole is in relation to the stator pole. In the brushless motor Hall devices and Hall ICs are widely used for this purpose, by detecting the electric power generated along the lines of magnetic force.

(1) Motor rotating force

The block diagram for this HIC is given in Fig. 2.

The conditions before input of $V_{CC}1$, with $V_{CC}2$ on, are START/$\overline{STOP}$ pin H level, CW/$\overline{CCW}$ pin H level, $\overline{BRAKE}$ pin H level and $Vref_1$ pin (speed control input) H level. The position detect signal at this time, due to the effect of the rotor magnetic field, will be output signals from 1 or 2 devices (of the 3) so that $H_{X+}>H_{X-}$ is input to HIC pins 7-12. The signals input to pins 7-12 are input to the motor controller and converted into signals compatible with 3-phase brushless motor revolution. When $V_{CC}1$ is supplied the charge pump circuit activates, generating $V_{CC}1$ MOSFET gate voltage V_Z. This outputs excitation current to the motor phase windings as indicated in the timing chart (Fig. 3), and rotating the motor.

For revolution speed control, the $Vref_1$ pin voltage is converted and used for PWM drive to increase GND transistor efficiency, controlling the conduction of motor current Io (Fig. 1). Control of Io means control of power supplied to the motor, which controls motor rpm. In general motor rpm N is proportional to the PWM on duty (when motor load is constant). The PWM on duty is proportional to the size of $Vref_1$ (see Fig. 13), and the relation of N is as outlined below.

$$N \propto \text{PWM ON Duty} \propto Vref_1$$

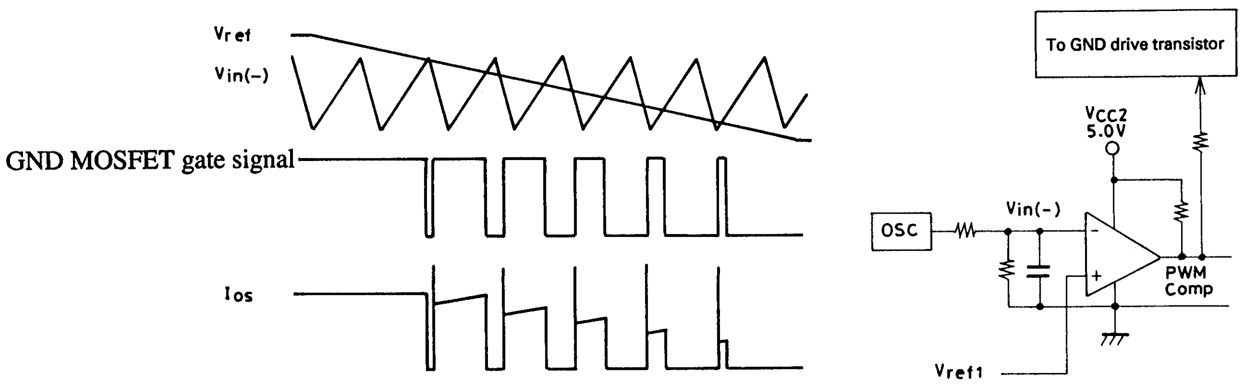
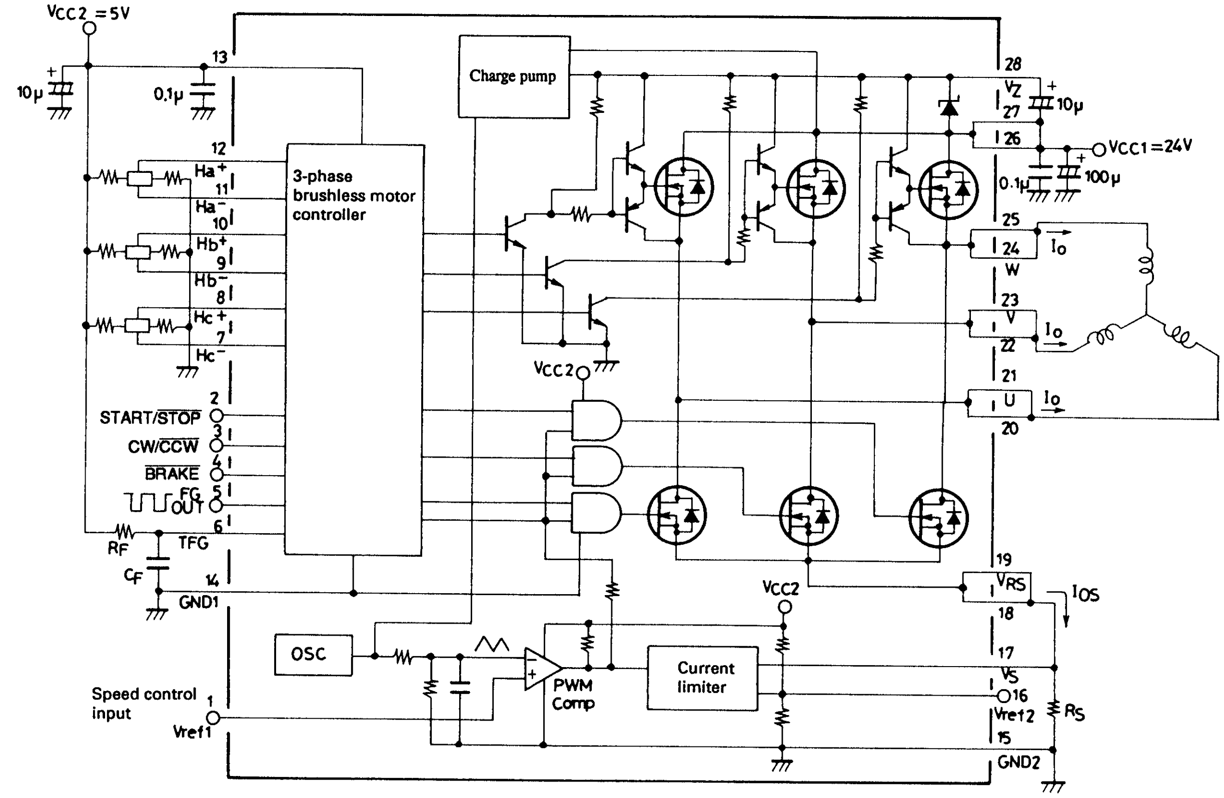


Fig.1 PWM Drive Principle

Motor revolution is stopped by setting START/$\overline{\text{STOP}}$ to L level to turn off all drive transistors, and cut the supply of current to the motor. Motor inertia will prevent instantaneous stopping. The brake function works to shorten the amount of time needed to come to a complete stop. In input level L the $V_{CC}1$ driver transistor is turned off, all GND driver transistors are turned on, and the amount of power generated by the rotating motor windings reduced to reduce the rpms. This brake function has priority over all START/$\overline{\text{STOP}}$, CW/$\overline{\text{CCW}}$ and position detect input conditions.



Unit (capacitance : F)

Fig. 2 Block Diagram

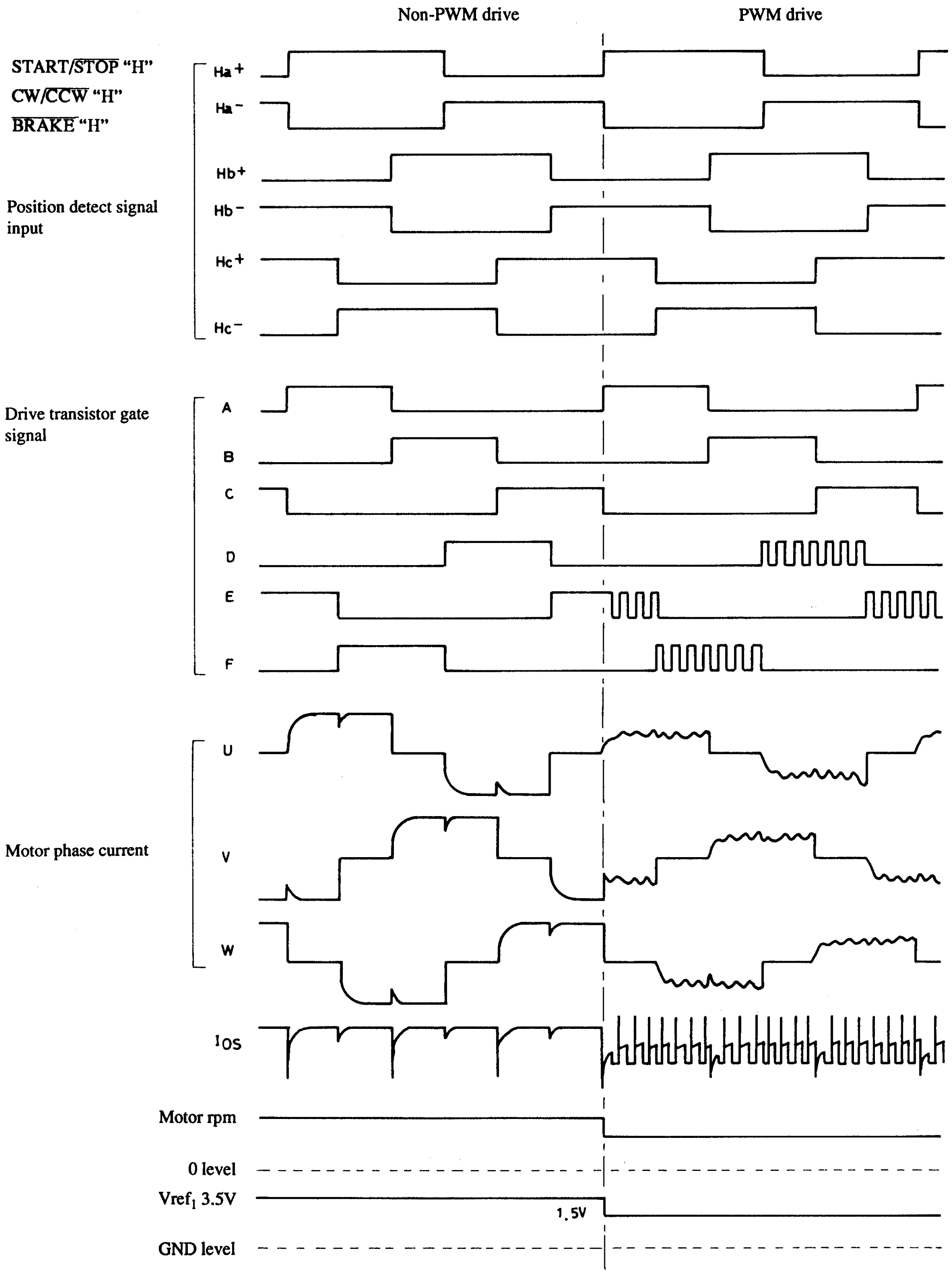


Fig. 3 I/O Timing Chart

(2) Other functions

① CW/$\overline{CCW}$

The direction of motor revolution can be selected by setting the input level to H or L. CW is H level and CCW is L level. The CW timing chart is indicated in Fig. 3, and the CCW timing chart in Fig. 5.

② Current limiter function

The current limiter converts the GND driver transistor source current into V_{RS} through the external R_S, and controls GND driver transistor conduction based on a comparison of this voltage to $Vref_2$. $Vref_2$ generates a $0.167V_{CC}2$ voltage in pin open state. $Vref_2$ is generated by the voltage division between 15 kΩ and 3 kΩ resistances, and so the $Vref_2$ level can be readily reduced by attaching an external resistor. To prevent HIC destruction in the event of motor lock, a current limiter can be enabled by setting $Vref_2$ at or below Io ave. If no such protection is required, set $Vref_2$ between Io max and Io ave to limit rush current.

③ FG OUT

This pin outputs a square wave pulse proportional to one motor revolution, which can be used as the motor servo-control PLL IC FG input signal. The square wave L level time t_1 is set by the time constant of C_F and L_F connected to the TFG pin (Fig. 4).

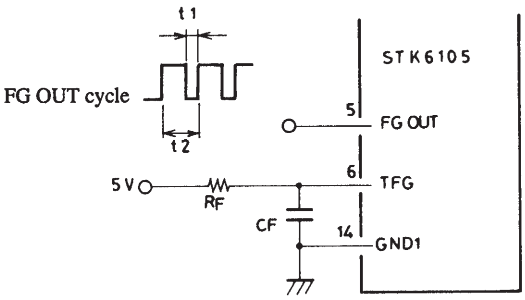


Fig. 4

In general, when the n-pole 3-phase brushless motor fixed-speed rpm is expressed as N(rpm), the setting for t_1 so that $t_1 = 0.5\ t_2$ is given by expression ①.

$$t_1 = \frac{1000}{\frac{N}{60} \times 6 \times \frac{n}{2}} \times 0.5 \quad [\mathrm{ms}] \cdots\cdots ①$$

The relation between C_F, R_F and t_1 is given by expression ②.

$$t_1 = a \cdot R_F \cdot C_F \cdots\cdots ②$$

$$\text{However, } a = 1 \left(\frac{s}{\Omega \cdot F}\right),\ R_F = 3\ k\Omega \text{ to } 30\ k\Omega,\ t_1 > 50\ \mu s$$

Expression ① is designed to be half that of fixed speed t_2, but when an FV conversion circuit is connected to the FG OUT pin, it is necessary to reduce the duty to under 50%. In this case, adjust R_F or C_F as needed.

(3) Precautions in drive

① Start current (rush current)

The motor start Rs current waveform is shown in Fig. 6. Current peak I_{OH} must not exceed Io max.

② Position detect signal

Because signal input sensitivity V_H is ±500 mV max, the level of the output signal (open collector) from the Hall IC must be reduced through conversion. A sample of this circuit is shown in Fig. 7. The position detect signal must be compatible with the motor phase winding even in the time chart state shown in Fig. 3, or the motor may not revolve smoothly.

③ Motor phase winding current during braking

The motor phase winding current during braking must not exceed Io max even during peak, although several times set current levels are input.

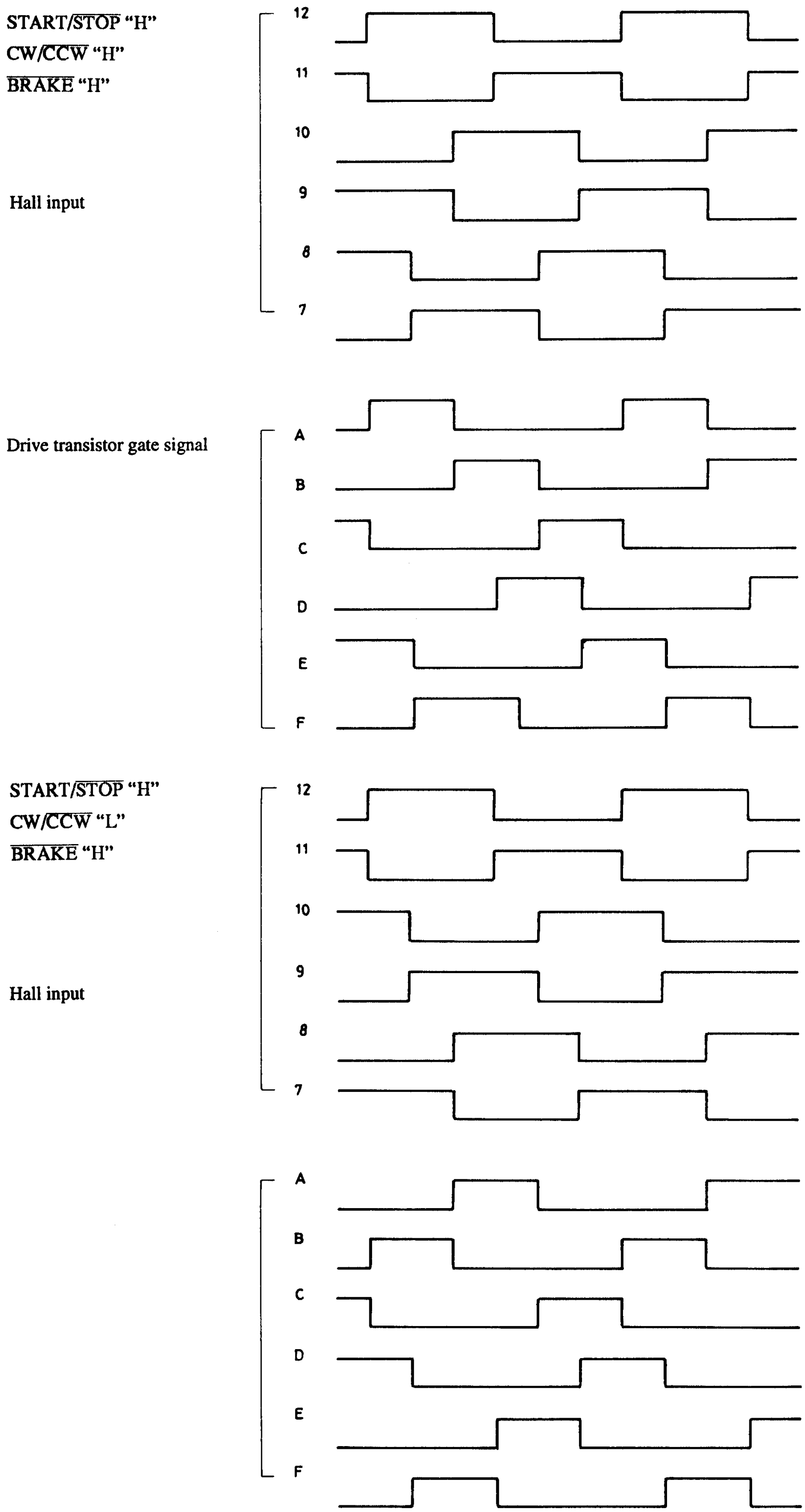


Fig. 5 CW/$\overline{\text{CCW}}$ I/O Timing Chart

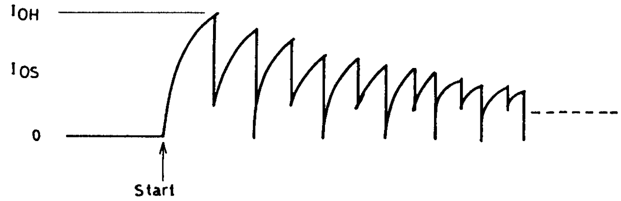
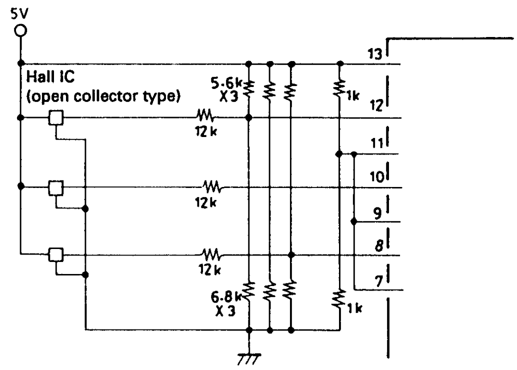


Fig.6 Starting Current



Unit (resistance: Ω)

Fig.7 Conversion Circuit for Hall IC and Hall Device Signal

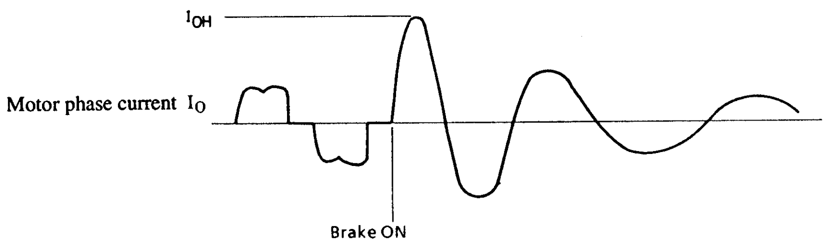


Fig.8

Thermal Radiation Design

(1) Internal average power dissipation Pd

The driver transistors represent the majority of the power dissipation in operation. Other losses are $V_{CC}2$ and the charge pump circuit. In PWM drive in particular, the diode in the $V_{CC}1$ transistor is being used as a flywheel diode, increasing $V_{CC}1$ transistor loss. When these are included, internal mean power dissipation is:

$$Pd = Io\ (Vst_1 + V_F d_2 + Vst_2 d_1) + Pd_A + Pd_B + Pd_C \quad \cdots\cdots ①$$

Io : Motor current
Vst_1 : $V_{CC}1$ transistor saturation voltage
Vst_2 : GND transistor saturation voltage
d_1 : GND transistor PWM operation on duty
d_2 : GND transistor PWM operation off duty
Pd_A : $V_{CC}2$ loss
Pd_B : Charge pump circuit loss
Pd_C : GND transistor switching loss
V_F : $V_{CC}1$ transistor internal diode normal direction voltage

Because the driver transistor is a MOSFET, Vst_1 and Vst_2 will increase with an increase in I_O or substrate temperature Tc.

Pd_A and Pd_B are generally given as:

$$Pd_A \approx V_{CC}2 \times I_{CCO1} \quad \cdots\cdots ②$$
$$Pd_B \approx V_{CC}1 \times (0.49V_{CC}1 - 4.2) \times 0.001 \quad \cdots\cdots ③$$

where, $V_{CC}1$ = 16 to 42V

Refer to Figs. 11-14 for data on Vst_1, Vst_2, d_1 and V_F.

(2) Thermal radiation design

Actual thermal radiation design requires determination of the IC internal average power Pd from the motor phase current Io (Fig. 9). Pd is then used to determine the thermal resistance for the radiator from the following expression.

$$\theta c - a = \frac{Tc\ max - Ta}{Pd}\ (°C/W)$$

where Tc max = 105°C
Ta = ambient temperature

With a 2.00 mm radiation plate, the required area can be determined form Fig. 10. Note that substrate temperature will vary widely with set internal air temperature, and Tc for the mounted state must be 105°C max.

Fig.9 Pd – I_O (for example)

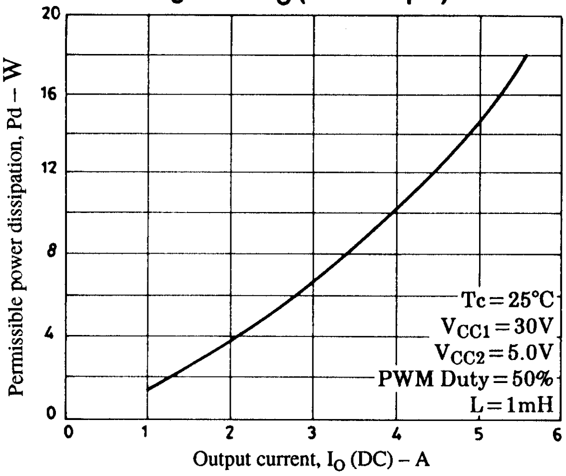


Fig. 10 θ – S

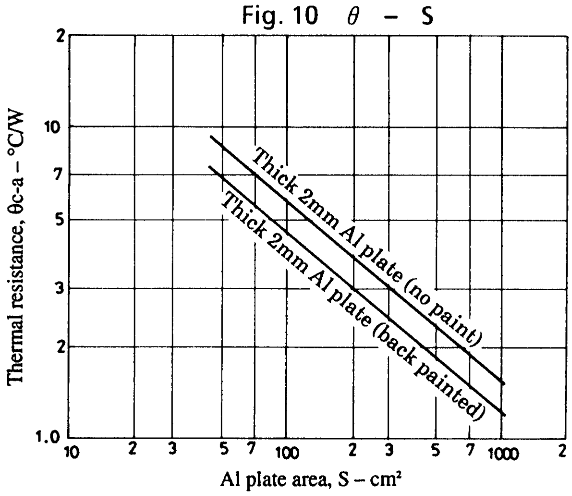


Fig. 11 Vst_1 – I_O

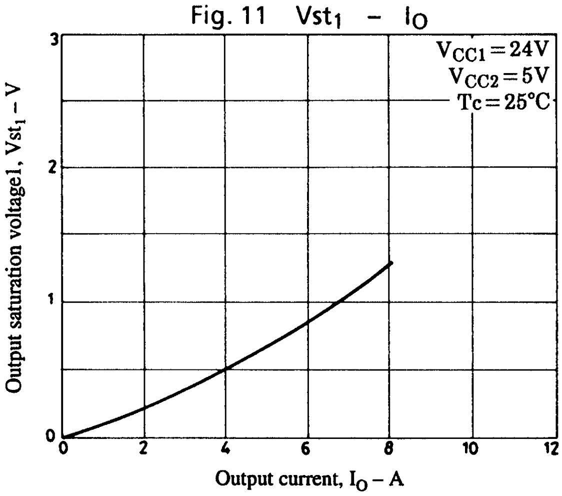


Fig. 12 Vst_2 – I_O

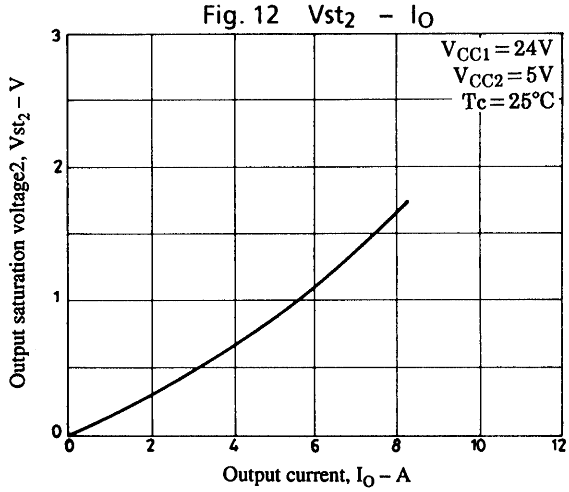


Fig. 13 $Vref_1$ – d_1

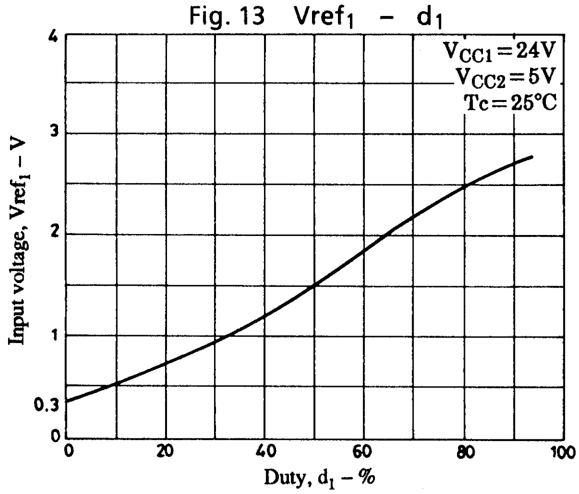


Fig. 14 I_F – V_F

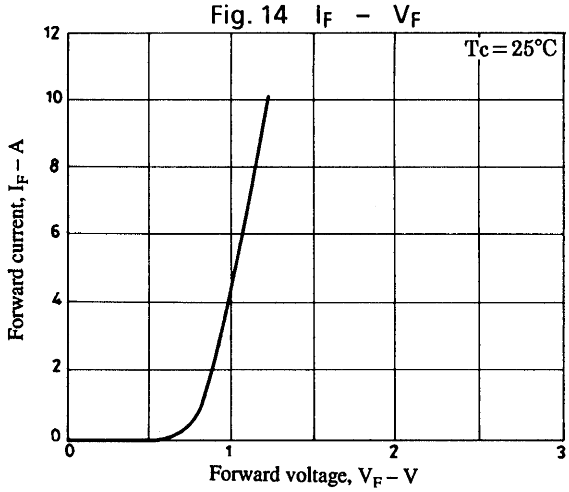
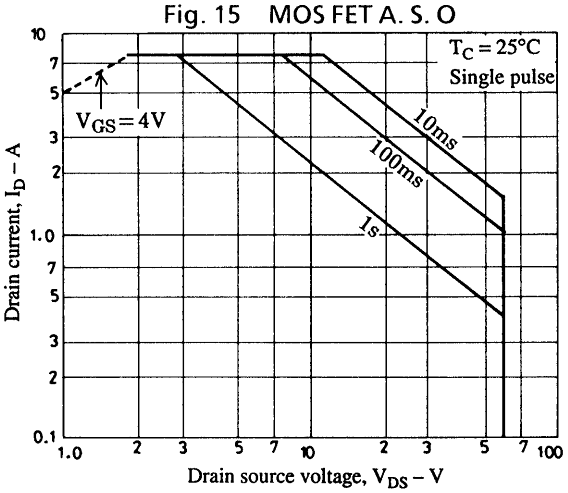


Fig. 15 MOS FET A. S. O



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