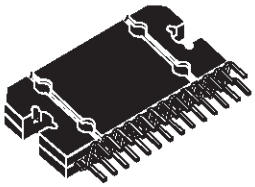
STA530

4 X 30W STEREO BASH® POWER AMPLIFIER

TARGET SPECIFICATION

- MONOCHIP BRIDGE QUAD CONFIGURABLE AMPLIFIER OPTIMIZED FOR BASH® ARCHITECTURE
- 4 X 30W OUTPUT POWER @ R_L = 4/8 Ω, THD = 1% or (2 X 30W + 1 X 60W) or (2 X 60W)
- PRECISION RECTIFIERS TO DRIVE THE BUCK REGULATOR
- ON-OFF SEQUENCE/ TIMER WITH MUTE AND STANDBY
- PROPORTIONAL OVER POWER OUTPUT CURRENT TO LIMIT THE BUCK REGULATOR
- ABSOLUTE POWER BRIDGE OUTPUT TRANSISTOR POWER PROTECTION
- ABSOLUTE OUTPUT CURRENT LIMIT
- INTEGRATED THERMAL PROTECTION
- POWER SUPPLY OVER VOLTAGE PROTECTION



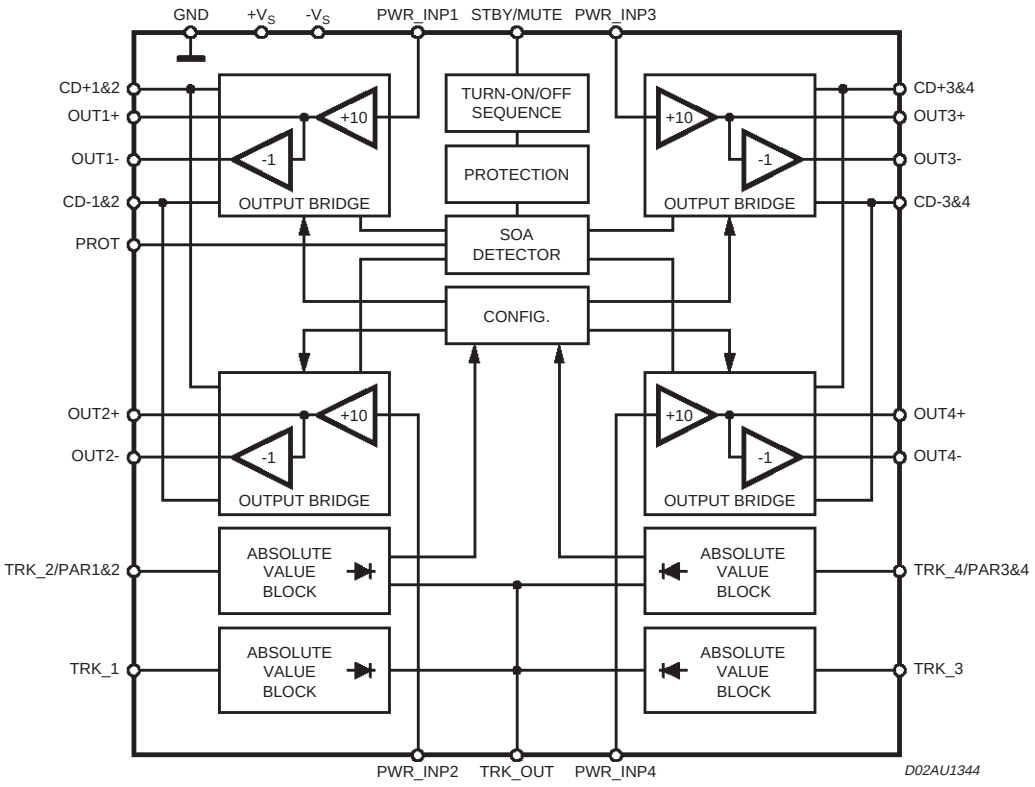
FLEXIWATT27

- FLEXIWATT POWER PACKAGE WITH 27 PIN
- **BASH® LICENCE REQUIRED**

DESCRIPTION

The STA530 is a BASH® power amplifier where BASH® means “High Efficiency”.

BLOCK DIAGRAM



DESCRIPTION (continued)

In fact it's permits to build a BASH® architecture amplifier adding only few external components and a variable Buck regulator tracking the audio signal. Notice that normally only one Buck regulator is used to supply a multichannel amplifiers system , therefore most of the functions implemented in the circuit have a summing output pin.

The signal circuits are biased by fixed negative and positive voltages referred to Ground. Instead the final stages of the output amplifiers are supplied by two external voltages that are following the audio signal . In this way the headroom for the output transistors is kept at minimum level to obtain a high efficiency power amplifier.

The circuit contains all the blocks to build a configurable four channel amplifier.

The tracking signal for the external Buck regulator is generated from the Absolute Value Block (AVB) that rectifies the audio signal. The outputs of these blocks are decoupled by a diode to permit an easy sum of this signal for the multichannel application. The gain of the stage AVB is equal to 70 (+36.9 dB). A sophisticated circuit performs the output transistor power detector that , with the buck regulator, reduces the power supply voltage . Moreover, a maximum current output limiting and the over temperature sensor have been added to protect the circuit itself. The external voltage applied to the STBY/MUTE pin forces the two amplifiers in the proper condition to guarantee a silent turn-on and turn-off.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$+V_S$	Positive supply voltage referred to pin 14 (GND)	27	V
$-V_S$	Negative supply voltage referred to pin 14 (GND)	-27	V
V_{CD+}	Positive supply voltage tracking rail referred to pin 14 (GND)	20	V
V_{CD-}	Negative supply voltage referred to -Vs (1)	-0.3	V
V_{CD-}	Negative supply voltage tracking rail referred to pin 14 (GND)	-20	V
V_{PWR_Imp1} V_{PWR_Imp2} V_{TRK_1} V_{TRK_2}	Pin 11, 10, 9, 8 Negative & Positive maximum voltage referred to GND (pin 14)	-25 to +25	V
$V_{PWR\_Imp\ 3}$ $V_{PWR\_Imp\ 4}$ V_{TRK_3} V_{TRK_4}	Pin 17, 18, 19, 20 Negative & Positive maximum voltage referred to GND (pin 14)	-25 to +25	V
$I_{STBY-max}$	Pin 12 maximum input current (Internal voltage clamp at 5V)	500	µA
$V_{STBY/MUTE}$	Pin 12 negative maximum voltage referred to GND (pin 14)	-0.5	V

Notes: 1. V_{CD-} must not be more negative than -Vs

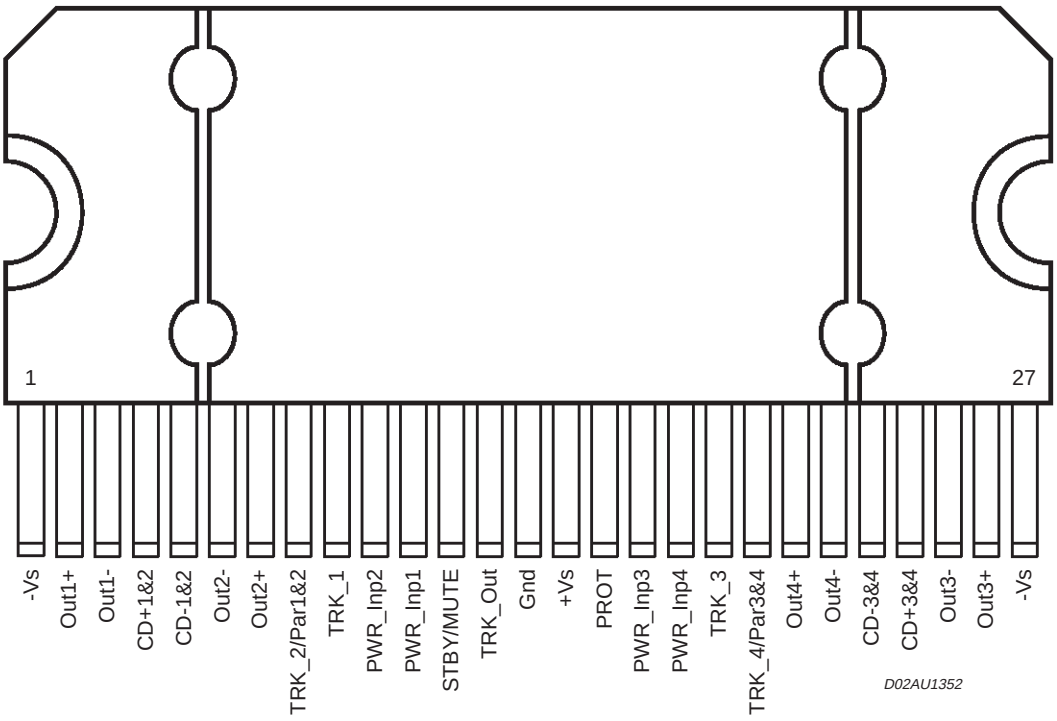
THERMAL DATA

Symbol	Parameter		Value	Unit
T_j	Max Junction temperature		150	°C
$R_{th\ j\_case}$	Thermal Resistance Junction to case	max	1	°C/W

OPERATING RANGE

Symbol	Parameter	Value	Unit
$+V_S$	Positive supply voltage	+15 to +25	V
$-V_S$	Negative supply voltage	-15 to -25	V
ΔV_{S+}	Delta positive supply voltage	5V ≤ (Vs+ - VCD+) ≤ 10V	V
V_{CD+}	Positive supply voltage tracking rail	+3 to +15	V
V_{CD-}	Negative supply voltage tracking rail	-15 to -3	V
T_{amb}	Ambient Temperature Range	0 to 70	°C
I_{sb_max}	Pin 12 maximum input current (Internal voltage clamp at 5V)	200	µA

PIN CONNECTION



NOTE

Slug connected to PINs No. 1 & 27

PIN CONNECTION

N°	Name	Description
1	-Vs	Negative Bias Supply
2	Out1+	Channel 1 speaker positive output
3	Out1-	Channel 1 speaker negative output
4	CD+1&2	Channels 1 & 2 Time varying tracking rail positive power supply
5	CD-1&2	Channels 1 &2 Time varying tracking rail negative power supply
6	Out2-	Channel 2 speaker negative output
7	Out2+	Channel 2 speaker positive output
8	TRK_2/ Par1&2	Absolute value block input for channel 2,and parallel command for channels 1&2
9	TRK_1	Absolute value block input for channel 1
10	PWR_Inp2	Input to channel 2 power stage
11	PWR_Inp1	Input to channel 1 power stage
12	STBY/MUTE	Standby/mute input voltage control
13	TRK_Out	Absolute value block output
14	Gnd	Analog Ground
15	+Vs	Positive Bias Supply
16	PROT	Channel Protection signal for STABP01
17	PWR_Inp3	Input to channel 3 power stage
18	PWR_Inp4	Input to channel 4 power stage
19	TRK_3	Absolute value block input for channel 3
20	TRK_4/ Par3&4	Absolute value block input for channel 4,and parallel command for channels 3&4
21	Out4+	Channel 4 speaker positive output
22	Out4-	Channel 4 speaker negative output
23	CD-3&4	Channels 3 & 4 Time varying tracking rail negative power supply
24	CD+3&4	Channels 3 & 4 Time varying tracking rail positive power supply
25	Out3-	Channel 3 speaker negative output
26	Out3+	Channel 3 speaker positive output
27	-Vs	Negative Bias Supply

ELECTRICAL CHARACTERISTCS (Test Condition: Vs+ = 25V, Vs- = -25V, V_{CD+} = 15V, V_{CD-} = -15V, R_L = 8Ω, external components at the nominal value f = 1KHz, Tamb = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
TRACKING PARAMETERS						
G_{TRK}	Tracking reference voltage gain		66	70	74	
V_{TRK_out}	Tracking ref. output voltage		0	15		V
I_{TRK_out}	Current capability		5	6		mA
Z_{TRK_in}	Input impedance ($T_{RK1/2}$)			1		MΩ
V_{OFFSET}	Output traking DC offset			100		mV
OUTPUT BRIDGE						
G_{out}	Half Output bridge gain		19	20	21	dB
G_{ch}	Output bridge differential gain		25	26	27	dB
ΔG_{ch}	Output bridges gain mismatch		-1		1	dB
P_{out}	Continuous Output Power	THD = 1%		30		W
		THD = 10%		38		W
P_{out} 2 ch par	Continuous Output Power	THD = 1% RL = 4Ω		60		W
		THD = 10% R_L = 4Ω		76		W
THD	Total harmonic distortion of the output bridge	Po = 5W		0.01	0.1	%
		f = 20Hz to 20KHz; Po = 20W			0.2	%
V_{Off}	Output bridge D.C. offset		-100		100	mV
EN	Noise at Output bridge pins	f = 20Hz to 20KHz; Rg = 50Ω		60		µV
Z_{br_in}	Input impedance		100	140	180	KΩ
R_{dson}	Output power Rdson	I_O = 1A Tj=25° C		400	500	mΩ
$R_{dsonMAX}$	Maximum Output power Rdson	I_O = 1A		800		mΩ
OLG	Open Loop Voltage Gain			100		dB
GB	Unity Gain Bandwidth			6		MHz
SR	Slew Rate			8		V/µs
PROTECTION						
V_{STBY}	Stby voltage range		0		0.8	V
V_{MUTE}	Mute voltage range		1.6		2.5	V
V_{PLAY}	Play voltage range		4		5	V
T_{h1}	First Over temperature threshold			130		°C
T_{h2}	Second Over temperature threshold			150		°C

ELECTRICAL CHARACTERISTCS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Unbal. Ground	Upper Unbalancing ground threshold	Referred to $(CD^+ - CD^-)/2$		5		V
Unbal. Ground	Lower Unbalancing ground threshold	Referred to $(CD^+ - CD^-)/2$		-5		V
UV_{th}	Under voltage threshold	|Vs+| + |Vs-|	18		22	V
$P_{d\_reg.}$	Power dissipation threshold for system regulation	I_{prot} = 50µA; @ Vds = 8V	18	20	23	W
P_{d_max}	Switch off power dissipation threshold	@ Vds = 8V		30		W
$I_{prot\ Pd}$	Protection current slope	for Pd > Pd_{reg}		400		µA/W
$I_{prot\ Id}$	Protection current slope	for Id > Id_{reg}		400		µA/A
$I_{lct\ s}$	Limiting Current threshold “soft”		4	4.5	5	A
$I_{lct\ h}$	Limiting Current threshold “hard”		4.5	5	5.5	A
I+Vs	Positive supply current	Stby (Vstby/mute pin = 0V) Mute (Vstby/mute pin = 2.5V) Play (Vstby/mute pin = 5V no signal)		5 TBD TBD		mA mA mA
I-Vs	Negative supply current	Stby (Vstby/mute pin = 0V) Mute (Vstby/mute pin = 2.5V) Play (Vstby/mute pin = 5V no signal)		6 29 33		mA mA mA
ICD+	Positive traking rail supply current	Stby (Vstby/mute pin = 0V) Mute (Vstby/mute pin = 2.5V) Play (Vstby/mute pin = 5V no signal)		200 85 85		µA mA mA
ICD-	Negative traking rail supply current	Stby (Vstby/mute pin = 0V) Mute (Vstby/mute pin = 2.5V) Play (Vstby/mute pin = 5V no signal)		200 85 85		µA mA mA

FUNCTIONAL DESCRIPTION

The circuit contains all the blocks to build a configurable four channel amplifier.

In fact, only driving properly the TRK_2 (and TRK_4) pins, it's possible to change the chip configuration:

- 30 Watt x 4
- 30 Watt x 2 + 60 Watt x1 (TRK_2/Par1&2 or TRK_4/Par3&4 at -Vs)
- 60 Watt x 2 (TRK_2/Par1&2 and TRK_4/Par3&4 at -Vs)

Each single channel is based on the Output Bridge Power Amplifier, and its protection circuit. Moreover, a signal rectifier are added to complete the circuit.

The operation modes are driven by The Turn-on/off sequence block. In fact the IC can be set in three states by the Stby/mute pin:

STANDBY ($V_{pin} < 0.8V$), MUTE ($1.6V < V_{pin} < 2.5V$), and PLAY ($V_{pin} > 4V$).

In the Standby mode all the circuits involved in the signal path are uninhabited, instead

in Mute mode the circuits are biased but the Speakers Outputs are forced to ground potential.

These voltages can be get by the external RC network connected to Stby/Mute pin.

The same block is used to force quickly the I.C. In standby mode or in mute mode when the I.C. dangerous condition has been detected. The RC network in these cases is used to delay the Normal operation restore.

The protection of the I.C. are implemented by the Over Temperature, Unbalance Ground, Output Short circuit, Under voltage, and output transistor Power sensing as shown in the following table:

Table 1. Protection Implementation

Fault Type	Condition	Protection strategy	Action time	Release time
Chip Over temperature	Tj > 130 °C	Mute	Fast	Slow Related to Turn_on sequence
Chip Over temperature	Tj > 150 °C	Standby	Fast	Slow, Related to Turn_on sequence
Unbalancing Ground	|Vgnd| > ((CD+) - (CD-))/2 + 5V	Standby	Fast	Slow, Related to Turn_on sequence
Over Current	Iout > 4.5A	Reducing Buck regulator output voltage.	Related to the Buck regulator	Related to the Buck regulator
Short circuit	Iout > 5A	Standby	Fast	Slow, related to Turn_on sequence
Under Voltage	|Vs+| + |Vs-|< 20V	Standby	Fast	Slow, related to Turn_on sequence
Extra power dissipation at output transistor	Pd tr. > 18W	Reducing Buck regulator output voltage.	Related to the Buck regulator	Related to the Buck regulator
Maximum power dissipation at output transistor	Pd tr. > 30W	Standby	Fast	Slow, related to Turn_on sequence

ABSOLUTE VALUE BLOCK

The absolute value block rectifies the signal to extract the control voltage for the external Buck regulator. The output voltage swing is internally limited, the gain is internally fixed to 70.

The input impedance of the rectifier is very high , to allow the appropriate filtering of the audio signal before the rectification.

OUTPUT BRIDGE

The Output bridge amplifier makes the single-ended to Differential conversion of the Audio signal using two power amplifiers, one in non-inverting configuration with gain equal to 10 and the other in inverting configuration with unity gain. To guarantee the high input impedance at the input pins, PWR_Inp1....4, the second amplifier stages are driven by the output of the first stages respectively.

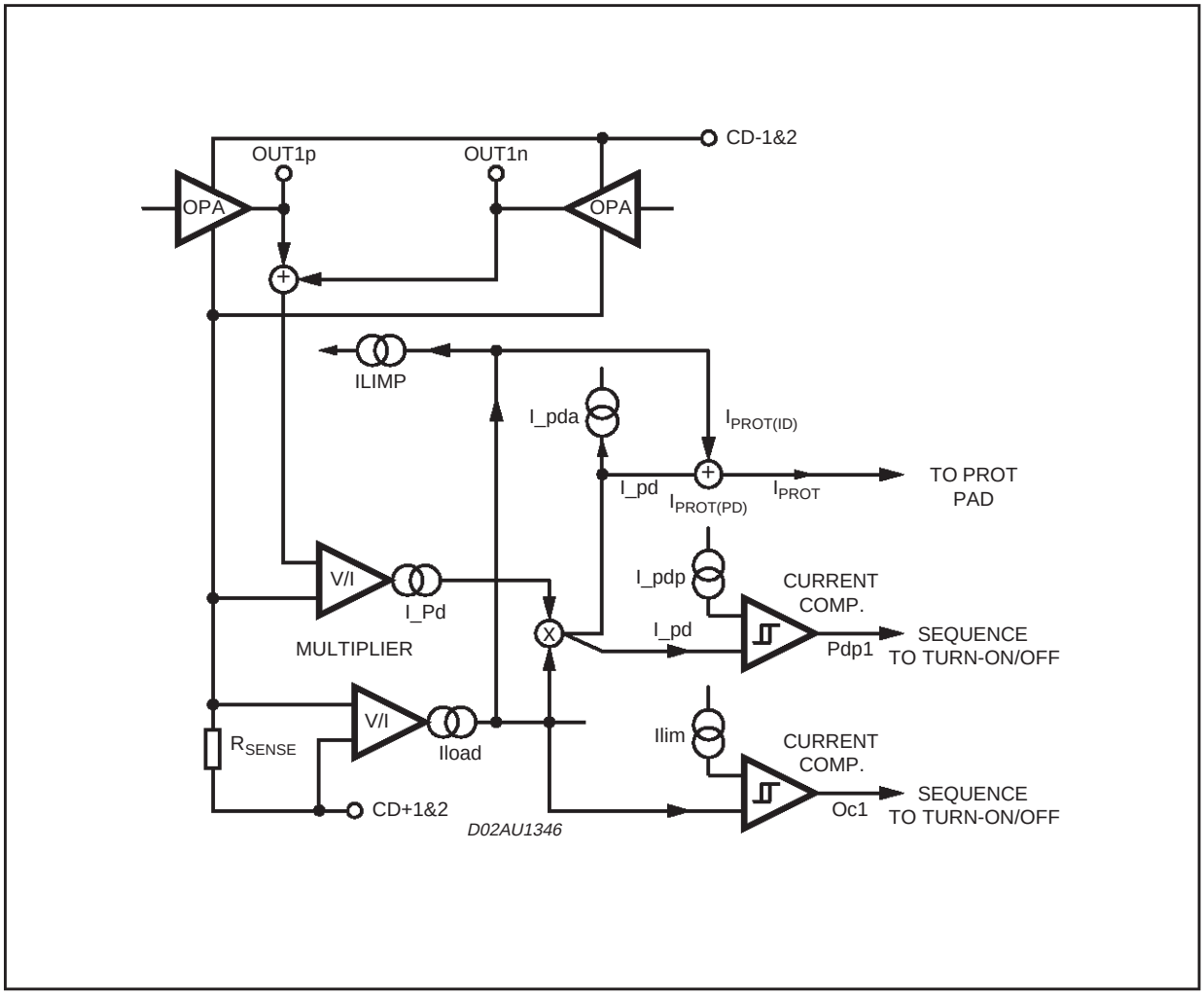
In 60W x2 channel configuration the "slave" inputs (INPUT 2/4) must be connected to GND.

POWER PROTECTION

To protect the output transistors of the power bridge a power detector is implemented (fig 1).

The current flowing in the power bridge and the voltage drop on the relevant power (Vds) are internally measured. These two parameters are converted in current and multiplied: the resulting current , Ipd, is proportional to the instantaneous dissipated power on the relevant output transistor. The current Ipd is compared with the reference current Ipda, if bigger (dissipated power > 18W) a current, Iprot(P_D), is supplied to the Protection pin. The aim of the current Iprot is to reduce the reference voltage for the Buck regulator supplying the power stage of the chip, and than to reduce the dissipated power. The response time of the system must be less than 200 µSec to have an effective protection. As further protection, when Ipd reaches an higher threshold (when the dissipated value is higher then 30W) the chip is shut down, forcing low the Stby/Mute pin, and the turn on sequence is restarted. The above description is relative for each channel in 4x30W configuration.

Figure 1. Power Protection Block Diagram



In fig. 2 there is the power protection strategy pictures. Under the curve of the 18W power, the chip is in normal operation, over 30W the chip is forced in Standby. This last status would be reached if the Buck regulator does not respond quikly enough reducing the stress to less than 30W.

The fig.3 gives the protection current, Iprot(P_D), behavior. The current sourced by the pin Prot follows the formula:

$$I_{prot(PD)} \equiv \frac{(P_d - P_{d\_av\_th}) \cdot 5 \cdot 10^{-4}}{1.25V} -$$

(for each channel)

for $P_d < P_{d\_av\_th}$ the Iprot(P_D)= 0.

Figure 2. Power protection threshold

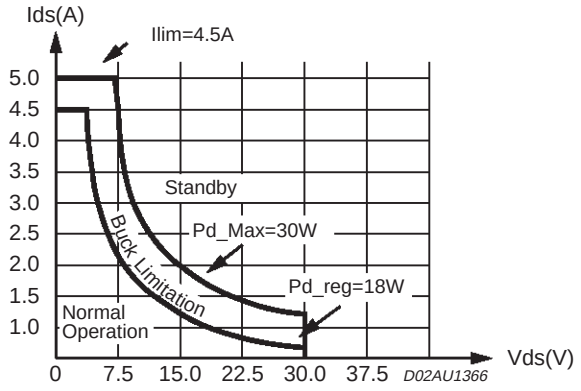
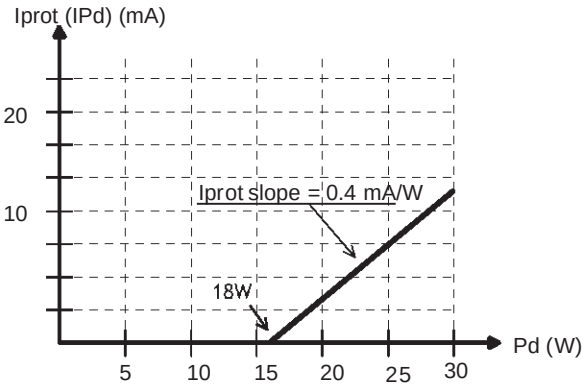


Figure 3. Protection current behaviour Iprot (P_D)



CURRENT PROTECTION

The chip is also protected by a current detection.

The current I_{LOAD} is compared with the reference current I_{LIMP}, if bigger (I_{LOAD}> 4,5 A)a current Iprot(I_L), is supplied to the Protection pin.

As further protection, when I_{LOAD} reaches an higher threshold (5 A) the chip is shut down, forcing low the Stby/Mute pin, and the turn on sequence is restarted.

The above description is relative for each channel in 4x30W configuration.

The fig.4 gives the protection current, Iprot(I_L), behavior. The current sourced by the pin Prot follows the formula:

$$I_{prot(IL)} \equiv \frac{(I_{LOAD} - I_{ict,s})}{2500} \quad \text{(for each channel)}$$

for $I_{ILOAD} < I_{ict,s}$ the Iprot(I_L) = 0.

For the parallel channel Iprot is double.

The chip is also shut down in the following conditions:

When the average junction temperature of the chip reaches 150°C.

When the ground potential differ from more than 5V from the half of the power supply voltage, ((CD+)-(CD-))/2

When the sum of the supply voltage |Vs+| + |Vs-| <20V

The output bridge is muted when the average junction temperature reaches 130°C.

Figure 4. Protection current behaviour Iprot (I_L)

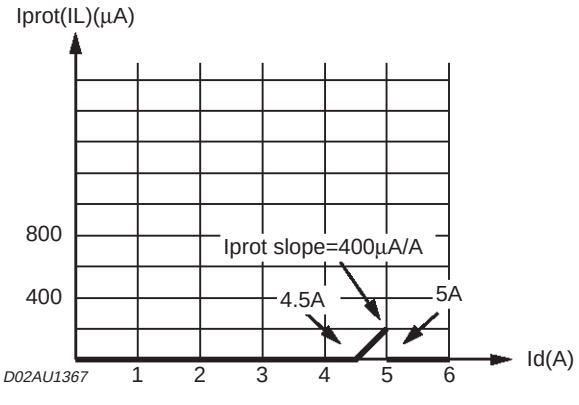


Figure 5. Test and Application Circuit (4x30W)

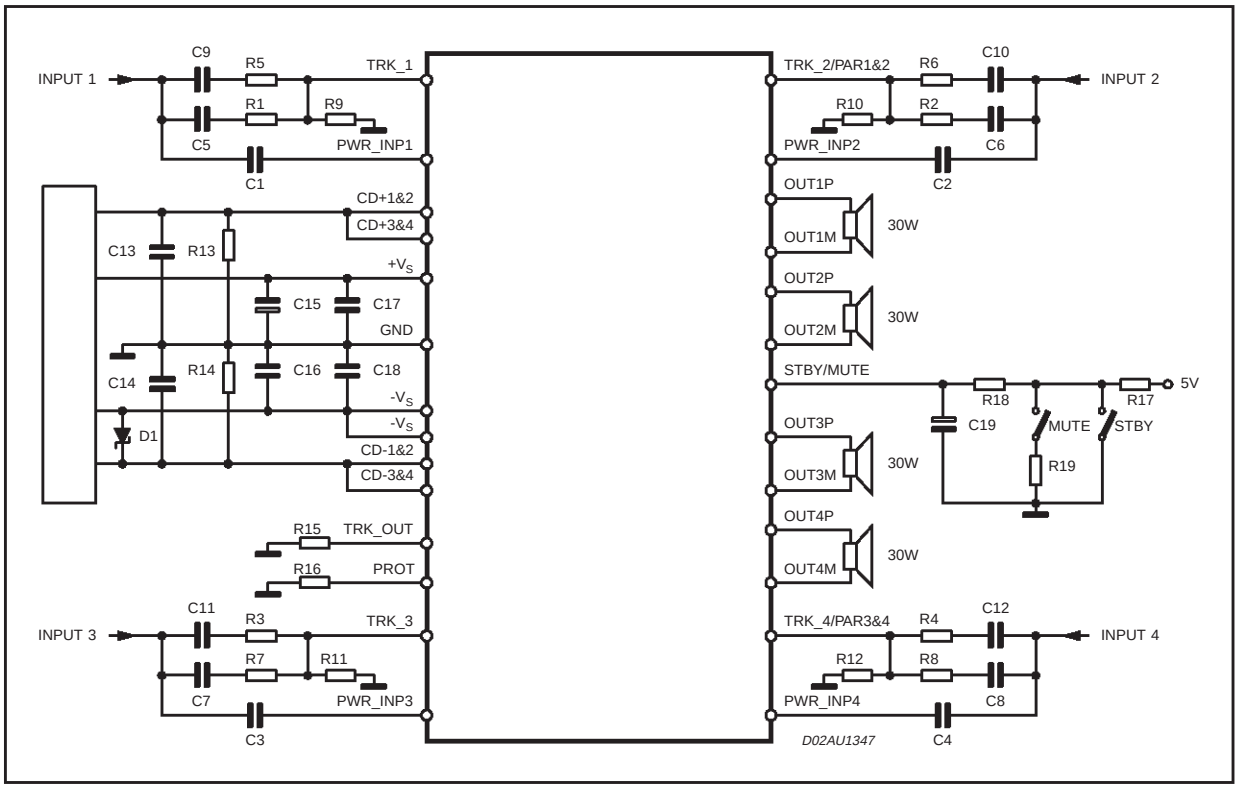
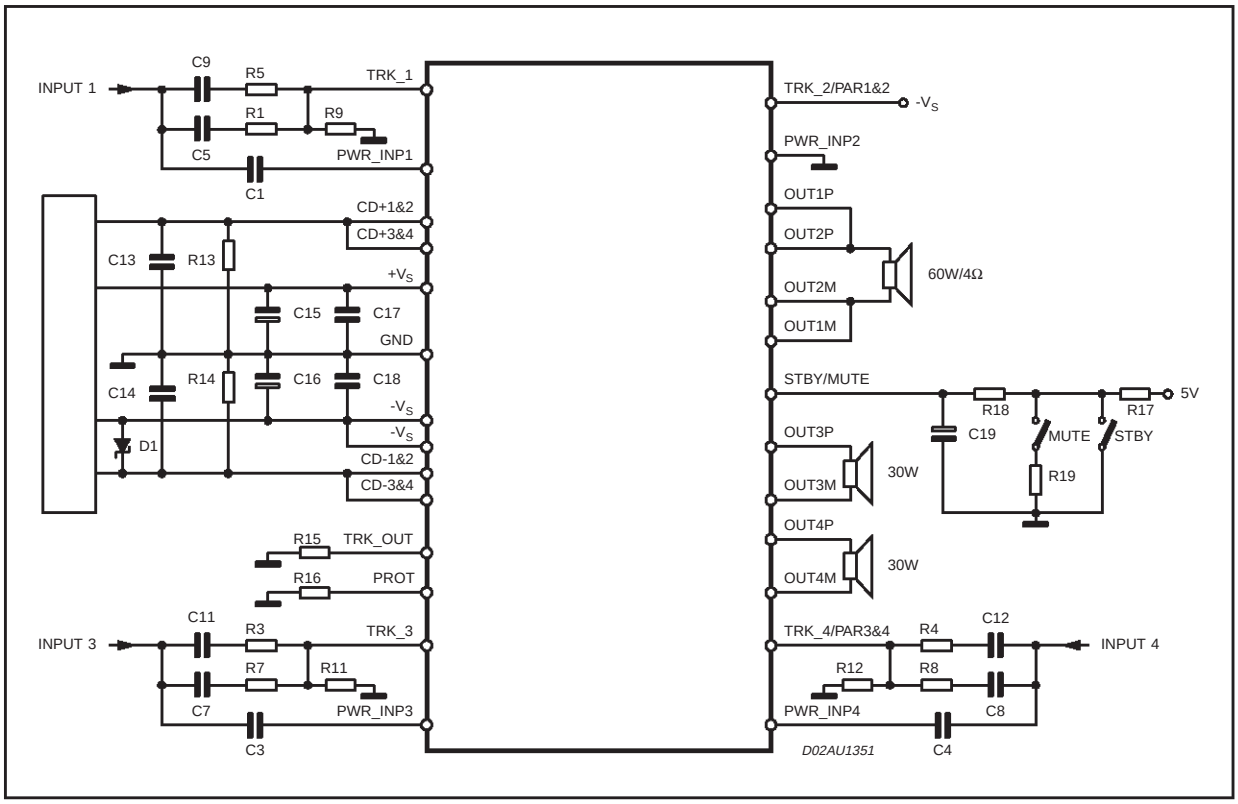


Figure 6. Test and Application Circuit (2x30W & 1x60W)



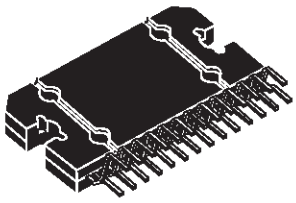
EXTERNAL COMPONENTS

Name	Function	Value	Formula
R1 = R2 =R3 = R4	Resistor for tracking input voltage filter	10KΩ	
R5 = R6 =R7 = R8	Resistor for tracking input voltage filter	56KΩ	
Cac C1 = C2 = C3 = C4	AC Decoupling capacitor	100nF (fp = 16Hz, Rac =100KΩ)	$Cac = \frac{1}{2\pi \cdot fp \cdot Rac}$
R9=R10=R11=R12	Resistor for tracking input voltage filter	10KΩ	
C5 = C6 = C7 = C8	Capacitor for Tracking input voltage filter	1nF	
C9=C10=C11=C12	Dc decoupling capacitor	1μF	
R17	Bias Resistor for Stby/Mute function	10KΩ	
R18	Stby/Mute constant time resistor	30KΩ	
R19	Mute resistor	30KΩ	
C19	Capacitor for Stby/Mute resistor	2.2μF	
C17 = C18	Power supply filter capacitor	100nF	
R13 = R14	Centering resistor	330 Ω , 1W	
C13 = C14	Tracking rail power supply filter	680nF	
R15	TRK_out	40KΩ	
R16	Protection	1KΩ	
C15 = C16	Power supply filter capacitor	470 μF , 63V	
D1	Schottky diode	SB360	

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.45	4.50	4.65	0.175	0.177	0.183
B	1.80	1.90	2.00	0.070	0.074	0.079
C		1.40			0.055	
D	0.75	0.90	1.05	0.029	0.035	0.041
E	0.37	0.39	0.42	0.014	0.015	0.016
F (1)			0.57			0.022
G	0.80	1.00	1.20	0.031	0.040	0.047
G1	25.75	26.00	26.25	1.014	1.023	1.033
H (2)	28.90	29.23	29.30	1.139	1.150	1.153
H1		17.00			0.669	
H2		12.80			0.503	
H3		0.80			0.031	
L (2)	22.07	22.47	22.87	0.869	0.884	0.904
L1	18.57	18.97	19.37	0.731	0.747	0.762
L2 (2)	15.50	15.70	15.90	0.610	0.618	0.626
L3	7.70	7.85	7.95	0.303	0.309	0.313
L4		5			0.197	
L5		3.5			0.138	
M	3.70	4.00	4.30	0.145	0.157	0.169
M1	3.60	4.00	4.40	0.142	0.157	0.173
N		2.20			0.086	
O		2			0.079	
R		1.70			0.067	
R1		0.5			0.02	
R2		0.3			0.12	
R3		1.25			0.049	
R4		0.50			0.019	
V	5° (Typ.)					
V1	3° (Typ.)					
V2	20° (Typ.)					
V3	45° (Typ.)					

(1): dam-bar protusion not included
(2): molding protusion included

OUTLINE AND MECHANICAL DATA



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