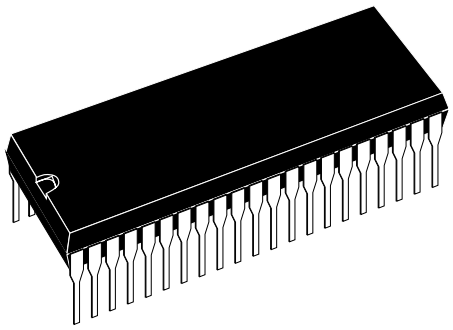
SGS-THOMSON MICROELECTRONICS

ST9294

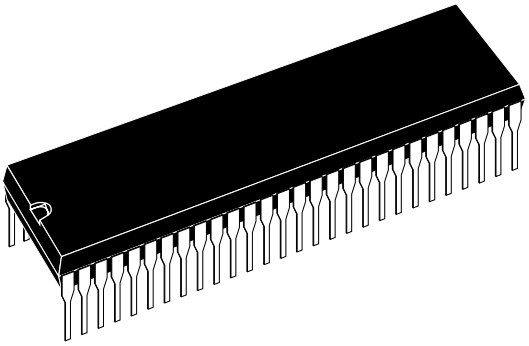
24K ROM HCMOS MCU WITH ON SCREEN DISPLAY AND CLOSED-CAPTION DATA SLICER

FUNCTIONAL DESCRIPTION

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 12 to 32K bytes of ROM, 384/640 bytes of RAM, 224 general purpose registers available as RAM, accumulators or index registers (Register File)
- 42-lead Shrink DIP package or 56-lead Shrink DIP package
- Interrupt handler and Serial Peripheral Interface as standard features
- 31 (42 pin package) / 42 (56 pin package) fully programmable I/O pins
- 34 character x15 rows software programmable On Screen Display module with colour, italic, underline, flash, transparent and fringe attribute options
- Digital Data Slicer extracting closed caption data from video
- 8 8-bit PWM D/A outputs with repetition frequency 2 to 32kHz and 12V Open Drain Capability
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- 16-bit programmable Slice Timer with 8-bit prescaler
- 3 channel Analog to Digital Converter, with integral sample and hold, fast 5.75µs conversion time, 6-bit guaranteed resolution
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Windowed EPROM parts available for prototyping and pre-production development phases



PSDIP42



PSDIP56

(Ordering Information at the end of the Datasheet)

Figure 1a. 42 Pin Shrink DIP Pinout

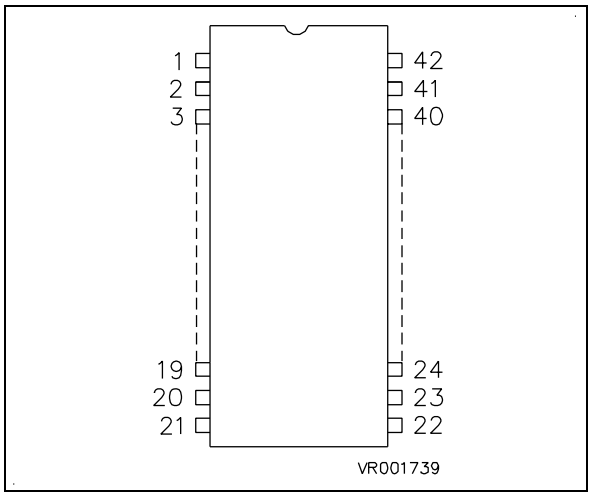
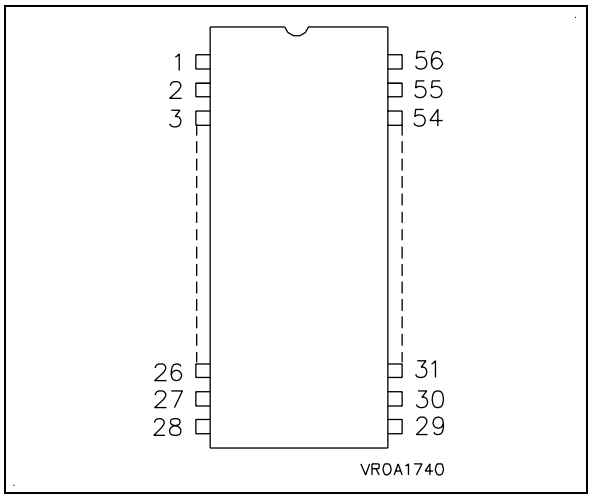


Figure 1b. 56 Pin Shrink DIP Pinout



ST9294J Pin Description

Pin	Pin name	Pin	Pin name
1	P2.0/INT7	42	P2.1/INT5/AIN1
2	$\overline{\text{RESET}}$	41	P2.2/INT0/AIN2
3	P0.7	40	P2.3/INT6/SDO
4	P0.6	39	P2.4/NMI
5	P0.5	38	P2.5/AIN3
6	P0.4	37	OSCIN
7	P0.3	36	OSCOUT
8	P0.2	35	P4.7/PWM7/ EXTRG (AD)
9	P0.1	34	P4.6/PWM6
10	P0.0	33	P4.5/PWM5
11	CCVideo	32	P4.4/PWM4
12	P3.6	31	P4.3/PWM3
13	P3.5	30	P4.2/PWM2
14	P3.4	29	P4.1/PWM1
15	P3.3/B	28	P4.0/PWM0
16	P3.2/G	27	VSYNC
17	P3.1/R	26	HSYNC
18	P3.0/FB	25	AV_{DD}
19	P5.1/SDIO	24	PLLR
20	P5.0/SCK/INT2	23	PLLF
21	V_{DD}	22	V_{SS}

ST9294N Pin Description

Pin	Pin name	Pin	Pin name
1	P2.1/INT5/AIN1	56	P2.2/INT0/AIN2
2	P2.0/INT7	55	P2.3/INT6/SDO
3	$\overline{\text{RESET}}$	54	P2.4/NMI
4	P0.7	53	P2.5/AIN3
5	P0.6	52	P1.0
6	P0.5	51	P1.1
7	NC	50	P1.2
8	P0.4	49	P1.3
9	P0.3	48	P1.4
10	P0.2	47	P1.5
11	P0.1	46	P1.6
12	P0.0	45	P1.7
13	NC	44	OSCIN
14	V_{DD}	43	OSCOUT
15	CCVideo	42	P4.7/PWM7/ EXTRG (AD)
16	P3.7	41	P4.6/PWM6
17	P3.6	40	P4.5/PWM5
18	P3.5	39	P4.4/PWM4
19	P3.4	38	P4.3/PWM3
20	P3.3/B	37	P4.2/PWM2
21	P3.2/G	36	P4.1/PWM1
22	P3.1/R	35	P4.0/PWM0
23	P3.0/FB	34	VSYNC
24	P5.3	33	HSYNC
25	P5.2	32	AV_{DD}
26	P5.1/SDIO	31	PLLR
27	P5.0/SCK/INT2	30	PLLF
28	V_{DD}	29	V_{SS}

1.1 GENERAL DESCRIPTION

The ST9294 is a ROM member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROM parts are fully compatible with their EPROM versions, which may be used for the prototyping and pre-production phases of development.

The nucleus of the ST9294 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16-bit Timer/Watchdog with 8-bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8-bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST9294 with up to 31/42 I/O lines dedicated to digital Input/Output. These lines are grouped into up to six I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O.

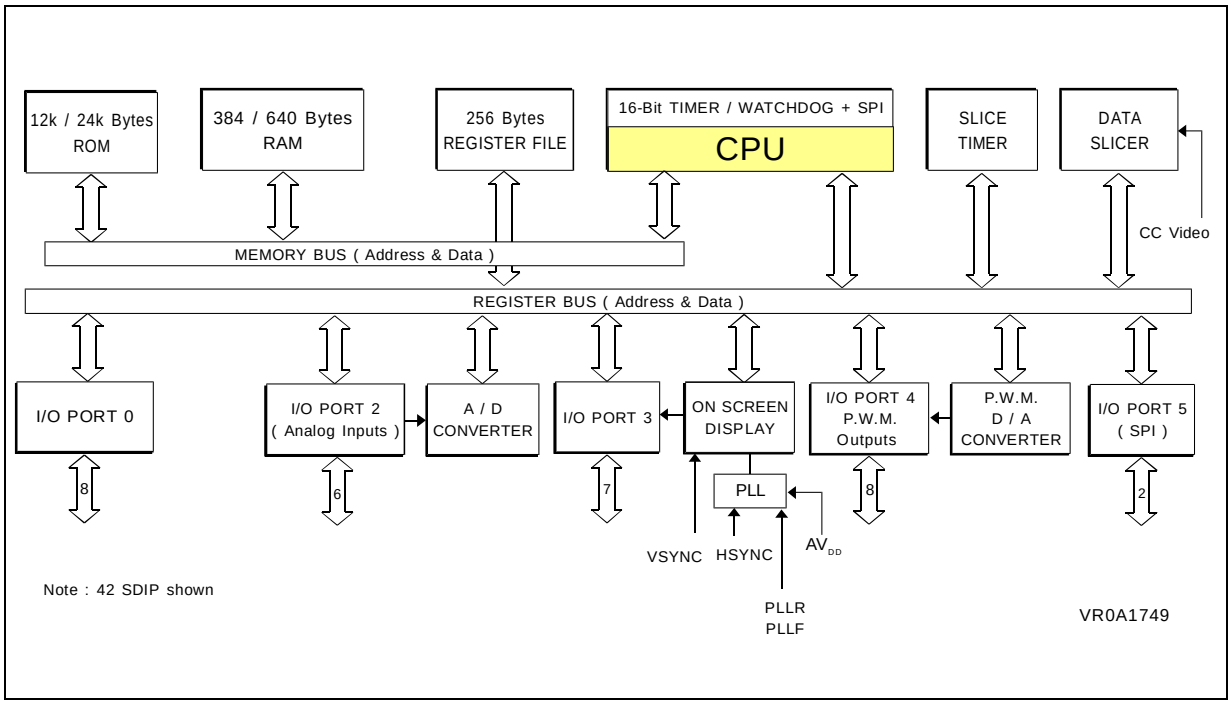
Three basic memory spaces are available to support this wide range of configurations: Program Memory, Data Memory and the Register File, which includes the control and status registers of the on-chip peripherals.

The 16-bit Slice Timer with an 8-bit Prescaler.

The human interface is provided by the On Screen Display module, this can produce up to 15 lines of up to 34 characters from a ROM defined 128 character set. The 9x13 character can be modified by 4 different pixel sizes, with character rounding, and formed into words with colour and format attributes.

Closed Caption control for the display of information transmitted through the video input is facilitated with the Data Slicer. This module has manual and automatic Slicing levels for both Sync and Data and allows the user to select the video line containing the data relative to the Vertical synchronisation pulse.

Figure 1-2. ST9294 Block Diagram



GENERAL DESCRIPTION (Continued)

Control of TV settings is able to be made with up to eight 8-bit PWM outputs, with a frequency maximum of 23,437Hz at 8-bit resolution (INTCLK = 12MHz). Low resolutions with higher frequency operation can be programmed.

In addition there is a 3 channel Analog to Digital Converter with integral sample and hold, fast 5.75µs conversion time and 6-bit guaranteed resolution.

1.2 PIN DESCRIPTION

VSYNC. *Vertical Synch.* Vertical video synchronisation input to OSD. Positive or negative polarity.

HSYNC. *Horizontal Synch.* Horizontal video synchronisation input to OSD. Positive or negative polarity.

CCVideo. *Composite Video Input*. Input to Data Slicer for Closed Caption extraction, 1V± 6dB or 2V± 3dB.

PLLF. *PLL Filter input.* Filter input for the OSD for PLL feed-back.

PLLR. *PLL Resistor connection pin.* For resistor connection to select the PLL gain adjust.

$\overline{\text{RESET}}$. *Reset (input, active low).* The ST9 is initialised by the Reset signal. With the deactivation of $\overline{\text{RESET}}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h.

OSCIN, OSCOUT. *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

AV_{DD}. Analog V_{DD} of PLL. This pin must be tied to V_{DD} externally to the ST9294.

V_{DD}. Main Power Supply Voltage (5V±10%)

V_{SS}. Digital Circuit Ground.

P0.0-P0.7, P2.0-P2.5, P3.0-P3.6, P4.0-P4.7, P5.0-P5.1 (J suffix)
P0.0-P0.7, P1.0-P1.7, P2.0-P2.5, P3.0-P3.7, P4.0-P4.7, P5.0-P5.3 (N suffix) *I/O Port Lines (Input/Output, TTL or CMOS compatible).* 31/42 lines grouped into I/O ports, bit programmable under program control as general purpose I/O or as Alternate functions (see next section).

P4.0 - P4.7 are high voltage (12V) open drain

1.2.1I/O Port Alternate Functions.

Each pin of the I/O ports of the ST9294 may assume software programmable Alternative Functions as shown in the Pin Configuration Drawings. Table 1 shows the Functions allocated to each I/O Port pin.

PIN DESCRIPTION (Continued)

Table 1-1. ST9294 I/O Port Alternative Function Summary

I/O PORT	Name	Function	Alternate Function	Pin Assignment	
Port.bit				9294J	9294N
P0.0		I/O		10	12
P0.1		I/O		9	11
P0.2		I/O		8	10
P0.3		I/O		7	9
P0.4		I/O		6	8
P0.5		I/O		5	6
P0.6		I/O		4	5
P0.7		I/O		3	4
P1.0		I/O		-	52
P1.1		I/O		-	51
P1.2		I/O		-	50
P1.3		I/O		-	49
P1.4		I/O		-	48
P1.5		I/O		-	47
P1.6		I/O		-	46
P1.7		I/O		-	45
P2.0	INT7	I	External Interrupt 7 with Schmitt Trigger	1	2
P2.1	INT5	I	External Interrupt 5 with Schmitt Trigger	42	1
P2.1	AIN1	I	A/D Analog Input 1	42	1
P2.2	INT0	I	External Interrupt 0	41	56
P2.2	AIN2	I	A/D Analog Input 2	41	56
P2.3	INT6	I	External Interrupt 6	40	55
P2.3	SDO	O	MSPI Serial Data Output	40	55
P2.4	NMI	I	Non-Maskable Interrupt	39	54
P2.5	AIN3	I	A/D Analog Input 3	38	53
P3.0	FB	O	Fast Blanking OSD output	18	23
P3.1	R	O	Red Video Colour OSD output	17	22
P3.2	G	O	Green Video Colour OSD output	16	21
P3.3	B	O	Blue Video Colour OSD output	15	20

PIN DESCRIPTION (Continued)

Table 1-1. ST9294 I/O Port Alternative Function Summary

I/O PORT	Name	Function	Alternate Function	Pin Assignment	
Port.bit				9294J	9294N
P3.4		I/O		14	19
P3.5		I/O		13	18
P3.6		I/O		12	17
P3.7		I/O		-	16
P4.0	PWM0	O	PWM Output 0	28	35
P4.1	PWM1	O	PWM Output 1	29	36
P4.2	PWM2	O	PWM Output 2	30	37
P4.3	PWM3	O	PWM Output 3	31	38
P4.4	PWM4	O	PWM Output 4	32	39
P4.5	PWM5	O	PWM Output 5	33	40
P4.6	PWM6	O	PWM Output 6	34	41
P4.7	PWM7	O	PWM Output 7	35	42
P4.7	EXTRG	I	A/D External Trigger	35	42
P5.0	SCK	O	SPI Serial Clock (1)	20	27
P5.0	INT2	I	External Interrupt 2 (1)	20	27
P5.1	SDIO	O	SPI Serial Data Input/Output (1)	19	26
P5.2		I/O		-	25
P5.3		I/O		-	24

Notes.

1. The alternate functions of SCK/INT2 and SDIO may be swapped by using the SWAP Register Function.
2. Schmitt trigger options are available as a mask option for any input pin.