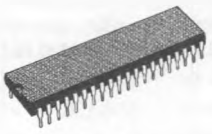
SGS-THOMSON MICROELECTRONICS

ST6356/57/58

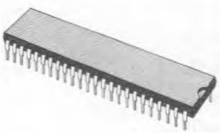
8-BIT HCMOS MCUs FOR TV VOLTAGE SYNTHESIS WITH OSD

ADVANCE DATA

- 8-BIT ARCHITECTURE
- STATIC HCMOS OPERATION
- 4.5 TO 5.5 V SUPPLY OPERATING RANGE
- 4MHZ OR 8MHZ CLOCK OPTIONS
- PROGRAM ROM : 8192 BYTES
- DATA ROM : USER SELECTABLE
- DATA RAM : 256 BYTES
- DATA EEPROM : 128 BYTES
- 40/42 SHRINK/48 DIP PACKAGES
- 14 BIT VOLTAGE SYNTHESIS TUNING PERIPHERAL (VS)
- ON-CHIP 5 LINES BY 15 COLUMNS ON-SCREEN-DISPLAY GENERATOR (OSD)
- 17/19/24 (ST6356/57/58) SOFTWARE PROGRAMMABLE GENERAL PURPOSE INPUTS/OUTPUTS, INCLUDING 6 (ST6356) OR 8 (ST6357/58) DIRECT LED DRIVING OUTPUTS
- TWO TIMERS EACH INCLUDING AN 8-BIT COUNTER WITH A 7-BIT PROGRAMMABLE PRESCALER
- DIGITAL WATCHDOG FUNCTION
- SERIAL PERIPHERAL INTERFACE (SPI) SUPPORTING S-BUS/I^2CBUS AND STANDARD SERIAL PROTOCOLS
- FOUR 6-BIT PWM D/A CONVERTERS
- AFC A/D CONVERTER WITH 0.5V RESOLUTION
- INFRARED SIGNAL PRE-PROCESSOR
- FOUR INTERRUPT VECTORS (IR, Timer 1 & 2, OSD VSYNC)



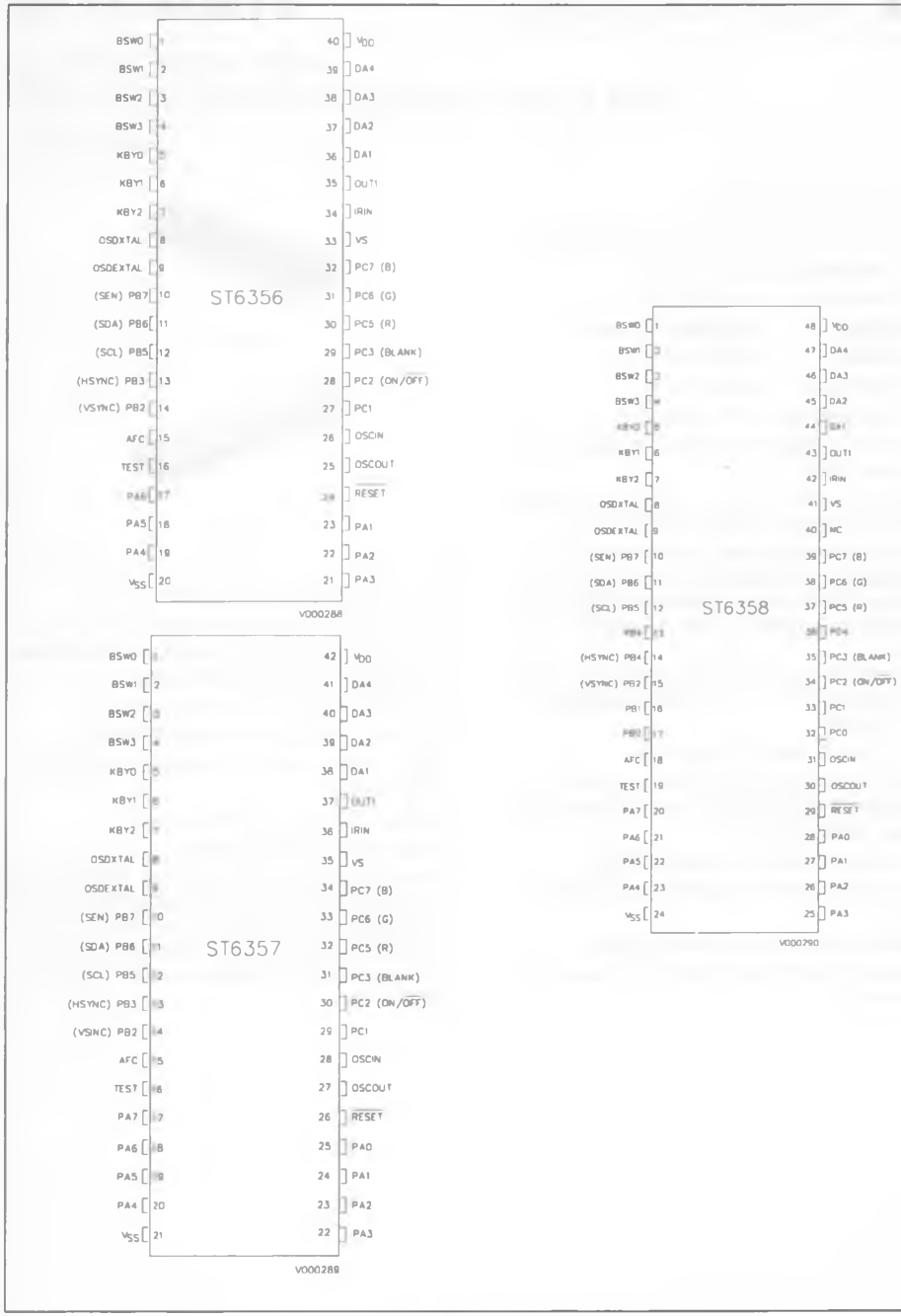
PDIP-40



PDIP-48

- ON-CHIP CLOCK OSCILLATOR
- ON-BOARD POWER-ON RESET CIRCUITRY
- ALL ROM TYPES ARE SUPPORTED BY PIN-TO-PIN PIGGYBACK VERSIONS
- BYTE EFFICIENT INSTRUCTION SET
- BIT TEST AND JUMP INSTRUCTIONS
- WAIT, STOP AND BIT MANIPULATION INSTRUCTIONS
- 1.625µS TCYCLE (8.0 MHz clock)
- TRUE LIFO 6-LEVEL STACK
- THE DEVELOPMENT TOOL OF THE ST63XX MICROCONTROLLERS CONSISTS OF THE EMST63HW/TVS EMULATION AND DEVELOPMENT SYSTEM AND CONNECTED VIA A STANDARD RS232 SERIAL LINE TO AN MS-DOS™PC

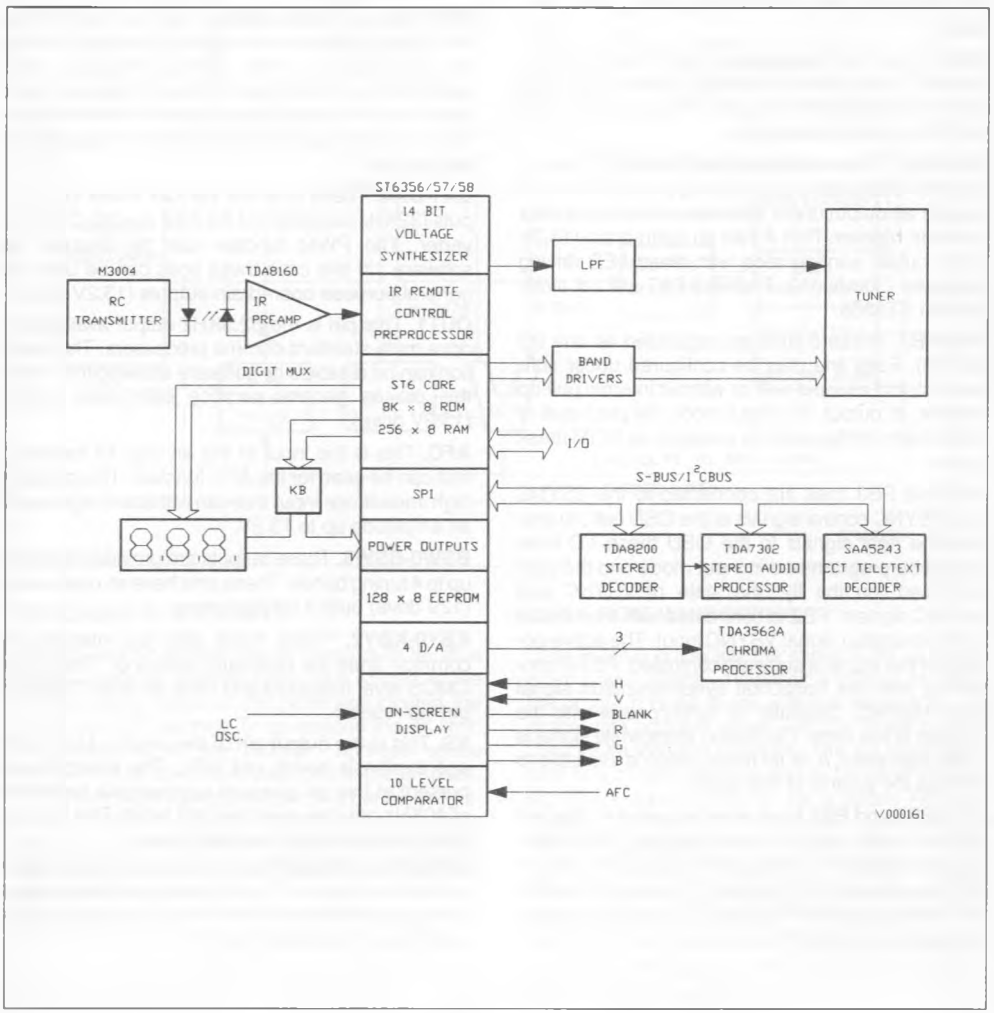
Figure 1 : ST6356/57/58 Pin Configurations



GENERAL DESCRIPTION

The ST6356/57/58 microcontrollers are powerful members of the 8-bit HCMOS ST63XX family, a series of devices specially oriented to TV applications. Different packages and configurations are available to offer different performance/cost tradeoffs. All ST63XX members are based on a building block approach: to a common Core is associated a combination of on-chip peripherals (macrocells) available from a standard library. These peripherals are designed with the same Core technology providing full compatibility, short design and testing time. Many of these macrocells are specially dedicated to TV applications. The macrocells of the ST6356/57/58 are: two 8-bit counter with a 7-bit programmable prescaler (Timer), a Digital Watchdog Timer, a Serial Peripheral Interface (SPI), a 5 lines by 15 columns On-screen display generator (OSD), four 6-Bit PWM D/A Converters, an AFC A/D converter with 0.5V resolution, a 14 bit Voltage synthesis tuning peripheral (VS). In addition all these devices have 128 bytes of on-chip EEPROM.

Figure 2 : ST6356/57/58 System Description.



PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCIN and OSCOUT. These pins are internally connected with the on-chip oscillator circuit. A crystal quartz, a ceramic resonator or an external signal has to be connected between these two pins in order to allow the right operating of the MCU. The OSCIN pin is the input pin, the OSCOUT pin is the output pin. A mask option allows the selection of a 4MHz or 8MHz oscillator frequency.

$\overline{\text{RESET}}$. The active low RESET pin is used to start the microcontroller from the beginning of its program.

TEST. The TEST (mode select) pin is used to place the MCU into special operating mode if kept high when Reset is active. This pin has to be connected to VSS for normal operation.

PA0-PA7. These 8 lines are organized as one I/O port (A). Each line may be configured as either an input or an output under software control of the data direction register. Port A has an open-drain (13.2V drive) output configuration with direct LED driving capability (30mA, 1V). PA0 and PA7 are not available on ST6356.

PB0-PB7. These 8 lines are organized as one I/O port (B). Each line may be configured under software control as input with or without internal pull-up resistor, or output. In output mode the push-pull or open-drain configuration is available as ROM mask option.

PB2 and PB3 lines are connected to the VSYNC and HSYNC control signals of the OSD cell ; to provide the right signals to the OSD these I/O lines should be programmed in input mode and the user can read "on the fly" the state of VSYNC and HSYNC signals. PB2 is connected with the vertical synchronization signal VSYNC input. The active polarity of this signal is software controlled. PB3 is connected with the horizontal synchronization signal input HSYNC. Oscillator is synchronous with the change to low state. Oscillation stops while signal is in the high state. A ROM mask option is available to change the polarity of this signal.

PB5, PB6 and PB7 lines when in output modes are "ANDed" with the SPI control signals. PB5 is connected with the SPI clock signal (SCK), PB6 with the SPI data signal (SDA) while PB7 is connected with SPI enable signal (SEN). PB0, PB1 and PB4 are not available on ST6356/57.

PC0-PC7. These 8 lines are organized as one I/O port (C). Each line may be configured under software control as input with or without internal pull-up resistor or output. In output mode the push-pull or open-drain configuration is available as ROM mask option. PC3, PC5, PC6 and PC7 lines when in output modes are "ANDed" with the character and blank signal of the OSD cell. PC3 is connected with the OSD BLANK signal, PC5, PC6 and PC7 with the OSD R, G and B signals. These signals are active high. PC2 is also used as TV set On-Off (12V drive) switch. PC0 and PC4 are not available on ST6356/57.

IRIN. This pin is the external interrupt input of the MCU and is directly connected to the infra-red signal pre-processor which allows, through a band pass filter, to reduce the number of interrupts sent to the Core. A mask option allows the direct connection of the interrupt pin to the Core non maskable interrupt line.

DA1-DA4. These pins are the four PWM D/A outputs (32KHz repetition) of the 6-bit on-chip D/A converter. The PWM function can be disabled by software ; in this case these lines can be used as general purpose open-drain outputs (13.2V drive).

OUT1. This pin is the 62.5KHz output available to drive multi-standard chroma processors. This function can be disabled by software allowing the use of this pin as general purpose open-drain output (13.2V drive).

AFC. This is the input of the on-chip 10 level A/D that can be used for the AFC function. This pin is an high impedance input that can withstand signal with an amplitude up to 13.2V.

BSW0-BSW3. These outputs are provided to select up to 4 tuning bands. These pins have an open-drain (12V drive) output configuration.

KBY0-KBY2. These inputs pins are intended as common lines for keyboard scanning. They have CMOS level threshold and have on-chip 100Kohm pull-up resistor.

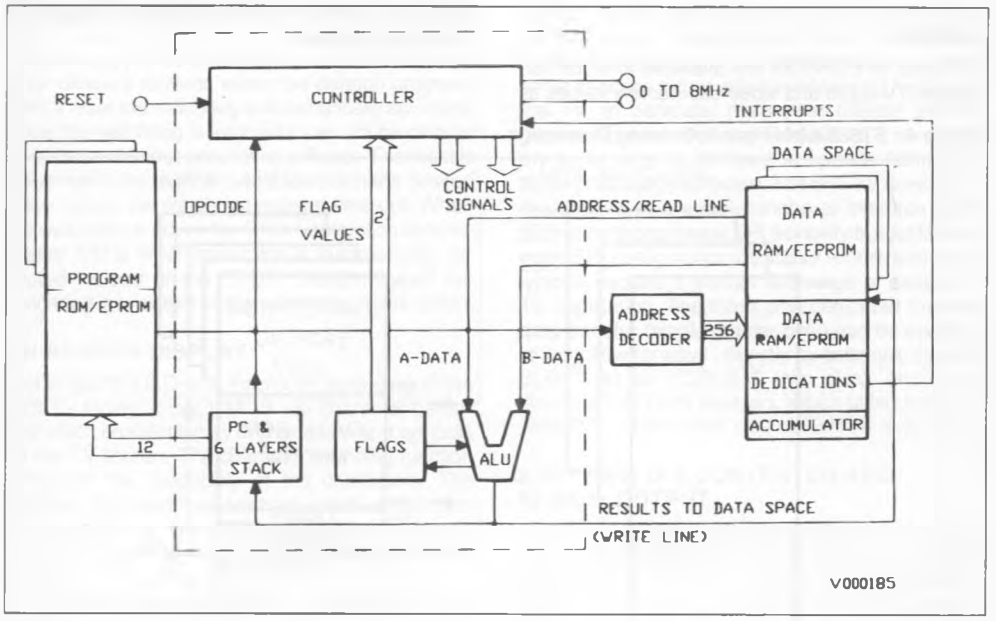
VS. This is the output pin of the on-chip 14-bit voltage synthesis tuning cell (VS). The tuning signal present at this pin gives an approximate resolution of 40KHz per step over the UHF band. This line is a push-pull output with standard drive.

ODSXTAL, OSDEXTAL. These pins are the OSD oscillator terminals. To this pins an oscillation capacitor and coil network have to be connected to provide the right signal to the OSD.

ST63XX CORE

The ultra small and fast Micro-Core of the ST63XX TV chips microcontrollers is designed to provide the economy of small die size through advanced HCMOS technologies. The ST63XX core can directly address 4 Kbyte of program memory with extension capability by 2 Kbyte bank addition. The directly addressable data space is 256 bytes sized with extension capability by 64 byte bank addition. The data ROM which is addressed in the data space is physically located in the program area. The core includes an 8-bit accumulator, two 8-bit index registers and a 12-bit program counter. These pairs of flags monitor the processor operations while a six levels LIFO hardware stack is available for subroutine & interrupt return address storage. One NMI and four normal interrupt vectors are available. STOP and WAIT modes are included to reduce overall power consumption.

Figure 3 : ST63XX Core Block Diagram.



PROGRAM ROM PAGING

ST63XX has 12 address bits for program ROM, thus giving a program address space of 4 Kbytes. In the highest twelve bytes of the ROM are located the restart and INT vectors. To go beyond the 4K limit, the lower half of the program address space (0...7FFH) has been used as paged address space, the current page being selected by a banking register. Only the lower part of address space has been bak-switched because of interrupt (vectors and drivers) and common subroutines, that should be available all the time.

DATA ROM WINDOWING

Data ROM is physically the same ROM as for program space. Simply, it is possible to read as data all the program ROM space with the range 40H..7FH of the data address space and the contents of the Data ROM Window Register. The six least significant bits of data address space become the least significant address bits of the program ROM address to the build. This only when addressing the data space locations mentioned above. The bits coming out from Data ROM Window register become the most significant ones ; they are 6 if the program ROM is of 4 Kbytes, 7 if 8 Kbytes. So, when addressing location 40H of data space, and 0 is loaded in the register, the physical location addressed is at location 0.

PAGED RAM ADDRESS RANGE

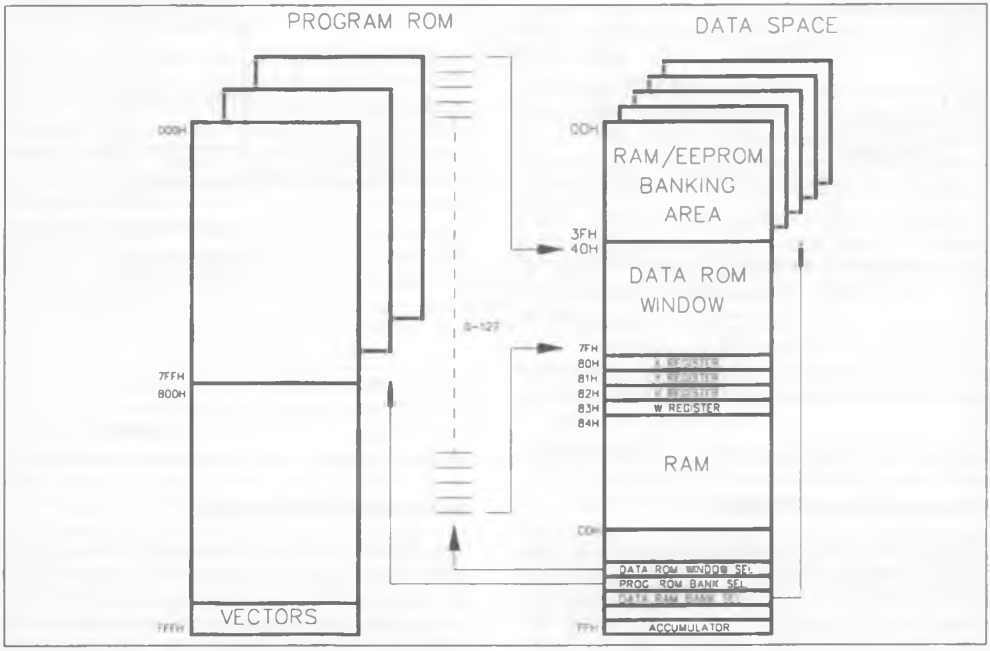
A 64 bytes range inside the data space is paged to allow extension of the RAM memory available for the user. Paged RAM address range can be switched to address up to 8 different 64 bytes pages, in which any kind of memory and/or additional control registers can be mapped. On ST6356/57/58 three pages of general purpose RAM plus two additional pages for ODS data/control registers are available. The 192 bytes of general purpose paged RAM plus 64 Bytes of non-paged RAM give a total of 256 RAM bytes available for the user.

EEPROM

128 bytes of EEPROM are available to store normalized TV audio and video user/factory values as well as 40 favorite programs. The EEPROM is physically organized in 32 byte modules (2 modules per page) and does not require dedicated instructions to be accessed in reading or writing. Any EEPROM location can be read just like any other data location, also in terms of access time.

A writing of an EEPROM location takes about 5msec and during this time the EEPROM is not accessible by the Core. Two programming modes are available : BYTE MODE (BMODE) and PARALLEL MODE (PMODE). The BMODE is the normal way to write the EEPROM and consists in accessing one byte per time. The PMODE consists in accessing up to 8 bytes per time.

Figure 4 : ST63XX Memory Addressing Description.



I/O PORTS

Each ST63XX general I/O port normally consists of eight identical cells, each containing a separately addressable data latch and data direction latch ; together they form an eight bit data register and an eight bit data direction register. The I/O uses two addresses of the data space, one for the data register and one for the data direction register. Each of the eight pins can be programmed independently as an input or as an output with various additional modes under control of the data direction register. When programmed as an input a pull-up resistor can be switched active under program control. When programmed as an output the I/O port will operate either in the push-pull mode or the open-drain mode ; this is defined during manufacture by a program ROM mask option. One I/O port (A) has an open-drain (13.2V drive) output configuration with high current drive capability for direct LED driving.

TIMERS

Each Timer peripheral consists of an 8-bit counter with a 7-bit programmable prescaler, thus giving a maximum count of 2^{15}, and a control logic that allows configuring the peripheral in three operating modes : event counter, input gated and output modes. The content of the 8-bit counter can be read/written in the Timer/Counter register. The state of the 7-bit prescaler can be read in the prescaler register. A maskable interrupt is associated with the end-of-count.

DIGITAL WATCHDOG

The digital watchdog consists of a down counter that can be used to provide a controlled recovery from a software upset. The check time can be set differently for different routines within the general program. After a reset the watchdog is automatically activated. Once the watchdog is enabled it can not be cleared by software without generating a Reset. The reset is prevented if the register is reloaded with the desired value before the watchdog register time-out. When the watchdog is active the STOP instruction is deactivated and a WAIT instruction is automatically executed instead of the STOP. Deactivation of the watchdog is available as manufacturing mask option.

ON-SCREEN DISPLAY

The ST63XX OSD is a macrocell belonging to the ST6 TV family. It is a CMOS LSI character generator which enable display of characters and symbols on the TV screen. The character rounding function enhances the readability of the characters. The ST63XX OSD receives horizontal and vertical synchronization signal and outputs screen information via R, G, B and Blanking signals. The main characteristics of the celle are listed below :

- Number of display characters : 5 lines by 15 columns
- Number of character types : 64 characters
- Character size : Four character heights (18H, 36H, 54H, 72H), two available per screen, programmable by line
- Charactyer format : 6x9 dots with character rounding function
- Character color : Eight colors available, programmable by word.
- Display position : 64 horizontal positions by 2/fosc and 63 vertical positions by 4H
- Word spacing : 64 positions programmable from 2/fosc to 128/fosc
- Line spacing : 63 positions programmable from 4 to 252H
- Background : No background, square background or fringe background programmable by word
- Background color : Two of eight colors available per screen, programmable by word.
- Display output : Three character data output terminals (R, G, B) and a blank output terminal
- Display on/off : Display data may be programmed on or off by word or entire screen. Entire screen may be blanked.

SPI

The SPI macrocell has been designed to be cost effective and very flexible in order to interface to the external peripherals generally present in TV application that are often characterized by different serial input/output specification (Audio Processors, Teletext Decoders, etc.). The reason of an hardware serial interface is that with the increasing features of the TV, in particular the newer teletext and the greater diffusion of digital TV devices, it is necessary to be able to interface at speeds faster than those practical by software. The ST6 TV devices are designed with a serial peripheral interface which maintains the software SPI flexibility but adds hardware SPI configurations suitable for devices which typically require a greater exchange of data in the TV application. The three pins dedicated for serial data transfer (single master only) can be operated in the following ways : directly by software, as an S-BUS™, as an I^2CBUS™ (two pins), and as an standard SPI (shift register). When using the hardware SPI, a fixed clock rate of 62.5kHz is provided.

6-BIT PWM D/A CONVERTER AND 62.5KHz OUTPUT

The D/A macrocell offers four PWM D/A outputs (31.2Khz repetition) with six bit resolution and with possibilities to disable the PWM in order to use the pins as standard open drain outputs. In addition a 62.5kHz output pin is available. Also this function can be disabled and the line can be used as a standard open drain output.

AFC, KB, BAND SWITCH

This macrocell contains several dedicated functions for TV applications :

- An A/D converter with five levels at intervals of 1V from 1V to 5V. The levels can all be lowered by 0.5V to effectively double the resolution.
- A keyboard input register of three bits which provides three inputs lines dedicated to keyboard scanning. These lines are CMOS levels compatible with an on-chip 100Kohm pull-up resistor.
- Band switch select outputs. These pins are provided to select up to 4 tuning bands and have an open-drain (13.2V drive) output configuration.

VOLTAGE SYNTHESIS TUNING PERIPHERAL

The voltage synthesis tuning cell consists of a 14-bit counter ; the contents of this counter are converted using PWM and BRM techniques. The 14-bit gives 16384 steps which results in a resolution of approximately 2mV over a tuning voltage of 32V ; this corresponds to a tuning resolution of about 40KHz per step in UHF band (the actual value will depend on the characteristics of the tuner).

The tuning word consists of 14 bits contained in two dedicated registers. Course tuning (PWM) is performed using the seven MSBs, while the fine tuning (BRM) is performed using the data in the seven LSBs. With all zeros loaded the output is zero ; as the tuning voltage increases from all zeros, the number of pulses in one period increases to 128 with all pulses being the same width. For values larger than 128, the PWM takes over and the number of pulses in one period stays constant at 128, but the width changes. At the other end of the scale, when almost all ones are loaded, the pulses will start to link together and the number of pulses will decrease. When all ones are loaded, the output will be almost 100% high but will have a low pulse (1/16384 of the high pulse).

In the ST63XX VS macrocell, the clock frequency for the 14 bit reference counter is 2MHz from a 4MHz input clock (a program ROM mask option is available to enable a 2MHz option from an 8MHz clock).

INFRARED DIGITAL FILTER

The IR signal pre-processor is designed to be used with M3004 or M708 transmitters and with any other IR transmitter having a carrier frequency in the range 35.8-40KHz. (For details of the transmitters please refer to their specification). The unique feature of this pre-processor is its band pass filter. It can distinguish the signal in the presence of extreme noise conditions and thus ensures a minimum number of interrupt the ST63XX core, leaving the latter to concentrate on other tasks. This cell can be bypassed by ROM mask option. In this case the INT pin is directly connected to the NMI of ST63 Core.

DEVELOPMENT SUPPORT & EMULATION SYSTEM

The ST63XX TV family is completed with a comprehensive set of emulation devices. This set includes the piggyback device for pin-to-pin replacement of all DIP masked devices In addition the ST63RT1 universal romless device (PLCC-84) is available for emulation of all ST63XX devices. The universal romless can be used as stand alone emulation chip or in conjunction with the OSD romless emulation chip ST63RS1 (84 LLCC). The connection of an external OSD generator allows the emulation of customized character sets.

The EMST63-HW/TVS hardware emulator and development system is also available offering powerful in-circuit emulator and easy-to-use sets (dedicated boards) of modular hardware and software tools to shorten the total system development time of the final application. The ST63XX emulator offers emulation power with plug-in flexibility in the selection of emulation hardware modules for the dedicated macrocells. The emulator can be interfaced with a standard RS232 serial link to industry standard MS-DOS™ personal computers.