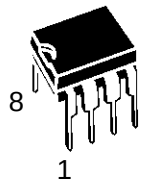
SGS-THOMSON MICROELECTRONICS

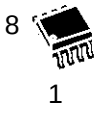
ST24/25C02, ST24C02R
ST24/25W02

SERIAL 2K (256 x 8) EEPROM

- 1 MILLION ERASE/WRITE CYCLES with 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 3V to 5.5V for ST24x02 versions
  - 2.5V to 5.5V for ST25x02 versions
  - 1.8V to 5.5V for ST24C02R version only
- HARDWARE WRITE CONTROL VERSIONS: ST24W02 and ST25W02
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 4 BYTES)
- PAGE WRITE (up to 8 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH-UP PERFORMANCES

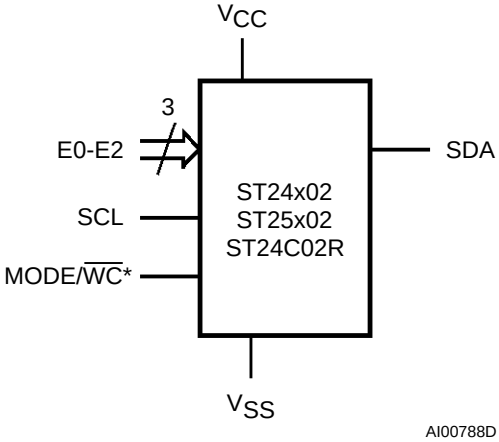


PSDIP8 (B)
0.25mm Frame



SO8 (M)
150mil Width

Figure 1. Logic Diagram



Note: $\overline{WC}$ signal is only available for ST24/25W02 products.

DESCRIPTION

This specification covers a range of 2K bits I^2C bus EEPROM products, the ST24/25C02, the ST24C02R and ST24/25W02. In the text, products are referred to as ST24/25x02, where "x" is: "C" for Standard version and "W" for hardware Write Control version.

Table 1. Signal Names

E0-E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multibyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

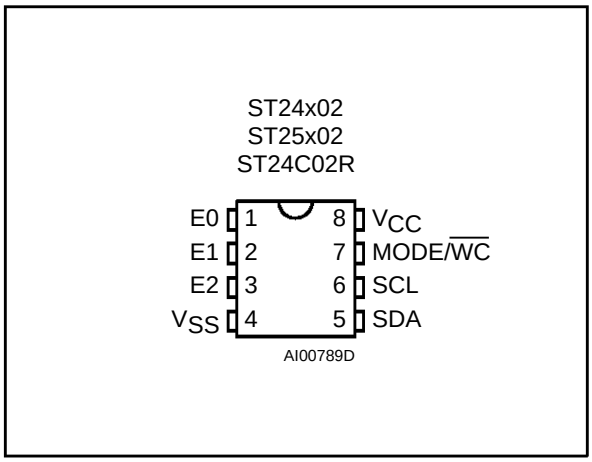


Figure 2B. SO Pin Connections

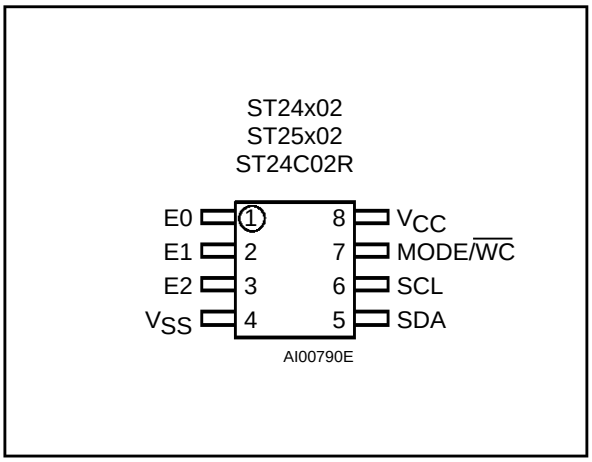


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature			–40 to 125	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.6 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

The ST24/25x02 are 2K bit electrically erasable programmable memories (EEPROM), organized as 256 x 8 bits. They are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of one million erase/write cycles with a data retention of 40 years. The memories operate with a power supply value as low as 1.8V for the ST24C02R only.

Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memories are compatible with the I^2C standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memories carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. This is used together with 3 chip enable inputs (E2, E1, E0) so that up to 8 x 2K devices may be attached to the I^2C bus and selected individually. The memories behave as a slave device in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits (identification code 1010), plus one read/write bit and terminated by an acknowledge bit.

Table 3. Device Select Code

	Device Code				Chip Enable			RW
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	E0	RW

Note: The MSB b7 is sent first.

Table 4. Operating Modes (1)

Mode	RW bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, RW = '1'
Random Address Read	'0'	X	1	START, Device Select, RW = '0', Address,
	'1'			reSTART, Device Select, RW = '1'
Sequential Read	'1'	X	1 to 256	Similar to Current or Random Mode
Byte Write	'0'	X	1	START, Device Select, RW = '0'
Multibyte Write (2)	'0'	V_{IH}	4	START, Device Select, RW = '0'
Page Write	'0'	V_{IL}	8	START, Device Select, RW = '0'

Notes: 1. X = V_{IH} or V_{IL}
2. Multibyte Write not available in ST24/25W02 versions.

When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Chip Enable (E2 - E0). These chip enable inputs are used to set the 3 least significant bits (b3, b2, b1) of the 7 bit device select code. These inputs may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code.

Mode (MODE). The MODE input is available on pin 7 (see also $\overline{WC}$ feature) and may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. When unconnected, the MODE input is internally read as a V_{IH} (Multibyte Write mode).

Write Control ($\overline{WC}$). An hardware Write Control feature ($\overline{WC}$) is offered only for ST24W02 and ST25W02 versions on pin 7. This feature is usefull to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ = V_{IH}) or disable ($\overline{WC}$ = V_{IL}) the internal write protection. When unconnected, the $\overline{WC}$ input is internally read as V_{IL} and the memory area is not write protected.

SIGNAL DESCRIPTIONS (cont'd)

The devices with this Write Control feature no longer support the Multibyte Write mode of operation, however all other write modes are fully supported.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

DEVICE OPERATION

I²C Bus Background

The ST24/25x02 support the I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25x02 are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25x02 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25x02 and the bus master. A STOP condition at the end of a Read command, after and only after a No Acknowledge, forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25x02 sample the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave ST24/25x02, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code (7 bits) and a READ or WRITE bit.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I²C Bus

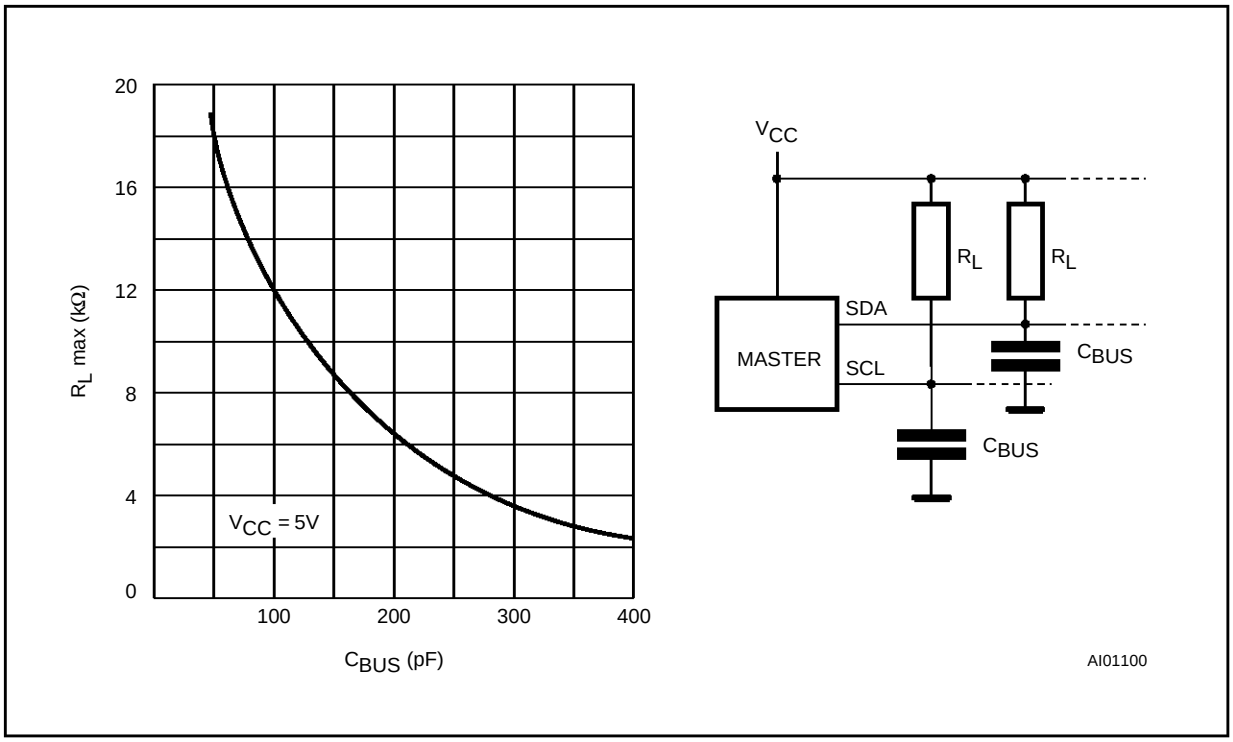


Table 5. Input Parameters (1) (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance (ST24/25W02)	$V_{IN} \le 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance (ST24/25W02)	$V_{IN} \ge 0.7\ V_{CC}$	500		kΩ
t_{LP}	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C; V_{CC} = 3V to 5.5V, 2.5V to 5.5V or 1.8V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current (ST24 series)	V_{CC} = 5V, f_C = 100kHz (Rise/Fall time < 10ns)		2	mA
	Supply Current (ST25 series)	V_{CC} = 2.5V, f_C = 100kHz		1	mA
I_{CC1}	Supply Current (Standby) (ST24 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 100kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V		5	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V, f_C = 100kHz		50	µA
I_{CC3}	Supply Current (Standby) (ST24C02R)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 3.6V		20	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 3.6V, f_C = 100kHz		60	µA
I_{CC4}	Supply Current (Standby) (ST24C02R)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8V		10	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8V, f_C = 100kHz		20	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E0-E2, MODE, WC)		–0.3	0.5	V
V_{IH}	Input High Voltage (E0-E2, MODE, WC)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage (ST24 series)	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V
	Output Low Voltage (ST24C02R)	I_{OL} = 1mA, V_{CC} = 1.8V		0.3	V

Table 7. AC Characteristics
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C; V_{CC} = 3V to 5.5V, 2.5V to 5.5V or 1.8V to 5.5V)

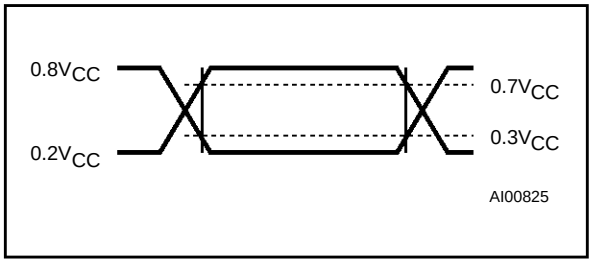
Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU:STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV} (2)	t_{AA}	Clock Low to Next Data Out Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Data Out Hold Time	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_W (3)	t_{WR}	Write Time		10	ms

Notes: 1. For a reSTART condition, or following a write cycle.
2. The minimum value delays the falling/rising edge of SDA away from SCL = 1 in order to avoid unwanted START and/or STOP conditions.
3. In the Multibyte Write mode only, if accessed bytes are on two consecutive 8 bytes rows (6 address MSB are not constant) the maximum programming time is doubled to 20ms.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 4. AC Testing Input Output Waveforms



DEVICE OPERATION (cont'd)

The 4 most significant bits of the device select code are the device type identifier, corresponding to the I^2C bus definition. For these memories the 4 bits are fixed as 1010b. The following 3 bits identify the specific memory on the bus. They are matched to the chip enable signals E2, E1, E0. Thus up to 8 x 2K memories can be connected on the same bus giving a memory capacity total of 16K bits. After a START condition any memory on the bus will identify the device code and compare the following 3 bits to its chip enable inputs E2, E1, E0.

The 8th bit sent is the read or write bit ($R\overline{W}$), this bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time.

Figure 5. AC Waveforms

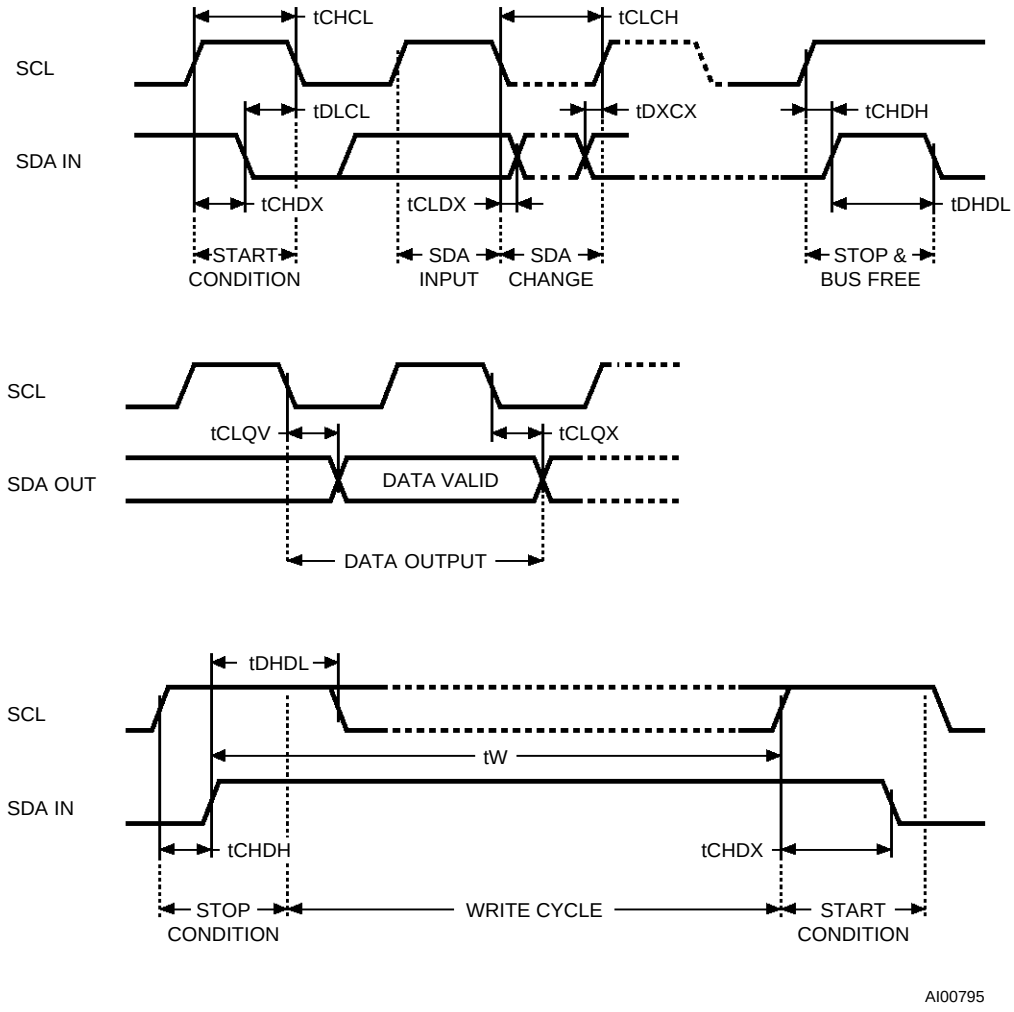
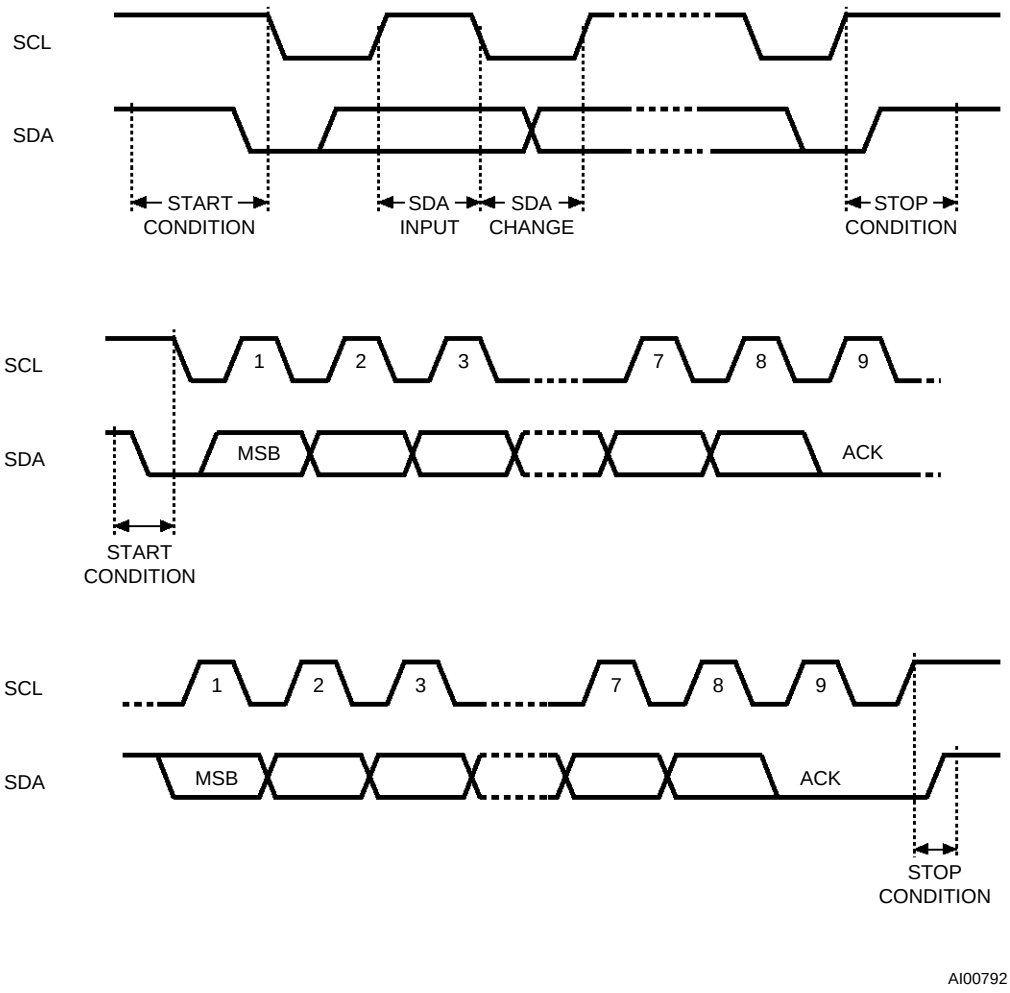


Figure 6. I²C Bus Protocol



Write Operations

The Multibyte Write mode (only available on the ST24/25C02 and ST24C02R versions) is selected when the MODE pin is at V_{IH} and the Page Write mode when MODE pin is at V_{IL}. The MODE pin may be driven dynamically with CMOS input levels.

Following a START condition the master sends a device select code with the $\overline{RW}$ bit reset to '0'. The memory acknowledges this and waits for a byte address. The byte address of 8 bits provides access to 256 bytes of the memory. After receipt of the byte address the device again responds with an acknowledge.

For the ST24/25W02 versions, any write command with $\overline{WC}$ = 1 will not modify the memory content.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition. The Write mode is independant of the state of the MODE pin which could be left floating if only this mode was to be used. However it is not a recommended operating mode, as this pin has to be connected to either V_{IH} or V_{IL}, to minimize the stand-by current.

Multibyte Write. For the Multibyte Write mode, the MODE pin must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 4 bytes of data, which are each acknowledged by the memory. The transfer is terminated by the master generating a STOP condition. The duration of the write cycle is t_W = 10ms maximum except when bytes are accessed on 2 rows (that is have different values for the 6 most significant address bits A7-A2), the programming time is then doubled to a maximum of 20ms. Writing more than 4 bytes in the Multibyte Write mode may modify data bytes in an adjacent row (one row is 8 bytes long). However, the Multibyte Write can properly write up to 8 consecutive bytes only if the first address of these 8 bytes is the first address of the row, the 7 following bytes being written in the 7 following bytes of this same row.

Page Write. For the Page Write mode, the MODE pin must be at V_{IL}. The Page Write mode allows up to 8 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 5 most significant memory address bits (A7-A3) are the same. The master sends from one up to 8 bytes of data, which are each acknowledged by the memory. After each byte is transfered, the internal byte address counter (3 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Figure 7. Write Cycle Polling using ACK

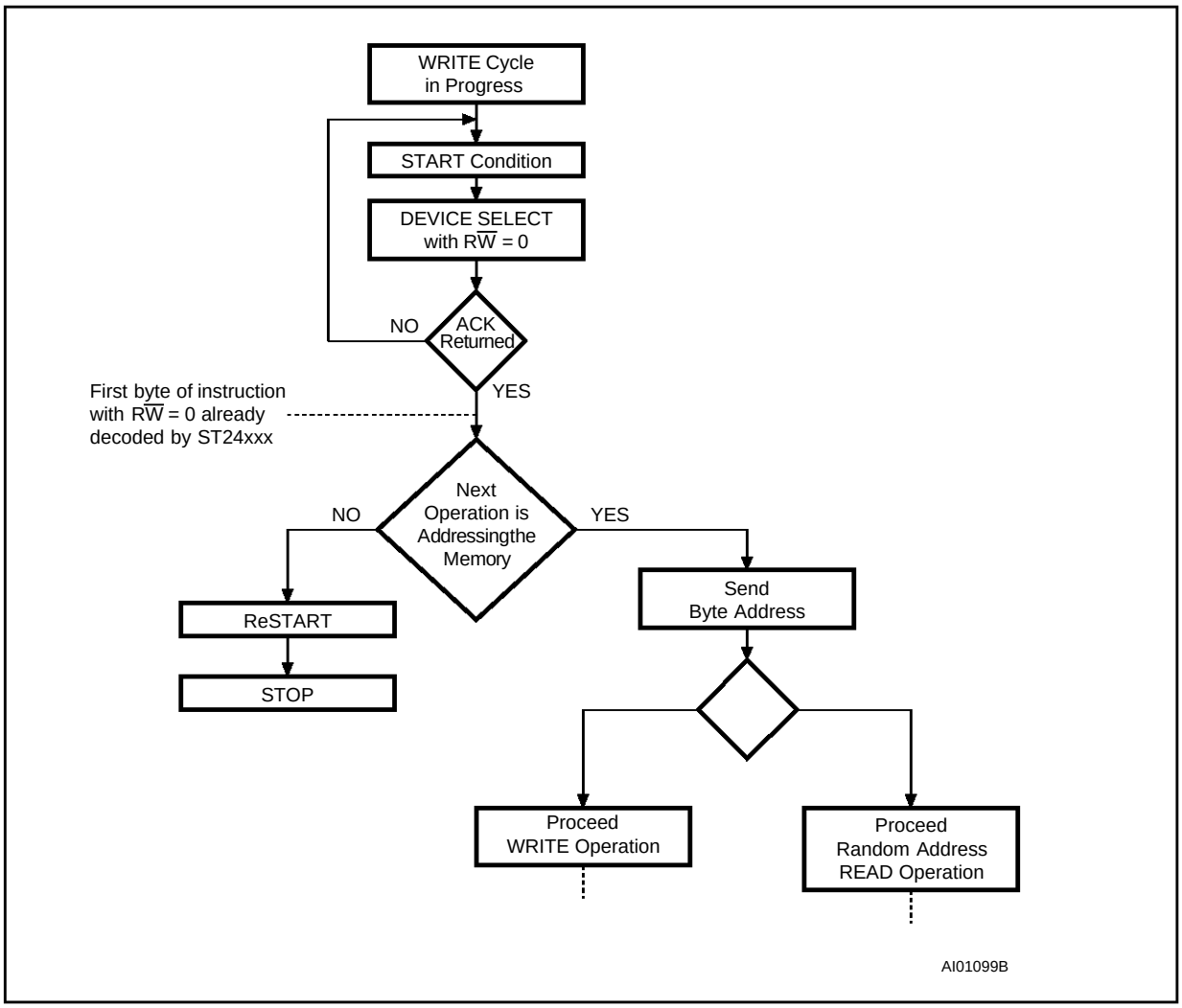
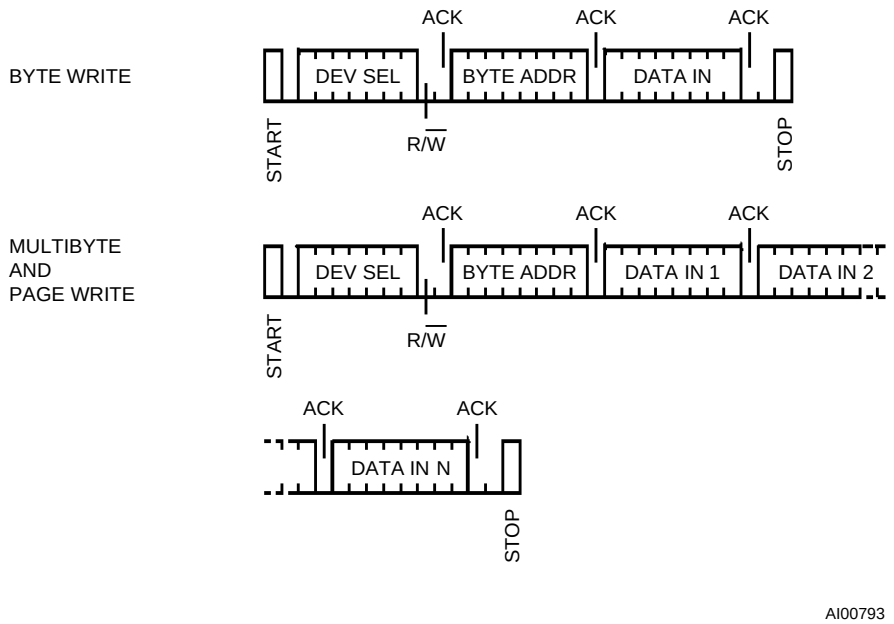


Figure 8. Write Modes Sequence (ST24/25C02 and ST24C02R)



Minimizing System Delays by Polling On ACK. During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (t_W) is given in the AC Characteristics table, since the typical time is shorter, the time seen by the system may be reduced by an ACK polling sequence issued by the master. The sequence is as follows:

– Initial condition: a Write is in progress (see Figure 7).
– Step 1: the master issues a START condition followed by a device select byte (1st byte of the new instruction).
– Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction was already sent during Step 1).

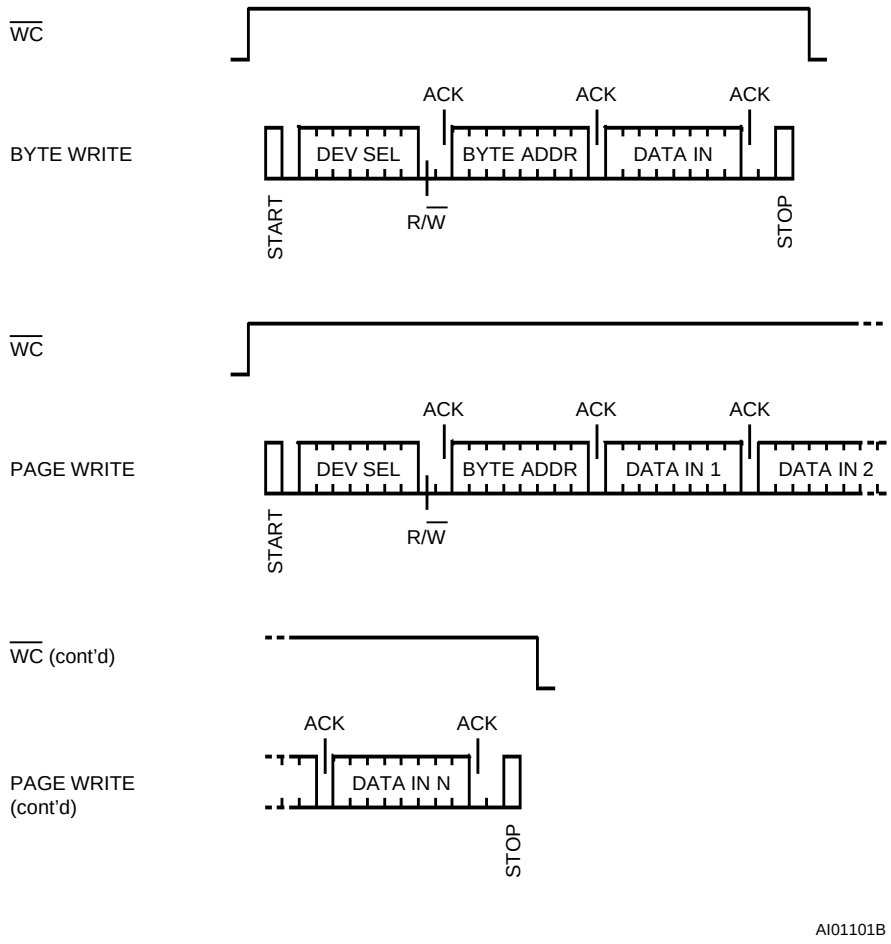
Read Operations

Read operations are independent of the state of the MODE pin. On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 10. This is followed by another START condition from the master and the byte address is repeated with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master have to NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

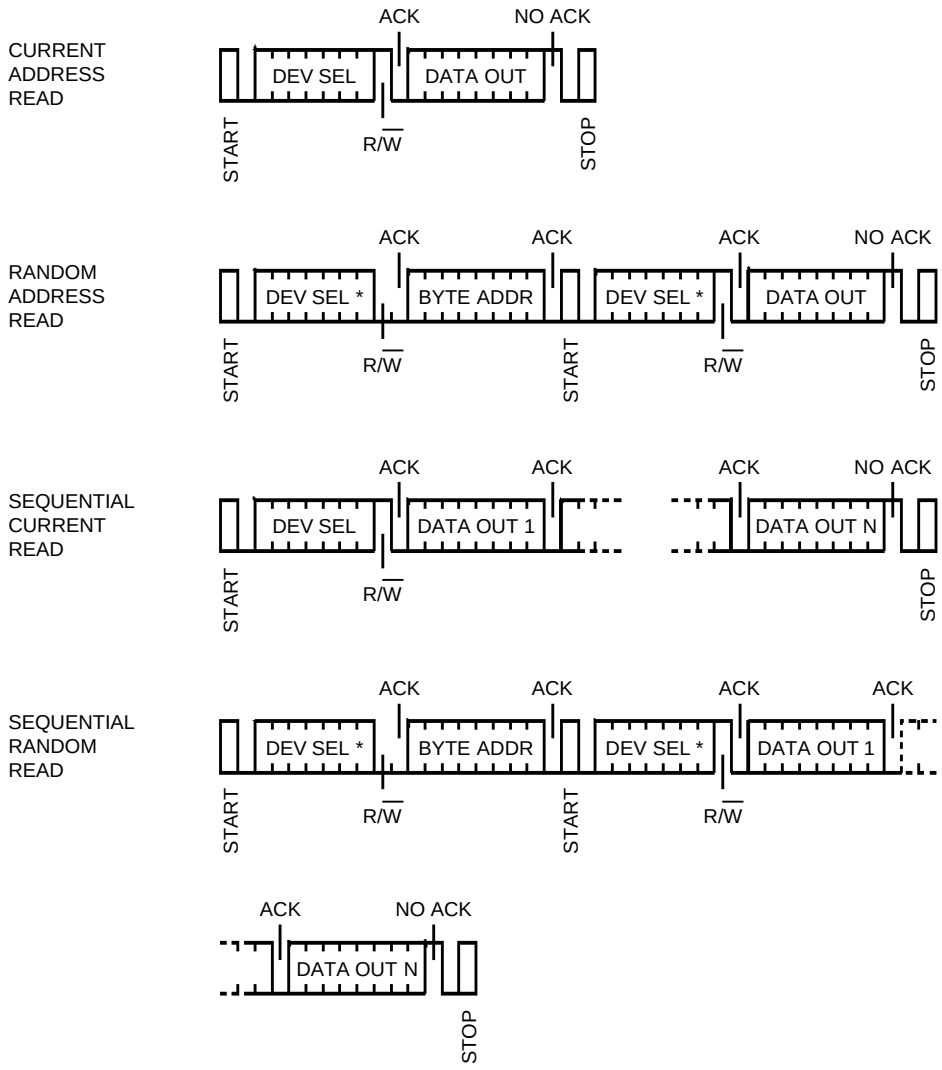
Figure 9. Write Modes Sequence with Write Control = 1 (ST24/25W02)



Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll- over' and the memory will continue to output data.

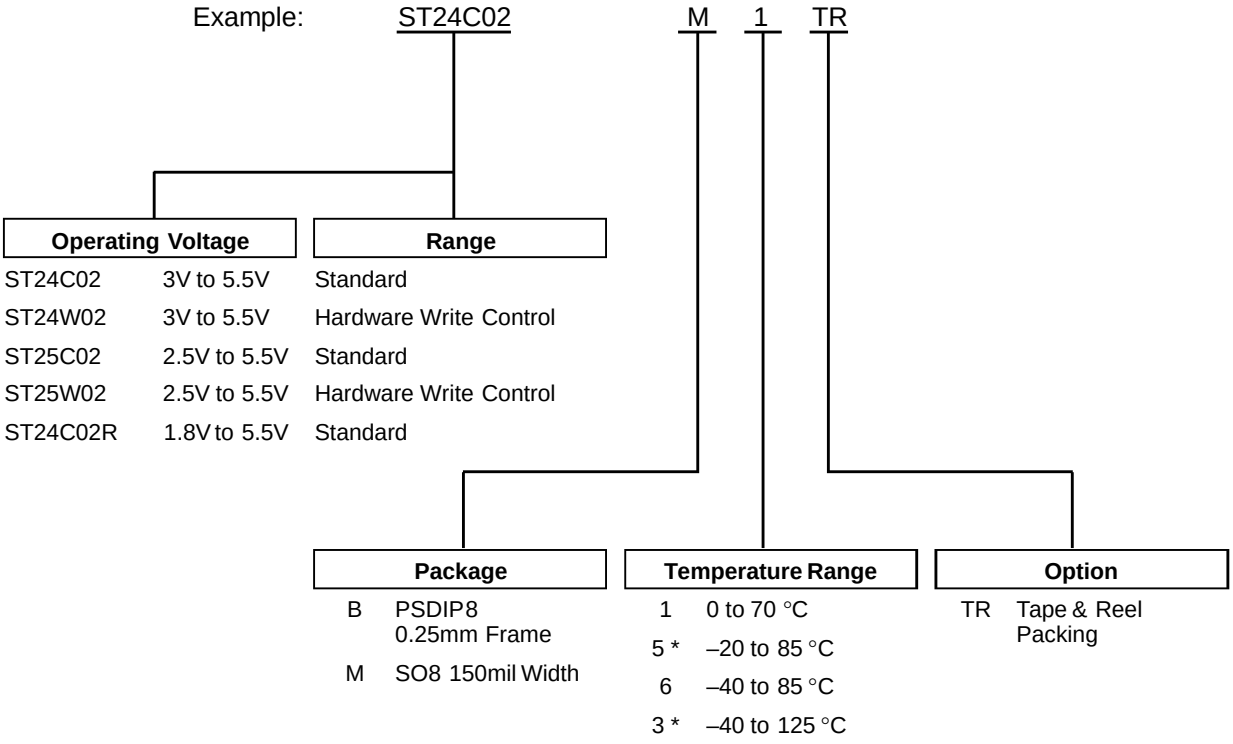
Acknowledge in Read Mode. In all read modes the ST24/25x02 wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25x02 terminate the data transfer and switches to a standby state.

Figure 10. Read Modes Sequence



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 3rd byte) must be identical.

ORDERING INFORMATION SCHEME



Notes: 3 * Temperature range on special request only.
5 * Temperature range for ST24C02R only.

Parts are shipped with the memory content set at all "1's" (FFh).

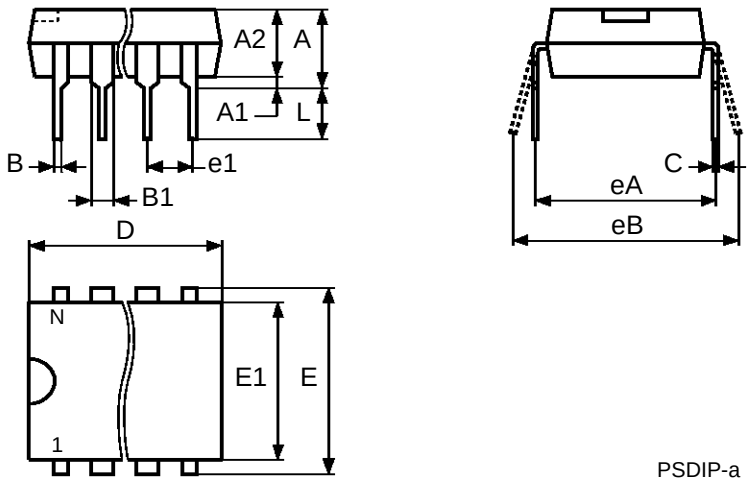
For a list of available options (Operating Voltage, Range, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

PSDIP8



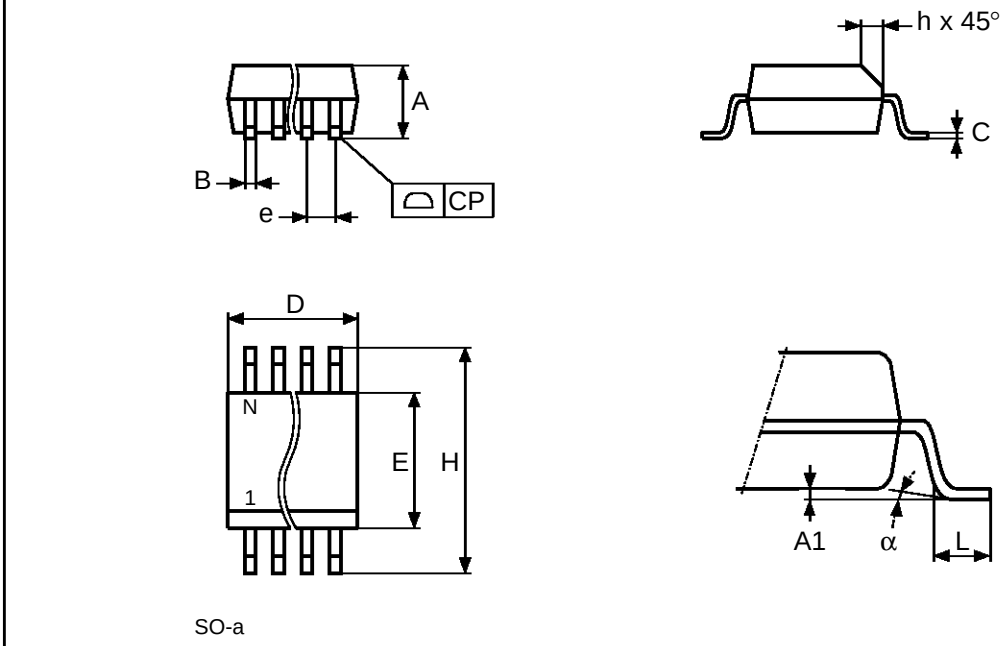
PSDIP-a

Drawing is not to scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8



SO-a

Drawing is not to scale

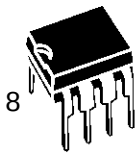
SGS-THOMSON MICROELECTRONICS

ST24C04, ST25C04
ST24W04, ST25W04

SERIAL 4K (512 x 8) EEPROM

DATA BRIEFING

- 1 MILLION ERASE/WRITE CYCLES with 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 3V to 5.5V for ST24x04 versions
  - 2.5V to 5.5V for ST25x04 versions
  - 1.8V to 5.5V for ST24C04R version only
- HARDWARE WRITE CONTROL VERSIONS: ST24W04 and ST25W04
- PROGRAMMABLE WRITE PROTECTION
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 4 BYTES)
- PAGE WRITE (up to 8 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES



PSDIP8 (B)
0.25mm Frame

SO8 (M)
150mil Width

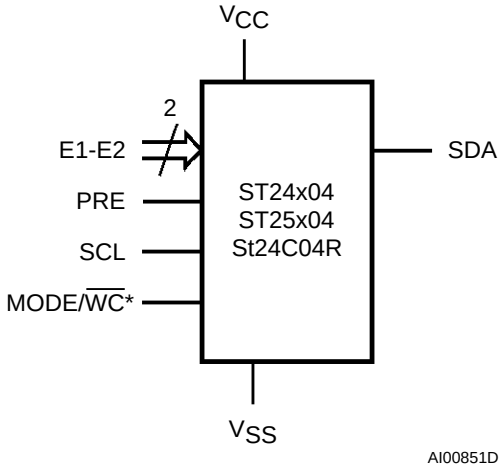
DESCRIPTION

This specification covers a range of 4K bits I^2C bus EEPROM products, the ST24/25C04, the ST24C04R and the ST24/25W04. In the text, products are referred to as ST24/25x04, where "x" is: "C" for Standard version and "W" for hardware Write Control version.

The ST24/25x04 are 4K bit electrically erasable programmable memories (EEPROM), organized as 2 blocks of 256 x 8 bits. They are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of one million erase/write cycles with a data retention of 40 years. The memories operate with a power supply value as low as 1.8V for the ST24C04R only.

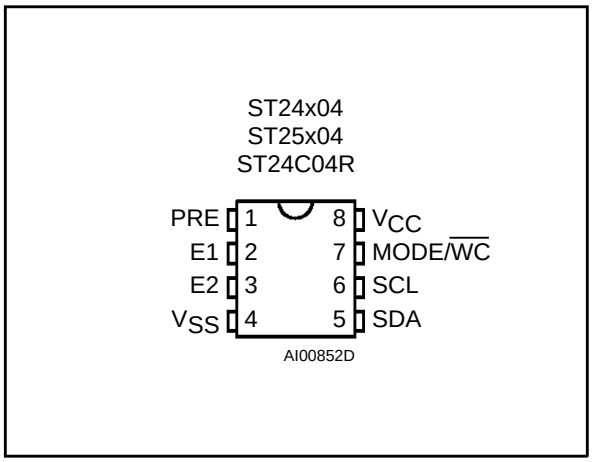
Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

Logic Diagram

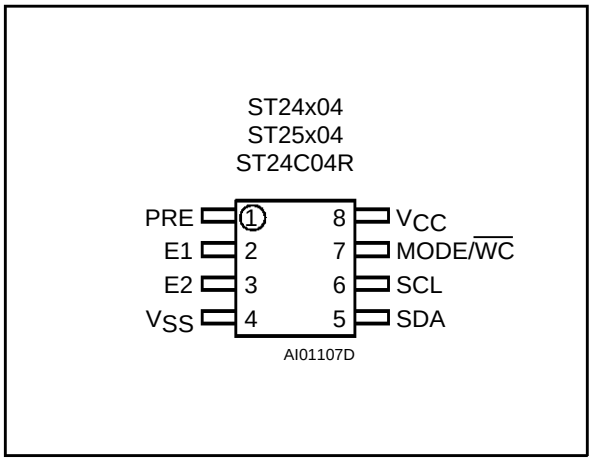


Note: $\overline{WC}$ signal is only available for ST24/25W04 products.

DIP Pin Connections



SO Pin Connections



Signal Names

PRE	Write Protect Enable
E1-E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multibyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Ordering Information Scheme

For a list of available options refer to the current Memory Shortform catalogue.
For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

Example: ST24C04 M 1 TR

Operating Voltage		Range
24C04	3V to 5.5V	Standard
24W04	3V to 5.5V	HW Write Control
25C04	2.5V to 5.5V	Standard
25W04	2.5V to 5.5V	HW Write Control
24C04R	1.8V to 5.5V	Standard

Package

- B PSDIP8 0.25mm Frame
- M SO8 150mil Width

Temp. Range

- 1 0 to 70 °C
- 5 –20 to 85 °C
- 6 –40 to 85 °C
- 3 –40 to 125 °C

Option

- TR Tape & Reel Packing

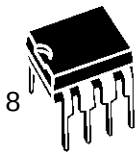
SGS-THOMSON MICROELECTRONICS

ST24C08, ST25C08
ST24W08, ST25W08

SERIAL 8K (1K x 8) EEPROM

DATA BRIEFING

- 1 MILLION ERASE/WRITE CYCLES with 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 3V to 5.5V for ST24x08 versions
  - 2.5V to 5.5V for ST25x08 versions
  - 1.8V to 5.5V for ST24C08R version only
- HARDWARE WRITE CONTROL VERSIONS: ST24W08 and ST25W08
- PROGRAMMABLE WRITE PROTECTION
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 8 BYTES)
- PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES



PSDIP8 (B)
0.25mm Frame

SO8 (M)
150mil Width

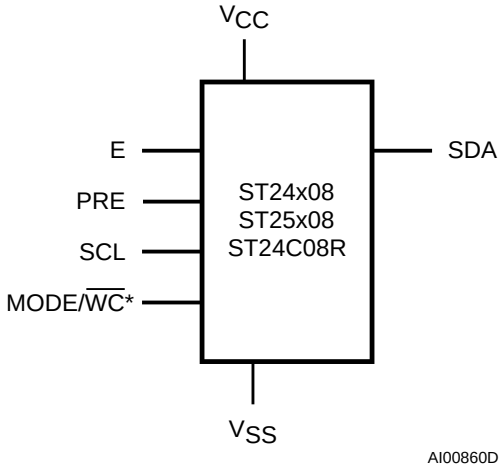
DESCRIPTION

This specification covers a range of 8K bits I^2C bus EEPROM products, the ST24/25C08, the ST24C08R and the ST24/25W08. In the text, products are referred to as ST24/25x08, where "x" is: "C" for Standard version and "W" for Hardware Write Control version.

The ST24/25x08 are 8K bit electrically erasable programmable memories (EEPROM), organized as 4 blocks of 256 x 8 bits. They are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of one million erase/write cycles with a data retention of 40 years. The memories operate with a power supply value as low as 1.8V for the ST24C08R only.

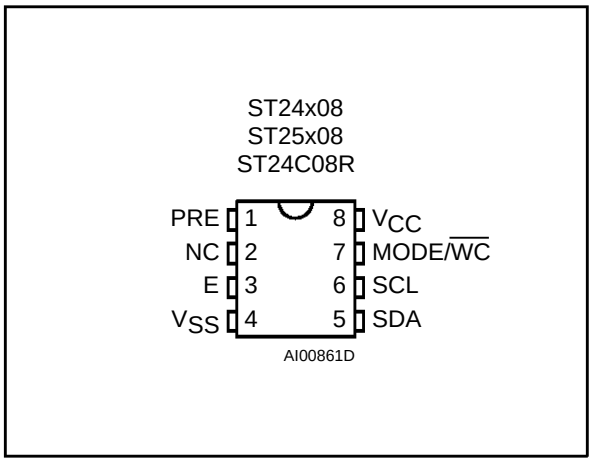
Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

Logic Diagram

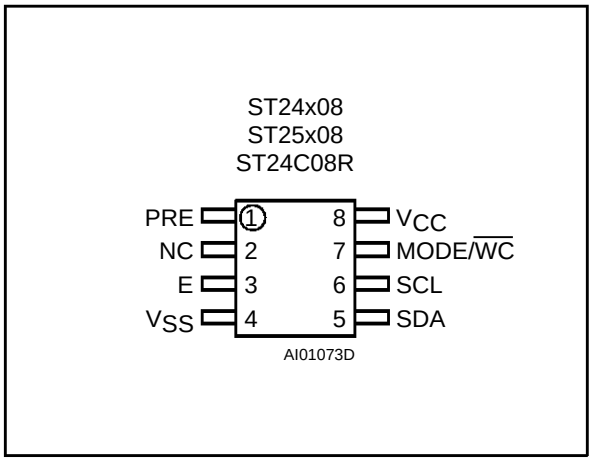


Note: $\overline{WC}$ signal is only available for ST24/25W08 products.

DIP Pin Connections



SO Pin Connections



Signal Names

PRE	Write Protect Enable
E	Chip Enable Input
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multibyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Ordering Information Scheme

For a list of available options refer to the current Memory Shortform catalogue.
For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

Example: ST24C08 M 1 TR

Operating Voltage		Range
24C08	3V to 5.5V	Standard
24W08	3V to 5.5V	HW Write Control
25C08	2.5V to 5.5V	Standard
25W08	2.5V to 5.5V	HW Write Control
24C08R	1.8V to 5.5V	Standard

Package

- B PSDIP8 0.25mm Frame
- M SO8 150mil Width

Temp. Range

- 1 0 to 70 °C
- 5 –20 to 85 °C
- 6 –40 to 85 °C
- 3 –40 to 125 °C

Option

- TR Tape & Reel Packing

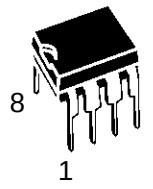
SGS-THOMSON MICROELECTRONICS

ST24C16, ST25C16
ST24W16, ST25W16

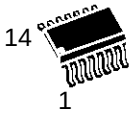
SERIAL 16K (2K x 8) EEPROM

DATA BRIEFING

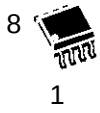
- 1 MILLION ERASE/WRITE CYCLES, with 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 4.5V to 5.5V for ST24x16 versions
  - 2.5V to 5.5V for ST25x16 versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W16 and ST25W16
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 8 BYTES) for the ST24C16
- PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES



PSDIP8 (B)
0.25mm Frame

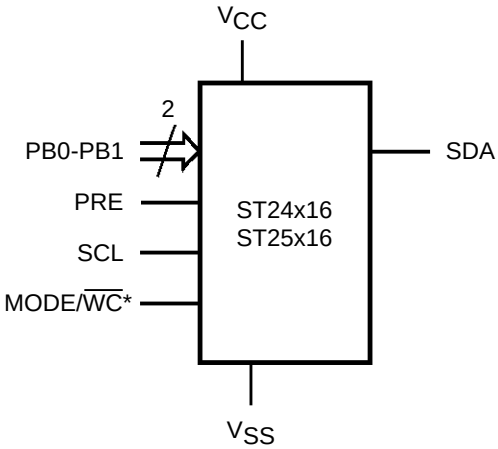


SO14 (ML)
150mil Width



SO8 (M)
150mil Width

Logic Diagram



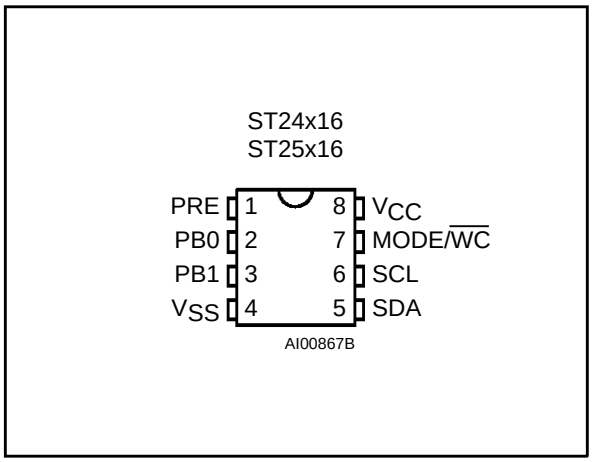
Note: $\overline{WC}$ signal is only available for ST24/25W16 products.

DESCRIPTION

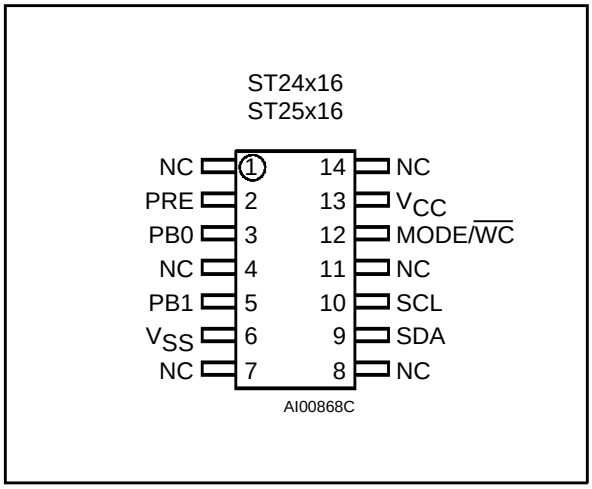
This specification covers a range of 16K bits I^2C bus EEPROM products, the ST24/25C16 and the ST24/25W16. In the text, products are referred to as ST24/25x16 where "x" is: "C" for Standard version and "W" for hardware Write Control version.

The ST24/25x16 are 16K bit electrically erasable programmable memories (EEPROM), organized as 8 blocks of 256 x 8 bits. These are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of one million erase/write cycles with a data retention of 40 years. The ST25x16 operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

DIP Pin Connections

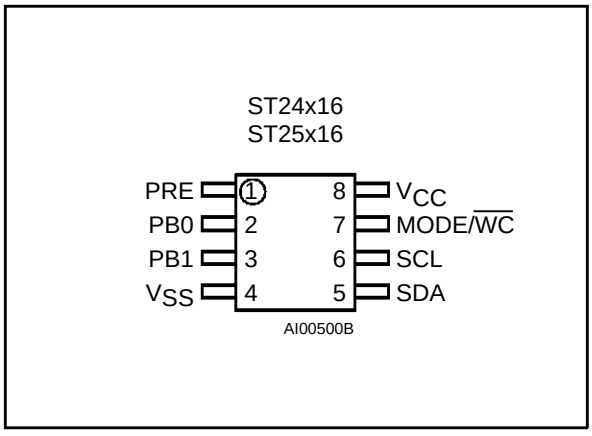


SO14 Pin Connections



Warning: NC = Not Connected.

SO8 Pin Connections



Signal Names

PRE	Write Protect Enable
PB0, PB1	Protect Block Select
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multybyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Ordering Information Scheme

For a list of available options refer to the current Memory Shortform catalogue.
For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

Example: ST24C16 M 1 TR

Operating Voltage
- 24 3V to 5.5V
- 25 2.5V to 5.5V

Range
- C Standard
- W Hardware Write Control

Package
- B PSDIP8 0.25mm Frame
- M SO8 150mil Width
- ML SO14 150mil Width

Temp. Range
- 1 0 to 70 °C
- 6 –40 to 85 °C
- 3 –40 to 125 °C

Option
- TR Tape & Reel Packing

SGS-THOMSON MICROELECTRONICS

ST93C06
ST93C06C

SERIAL MICROWIRE BUS 256 bit (16 x 16 or 32 x 8) EEPROM

- 1 MILLION ERASE/WRITE CYCLES, with 40 YEARS DATA RETENTION
- DUAL ORGANIZATION: 16 x 16 or 32 x 8
- BYTE/WORD and ENTIRE MEMORY PROGRAMMING INSTRUCTIONS
- SELF-TIMED PROGRAMMING CYCLE with AUTO-ERASE
- READY/BUSY SIGNAL DURING PROGRAMMING
- SINGLE 5V ±10% SUPPLY VOLTAGE
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME
- ENHANCED ESD/LATCH UP PERFORMANCES for "C" VERSION

PSDIP8 (B)
0.4mm Frame

SO8 (M)
150mil Width

DESCRIPTION

The ST93C06 and ST93C06C are 256 bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. In the text the two products are referred to as ST93C06.

The memory is divided into either 32 x 8 bit bytes or 16 x 16 bit words. The organization may be selected by a signal applied on the ORG input.

The memory is accessed through a serial input (D) and by a set of instructions which includes Read a byte/word, Write a byte/word, Erase a byte/word, Erase All and Write All. A Read instruction loads the address of the first byte/word to be read into an internal address pointer.

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
ORG	Organisation Select
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

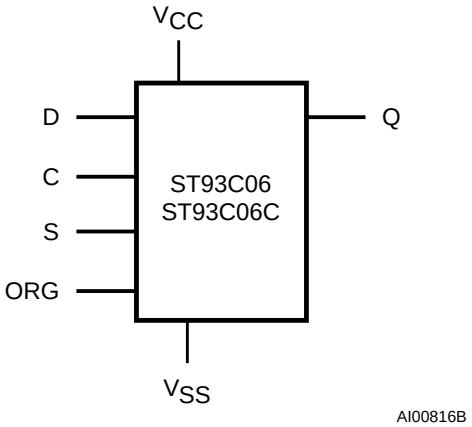
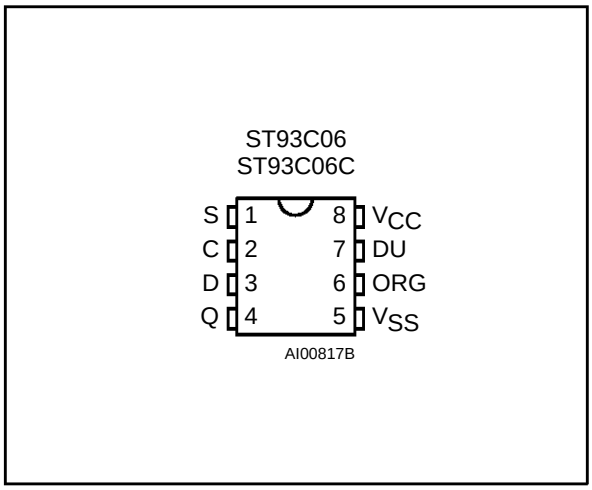
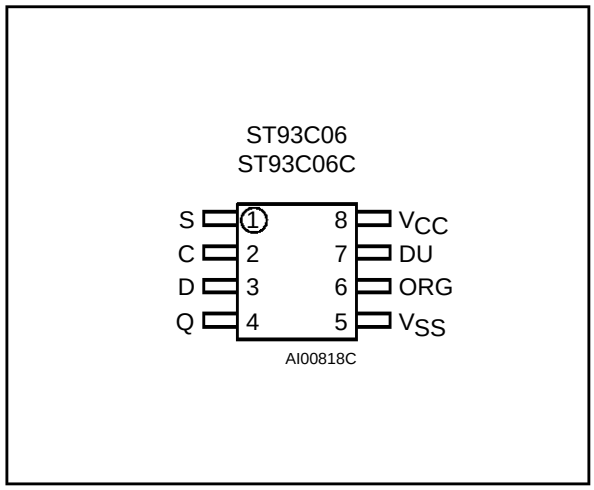


Figure 2A. DIP Pin Connections



Warning: DU = Don't Use

Figure 2B. SO Pin Connections



Warning: DU = Don't Use

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		–40 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) 40 sec (PSDIP8 package) 10 sec	215 260	°C
V_{IO}	Input or Output Voltages (Q = V_{OH} or Hi-Z)		–0.3 to V_{CC} +0.5	V
V_{CC}	Supply Voltage		–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)	ST93C06 ST93C06C	2000 4000	V
	Electrostatic Discharge Voltage (Machine model) (3)	ST93C06 ST93C06C	500 500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

The data contained at this address is then clocked out serially. The address pointer is automatically incremented after the data is output and, if the Chip Select input (S) is held High, the ST93C06 can output a sequential stream of data bytes/words. In this way, the memory can be read as a data stream from 8 to 256 bits long, or continuously as the address counter automatically rolls over to '00' when the highest address is reached. Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a Write cycle) and does not require an erase cycle prior to the Write instruction. The Write instruction writes 8 or 16 bits at one time into one of the 32 bytes or 16 words. After the start of the programming cycle a Busy/Ready signal is available on the Data output (Q) when Chip Select (S) is driven High.

The design of the ST93C06 and the High Endurance CMOS technology used for its fabrication give an Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of 40 years.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input Timing Reference Voltages	1V to 2.0V
Output Timing Reference Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

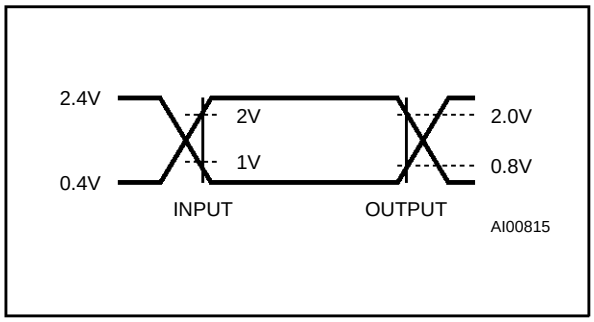


Table 3. Capacitance (1)
(T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: 1. Sampled only, not 100% tested.

Table 4. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±2.5	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current (TTL Inputs)	S = V_{IH}, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	S = V_{IH}, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}		50	µA
V_{IL}	Input Low Voltage (D, C, S)		–0.3	0.8	V
V_{IH}	Input High Voltage (D, C, S)		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
		I_{OL} = 10 µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
		I_{OH} = –10µA	V_{CC} – 0.2		V

Table 5. AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 5V ± 10%)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{CLSH}	t_{SKS}	Clock Low to Chip Select High		100		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition	Temp. Range: grade 1	100		ns
			Temp. Range: grades 3, 6	200		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low			500	ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid			500	ns
t_{CLSL}	t_{CSH}	Clock Low to Chip Select Low		0		ns
t_{SLCH}		Chip Select Low to Clock High		250		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid			500	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z	ST93C06		300	ns
			ST93C06C		200	ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_W	t_{WP}	Erase/Write Cycle time			10	ms
f_C	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1. Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles.
2. The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs. For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns.

Figure 4. Synchronous Timing, Start and Op-Code Input

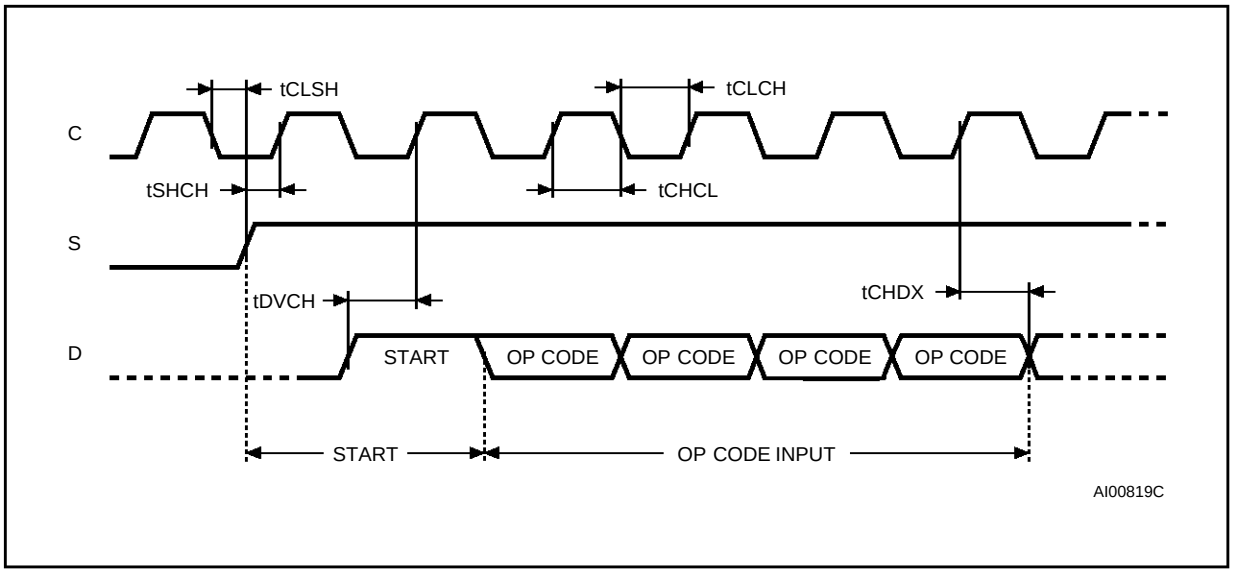
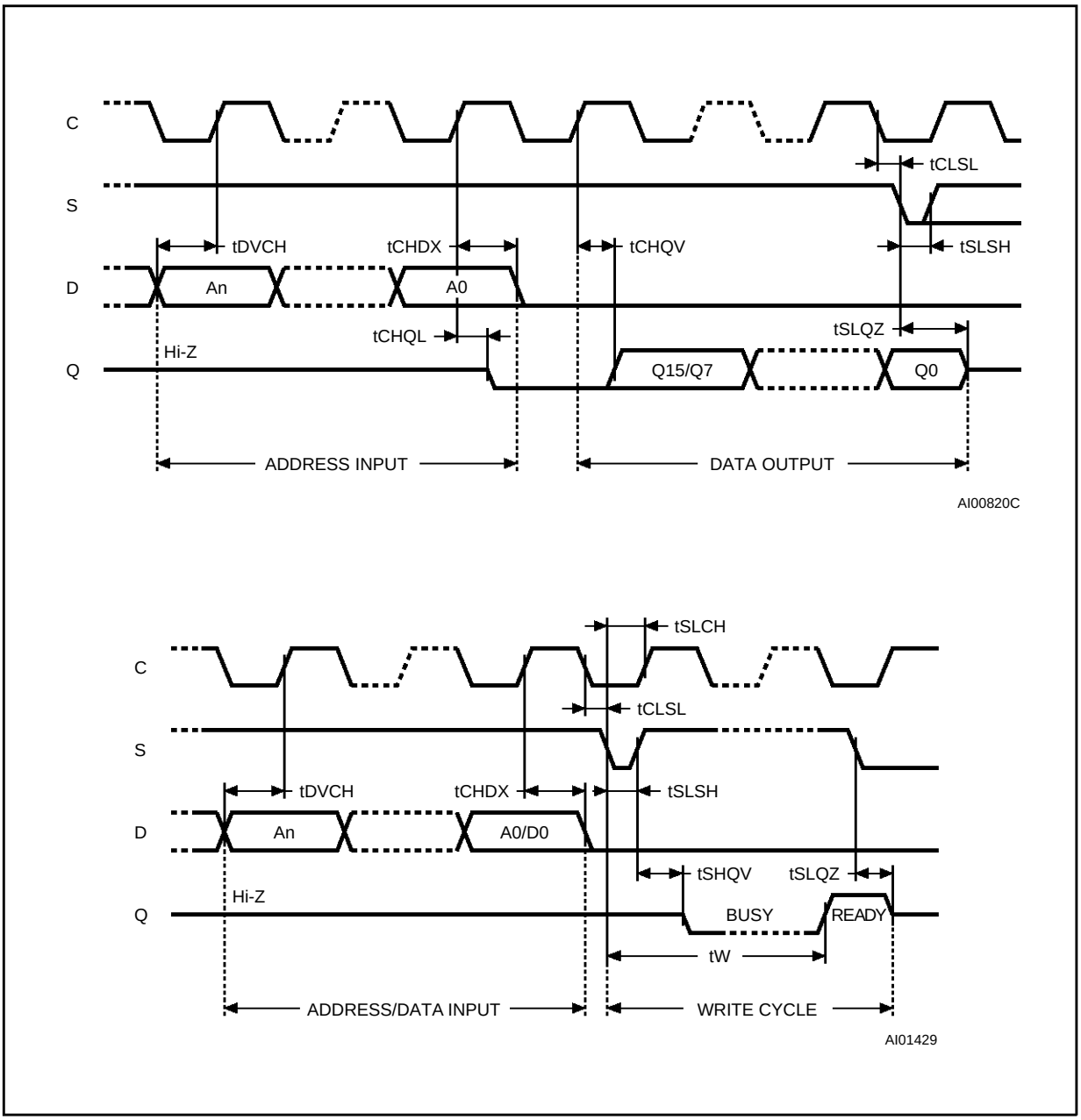


Figure 5. Synchronous Timing, Read or Write



DESCRIPTION (cont'd)

The DU (Don't Use) pin does not affect the function of the memory and it is reserved for use by SGS-THOMSON during test sequences. The pin may be left unconnected or may be connected to V_{CC} or V_{SS}. Direct connection of DU to V_{SS} is recommended for the lowest standby power consumption.

MEMORY ORGANIZATION

The ST93C06 is organized as 32 bytes x 8 bits or 16 words x 16 bits. If the ORG input is left unconnected (or connected to V_{CC}) the x16 organization is selected, when ORG is connected to Ground (V_{SS}) the x8 organization is selected. When the ST93C06 is in standby mode, the ORG input should be unconnected or set to either V_{SS} or V_{CC} in order to achieve the minimum power consumption. Any voltage between V_{SS} and V_{CC} applied to ORG may increase the standby current value.

POWER-ON DATA PROTECTION

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit resets all internal programming circuitry and sets the device in the Write Disable mode. When V_{CC} reaches its functional value, the device is properly reset (in the Write Disable mode) and is ready to decode and execute an incoming instruction. A stable V_{CC} must be applied before any logic signal.

INSTRUCTIONS

The ST93C06 has seven instructions, as shown in Table 6. The op-codes of the instructions are made up of 4 bits: some instructions use only the first two bits, others use all four bits to define the op-code. The op-code is followed by an address for the byte/word which is four bits long for the x16 organization or five bits long for the x8 organization.

Each instruction is preceded by the rising edge of the signal applied on the S input (assuming that clock C and data input D are low), followed by a first clock pulse which is ignored by the ST93C06 (optional clock pulse for the ST93C06C). The data input D is then sampled upon the following rising edges of the clock C untill a '1' is sampled and decoded by the ST93C06 as a Start bit. Even though the first clock pulse is ignored, it recommended to pull low the data input D during this first clock pulse in order to keep the timing upwardly compatible with other ST93Cxx devices.

The ST93C06 is fabricated in CMOS technology and is therefore able to run from zero Hz (static input signals) up to the maximum ratings (specified in Table 5).

Read

The Read instruction (READ) outputs serial data on the Data Output (Q). When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 8 bit byte or the 16 bit word with the MSB first. Output data changes are triggered by the Low to High transition of the Clock (C). The ST93C06 will automatically increment the address and will clock out the next byte/word as long as the Chip Select input (S) is held High. In this case the dummy '0' bit is NOT output between bytes/words and a continuous stream of data can be read.

Erase/Write Enable and Disable

The Erase/Write Enable instruction (EWEN) authorizes the following Erase/Write instructions to be executed, the Erase/Write Disable instruction (EWDS) disables the execution of the following Erase/Write instructions. When power is first applied, the ST93C06 enters the Disable mode. When the Erase/Write Enable instruction (EWEN) is executed, Write instructions remain enabled until an Erase/Write Disable instruction (EWDS) is executed or if the Power-on reset circuit becomes active due to a reduced V_{CC}. To protect the memory contents from accidental corruption, it is advisable to issue the EWDS instruction after every write cycle. The READ instruction is not affected by the EWEN or EWDS instructions.

Erase

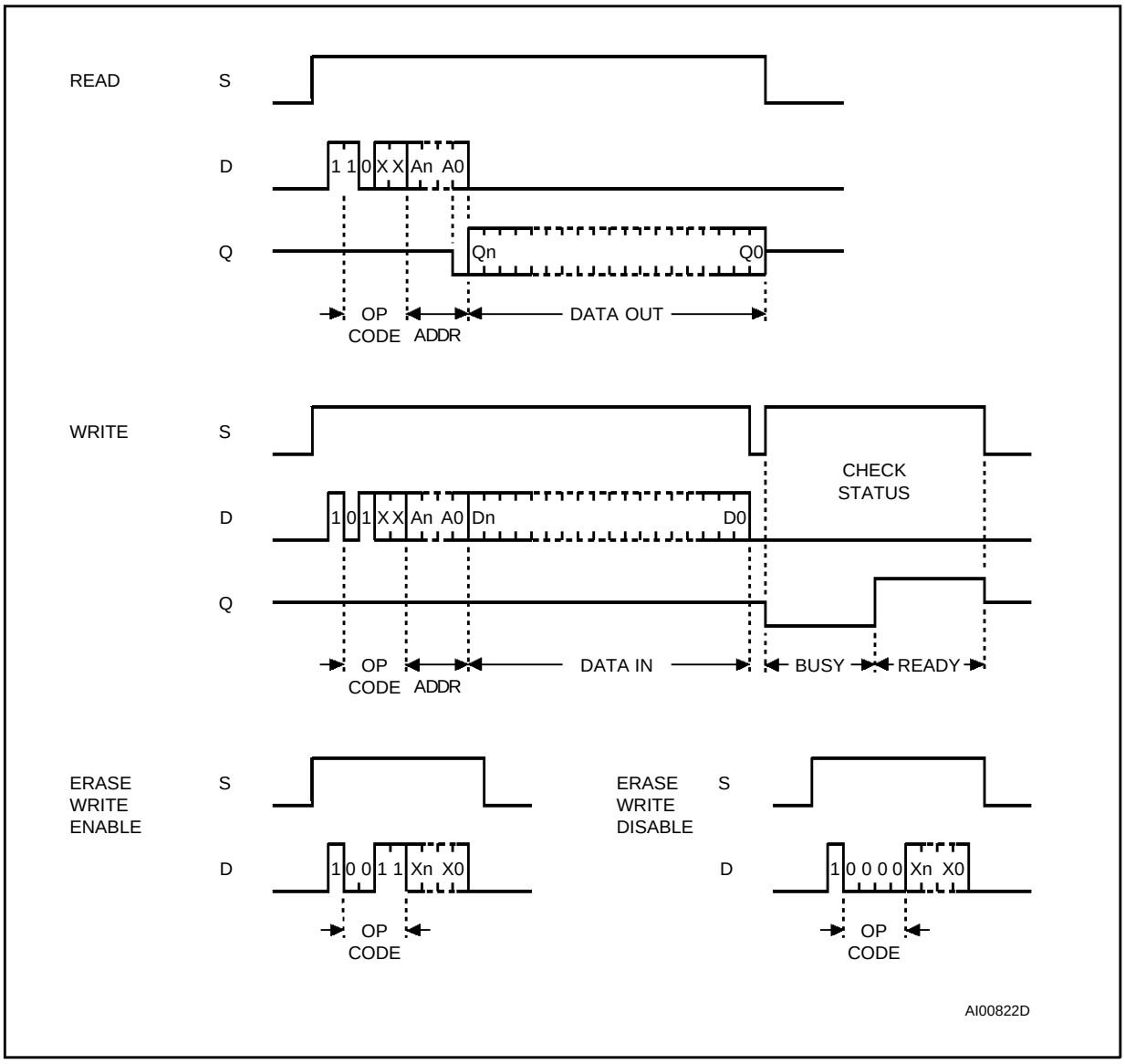
The Erase instruction (ERASE) programs the addressed memory byte or word bits to '1'. Once the address is correctly decoded, the falling edge of the Chip Select input (S) triggers a self-timed erase cycle.

Table 6. Instruction Set

Instruction	Description	Op-Code	x8 Org Address (ORG = 0)	Data	x16 Org Address (ORG = 1)	Data
READ	Read Data from Memory	10XX	A4-A0	Q7-Q0	A3-A0	Q15-Q0
WRITE	Write Data to Memory	01XX	A4-A0	D7-D0	A3-A0	D15-D0
EWEN	Erase/Write Enable	0011	XXXXX		XXXX	
EWDS	Erase/Write Disable	0000	XXXXX		XXXX	
ERASE	Erase Byte or Word	11XX	A4-A0		A3-A0	
ERAL	Erase All Memory	0010	XXXXX		XXXX	
WRAL	Write All Memory with same Data	0001	XXXXX	D7-D0	XXXX	D15-D0

Note: X = don't care bit.

Figure 6. READ, WRITE, EWEN, EWDS Sequences



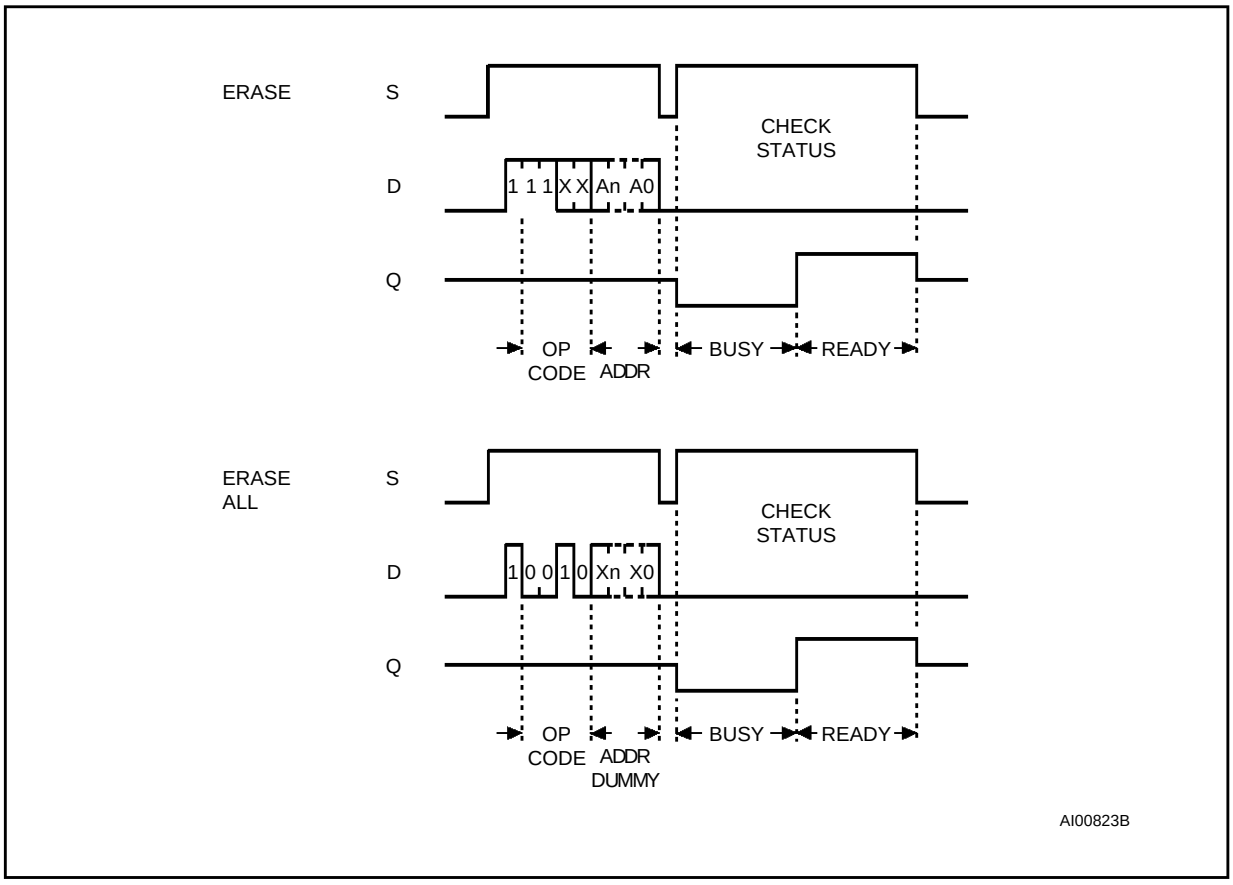
Notes: 1. An: n = 3 for x16 org. and 4 for x8 org.
2. Xn: n = 3 for x16 org. and 4 for x8 org.

If the ST93C06 is still performing the erase cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C06 will ignore any data on the bus. When the erase cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C06 is ready to receive a new instruction.

Write

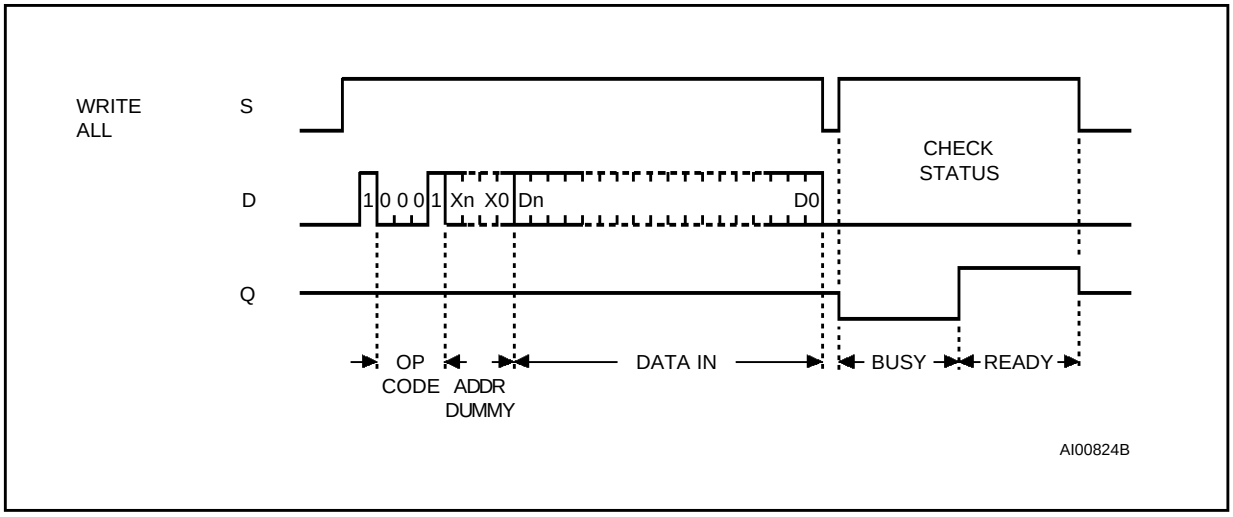
The Write instruction (WRITE) is followed by the address and the 8 or 16 data bits to be written. Data input is sampled on the Low to High transition of the clock. After the last data bit has been sampled, Chip Select (S) must be brought Low before the next rising edge of the clock (C) in order to start the self-timed programming cycle. If the ST93C06 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C06 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C06 is ready to receive a new instruction. Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a programming cycle) and does not require an Erase instruction prior to the Write instruction (The Write instruction includes an automatic erase cycle before programing data).

Figure 7. ERASE, ERAL Sequences



Notes: 1. An: n = 3 for x16 org. and 4 for x8 org.
2. Xn: n = 3 for x16 org. and 4 for x8 org.

Figure 8. WRAL Sequence



Note: 1 Xn: n = 3 for x16 org. and 4 for x8 org.

Erase All

The Erase All instruction (ERAL) erases the whole memory (all memory bits are set to '1'). A dummy address is input during the instruction transfer and the erase is made in the same way as the ERASE instruction. If the ST93C06 is still performing the erase cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C06 will ignore any data on the bus. When the erase cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C06 is ready to receive a new instruction.

Write All

For correct operation, an ERAL instruction should be executed before the WRAL instruction: the WRAL instruction DOES NOT perform an automatic erase before writing. The Write All instruction (WRAL) writes the Data Input byte or word to all the addresses of the memory. If the ST93C06 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C06 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C06 is ready to receive a new instruction.

READY/BUSY Status

During every programming cycle (after a WRITE, ERASE, WRAL or ERAL instruction) the Data Output (Q) indicates the Ready/Busy status of the memory when the Chip Select (S) is driven High. Once the ST93C06 is Ready, the Ready/Busy status is available on the Data Output (Q) until a new start bit is decoded or the Chip Select (S) is brought Low.

COMMON I/O OPERATION

The Data Output (Q) and Data Input (D) signals can be connected together, through a current limiting resistor, to form a common, one wire data bus. Some precautions must be taken when operating the memory with this connection, mostly to prevent a short circuit between the last entered address bit (A0) and the first data bit output by Q. The reader may also refer to the SGS-THOMSON application note "MICROWIRE EEPROM Common I/O Operation".

DIFFERENCES BETWEEN ST93C06 AND ST93C06C

Each instruction of the ST93C06 requires an Additional Dummy clock pulse after the rising edge of the Chip Select input (S) and before the START bit, see Figure 9. When replacing the ST93C06 with the ST93C06C in an application, it must be checked that this Dummy Clock cycle DOES NOT HAPPEN when D = 1: if it is so, this clock pulse will latch an information which is decoded by the ST93C06C as a START bit (see Figure 10) and the following bits will be decoded with a shift of one bit.

Figure 9. ST93C06 Timing

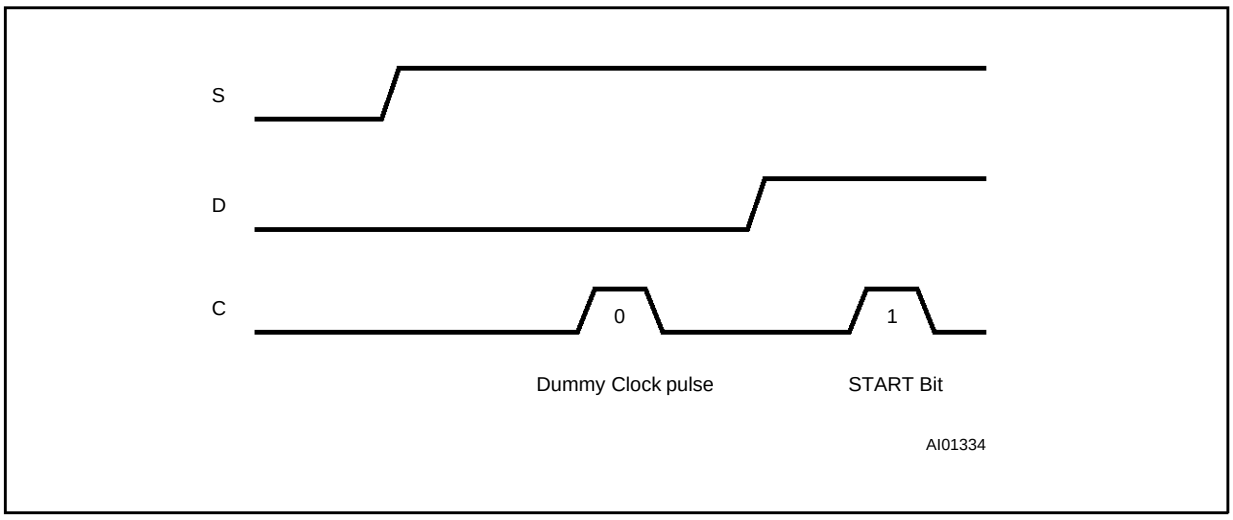


Figure 10. Comparative Timings

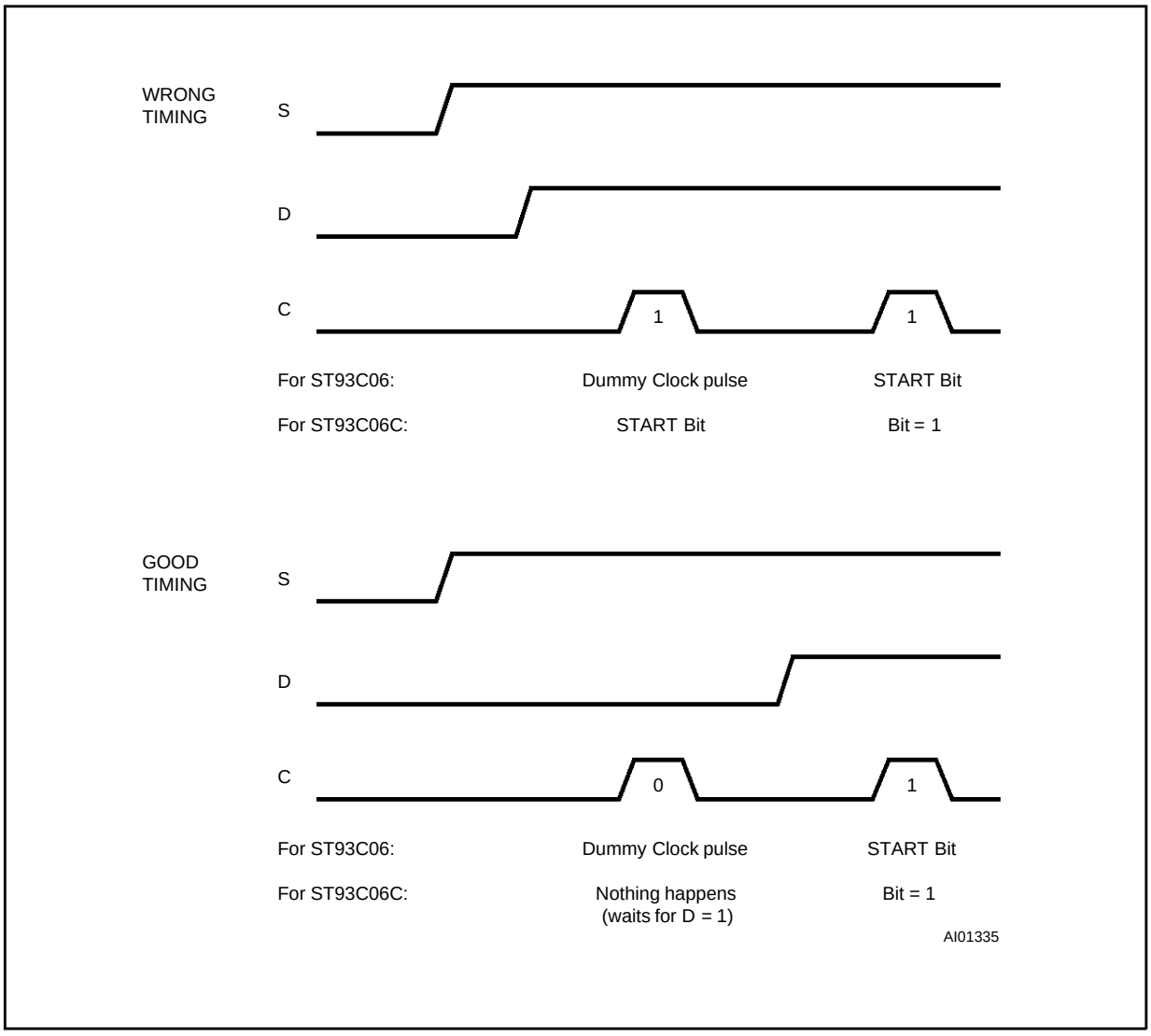
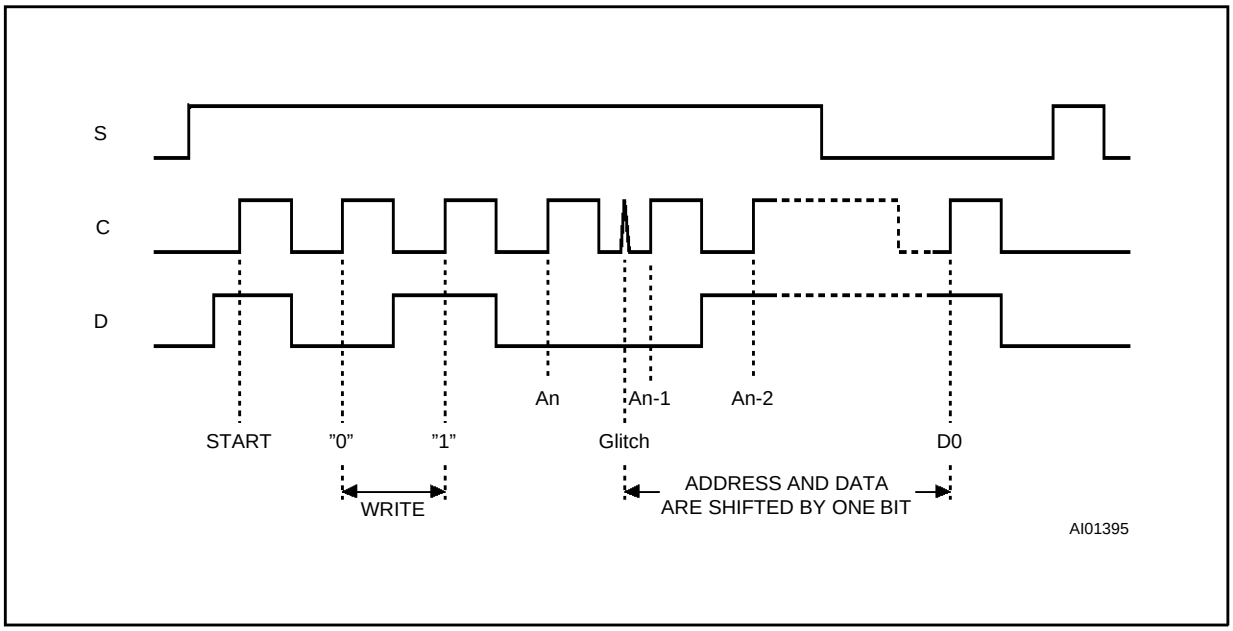


Figure 11. WRITE Swquence with One Clock Glitch



DIFFERENCES BETWEEN ST93C06 AND ST93C06C (cont'd)

The ST93C06C is an enhanced version of the ST93C06A and offers the following extra features:

– Enhanced ESD voltage

– Functional security filtering glitches on the clock input (C).

Refer to Table 2 (Absolute Maximum Ratings) for more about ESD limits. The following description will detail the Clock pulses counter (available only on the ST93C06C).

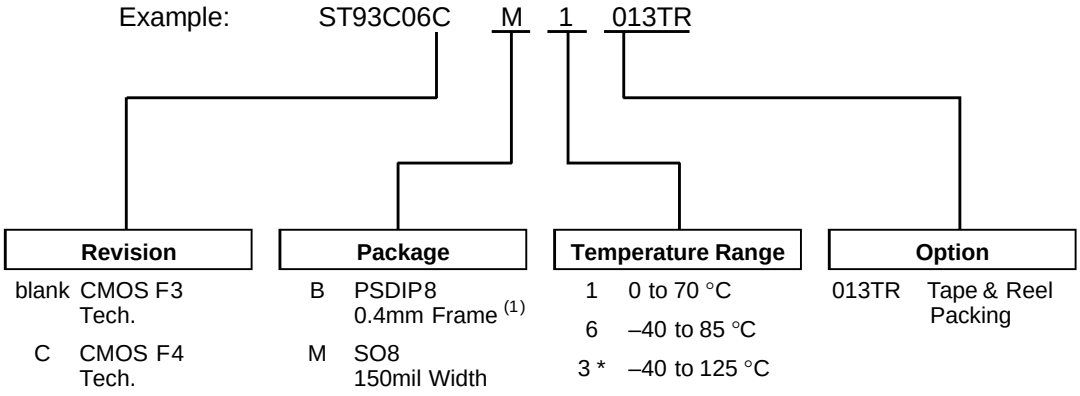
In a normal environment, the ST93C06 is expected to receive the exact amount of data on the D input, that is the exact amount of clock pulses on the C input.

In a noisy environment, the amount of pulses received (on the clock input C) may be greater than the clock pulses delivered by the Master (Microcontroller) driving the ST93C06C. In such a case, a part of the instruction is delayed by one bit (see Figure 11), and it may induce an erroneous write of data at a wrong address.

The ST93C46C has an on-board counter which counts the clock pulses from the Start bit until the falling edge of the Chip Select signal. For the WRITE instructions, the number of clock pulses incoming to the counter must be exactly 18 (with the Organisation by 8) from the Start bit to the falling edge of Chip Select signal (1 Start bit + 2 bits of Op-code + 7 bits of Address + 8 bits of Data = 18): if so, the ST93C06C executes the WRITE instruction; if the number of clock pulses is not equal to 18, the instruction will not be executed (and data will not be corrupted).

In the same way, when the Organisation by 16 is selected, the number of clock pulses incoming to the counter must be exactly 25 (1 Start bit + 2 bits of Op-code + 6 bits of Address + 16 bits of Data = 25) from the Start bit to the falling edge of Chip Select signal: if so, the ST93C06C executes the WRITE instruction; if the number of clock pulses is not equal to 25, the instruction will not be executed (and data will not be corrupted). The clock pulse counter is active only on ERASE and WRITE instructions (WRITE, ERASE, ERAL, WRALL).

ORDERING INFORMATION SCHEME



Notes: 1. ST93C06CB1 is available with 0.25mm lead Frame only.
3 * Temperature range on special request only.

Parts are shipped with the memory content set at all "1's" (FFFFh for x16, FFh for x8).

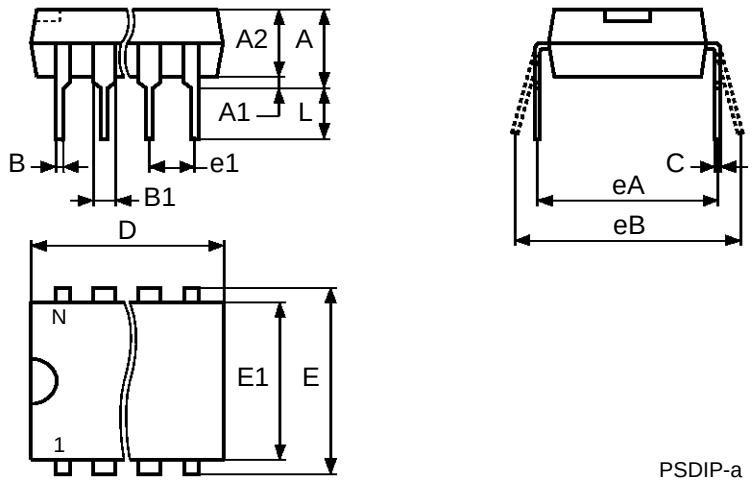
For a list of available options (Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.4mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			4.80			0.189
A1		0.70	–		0.028	–
A2		3.10	3.60		0.122	0.142
B		0.38	0.58		0.015	0.023
B1		1.15	1.65		0.045	0.065
C		0.38	0.52		0.015	0.020
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.30	7.10		0.248	0.280
e1	2.54	–	–	0.100	–	–
eA		8.40	–		0.331	–
eB			9.20			0.362
L		3.00	3.80		0.118	0.150
N	8			8		

PSDIP8



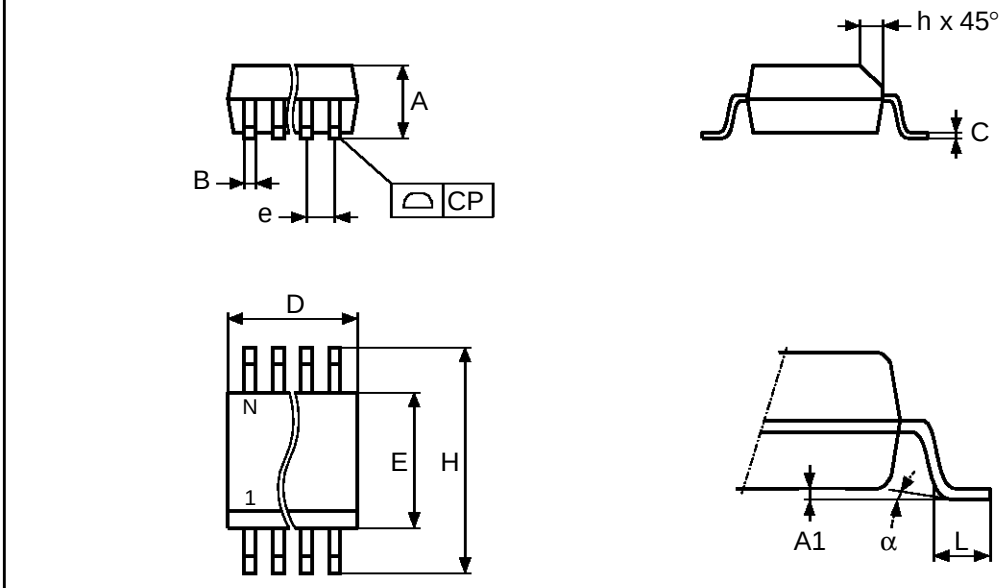
PSDIP-a

Drawing is not to scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8



SO-a

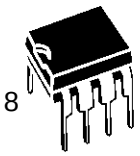
Drawing is not to scale

SGS-THOMSON MICROELECTRONICS

ST93C46A,46C,46T
ST93C47C,47T

SERIAL MICROWIRE BUS 1K (64 x 16 or 128 x 8) EEPROM

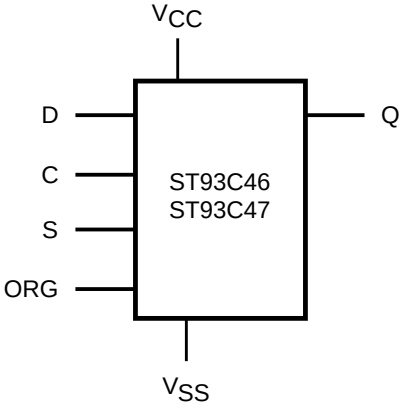
- 1 MILLION ERASE/WRITE CYCLES, with 40 YEARS DATA RETENTION
- DUAL ORGANIZATION: 64 x 16 or 128 x 8
- BYTE/WORD and ENTIRE MEMORY PROGRAMMING INSTRUCTIONS
- SELF-TIMED PROGRAMMING CYCLE with AUTO-ERASE
- READY/BUSY SIGNAL DURING PROGRAMMING
- SINGLE SUPPLY VOLTAGE:
  - 4.5V to 5.5V for ST93C46 version
  - 3V to 5.5V for ST93C47 version
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME
- ENHANCED ESD/LATCH UP PERFORMANCE for "C" VERSION



PSDIP8 (B)
0.4mm Frame

SO8 (M)
150mil Width

Figure 1. Logic Diagram



DESCRIPTION

This specification covers a range of 1K bit serial EEPROM products, the ST93C46A,46C,46T specified at 5V±10% and the ST93C47C,47T specified at 3V to 5.5V.

In the text, products are referred to as ST93C46. The ST93C46 is a 1K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed through a serial input (D) and output (Q).

Table 1. Signal Names

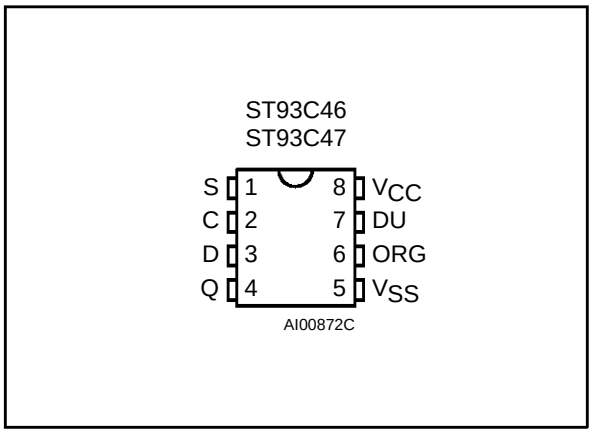
S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
ORG	Organisation Select
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature			–40 to 125	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages (Q = V_{OH} or Hi-Z)			–0.3 to V_{CC} +0.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		ST93C46A,T ST93C46C	2000 4000	V
	Electrostatic Discharge Voltage (Machine model) (3)		ST93C46	500	V

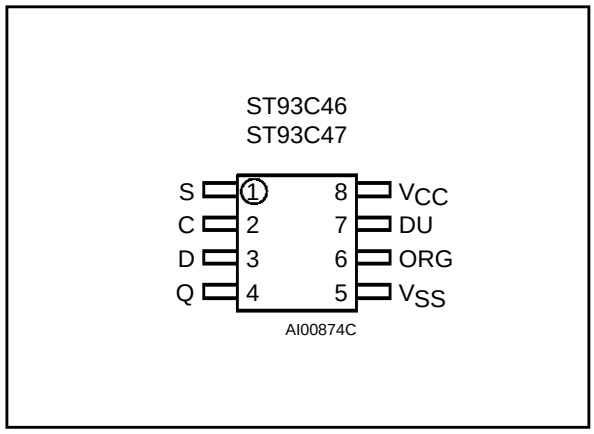
Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

Figure 2A. DIP Pin Connections



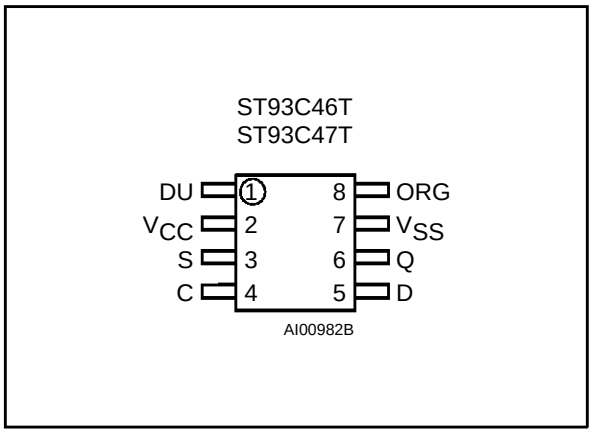
Warning: DU = Don't Use

Figure 2B. SO Pin Connections



Warning: DU = Don't Use

Figure 2C. SO, 90° Turn, Pin Connections



Warning: DU = Don't Use

DESCRIPTION (cont'd)

The 1K bit memory is divided into either 128 x 8 bit bytes or 64 x 16 bit words. The organization may be selected by a signal on the ORG input. The memory is accessed by a set of instructions which includes Read a byte/word, Write a byte/word, Erase a byte/word, Erase All and Write All.

A Read instruction loads the address of the first byte/word to be read into an internal address pointer. The data is then clocked out serially.

The address pointer is automatically incremented after the data is output and, if the Chip Select input (S) is held High, the ST93C46 can output a sequential stream of data bytes/words. In this way, the memory can be read as a data stream from 8 to 1024 bits long, or continuously as the address

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input Timing Reference Voltages	1V to 2.0V
Output Timing Reference Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

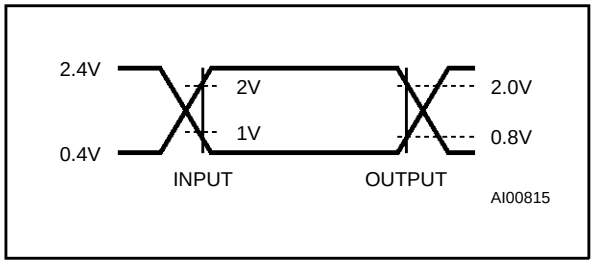


Table 3. Capacitance (1)
(T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: 1. Sampled only, not 100% tested.

Table 4. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V or 3V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±2.5	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current (TTL Inputs)	S = V_{IH}, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	S = V_{IH}, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}		50	µA
V_{IL}	Input Low Voltage (D, C, S)	V_{CC} = 5V ± 10%	–0.3	0.8	V
		3V ≤ V_{CC} ≤ 4.5V	–0.3	0.2 V_{CC}	V
V_{IH}	Input High Voltage (D, C, S)	V_{CC} = 5V ± 10%	2	V_{CC} + 1	V
		3V ≤ V_{CC} ≤ 4.5V	0.8 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
		I_{OL} = 10 µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
		I_{OH} = –10µA	V_{CC} – 0.2		V

Table 5. AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V or 3V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{CLSH}	t_{SKS}	Clock Low to Chip Select High		100		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition	Temp. Range: grade 1	100		ns
			Temp. Range: grades 3, 6	200		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low			500	ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid			500	ns
t_{CLSL}	t_{CSH}	Clock Low to Chip Select Low		0		ns
t_{SLCH}		Chip Select Low to Clock High		250		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid			500	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z	ST93C46A		300	ns
			ST93C46C, 47C		200	ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_W	t_{WP}	Erase/Write Cycle time			10	ms
f_C	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1. Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles.
2. The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs. For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns.

Figure 4. Synchronous Timing, Start and Op-Code Input

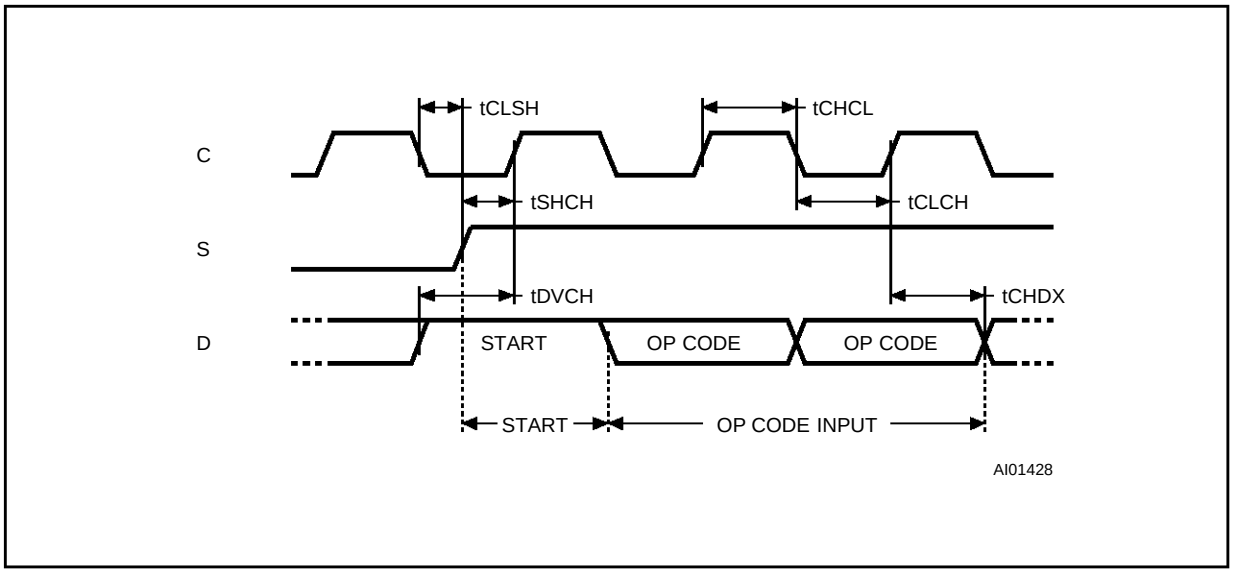
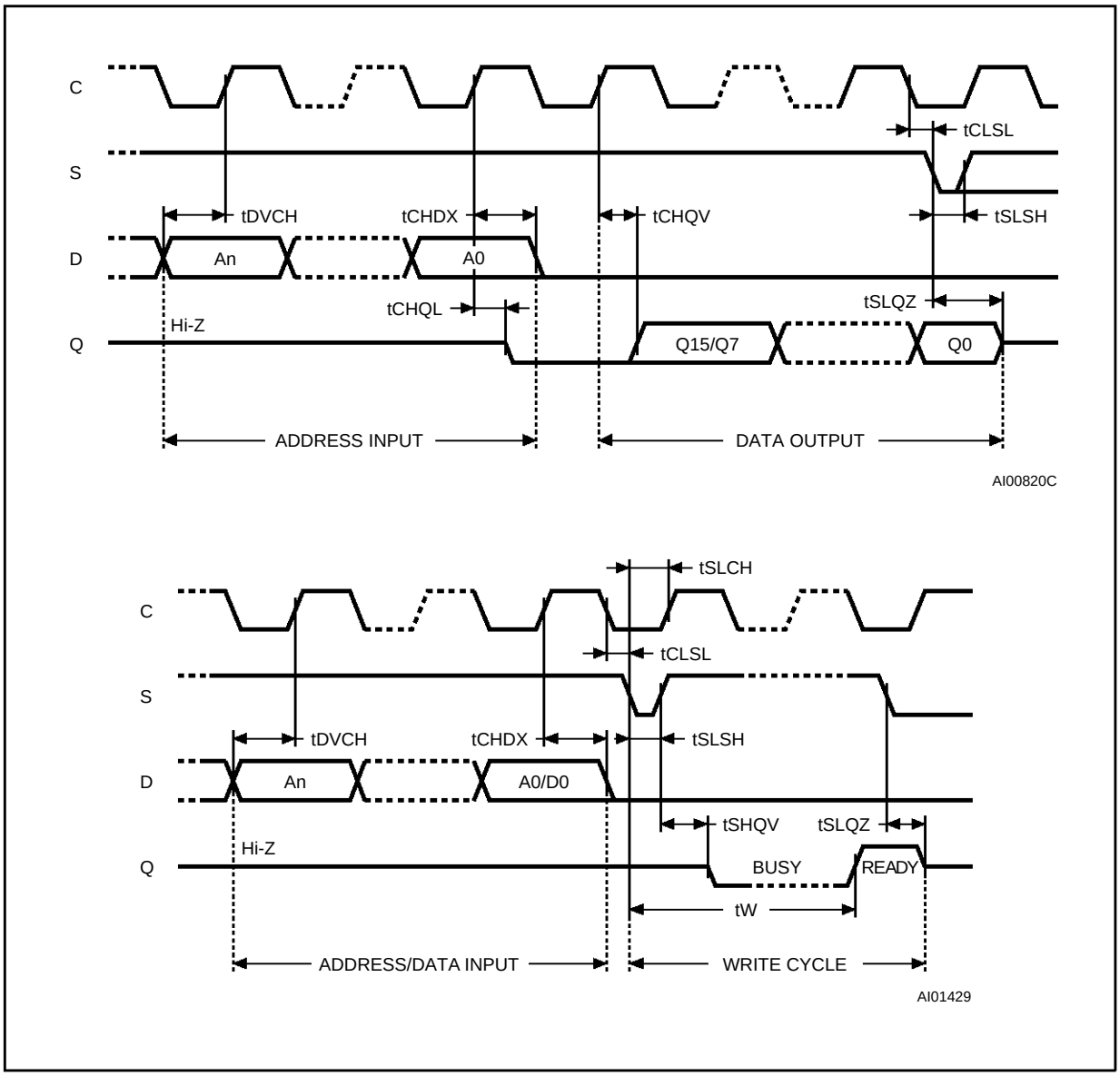


Figure 5. Synchronous Timing, Read or Write



DESCRIPTION (cont'd)

counter automatically rolls over to '00' when the highest address is reached.

Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a Write cycle) and does not require an erase cycle prior to the Write instruction. The Write instruction writes 8 or 16 bits at one time into one of the 128 bytes or 64 words. After the start of the programming cycle a Busy/Ready signal is available on the Data output (Q) when Chip Select (S) is High.

An internal feature of the ST93C46 provides Power-on Data Protection by inhibiting any operation when the Supply is too low. The design of the ST93C46 and the High Endurance CMOS technology used for its fabrication give an Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of 40 years.

The DU (Don't Use) pin does not affect the function of the memory and it is reserved for use by SGS-THOMSON during test sequences. The pin may be left unconnected or may be connected to V_{CC} or V_{SS}. Direct connection of DU to V_{SS} is recommended for the lowest standby power consumption.

MEMORY ORGANIZATION

The ST93C46 is organised as 128 bytes x 8 bits or 64 words x 16 bits. If the ORG input is left unconnected (or connected to V_{CC}) the x16 organization is selected, when ORG is connected to Ground (V_{SS}) the x8 organization is selected. When the ST93C46 is in standby mode, the ORG input should be unconnected or set to either V_{SS} or V_{CC} in order to get minimum power consumption. Any voltage between V_{SS} and V_{CC} applied to ORG may increase the standby current value.

POWER-ON DATA PROTECTION

During power-up, A Power On Reset sequence is run in order to reset all internal programming circuitry and the device is set in the Write Disable mode. When V_{CC} reaches its functional value, the device is properly reset (in the Write Disable mode) and is ready to decode and execute an incoming instruction.

INSTRUCTIONS

The ST93C46 has seven instructions, as shown in Table 6. Each instruction is preceded by the rising edge of the signal applied on the S input (assuming that the clock C is low), followed by a '1' read on D input during the rising edge of the clock C. The op-codes of the instructions are made up of the 2 following bits. Some instructions use only these first two bits, others use also the first two bits of the address to define the op-code. The op-code is followed by an address for the byte/word which is made up of six bits for the x16 organization or seven bits for the x8 organization.

The ST93C46 is fabricated in CMOS technology and is therefore able to run from zero Hz (static input signals) up to the maximum ratings (specified in Table 5).

Read

The Read instruction (READ) outputs serial data on the Data Output (Q). When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 8 bit byte or the 16 bit word with the MSB first. Output data changes are triggered by the Low to High transition of the Clock (C). The ST93C46 will automatically increment the address and will clock out the next byte/word as long as the Chip Select input (S) is held High. In this case the dummy '0' bit is NOT output between bytes/words and a continuous stream of data can be read.

Erase/Write Enable and Disable

The Erase/Write Enable instruction (EWEN) authorizes the following Erase/Write instructions to be executed, the Erase/Write Disable instruction (EWDS) freezes the execution of the following Erase/Write instructions. When power is first applied to the ST93C46, Erase/Write is inhibited. When the EWEN instruction is executed, Write instructions remain enabled until an Erase/Write Disable instruction (EWDS) is executed or V_{CC} falls below the power-on reset threshold. To protect the memory contents from accidental corruption, it is advisable to issue the EWDS instruction after every write cycle.

The READ instruction is not affected by the EWEN or EWDS instructions.

Table 6. Instruction Set

Instruction	Description	Op-Code	x8 Org Address (ORG = 0)	Data	x16 Org Address (ORG = 1)	Data
READ	Read Data from Memory	10	A6-A0	Q7-Q0	A5-A0	Q15-Q0
WRITE	Write Data to Memory	01	A6-A0	D7-D0	A5-A0	D15-D0
EWEN	Erase/Write Enable	00	11XXXXX		11XXXX	
EWDS	Erase/Write Disable	00	00XXXXX		00XXXX	
ERASE	Erase Byte or Word	11	A6-A0		A5-A0	
ERAL	Erase All Memory	00	10XXXXX		10XXXX	
WRAL	Write All Memory with same Data	00	01XXXXX	D7-D0	01XXXX	D15-D0

Note: X = don't care bit.

Erase

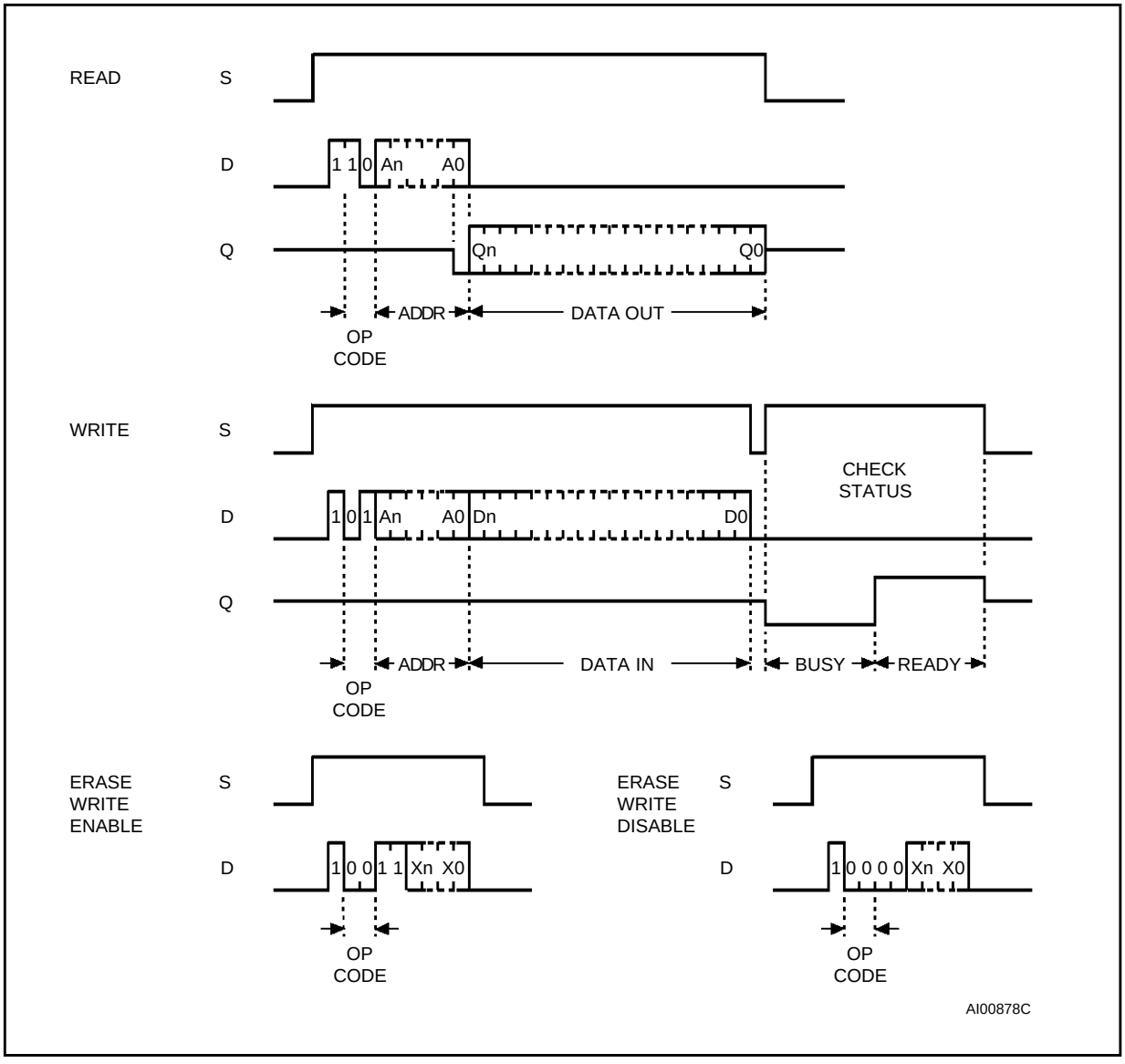
The Erase instruction (ERASE) programs the addressed memory byte or word bits to '1'. Once the address is correctly decoded, the falling edge of the Chip Select input (S) starts a self-timed programming cycle.

If the ST93C46 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C46 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C46 is ready to receive a new instruction.

Write

The Write instruction (WRITE) is followed by the address and the 8 or 16 data bits to be written. Data input is sampled on the Low to High transition of the clock. After the last data bit has been sampled, Chip Select (S) must be brought Low before the next rising edge of the clock (C), in order to start the self-timed programming cycle. If the ST93C46 is still performing the write cycle, the Busy signal

Figure 6. READ, WRITE, EWEN, EWDS Sequences



Notes: 1. An: n = 5 for x16 org. and 6 for x8 org.
2. Xn: n = 3 for x16 org. and 4 for x8 org.

INSTRUCTIONS (cont'd)

(Q = 0) will be returned if S is driven high, and the ST93C46 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C46 is ready to receive a new instruction.

The Write instruction includes an automatic Erase cycle before writing the data, it is therefore unnecessary to execute an Erase instruction before a Write instruction execution.

Erase All

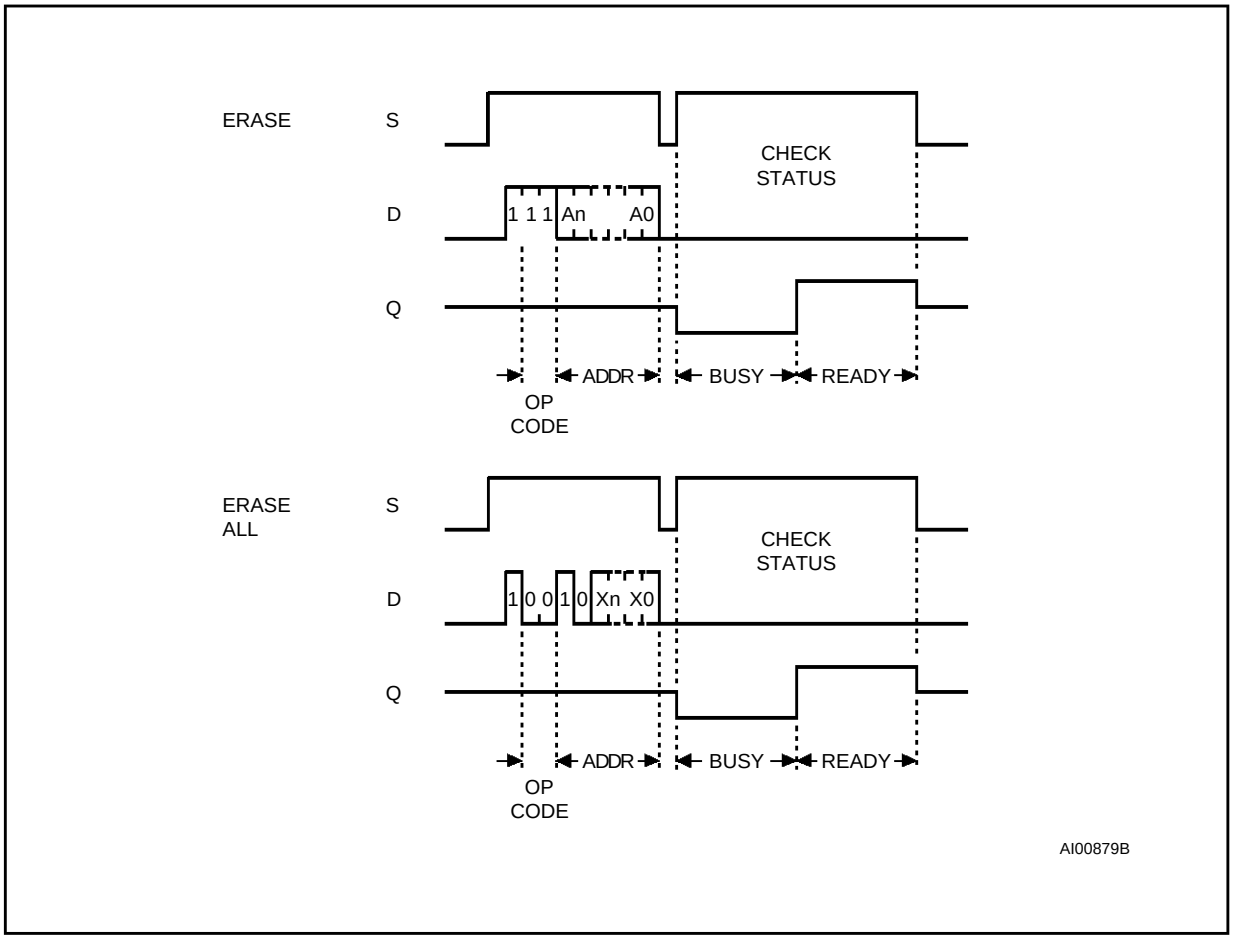
The Erase All instruction (ERAL) erases the whole memory (all memory bits are set to "1"). A dummy address is input during the instruction transfer and the erase is made in the same way as the ERASE instruction above. If the ST93C46 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C46 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C46 is ready to receive a new instruction.

Write All

For correct operation, an ERAL instruction should be executed before the WRAL instruction.

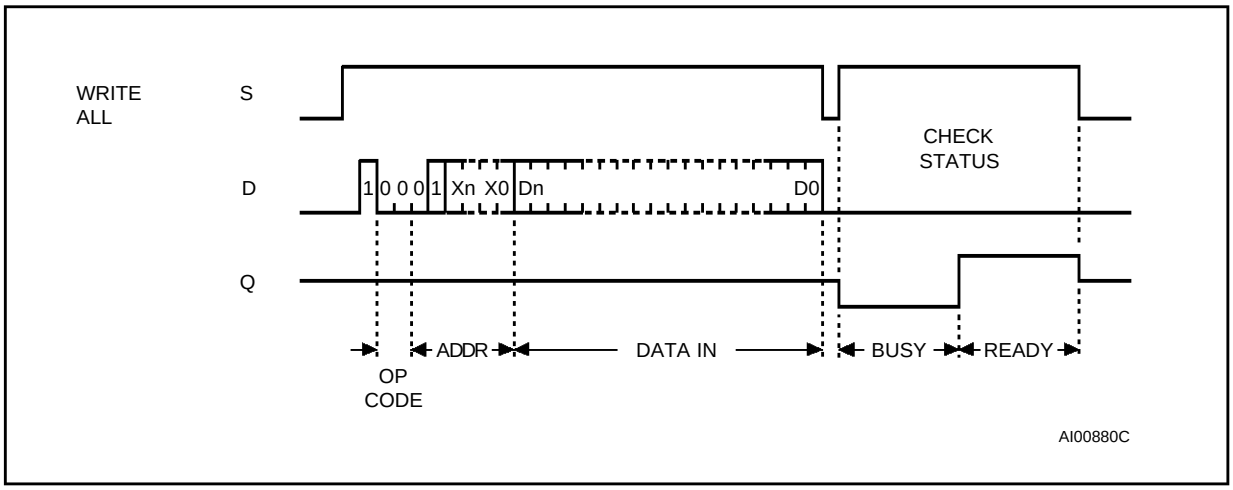
The Write All instruction (WRAL) writes the Data Input byte or word to all the addresses of the memory. In the WRAL instruction, NO automatic erase is made so all bytes/words must be erased before the WRAL instruction. If the ST93C46 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C46 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C46 is ready to receive a new instruction.

Figure 7. ERASE, ERAL Sequences



Notes: 1. An: n = 5 for x16 org. and 6 for x8 org.
2. Xn: n = 3 for x16 org. and 4 for x8 org.

Figure 8. WRAL Sequence



Note: 1. Xn: n = 3 for x16 org. and 4 for x8 org.

READY/BUSY Status

During every programming cycle (after a WRITE, ERASE, WRAL or ERAL instruction) the Data Output (Q) indicates the Ready/Busy status of the memory when the Chip Select is driven High. Once the ST93C46 is Ready, the Data Output is set to '1' until a new start bit is decoded or the Chip Select is brought Low.

COMMON I/O OPERATION

The Data Output (Q) and Data Input (D) signals can be connected together, through a current limiting resistor, to form a common, one wire data bus. Some precautions must be taken when operating the memory with this connection, mostly to prevent a short circuit between the last entered address bit (A0) and the first data bit output by Q. The reader should refer to the SGS-THOMSON application note "MICROWIRE EEPROM Common I/O Operation".

DIFFERENCES BETWEEN ST93C46A AND ST93C46C

The ST93C46C is an enhanced version of the ST93C46A and offers the following extra features:

– Enhanced ESD voltage

– Functional security filtering glitches on the clock input (C).

Refer to Table 2 (Absolute Maximum Ratings) for more about ESD limits. The following description will detail the Clock pulses counter (available only on the ST93C46C).

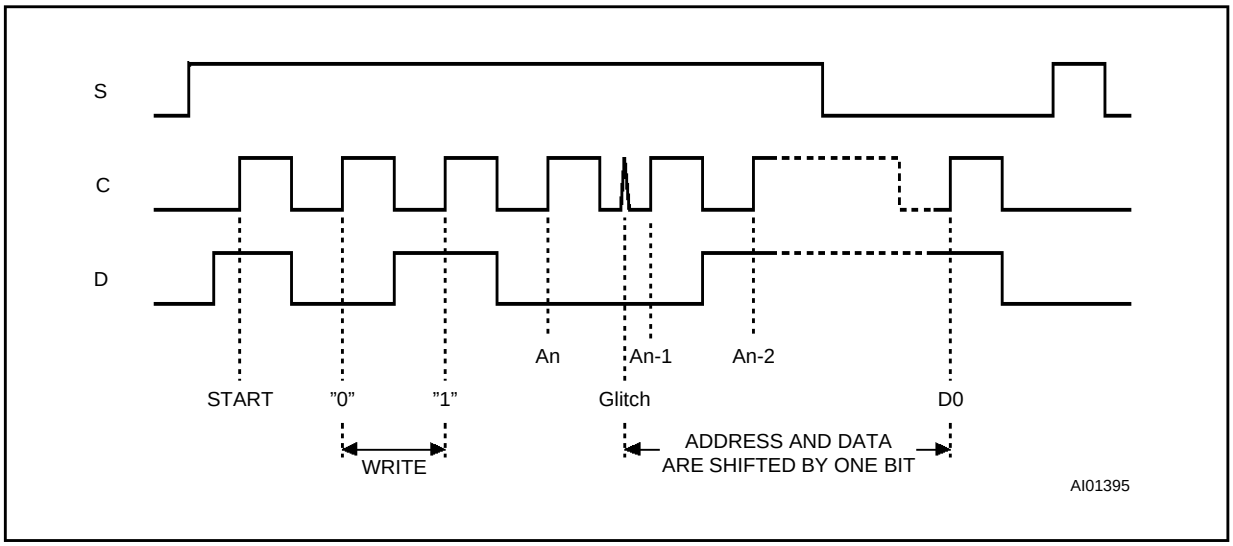
In a normal environment, the ST93C46 is expected to receive the exact amount of data on the D input, that is the exact amount of clock pulses on the C input.

In a noisy environment, the amount of pulses received (on the clock input C) may be greater than the clock pulses delivered by the Master (Microcontroller) driving the ST93C46C. In such a case, a part of the instruction is delayed by one bit (see Figure 9), and it may induce an erroneous write of data at a wrong address.

The ST93C46C has an on-board counter which counts the clock pulses from the Start bit until the falling edge of the Chip Select signal. For the WRITE instructions, the number of clock pulses incoming to the counter must be exactly 18 (with the Organisation by 8) from the Start bit to the falling edge of Chip Select signal (1 Start bit + 2 bits of Op-code + 7 bits of Address + 8 bits of Data = 18): if so, the ST93C46C executes the WRITE instruction; if the number of clock pulses is not equal to 18, the instruction will not be executed (and data will not be corrupted).

In the same way, when the Organisation by 16 is selected, the number of clock pulses incoming to the counter must be exactly 25 (1 Start bit + 2 bits of Op-code + 6 bits of Address + 16 bits of Data = 25) from the Start bit to the falling edge of Chip Select signal: if so, the ST93C46C executes the WRITE instruction; if the number of clock pulses is not equal to 25, the instruction will not be executed (and data will not be corrupted). The clock pulse counter is active only on ERASE and WRITE instructions (WRITE, ERASE, ERAL, WRALL).

Figure 9. WRITE Sequence with One Clock Glitch



ORDERING INFORMATION SCHEME

Example: ST93C46A M 1 013TR

Operating Voltage	Revision	Package	Temperature Range	Option
46 4.5V to 5.5V	A (1) CMOS F3	B PSDIP8 0.4 mm Frame(2)	1 0 to 70 °C	013TR Tape & Reel Packing (A, T ver.)
47 3V to 5.5V	C CMOS F4	M SO8 150mil Width	6 –40 to 85 °C	TR Tape & Reel Packing (C version)
	T CMOS F3 90° Turn pin out		3 * –40 to 125 °C	

Notes: 1. Revision "A" is not available for the ST93C47 product.
2. ST93C46CB1 is available in 0.25mm lead Frame only.
3 * Temperature range on special request only.

Parts are shipped with the memory content set at all "1's" (FFFFh for x16, FFh for x8).

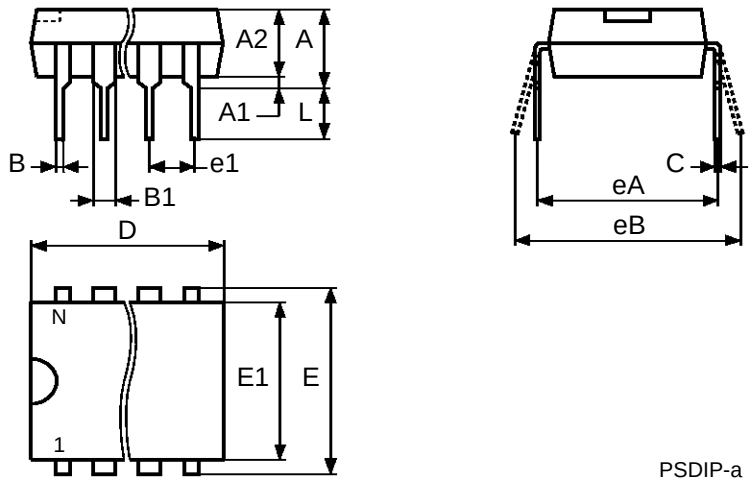
For a list of available options (Revision, Package etc...) refer to the the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.4mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			4.80			0.189
A1		0.70	–		0.028	–
A2		3.10	3.60		0.122	0.142
B		0.38	0.58		0.015	0.023
B1		1.15	1.65		0.045	0.065
C		0.38	0.52		0.015	0.020
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.30	7.10		0.248	0.280
e1	2.54	–	–	0.100	–	–
eA		8.40	–		0.331	–
eB			9.20			0.362
L		3.00	3.80		0.118	0.150
N	8			8		
CP			0.10			0.004

PSDIP8



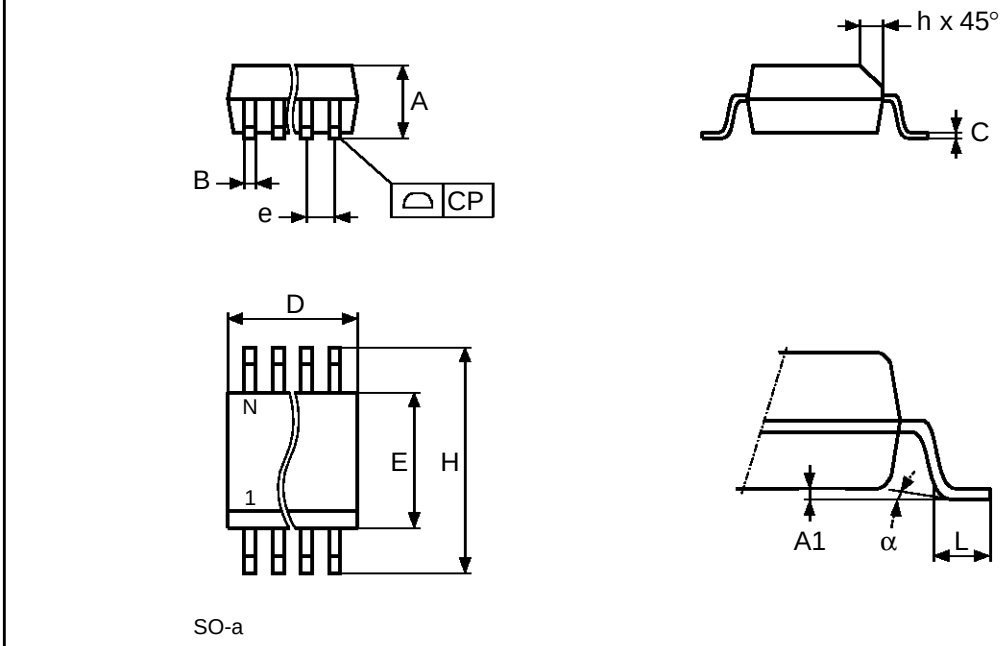
PSDIP-a

Drawing is not to scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8



SO-a

Drawing is not to scale