

**SP 8750 B,M**  
**1.0 GHz**
**SP 8751 B,M**  
**1.1 GHz**
**SP 8752 B**  
**1.2 GHz**
**UHF ÷ 64 PRESCALERS**

The SP8750 range of devices are ECL divide-by-sixtyfours which will operate at frequencies up to 1.2GHz.

The device has a typical power dissipation of 470mW at the nominal supply voltage of +6.8V.

### FEATURES

- Input Ports for VHF and UHF
- Self-Biasing Clock Inputs
- Variable Input Hysteresis Capability for Wide Band Operation
- TTL/MOS Compatible Band Change Input
- Push Pull TTL. O/P

### ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	0V to +10V
Input voltage, clock inputs	2.5V p-p
Band change input	+7.2 V to -0.5V or -10mA
Output current	+30 mA to -30 mA
Operating junction temperature	+150°C
Storage Temperature	-55°C to +150°C

### OPERATING NOTES

Two input ports are available on this device. Switching between these inputs is accomplished by operation of the band change input. A logic '1' activates the UHF input, logic '0' the VHF input. When an input is not in use the input signal must be removed to prevent cross-modulation occurring on the other input at high frequencies. Both inputs are terminated by a nominal 400  $\Omega$  and should be AC coupled to their respective signal sources. Input power to the device is terminated to ground by the two decoupling capacitors on the reference pins. Input coupling and reference decoupling capacitors should be of a type suitable for use at a frequency of 1.2Hz.

When the device is switched to the VHF input, an input hysteresis of 50mV is set by the internal band change circuit. This improves the low frequency sinewave operation of the device. The hysteresis level may be measured as  $V_{REF1} - V_{REF2}$ .

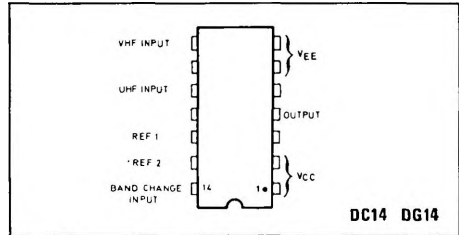


Fig. 1 Pin connections

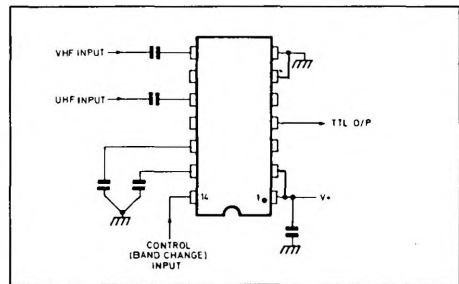


Fig. 2 Typical application

If the UHF input only is used and the device is required to operate with a sinewave input below 100 MHz, then the required hysteresis may be applied externally as shown in Fig. 5. Large values of hysteresis should be avoided as this will degrade the input sensitivity of the device at the maximum frequency. The divide by 64 output is designed to interface with TTL which has a common  $V_{EE}$  (ground). The specified fan-out of 3 standard TTL inputs may be increased to 6 standard or 5 high power/Schottky inputs at a logic zero level of 0.5V. At low frequency the output will change when one of the clock inputs changes from a low to a high level.

The devices may be operated down to very low frequencies if a square wave input is applied with an edge speed of greater than 200V/ $\mu$ s.

The divider is clocked on low to high transitions of either clock input.

**ELECTRICAL CHARACTERISTICS**

Supply voltage:  $6.8V \pm 0.35V$

Supply current: 68 mA typ., 90 mA max.

Temperature range: 'B' grade  $0^{\circ}C$  to  $+70^{\circ}C$ , 'M' grade  $-40^{\circ}C$  to  $+85^{\circ}C$

Clock inputs: AC coupled, self-biasing via  $400\Omega$

Band change input: TTL type including negative input voltage clamp, 0.8 mA max. sink current

**Test conditions (unless otherwise stated):**

Supply voltage:  $V_{EE} = 0V$ ,  $V_{CC} = +6.45V$  to  $+7.15V$

Clock input voltage: 400mV to 1.0Vp-p

$T_{amb} = 0^{\circ}C$  to  $+70^{\circ}C$  ('B' grade),  $-40^{\circ}C$  to  $+85^{\circ}C$  ('M' grade)

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
<b>UHF clock input</b>						
Max. input frequency	SP8752	1.2			GHz	600mV p-p input
	SP8751	1.1			GHz	600mV p-p input
	SP8750	1.0			GHz	400mV p-p input
Min. input frequency	All			100	MHz	600mV p-p sinewave input
Min. slew rate for square wave input	All			200	v/ $\mu$ s	
<b>VHF clock input</b>						
Max. input frequency	All		1.0		GHz	
Min. input frequency	All		30	50	MHz	600mV p-p sinewave input
<b>Band change input</b>						
High level	All	2.5			V	
Low level	All			0.4	V	
Low level input current	All			0.8	mA	at 0.4V
Max. clamp current	All	-3			mA	at approx. -0.7V
<b>Output</b>						
High level	All	2.5	3.5	4.5	V	
Low level	All			0.4	V	5mA current sink
Supply current	All		68	90	mA	$V_{CC} = 6.8V$

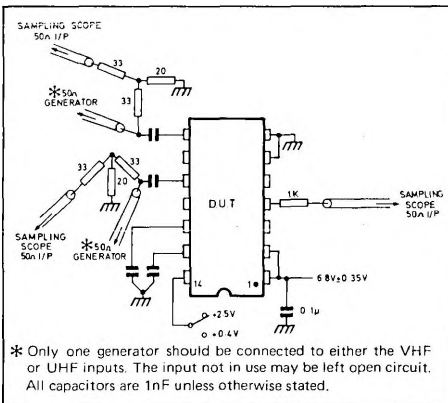


Fig. 3 AC test circuit

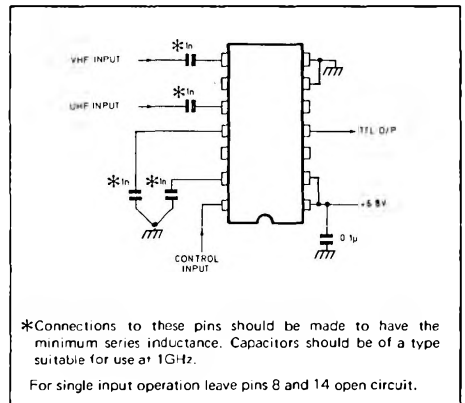
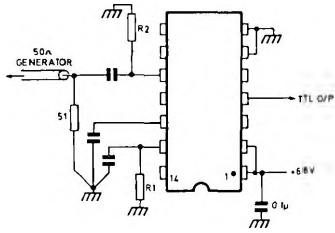


Fig. 4 Application circuit



Capacitors are 1 nF unless otherwise stated. Values should be increased if operation below 10 MHz is desired.  
 For 50 mV hysteresis  $R1 = 36k\Omega$   $R2 = \infty$   
 For 100 mV hysteresis  $R1 = 18k\Omega$   $R2 = 18k\Omega$

*Fig. 5 Wideband operation*