PLESSEY
SEMICONDUCTORS

SP 8000 SERIES
HIGH SPEED DIVIDERS

SP8735B ÷8 AT 600MHz WITH BINARY OUTPUTS
SP8736B ÷8 AT 500MHz WITH BINARY OUTPUTS

The SP8735B and SP8736B are divide-by-eight circuits with binary outputs for operation from DC up to specified input frequencies of 600 MHz and 500 MHz respectively over a guaranteed temperature range of 0°C to +70°C.

These devices, optimised for counter applications in systems using both ECL and TTL, are intended to be operated between 0V and −5.2V power rails and to interface with TTL operating between 0V and +5V. The binary outputs and one of two carry outputs are TTL-compatible, while the second carry output is ECL-compatible. The clock input, which is normally capacitively coupled to the signal source, is gated by an ECL III/ECL 10K compatible input. The TTL-compatible reset forces the 0000 state regardless of the state of the other inputs.

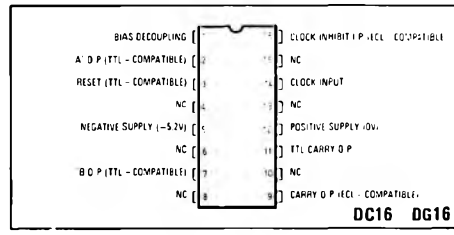

Fig. 1 Pin connections (viewed from top)

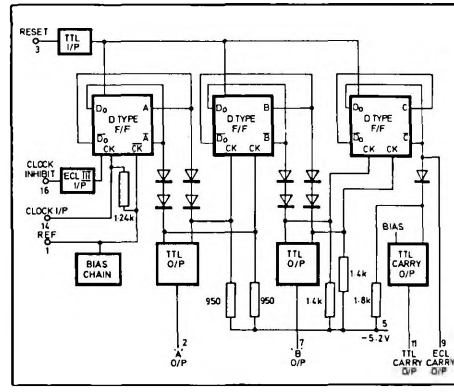

Fig.2 SP8735/6 logic diagram

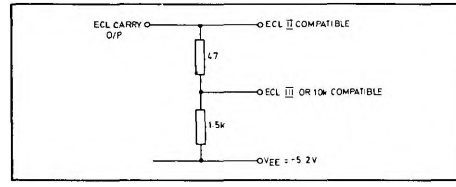

Fig.3 ECL II to ECL 10K interface

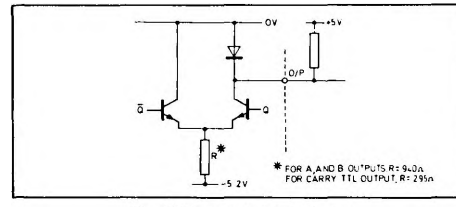

Fig. 4 TTL output circuit diagram

FEATURES

- Direct Gating Capability at up to 600 MHz
- TTL Compatible Binary Outputs
- TTL and ECL Compatible Carry Outputs
- Power Consumption Less Than 450mW
- Wide Dynamic Input Range

APPLICATIONS

- Counters
- Timers
- Synthesisers

QUICK REFERENCE DATA

- Power Supplies : V_{cc} 0V
  V_{ee} −5.2V ± 0.25V
- Range of Clock Input Amplitude : 400 – 800 mV p-p
- Operating Temperature Range :
  0°C to 70°C
- Frequency Range with Sinusoidal I/P : 40 – 600MHz (SP8735)
- Frequency Range with Square Wave I/P : DC to 600MHz (SP8735)

ELECTRICAL CHARACTERISTICS (All types except where otherwise stated)

Test Conditions (unless otherwise stated):
T_{amb} 0°C to +70°C
Power Supplies V_{CC} OV
V_{EE} −5.2V ±0.25V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Clock input (pin 14)					
Max. input frequency					
SP8735B	600			MHz	Input voltage 400–800mV p-p
SP8736B	500			MHz	
Min. input frequency with sinusoidal I/P			40	MHz	
Min. slew rate of square wave for correct operation down to DC			100	V/μs	
Clock inhibit input (pin 16)					
High level (inhibit)	−0.960			V	T_{amb} = +25°C (see note 1)
Low level			−1.650	V	
Edge speed for correct operation at max. clock I/P frequency			2.5	ns	10% to 90%
Reset input (pin 3)					
High level (reset)	See note 2				See note 2
Low level			+0.4	V	
Reset ON time	100			ns	
TTL outputs A & B (pins 2 & 7)					
Output high level	+2.4			V	10k Ω resistor and 3 TTL gate
Output low level			+0.4	V	from O/P to 5V rail (see note 3)
TTL carry output (pin 11)					
Output high level	+2.4			V	5k Ω resistor and 3 TTL gates from O/P to +5V rail
Output low level			+0.4	V	
ECL carry output (pin 9)					
Output high level	−0.975			V	T_{amb} = +25°C
Output low level			−1.375	V	External current = 0mA (See note 4)
Power supply drain current		70	90	mA	V_{EE} − 5.2V

NOTES

1. The clock inhibit input levels are compatible with the ECL III and ECL 10K levels throughout the temperature ranges specified.
2. For a high state, the reset input requires a more positive input level than the specified worst case TTL V_{OH} of +2.4V. Resetting should be done by connecting a 1.8k Ω resistor from the output of the driving TTL gate and only fanning out to the reset input of the SP8000 series devices.
3. These outputs are current sources which can be readily made TTL compatible voltages by connecting them to +5V via 10k Ω resistors (see Fig. 4).
4. The ECL carry output is compatible with ECL II throughout the temperature range but can be made compatible with ECL III using the simple interface shown in Fig. 3.

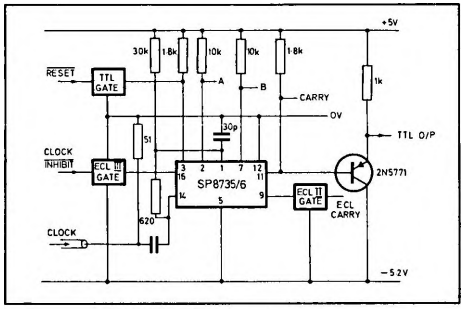

Fig.5 Typical operating diagram

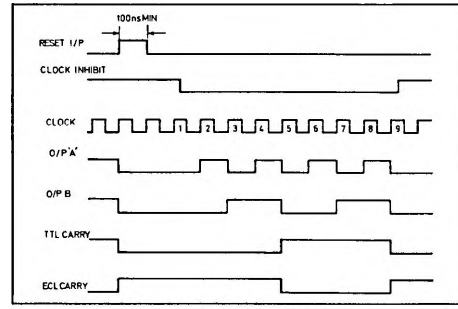

Fig.6 Output waveforms

OPERATING NOTES

The devices are intended to be used with TTL and ECL in a counting system — the ECL and the decade counter being connected between voltage rails of 0V and −5.2V and the TTL between voltage rails of 0V and +5V. Provided that this is done ECL and TTL compatibility is achieved. (See Figs. 4 and 5)

The clock is normally capacitively coupled to the signal source: a 1000 pF UHF capacitor should be adequate. For low frequency operation, the 1000 pF capacitor should be connected in parallel with a higher value capacitor. The bias decoupling (pin 1) should be connected to earth via a capacitor — preferably a chip type, but in any case a low inductance type suitable for UHF applications. The devices normally have an input amplitude operating range far greater than the specified 400 to 800 mV p – p. However, if the decoupling capacitor is not of a UHF type, or it is connected to an earth point that has a significant impedance between the capacitor and the V_{cc} connection, then the input dynamic range will suffer and the maximum signal for correct operation will be reduced.

Under certain conditions, the absence of an input signal may cause the device to self-oscillate. This can be prevented (while still maintaining the specified input sensitivity) by connecting a 30Ω resistor between the clock input and the positive supply and a 620Ω resistor between clock and pin 1. If the transition of either the clock input or the clock inhibit input is slow the device may start to self-oscillate during the transition. For this reason the input slew rates should be greater than 100V/μs. It should also be noted that a positive-going transition on either the clock input or the clock inhibit will clock the device, provided that the other input is in the low state.

The binary outputs give TTL-compatible outputs (fan out = 1) when a 10kΩ resistor is connected from the output to the −5V rail. In this configuration the outputs will be very slow compared with the clocking rate of the counter and so the state on the TTL outputs can only be determined when the clock has stopped or is inhibited.

The fan out capability of the TTL carry output can be increased by buffering it with a PNP emitter follower. The interface is shown in Fig. 5.

A typical application is shown in Fig. 7.

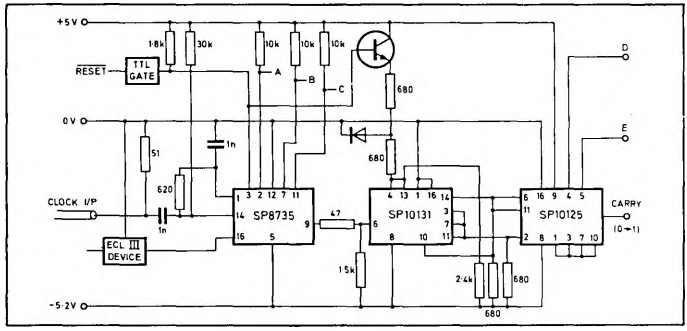

Fig.7 600MHz ÷ 32 with reset and inhibit