PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP 8720 A, B & M
UHF PROGRAMMABLE DIVIDER 300 MHz÷3/4

The SP8720 A, B & M are high speed programmable ÷3/4 counters operating at an input frequency of up to 300MHz over the temperature ranges —55°C to +125°C, 0°C to +70°C and —40°C to +85°C respectively.

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.

The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 3 when either input is in the high state, and by 4 when both inputs are in the low state. These inputs are compatible with standard ECL 10K inputs and have the same temperature characteristics. Both inputs have nominal 4.3kΩ internal pulldown resistors.

The true and inverse outputs are compatible with standard ECL II outputs. They may be used to drive ECL 10K circuits by the inclusion of two resistors as shown in Fig. 4.

When using the device as a divide-by-three prescaler the inverse output ($\overline{Q2}$) should be connected to a $\overline{PE}$ input.

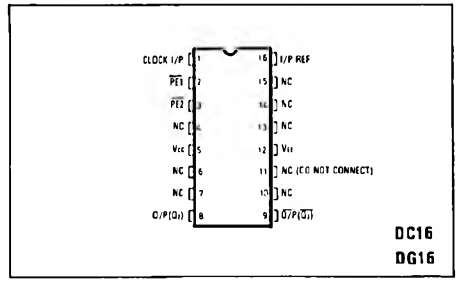


Fig. 1 Pin connections (top view)

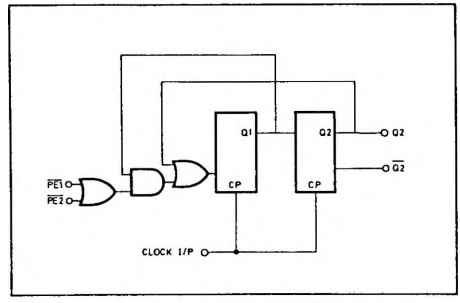


Fig. 2 Logic diagram SP8720

FEATURES

- Full temperature range operation:
  - 'A' Grade —55°C to +125°C
  - 'B' Grade 0°C to + 70°C
  - 'M' Grade — 40°C to + 85°C
- Self Biasing CP Input
- Wide Input Dynamic Range
- Control Inputs ECL 10K - Compatible
- Low Propagation Delay
- True and Inverse Outputs Available

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $\lvert V_{CC} - V_{EE} \rvert$	0V to +8V
Input voltage, $\overline{PE}$ inputs	0V to V_{CC}
Input voltage, CP input	2V peak-to-peak
Output current	20mA
Operating junction temperature	+150°C
Storage temperature	—55°C to + 150°C

Clock Pulse	Q_1	Q_2	
1	L	H	
2	L	L	
3	H	L	
4	H	H	← Extra State

Table 1 Count sequence

$\overline{PE_1}$	$\overline{PE_2}$	Div Ratio.
L	L	4
H	L	3
L	H	3
H	H	3

Table 2 Truth table for control inputs

ELECTRICAL CHARACTERISTICS

$\overline{PE}$ inputs - ECL 10K compatible
Outputs - ECL II compatible

Test conditions (unless otherwise stated)
Tamb 'A' Grade: −55°C to +125°C
'B' Grade: 0°C to + 70°C
'M' Grade: −40°C to + 85°C
Supply voltages: V_{CC} = + 5.2V ±0.25V
V_{EE}=0V
Clock input voltage: 400mV to 800mV (p-p)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Max. i/p frequency	300			MHz	V_{CC}= + 5.2V
Min.i/p frequency			40		Sinewave Input
Min. slew rate for square wave input			100	V/μs	
Propagation delay (clock i/p to device o/p)		4		ns	
PE input reference level		+ 3.9		V	V_{CC} = + 5.2V, 25°C
Power supply drain current		40	55	mA	V_{CC} = + 5.2V, 25°C
PE input pull down resistors		4.3		kΩ	
Clock i/p impedance (i/p to i/p ref. low frequency)		400		Ω	

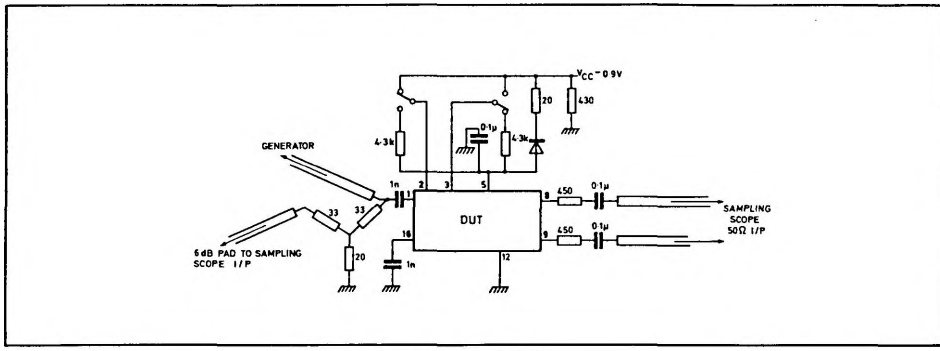


Fig. 3 Test circuit

APPLICATION NOTES

When operating the SP8720 in a synthesiser loop at 300MHz, the delay time through the programmable divider controlling the SP8720 is approximately 5.5ns, and will require ECL.

The simple passive interface from the output of the SP8720 into ECL 10K logic is defined in Fig. 4.

If TTL is required, the input interface to the $\overline{PE}$ pins, and the output of the SP8720 into TTL, is shown in Fig.5.

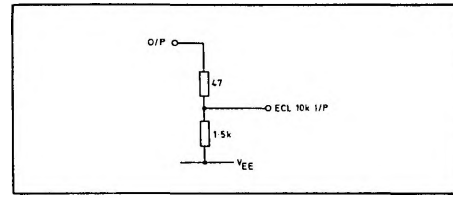


Fig. 4

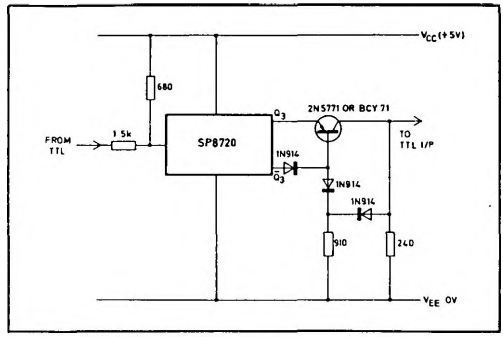


Fig. 5

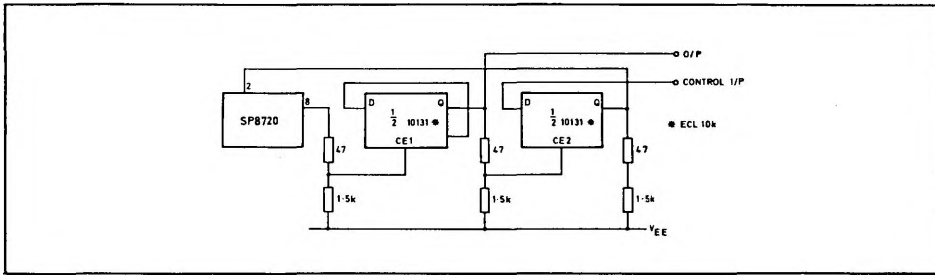
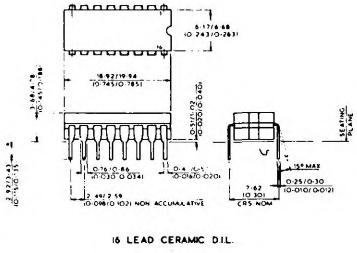


Fig. 6 Divide by 6/8 Control loop delay time approximately 20ns at 300MHz I/P frequency

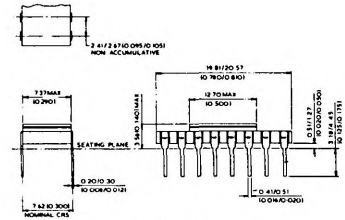
PACKAGE DETAILS

Dimensions are shown thus: mm(in)



16 LEAD CERAMIC D.I.L.

DG18



16 LEAD DILMON

DC16