PLESSEY
SEMICONDUCTORS

SP8000 SERIES

HIGH SPEED DIVIDERS

SP8690 A, B & M 200 MHz ÷ 10/11

AC COUPLED VHF, LOW POWER, PROGRAMMABLE DIVIDERS

The SP8690 A, B & M are divider circuits that can be logically programmed to divide by either 10 or 11.

The device is available over three temperature ranges: 'A' grade is —55 C to +125 C and the 'B' grade is 0 C to +70 C and the 'M' grade is —40 C to +85 C.

The clock inputs can be either single or differentially driven and must be AC-coupled to the signal source. If single driven then the unused input must be decoupled to the earth plane. The device will self-oscillate if no input is present; to prevent this, a 68kΩ resistor should be connected from pin 1 or 16 to 0V. This will reduce the sensitivity of the device by approximately 100mV p-p.

The division ratio is controlled by two $\overline{PE}$ inputs which are ECL III and ECL 10K compatible throughout the temperature range. The device will divide by ten when either input is high and by eleven when both inputs are low. These inputs may be interfaced to TTL and CMOS by the inclusion of 2 resistors, as shown in Fig. 3. There is a free collector, saturating output stage for interfacing with either TTL or CMOS, together with true and inverse outputs with ECL II compatible levels. These may be interfaced to ECL 10K as shown in Fig. 4.

The device may be used as a fixed ÷10 by connecting $\overline{Q4}$ to one $\overline{PE}$ input.

If the 0 → 1 transition of Q4 (or the 1 → 0 transition of $\overline{Q4}$) is used to clock the next stage then this will give the maximum loop delay for control, i.e. 10 clock periods minus the internal delays.

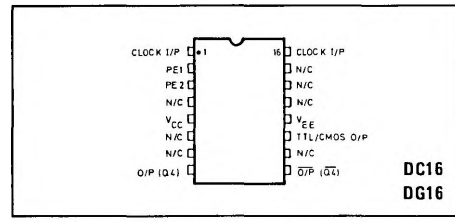
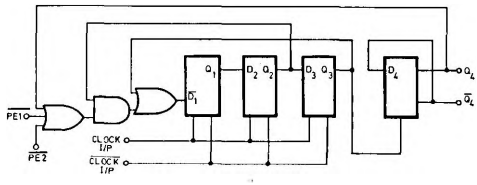


Fig.1 Pin connections

FEATURES

- Full Temperature Range Operation
  - 'A' Grade —55°C to —125°C
  - 'B' Grade 0°C to +70°C
  - 'M' Grade —40°C to +85°C
- Toggle Frequency in Excess of 200MHz
- Power Dissipation 70mW Typical
- ECL Compatibility on All Inputs
- Capacitively Coupled Clock Input for Synthesiser and Counter Applications
- True and Inverse Outputs Available with ECL Compatibility
- Output Available for Driving TTL or CMOS



Division ratio				
I/P	11	10	10	10
$\overline{PE1}$	L	H	L	H
$\overline{PE2}$	L	L	H	H

Count sequence				
Q_1	Q_2	Q_3	Q_4	
L	H	H	H	
L	L	H	H	
L	L	L	H	
H	L	L	H	
H	H	L	H	
L	H	H	L	
L	L	H	L	
L	L	L	L	
H	L	L	L	
H	H	L	L	
H	H	H	H	Extra state

Fig.2 Logic diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

T_{amb} 'A' grade −55°C to +125°C
'B' grade 0°C to +70°C
'M' grade −40°C to +85°C
Supply voltage V_{CC} = ÷5V ±0.25V
V_{EE} = 0V
Clock I/P voltage 400mV to 800mV peak to peak
Pin 16 (decoupled to 0V)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Max. toggle frequency	200			MHz	
Min. freq. with sine wave clock input		15		MHz	
Min. slew rate of square wave I/P for correct operation		40		V/µs	
$\overline{PE}$ input levels					
V_{INH}	+4.1		+4.5	V	Vcc=+5V
V_{INL}	0.0		+3.5	V	T_{amb}=+25°C (note 1)
Q4 & $\overline{Q4}$ output voltage levels					T_{amb}=+25°C (note 2)
V_{OH}	4.15			V	I_{out} (external) = 0mA
V_{OL}			+3.5	V	(There is internal circuitry equivalent to a 3.8kΩ pulldown resistor on each output)
TTL/CMOS output voltage levels					
V_{OL}			+0.4	V	Sink current 3.2mA on
V_{OH}	see note 3				TTL output
Input pulldown resistors between input pins 2 & 3 and −ve rail		10		kΩ	
Power supply drain current		14		mA	Vcc=+5V; T_{amb}=25°C
Impedance of clock I/P		1.6		kΩ	in=0Hz
Clock to TTL output delay (O/P −ve going)		22		ns	8mA sink current
Clock to TTL output delay (O/P −ve going)		8		ns	TTL output
Clock to ECL output delay		6		ns	
Set up time		2		ns	See note 4
Release time		4		ns	See note 5

NOTES
1. The $\overline{PE}$ reference voltage level is compatible with ECL II and ECL 10k over the specified temperature range.
2. The Q4 and $\overline{Q4}$ output levels are compatible with ECL II and ECL 10k over the specified temperature range.
3. The TTL/CMOS output has a free collector, and the high state output voltage will depend on the supply that the collector load is taken to. This should not exceed ÷12V.
4. Set up time is defined as the minimum time that can elapse between a L—H transition of a control input and the next L—H clock pulse transition to ensure that the ÷10 mode is forced by that clock pulse.
5. Release time is defined as the minimum time that can elapse between a L—H transition of a control input and the next L—H clock pulse transition to ensure that the ÷11 mode is forced by that clock pulse.

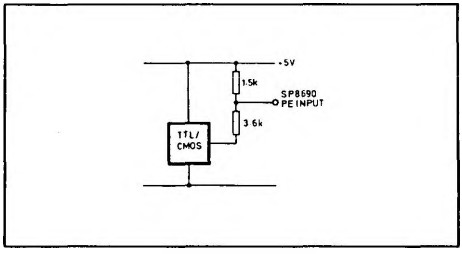


Fig.3 TTL/CMOS interface

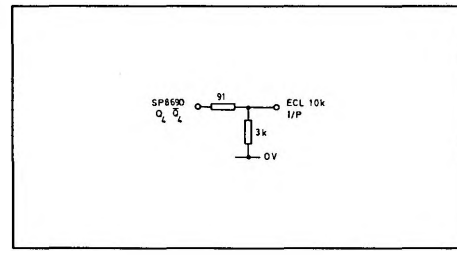


Fig.4 ECL 10K output interface

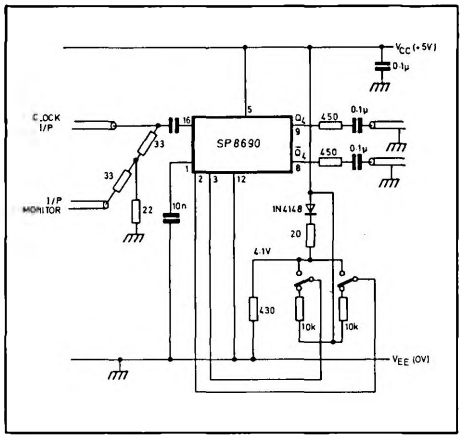


Fig.5 Test circuit for dynamic measurements

ABSOLUTE MAXIMUM RATINGS

Supply voltage $\lvert V_{CC} - V_{EE} \rvert$	V8
Input voltage V_{IN} d.c.	Not greater than the supply voltage in use
Output current I_{out} (Q_4 & $\overline{Q_4}$)	10mA
Maximum junction temperature	150°C
Storage temperature range	−55°C to +150°C