PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8685 A, B&M
UHF PROGRAMMABLE DIVIDER 500MHz ÷ 10/11

The SP8685 A, B & M are high speed programmable – 10/11 counters operating at an input frequency of up to 500 MHz over the temperature ranges -55°C to +125°C ('A' grade), 0°C to +70°C ('B' grade) and -40°C to +85°C respectively.

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.

The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 10 when either input is in the high state, and by 11 when both inputs are in the low state. These inputs are compatible with standard ECL 10K inputs and have the same temperature characteristics. Both inputs have nominal 4.3kΩ internal pulldown resistors.

The true and inverse outputs are compatible with standard ECL II outputs. They may be used to drive ECL 10K circuits by the inclusion of two resistors as shown in Fig. 4.

When using the device as a divide-by-ten prescaler the inverse output (o/p) should be connected to a PE input.

Clock Pulse	Q_1	Q_2	Q_3	Q_4
1	L	H	H	H
2	L	L	H	H
3	L	L	L	H
4	H	L	L	H
5	H	H	L	H
6	L	H	H	L
7	L	L	H	L
8	L	L	L	L
9	H	L	L	L
10	H	H	L	L
11	H	H	H	H

Table 1 Count sequence Extra state

$\overline{PE_1}$	PE_2	Div Ratio
L	L	11
H	L	10
L	H	10
H	H	10

Table 2 Truth table for control inputs

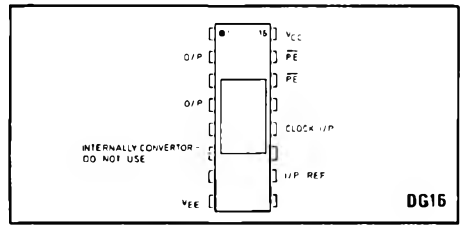

Fig. 1 Pin connections

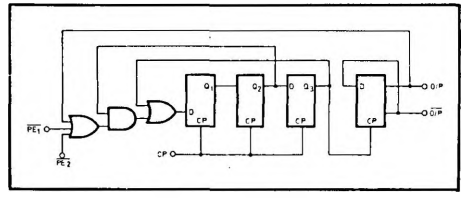

Fig. 2 Logic diagram SP8685

FEATURES

- Full temperature range operation:
  'A' grade -55°C to +125°C
  'B' grade 0°C to +70°C
  'M' grade -40°C to +85°C
- Self Biasing CP Input
- Wide Input Dynamic Range
- Control Inputs ECL 10K – Compatible
- Low Propagation Delay
- True and Inverse Outputs Available

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	0V to +8V
Input voltage, PE inputs	0V to V_{CC}
Input voltage, CP input	2V peak-to-peak
Output current	20mA
Operating junction temperature	+150°C
Storage temperature	−55°C to +150°C

ELECTRICAL CHARACTERISTICS

$\overline{PE}$ inputs – ECL 10K compatible

Outputs – ECL II compatible

Test conditions (unless otherwise stated)

Tamb 'A' grade -55°C to +125°C
'B' grade 0°C to +70°C
'M' grade -40°C to +85°C

Supply voltages: V_{CC} = +5.2V ±0.25V
V_{EE} = 0V

Clock input voltage: 400mV to 800mV (p-p)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Max i/p frequency	500			MHz	V_{cc} = +5.2V
Min i/p frequency			40		Sinewave Input
Min. slow rate for square wave input			100	V/μs	
Propogation delay (clock i/p to device o/p)		4		ns	
$\overline{PE}$ input reference level		+3.9		V	V_{cc} = +5.2V, 25°C
Power supply drain current		45	60	mA	V_{cc} = +5.2V, 25°C
$\overline{PE}$ input pulldown Resistors		4.3		KΩ	
Clock i/p impedance (i/p to i/p ref low frequency)		400		Ω	

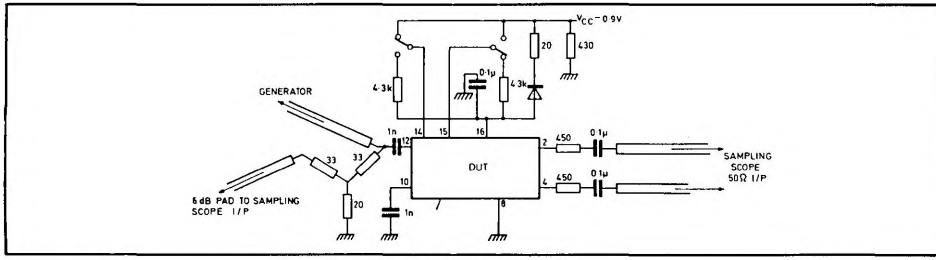

Fig. 3 Test circuit

APPLICATION NOTES

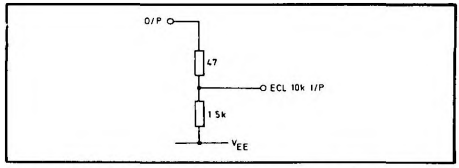

Fig. 4 SP8685 output – ECL 10K i/p and ECLII (for ECL 10K o/ps unloaded) – ECL 10K i/p

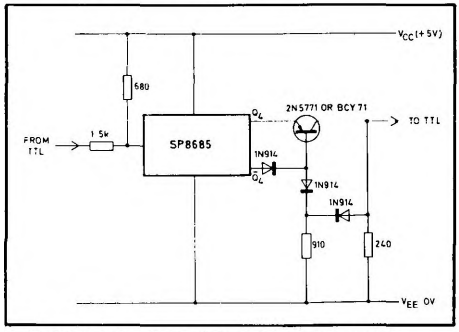

Fig. 5 TTL o/p – SP8685 $\overline{PE}$ i/p; SL8685 o/p – TTL i/p. (Total delay from SP8685 clock i/p to Schottky gate o/p = 15ns, typ.)

At an input frequency of 500 MHz the control loop delay time (SP8685 o/p to PE i/p) is approximately 16 ns. This will be a severe problem if TTL is used in the control loop.

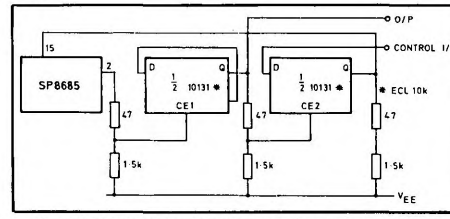

Fig. 6 Divide-by-20/22. Control loop delay time approximately 40ns.

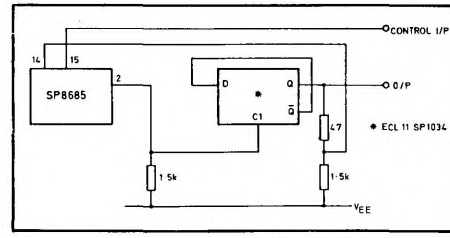

Fig. 7 Divide-by-20/21. Control loop delay time approximately 30ns using SP1034.