

SP8634B ÷ 10 700 MHz SP8636B ÷ 10 500 MHz

The SP8634B, SP8635B, SP8636B and SP8637B are divide-by-ten circuits with binary coded decimal outputs for operation from DC up to specified input frequencies of 700, 600, 500 and 400 MHz, respectively, over a guaranteed temperature range of 0° C to $+70^{\circ}$ C.

These devices, optimised for counter applications in systems using both ECL and TTL, are intended to be operated between 0V and -5.2V power rails and to

FEATURES

- Direct gating capability at up to 700 MHz
- TTL- compatible BCD outputs
- TTL- and ECL-compatible carry outputs
- Power consumption less than 500 mW
- Wide dynamic input range

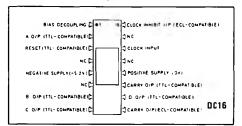
APPLICATIONS

- Counters
- Timers
- Synthesisers

SP8000 SERIES HIGH SPEED DIVIDERS

SP8635B ÷ 10 600 MHz SP8637B ÷ 10 400 MHz

interface with TTL operating between OV and +5V. The BCD outputs and one of two carry outputs are TTL-compatible, while the second carry output is ECL-compatible. The clock input, which is normally capacitively coupled to the signal source, is gated by an ECL III/ECL 10k-compatible input. The TTL-compatible reset forces the 0000 state regardless of the state of the other inputs.





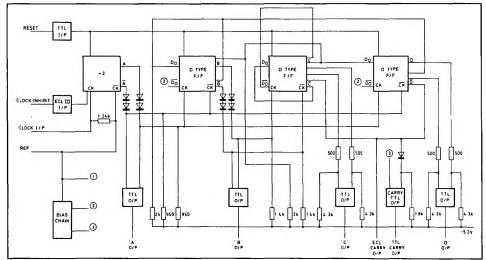


Fig. 2 Logic diagram

SP8634/5/6/7

ELECTRICAL CHARACTERISTICS (All types except where otherwise stated)

.

Test Conditions (unless otherwise stated)

Tamb		0°C to +70°C
Power Supplies	Vcc	0V
	VEE	-5.2V ± 0.25V

Characteristic	Value				
	Min.	Тур.	Max.	Units	Conditions
Clock Input (pin 14)					
Max. input frequency					
SP8634B	700)	MHz	
SP8635B	600		}	MHz	Input voltage
SP8636B	500		1	MHz	(400-800mV p
SP8637B	400			MHz	
Min, input frequency					+
with sinusoidal 1/P			40	MHz	
Min. slew rate of square wave for			100	V/µs	
correct operation					
down to DC] [
Clock inhibit input					
(pin 16)					
Logic levels			4		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
High (inhibit)	-0.960			v	T _{amb} = +25°C
Low			-1.650	v	(see Note 1)
Edge speed for correct operation	i (2,5	ns	10%-90%
at maximum clock I/P frequency					
Reset input (pin 3)					
Logic levels					
High (reset)	See Note 2				
Low			+0.4	v	
Reset ON time	100			ns	
TTL outputs ABCD (pins 2,7,8,10)					C. N
Output Voltage					See Note 3 and Fig
High	+2.4			v	$10k \Omega$ resistor and
				•	TTL gate from O/P
Low			+0.4	v	to +5V rail
TTL carry output (pin 11)					
Output Voltage					
High state	+2.4			v	5k Ω resistor and 3
U				•	TTL gates from o/
Low			+0.4	v	to 5V rail
ECL carry output (pin 9)					
Output Voltage					100 Aug. 1
High	-0.975			v	$T_{amb} = +25^{\circ}C$
				v	External current
Low			-1.375	v	= 0mA (See Note 4
Power supply drain current		75	90	mA	V _{EE} = 5.2V

NOTES

The clock inhibit input levels are compatible with ECL III and ECL 10000 levels throughout the temperature range 0°C to +70°C
For a high state, the reset input requires a more positive input level than the specified worst case TTL VOH of +2.4V. Resetting should be determined by the temperature range 0°C to +70°C.

be done by connecting a 1.8k Ω resistor from the output of the driving TTL gate and only fanning out to the reset input of the SP8000 series device.

3 These outputs are current sources which can be readily made TTL-compatible voltages by connecting them to +5V via 10kΩ resistors.

4 The ECL carry output is compatible with ECL II throughout the temperature range but can be made compatible with ECL III using the simple interface shown in Fig. 3.

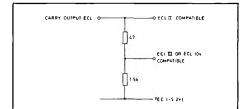


Fig. 3 ECL III/ECL 10000 interfacing

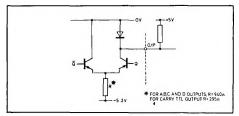


Fig. 4 TTL carry and ABCD output structure OPERATING NOTES

The devices are intended to be used with TTL and ECL in a counting system – the ECL and the decade counter being connected between voltage rails of OV and -5.2Vand the TTL between voltage rails of OV and +5.0V. Provided that this is done ECL and TTL compatability is achieved (see Figs. 4 and 5).

The clock is normally capacitively coupled to the signal source: a 1000pF UHF capacitor is normally adequate. If low frequency operation is required the 1000pF capacitor should be connected in parallel with a higher value capacitor. The bias decoupling (pin 1) should be connected to earth via a capacitor – preferably a chip type – but in any case a low inductance type suitable for UHF applications. The devices normally have an input amplitude operating range far greater than the specified 400 to 800 mV pk/pk. However, if the decoupling capacitor is not of a UHF type, or it is connected to an earth point that has a significant impedance between the capacitor and the V_{CC}.

connection, then the input dynamic range will suffer and the maximum signal for correct operation will be reduced.

Under certain conditions, the absence of an input signal may cause the device to self-oscillate. This can be prevented (while still maintaining the specified input sensitivity) by connecting a $68k\Omega$ resistor between the clock input and the negative supply. If the transition of either the clock input or the clock inhibit input is slow the device may start to self-oscillate during the transition. For this reason, the input slew rates should be greater than 100 V/µs. It should also be noted that a positive-going transition on either the clock input or the clock inhibit input will clock the device, provided that the other input is in the low state.

The BCD outputs give TTL-compatible outputs (fanout = 1) when a 10k Ω resistor is connected from the output to the +5V rail. In this configuration the outputs will be very slow compared with the clocking rate of the decade and so the state on the BCD outputs can only be determined when the clock has stopped or is inhibited.

The fan out capability of the TTL carry output can be increased by buffering it with a PNP emitter follower. The interface is shown in Fig. 5.

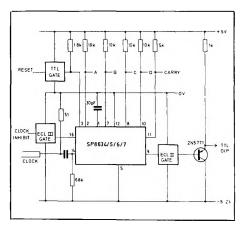


Fig. 5 Typical application configuration

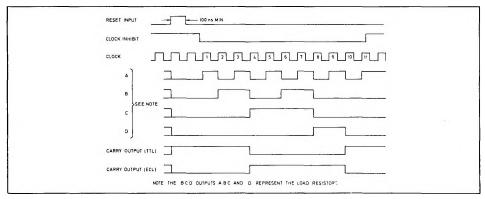


Fig. 6 Decade counter timing diagram

SP8634/5/6/7

ABSOLUTE MAXIMUM RATINGS

Power supply voltage 1V	8V		
Clock inhibit voltage	Not greater than the supply		
-	(*)	voltage in use	
Clock input voltage	2V pk/pk		
Bias voltage (V _{OUT}) on			
VOUT - VEE (10kΩ re	sistor in series		
with output)	11V		
Bias voltage (V _{OUT}) on			
output, Vour - Vee (output, $V_{\Omega UT} - V_{EE}$ (1.2k Ω resistor		
in series with output)	in series with output)		
Output current from EC	L carry		
output (IOUT) (Note: th	e device		
will be destroyed if the E	CL		
output is shorted to the			
negative rail)		10mA	
Operating junction temperature		+150°C	
Storage temperature range		–55°C to +150°C	
QUICK REFERENCE	ΑΤΑ		
Power Supplies	Vcc	ÛV	
	VEE	5 2V + 0 25V	

VEE	5.2V ± 0.25∨
Range of clock input amplitude	400-800mV p-p
Operational temperature range	0°C to +70°C
Frequency range with sinusoidal I/P	40-700 MHz (SP8634B)
Frequency range with square wave I/P	DC to 700 NiH7 (SP8634B)