SP5655



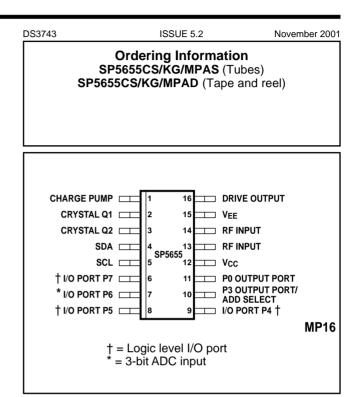
2-7GHz Bidirectional I²C Bus Controlled Synthesiser

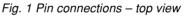
Datasheet

The SP5655 is a single chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. The device contains 2 addressable current limited outputs and 4 addressable bidirectional open-collector ports, one of which is a 3-bit ADC. The information on these ports can be read via the I²C BUS. the device has one fixed I²C BUS address and 3 programmable addresses, programmed by applying a specific input voltage to one of the current limited outputs. This enables two or more synthesisers to be used in a system.

FEATURES

- Complete 2.7GHz Single Chip System
- High Sensitivity RF Inputs
- Programmable via I²C BUS
- Low Power Consumption (5V, 30mA)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 6 Controllable Outputs, 4 Bidirectional
- 5-Level ADC
- Variable I²C BUS Address for Multi-tuner Applications
- ESD Protection: 4kV, Mil-Std-883C, Method 3015⁽¹⁾
- Switchable 4512/1024 Reference Divider
- Pin and Function Compatible with SP5055S ⁽²⁾
 - (1) Normal ESD handling precautions should be observed.
 - (2) The SP5055S does not have a switchable reference division ratio.





APPLICATIONS

- Satellite TV
- High IF Cable Tuning Systems

THERMAL DATA

 $\begin{array}{l} u_{JC} = 41^{\circ}C/W \\ u_{JA} = 111^{\circ}C/W \end{array}$

ELECTRICAL CHARACTERISTICS

 $T_{AMB} = -20^{\circ}$ C to $+80^{\circ}$ C, $V_{CC} = +4^{\circ}$ SV to $+5^{\circ}$ SV, reference frequency = 4MHz. These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Win.Typ.Max.ControlSupply current12 Prescaler input voltage13,14 13,1450 300 40 300 $mVms$ $V_{CC} = 4.5V$ to 5.5V (note 1) to 2.7GHz sinewave, see Fig. 5Prescaler input impedance13,1450 Ω pF Ω pF Ω pFSDA, SCL Input high voltage4,535.5V 10Input voltage = V _{CC} 10Input voltage = 0V When V _{CC} = 0VSDA Output voltage40.4VSink current = 3mACharge pump current low Charge pump output leakage current1 ± 170 ± 170 μ A ± 170 Byte 4, bit 2 = 0, pin 1 = 2V μ ACharge pump output leakage current Charge pump output leakage current Charge pump aptifier gain Recommended crystal series resistance External reference input requency 22 70000 200 Ω Ω Ω AC coupled sinewave Δ $\Delta C coupled sinewavePO, P3 sink currentP4-P7 isk currentP4-P7 leakage current111.5mAMHZVoir = 12VV_{OUT} = 32VPAPOP4-P5, P7 input voltage lowP4, P5, P7 input voltage low10\muAVoir = 12VV_{OUT} = 0V/V_VP4-P5, P7 input voltage lowP4, P5, P7 input voltage low10\muAVoir = 12VV_{OUT} = 132VP6 input current lighP410\muA\Psi Pin 10 = VCCP3 input current lighP410\muAV$	Obeve stevistic	Dim		Value		Unite		
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Leakage current4,510 μA When $V_{CC} = 0V$ SDA Output voltage40-4VSink current = 3mACharge pump current low Charge pump current high1 ± 50 ± 170 μA Byte 4, bit 2 = 0, pin 1 = 2VCharge pump current high Charge pump drive output leakage current Charge pump amplifier gain Recommended crystal series resistance External reference input frequency External reference input multide 200 2 μA Byte 4, bit 2 = 1, pin 1 = 2VOutput Ports P0, P3 sink current P4-P7 sink current P4-P7 leakage current $11, 10$ $9-6$ $0-7$ 10 1 10 $1-5$ 100 μA Byte 4, bit 4 = 1, pin 1 = 2VInput Ports P3 input current high P4, P5, P7 input voltage low P4, P5, P7 input voltage high P4, P5, P7 input voltage high P6 input current high10 T 10 PA 10 PA $4-10$ PA μA PAV pin 10 = V_{CC} V V pin 10 = 0VP4P5, P7 input voltage high P6 input current high P6 input current high10 T 7 $4-10$ P7 μA P4V pin 10 = V_{CC} V P4P3P3P3P3P4P3P4P3P4P3P4P3P4P4P4V pin 10 = 0VP4P5, P7 input voltage low P6 $9,8,6$ P6 $2-7$ $2-7$ $2-7$ $2-7$ $2-7$ <td></td> <td></td> <td></td> <td></td> <td>10</td> <td>· ·</td> <td></td>					10	· ·		
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$\begin{array}{cccccccccccccccccccccccccccccccccccc$	Output voltage	4			0.4	V	Sink current = 3mA	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	Charge pump current low	1		±50		μA	Byte 4, bit 2 = 0, pin 1 = 2V	
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$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Charge pump output leakage current	1			±5	nA	Byte 4, bit 4 = 1, pin 1 = 2V	
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Crystal oscillator drive level280mV p-pCrystal oscillator negative resistance27501000 Ω External reference input frequency222External reference input amplitude2708MHz Output Ports 27011.5mAP0, P3 sink current11, 100.711.5mAP0, P3 leakage current11, 100.711.5mAP4-P7 sink current9-61010 μA $V_{OUT} = 12V$ P4-P7 leakage current9-61010 μA $V_{OUT} = 13.2V$ P3 input current high1010 μA $V_{OUT} = 13.2V$ P3 input current low100.710 μA $V pin 10 = V_{CC}$ P4, P5, P7 input voltage low9,8,62.7 V V $V pin 10 = 0V$ P4, P5, P7 input voltage high9,8,62.7 V V $V pin 10 = 0V$ P6 input current high7 V V $V pin 10 = 0V$ $V pin 10 = 0V$	Charge pump amplifier gain			6400				
$\begin{array}{c} \mbox{Crystal oscillator negative resistance} \\ \mbox{External reference input frequency} \\ \mbox{External reference input amplitude} \end{array} \begin{array}{c} 2 \\ 2 \\ 2 \\ 2 \\ 70 \end{array} \begin{array}{c} 1000 \\ 8 \\ 200 \end{array} \begin{array}{c} \mbox{MHz} \\ MHz \\ 200 \end{array} \begin{array}{c} \mbox{AC coupled sinewave} \\ AC coupled sinew$	Recommended crystal series resistance		10		200	Ω	Parallel resonant crystal (note 2)	
External reference input frequency External reference input amplitude2228MHz 200AC coupled sinewave AC coupled sinewaveOutput Ports P0, P3 sink current P0, P3 leakage current11, 10 0.7 1 1.5 mA μ $V_{OUT} = 12V$ $V_{OUT} = 13.2V$ P4-P7 sink current P4-P7 leakage current9-61010 μA $V_{OUT} = 0.7V$ μA $V_{OUT} = 13.2V$ Input Ports P3 input current high1010 -10 μA $V pin 10 = V_{CC}$ P3 input current low P4, P5, P7 input voltage low P4, P5, P7 input voltage high P6 input current high10 -10 μA $V pin 10 = 0V$ P4 input current high9,8,6 2.7 V V $V pin 10 = 0V$ P4 input current high7 V V $V pin 10 = 0V$	Crystal oscillator drive level	2		80		mV p-p		
External reference input amplitude270200mVrmsAC coupled sinewaveOutput Ports $P0, P3 sink current11, 100.711.5mAV_{OUT} = 12VP0, P3 leakage current11, 100.711.5mAV_{OUT} = 12VP4-P7 sink current9.61010\mu AV_{OUT} = 0.7VP4-P7 leakage current9.61010\mu AV_{OUT} = 13.2VInput PortsP3 input current high10+10\mu AV pin 10 = V_{CC}P3 input current low100.8VV pin 10 = 0VP4, P5, P7 input voltage low9,8,62.7VVP6 input current high72.77VVVP6 input current high72.77VVV$	Crystal oscillator negative resistance	2	750	1000		Ω		
Output Ports P0, P3 sink current P0, P3 leakage current P4-P7 sink current P4-P7 leakage current11, 10 9-6 9-6 0.7 1 1.5 10 μA mA μA $V_{OUT} = 12V$ $V_{OUT} = 13.2V$ $V_{OUT} = 0.7V$ $V_{OUT} = 13.2V$ Input Ports P3 input current high P4, P5, P7 input voltage low P6 input current high10 10 9,8,6 9,8,6 $+10$ 0.8 μA $V_{OUT} = 12V$ $V_{OUT} = 0.7V$ $V_{OUT} = 13.2V$ Input Ports P3 input current low P4, P5, P7 input voltage low P6 input current high10 $9,8,6$ 2.7 $+10$ V μA V pin 10 = V_{CC} V V pin 10 = 0V	External reference input frequency	2	2		8	MHz	AC coupled sinewave	
P0, P3 sink current11, 10 0.7 1 1.5 mA $V_{OUT} = 12V$ P0, P3 leakage current11, 10 9.6 10 μA $V_{OUT} = 13.2V$ P4-P7 sink current 9.6 10 10 μA $V_{OUT} = 0.7V$ P4-P7 leakage current 9.6 10 10 μA $V_{OUT} = 13.2V$ Input Ports 9.6 10 10 μA $V_{OUT} = 13.2V$ P3 input current high10 10 $+10$ μA V pin 10 = V_{CC} P3 input current low10 -10 μA V pin 10 = V_{CC} P4, P5, P7 input voltage low $9.8.6$ 2.7 V V P4, P5, P7 input voltage high $9.8.6$ 2.7 V V P6 input current high7 $+10$ μA See Table 3 for ADC levels	External reference input amplitude	2	70		200	mVrms	AC coupled sinewave	
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P4-P7 sink current P4-P7 leakage current9-610mA $V_{OUT} = 0.7V$ μA Input Ports P3 input current high P3 input current low10+10 μA $V_{OUT} = 13.2V$ P3 input current low P4, P5, P7 input voltage low P6 input current high10+10 μA V pin 10 = V_{CC} V P6 input current high P6 input current high9,8,62.7 V Vpin 10 = 0VP6 input current high9,8,62.7 V VSee Table 3 for ADC levels	P0, P3 leakage current	11, 10			10	μA		
Input Ports10 $+10$ μA $V pin 10 = V_{CC}$ P3 input current high10 -10 μA $V pin 10 = 0V$ P3 input current low10 -10 μA $V pin 10 = 0V$ P4, P5, P7 input voltage low9,8,6 0.8 V P4, P5, P7 input voltage high9,8,6 2.7 V P6 input current high7 $+10$ μA See Table 3 for ADC levels	P4-P7 sink current		10			· ·	$V_{OUT} = 0.7V$	
P3 input current high10 $+10$ μA V pin 10 = V_{CC}P3 input current low10 -10 μA V pin 10 = 0VP4, P5, P7 input voltage low9,8,6 $2\cdot7$ $0\cdot8$ VP4, P5, P7 input voltage high9,8,6 $2\cdot7$ VP6 input current high7 $+10$ μA See Table 3 for ADC levels	P4-P7 leakage current	9-6			10	μA	$V_{OUT} = 13.2V$	
P3 input current high10 $+10$ μA V pin 10 = V_{CC}P3 input current low10 -10 μA V pin 10 = 0VP4, P5, P7 input voltage low9,8,6 $2\cdot7$ $0\cdot8$ VP4, P5, P7 input voltage high9,8,6 $2\cdot7$ VP6 input current high7 $+10$ μA See Table 3 for ADC levels	Input Ports							
P3 input current low10 -10 μA V pin 10 = 0VP4, P5, P7 input voltage low9,8,6 0.8 VP4, P5, P7 input voltage high9,8,6 2.7 VP6 input current high7 $+10$ μA See Table 3 for ADC levels	-	10			+10	μA	V pin 10 = V _{CC}	
P4, P5, P7 input voltage low 9,8,6 0.8 V P4, P5, P7 input voltage high 9,8,6 2.7 V P6 input current high 7 +10 μA See Table 3 for ADC levels		10			-10	· ·		
P4, P5, P7 input voltage high 9,8,6 2·7 V P6 input current high 7 +10 μA See Table 3 for ADC levels		9,8,6			0.8	· ·		
P6 input current high 7 +10 μA See Table 3 for ADC levels			2.7			V		
· · · · · · · · · · · · · · · · · · ·					+10	μA	See Table 3 for ADC levels	
	P6 input current low	7			-10	μA		

NOTES 1. Maximum power consumption is 220mW with $V_{CC} = 5.5V$ and all ports off. 2. Resistance specified is maximum under all conditions.

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V

Parameter	Pin	Va	lue	Units	Conditions
		Min.	Max.	onits	Conditions
Supply voltage	12	-0·3	7	V	
RF input voltage	13,14		2.5	V р-р	
Port voltage	6-11	-0·3	14	V	Port in off state
	6-9	-0·3	6	V	Port in on state
	10, 11	-0·3	14	V	Port in on state
Total port output current	6-9		50	mA	
Address select voltage	10	-0·3	V _{CC} +0·3	V	
RF input DC offset	13-14	-0·3	V _{CC} +0·3	V	
Charge pump DC offset	1	-0·3	$V_{CC}+0.3$	V	
Drive output DC offset	16	-0·3	V _{CC} +0·3	V	
Crystal oscillator DC offset	2	-0·3	$V_{CC}+0.3$	V	
SDA, SCL input voltage	4,5	-0·3	6	V	
Storage temperature		-55	+150	°C	
Junction temperature			+150	°C	

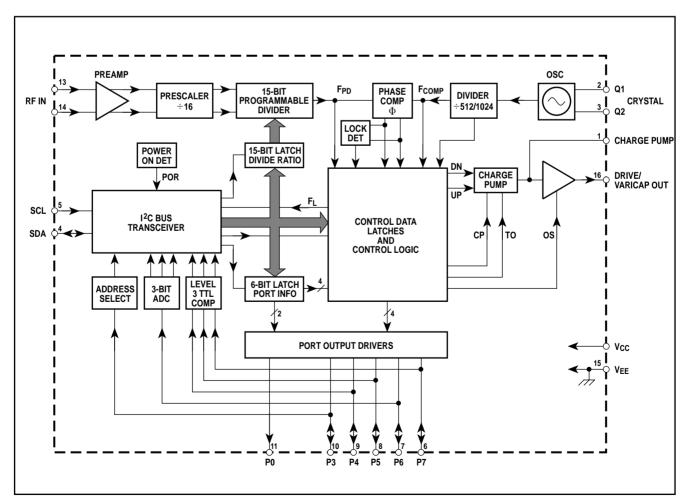


Fig. 2 Block diagram

FUNCTIONAL DESCRIPTION

The SP5655 is programmed from an I²C Bus. Data and Clock are fed in on the SDA and SCL lines respectively, as defined by the I²C Bus format. The synthesiser can either accept new data (write mode) or send data (read mode). The LSB of the address byte (R/W) sets the device into write mode if it is low and read mode if it is high. The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I²C Bus system. Table 4 shows how the address is selected by applying a voltage to P3.

When the device receives a correct address byte, it pulls the SDA line low during the acknowledge period, and during following acknowledge periods after further data bytes are programmed. When the device is programmed into the read mode, the controller accepting the data must pull the SDA line low during all status byte acknowledge periods to read another status byte. If the controller fails to pull the SDA line low during this period, the device generates an internal STOP condition, which inhibits further reading.

WRITE Mode (Frequency Synthesis)

When the device is in write mode bytes 2 and 3 select the synthesised frequency, while bytes 4 and 5 control the output port states, charge pump, reference divider ratio and various test modes.

Once the correct address is received and acknowledged, the first bit of the next byte determines whether that byte is interpreted as byte 2 or 4; a logic 0 for frequency information and a logic 1 for control and output port information. When byte 2 is received the device always expects byte 3 next. Similarly, when byte 4 is received the device expects byte 5 next. Additional data bytes can be entered without the need to readdress the device until an I^2C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid-byte (for example, by another device on the bus) then the previously programmed byte is maintained.

Frequency data from bytes 2 and 3 are stored in a 15-bit register and used to control the division ratio of the 15-bit programmable divider. This is preceded by a divide-by-16 prescaler and amplifier to give excellent sensitivity at the local oscillator input, see Fig. 5. The input impedance is shown in Fig. 7.

The programmed frequency can be calculated by multiplying the programmed division ratio by 16 times the comparison frequency F_{COMP} . When frequency data is entered, the phase comparator, via a charge pump and varicap drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phased locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2, or provided by an onchip crystal controlled oscillator. The comparison frequency F_{COMP} is derived from the reference frequency via the reference divider. The reference divider division ratio is switchable from 512 to 1024, and is controlled by bit 7 of byte 4 (TS0); a logic 1 to 512, a logic 0 for 1024. The SP5655 differs from the SP5055 in this respect, only 512 being available on the SP5055. Note that the comparison frequency is $7\cdot8125$ kHz when a 4MHz reference is used, and divide by 512 is selected.

Bit 2 of byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for $\pm 170\mu$ A and a logic 0 for $\pm 50\mu$ A, allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. When the device is frequency locked, the charge pump current is internally set to $\pm 50\mu$ A regardless of CP.

Bit 4 of byte 4 (T0) disables the charge pump when it is set to a logic 1.

Bit 8 of byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1.

Bit 3 of byte 4 (T1) enables various test modes when set high. These modes are selected by bits 5, 6 and 7 of byte 4 (TS2, and TS1, TS0) as detailed in Table 5. When T1 is set low, TS2 and TS1 are assigned a 'don't care' condition, and TS0 selects the reference divider ratio as previously described.

Byte 5 programs the output ports P0 and P3 to P7; a logic 0 for a high impedance output and a logic 1 for low impedance (on).

READ Mode

When the device is in read mode the status byte read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power-on reset indicator and is set to a logic 1 if the V_{CC} supply to the device has dropped below 3V (at 25°C), for example, when the device is initially turned on. The POR is reset to 0 when the read sequence is terminated by a stop command. When POR is set high (at low V_{CC}), the programmed information is lost and the output ports are all set to high impedance.

Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked, and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2, I1, I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic 1). These inputs will then respond to data complying with TTL type voltage levels.

Bits 6, 7 and 8 (A2, A1, A0) combine to give the output of the 5-level ADC. The ADC can be used to feed AFC information to the microprocessor from the IF section of the receiver, as illustrated in the typical application circuit.

APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6. The SP5655 is function and pin equivalent to the SP5055 device apart from the switchable reference divider, and has much lower power dissipation, improved RF sensitivity and better ESD performance.

	MSB							LSB				
Address	1	1	0	0	0	MA1	MA0	0	А	Byte 1		
Programmable divider	0	214	2 ¹³	2 ¹²	211	2 ¹⁰	2 ⁹	2 ⁸	А	Byte 2		
Programmable divider	2 ⁷	2 ⁶	2 ⁵	24	2 ³	2 ²	2 ¹	2 ⁰	А	Byte 3		
Charge pump and test bits	1	СР	T1	Т0	TS2	TS1	TS0	OS	А	Byte 4		
I/O port control bits	Ρ7	P6	P5	P4	P3	Х	Х	P0	А	Byte 5		

Table 1 Write data format (MSB transmitted first)

Address	1	1	0	0	0	MA1	MA0	1	Α	Byte 1
Status byte	POR	FL	12	11	10	A2	A1	A0	Α	Byte 2

Table 2 Read data format

A2	A 1	A0	Voltage input to P6
1	0	0	0·6V _{CC} to 13·2V
0	1	1	0·45V _{CC} to 0·6V _{CC}
0	1	0	$0.3V_{CC}$ to $0.45V_{CC}$
0	0	1	0·15V _{CC} to 0·3V _{CC}
0	0	0	0V to 0·15V _{CC}

MA1	MA0	Address select input voltage				
0	0	0V to 0·2V _{CC}				
0	1	Always valid				
1	0	0.3V _{CC} to 0.7V _{CC}				
1	1	0.8V _{CC} to 13.2V				

Table 3 ADC levels

Table 4 Address selection

T1	TS2	TS1	TS0	Operation mode description
0	Х	Х	0	Normal operation, test modes disabled, reference divider ratio = 1024
0	Х	Х	1	Normal operation, test modes disabled, reference divider ratio = 512
1	0	0	Х	Charge pump source (down). Status bit FL set to 0
1	0	1	Х	Charge pump sink (up). Status bit FL set to 1
1	1	0	0	Ports P4, P5, P6, P7set to state X
1	1	0	1	Port P7 = $F_{PD}/2$; P4, P5, P6 set to state X
1	1	1	Х	Port P7 = F_{PD} ; P6 = F_{COMP} ; P4, P5 set to state X

Table 5 Operation modes

NOTES

X = don't care

For further details of test modes, see Table 6

A MA1, MA0 CP T1 T0 TS2, TS1, TS0 OS P7, P6, P5, P4, P3, P0 POR FL I2, I1, I0	:	Acknowledge bit Variable address bits (see Table 4) Charge Pump current select Test mode selection Charge pump disable Operation mode control bits (see Table 5) Varactor drive Output disable Switch Control output port states Power On Reset indicator Phase lock detect flag Digital information from ports P7, P5 and P4 respectively
	: :	
X	:	Don't care

SP5655 Datasheet

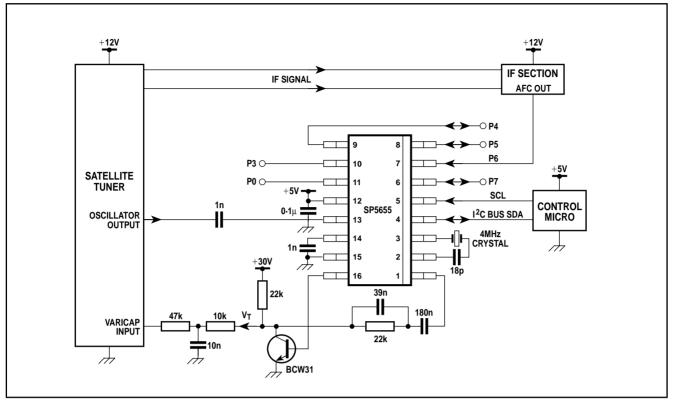


Fig. 4 Typical application

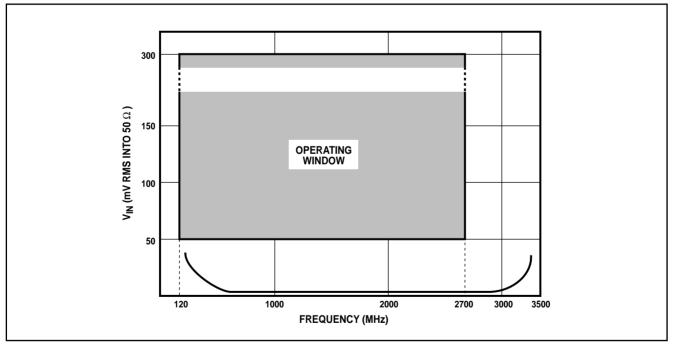


Fig. 5 Typical input sensitivity

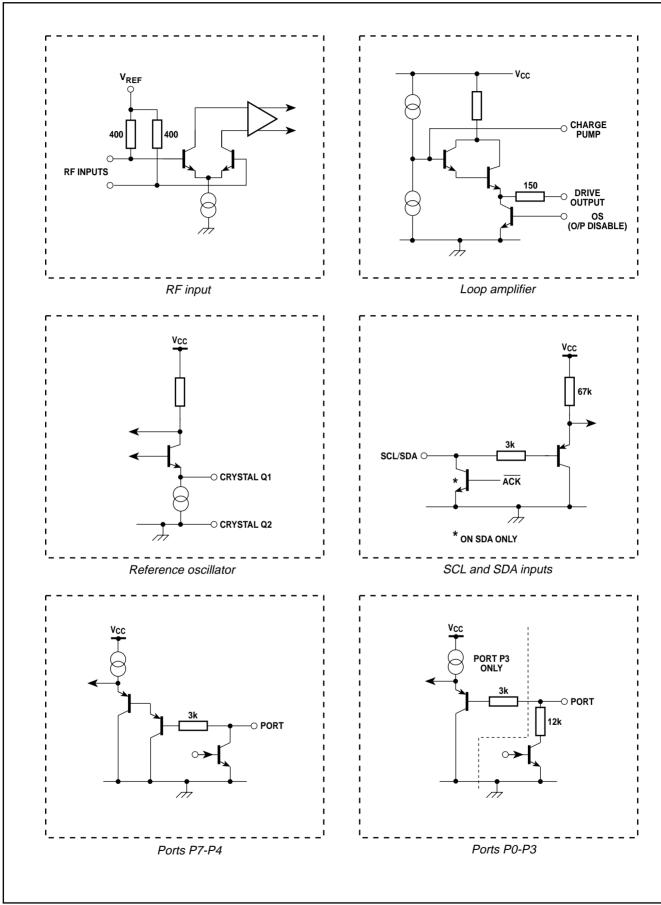


Fig. 6 SP5655 input/output interface circuits

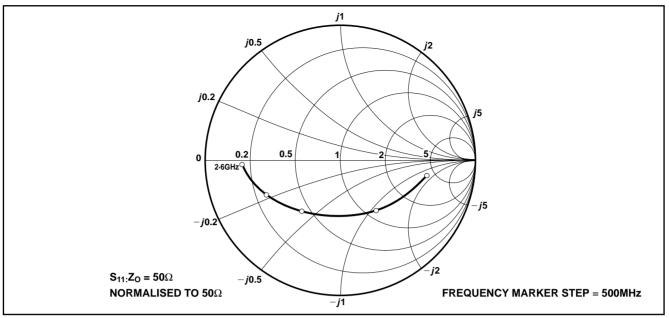


Fig. 7 Typical input impedance,

APPLICATION NOTES

An application note, AN168, is available for designing with synthesisers such as the SP5655. It covers aspects such as loop filter design, decoupling and I²C bus radiation problems.

The application note is published in the Zarlink Semiconductor Media IC Handbook. A generic test/demonstration board has been produced, which can be used for the SP5655. A circuit diagram and layout for the board are shown in Figs. 8 and 9.

The board can be used for the following purposes:

- (A) Measuring RF sensitivity perfomance (B) Indicating port function
- (C) Synthesising a voltage controlled oscillator
- (D)Testing external reference sources

The programming codes relevant to these tests are given in Table 6.

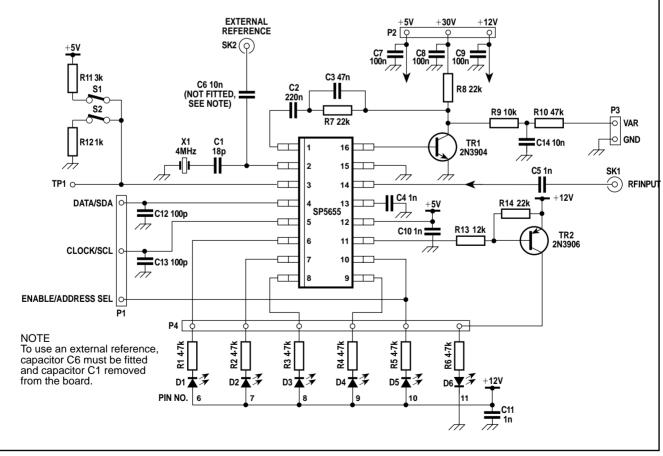


Fig. 8 Test board circuit

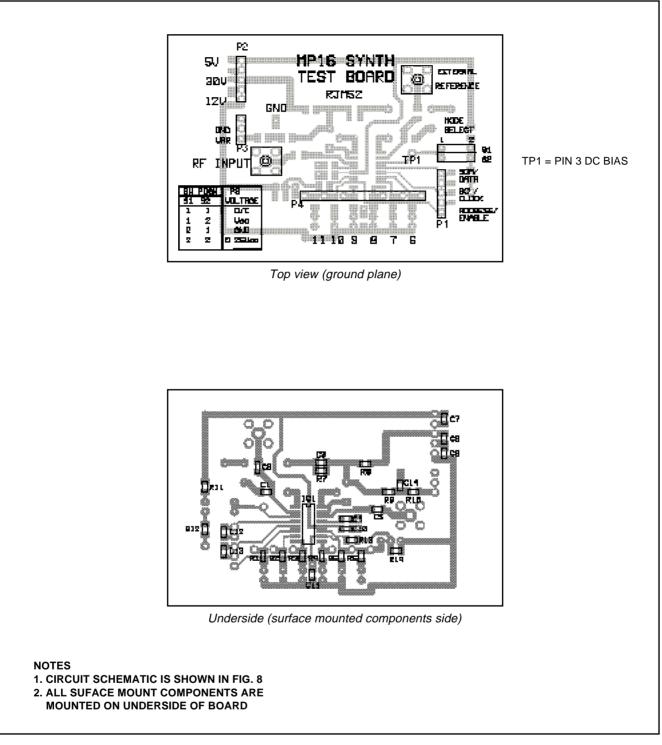


Fig. 9 Test board layout

SP5655 Datasheet

TEST MODES

As explained in the functional description, The SP5655 can be programmed into a numb er of test modes. These are invoked by programming Hex codes into byte 4, those most commonly used being shown in Table 6.

Other codes will also apply due to don't care conditions, which are assumed to be 1 in the Table.

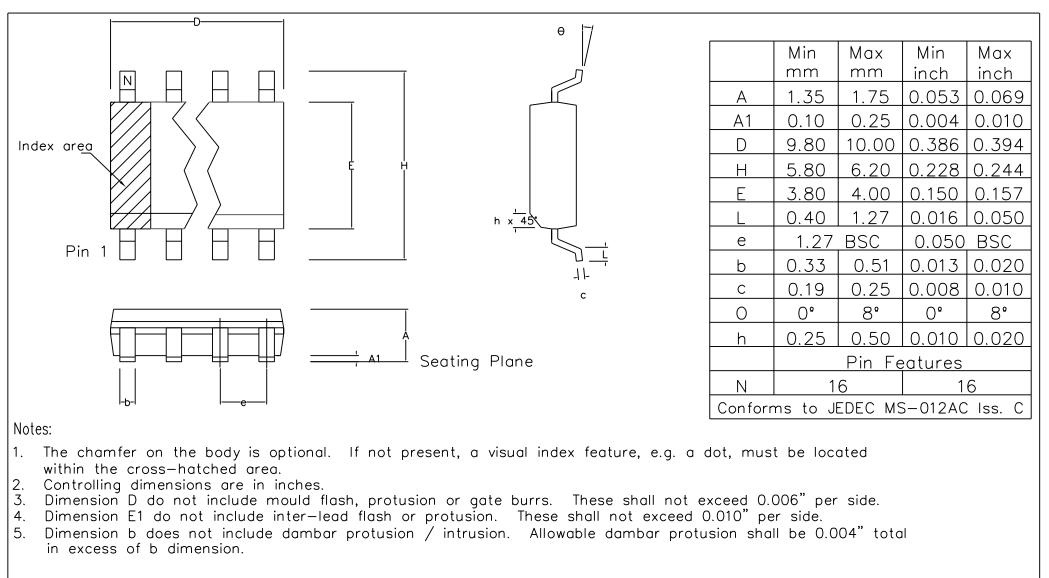
NOTE:

When looking at F_{PD} or F_{COMP} signals from ports P7 and P6. byte should be sent twice, first to set the desired reference division ratio then to switch on the chosen test mode.

The pulses can then be measured by simply connecting an oscilloscope or counter to the relevant output pin on the test board.

Ou constituer, une de la deservicitier	Hex code	e (byte 4)
Operation mode description	CP high mode	CP low mode
Normal operation, reference divider ratio = 1024	CC	8C
Normal operation, reference divider ratio = 512	CE	8E
Charge pump source (down), FL set to 0	E2	A2
Charge pump sink (up), FL set to 1	E6	A6
Port P7 = $F_{PD}/2$	EA	AA
Port P7 = F_{PD} , P6 = F_{COMP}	EE	AE
Charge pump disable, reference divider ratio = 512	DE	9E
Varactor line disable, reference divider ratio = 512	CF	8F
Charge pump and varactor line disable, reference divider ratio = 512	DF	9F

Table 5 Operation modes



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ISSUE	1	2	3	4	5		Previous package codes	Package Outline for
ACN	6745	201938	202597	203706	212431	ZARLINK SEMICONDUCTOR		16 lead SOIC (0.150" Body Width)
DATE	7Apr95	27Feb97	12Jun97	9Dec97	25Mar02			
APPRD.								GPD00012



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