PLESSEY
SEMICONDUCTORS

SP1600 SERIES
ECL III

SP1692B
QUAD LINE RECEIVER

Four differential amplifiers with emitter followers intended for use in sensing differential signals over long lines.

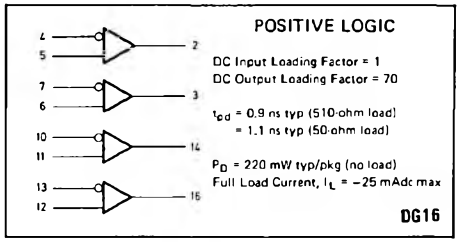

Fig. 1 Logic diagram of SP1692

ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC 14A2CB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is in either a test socket or is mounted on a printed circuit board.

@ Test Temperature	TEST VOLTAGE VALUES					
	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}
0°C	−0.840	−1.870	−1.135	−1.500	From Pin 9	−5.2
+25°C	−0.810	−1.850	−1.095	−1.485		−5.2
+75°C	−0.720	−1.830	−1.035	−1.035		−5.2

Characteristic	Symbol	Pin Under Test	SP1692 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	50	–	–	mAdc	–	4,7,10,13	–	–	5,6,11,12	8	1,16
Input Current	I_{in}	4	–	–	–	250	–	–	μAdc	4	7,10,13	–	–	5,6,11,12	8	1,16
Input Leakage Current	I_R	4	–	–	–	100	–	–	μAdc	–	7,10,13	–	–	5,6,11,12	8,4	1,16
Logic "1" Output Voltage	V_{OH}	2	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	7,10,13	4	–	–	5,6,11,12	8	1,16
Logic "0" Output Voltage	V_{OL}	2	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	Vdc	4	7,10,13	–	–	5,6,11,12	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	−1.020	–	−0.980	–	−0.920	–	Vdc	–	7,10,13	–	4	5,6,11,12	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1.615	–	−1.600	–	−1.575	Vdc	–	7,10,13	4	–	5,6,11,12	8	1,16
Reference Voltage	V_{BB}	9	1.375	1.275	−1.35	−1.25	−1.30	−1.20	Vdc	–	–	–	–	5,6,11,12	8	1,16
Switching Times (50Ω Load)			Typ	Max	Typ	Max	Typ	Max		Pulse In		Pulse Out				
Propagation Delay	t_{4-2+}	2	1.0	1.5	1.0	1.5	1.1	1.7	ns	4		2		5,6,11,12	8	1,16
	t_{4+2-}	2	1.1	1.7	1.1	1.7	1.2	1.9								
Rise Time	t_{2+}	2	1.4	2.1	1.4	2.1	1.5	2.3								
Fall Time	t_{2-}	2	1.2	2.1	1.2	2.1	1.3	2.3								

PLESSEY
SEMICONDUCTORS

SUB-NANOSECOND LOGIC

SP16F60

DUAL 4-INPUT OR/NOR GATE

SP16F60 provides simultaneous OR-NOR output functions with the capability of driving 50 Ω lines. This device contains an internal bias reference voltage, ensuring that the threshold point is always in the centre of the transition region over the temperature range (−30°C to +85°C). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

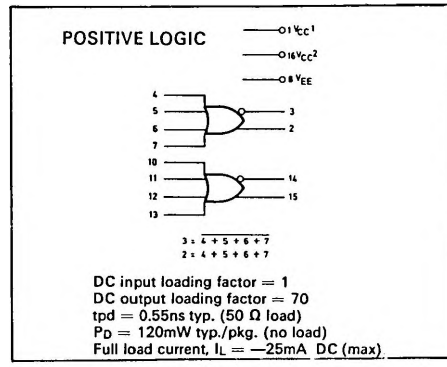

Fig. 1 Logic diagram

FEATURES

- Gate Switching Speed 550ps Typ.
- ECL III and ECL 10K Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation
- Pin and Power Compatible with SP1660

APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems
- Nucleonics

ABSOLUTE MAXIMUM RATINGS

Power supply voltage | V_{CC} - V_{EE} |	8V
Base input voltage	OV to V_{EE}
O/P source current	<40mA
Storage temperature	−55°C to +150°C
Junction operating temperature	< +125C

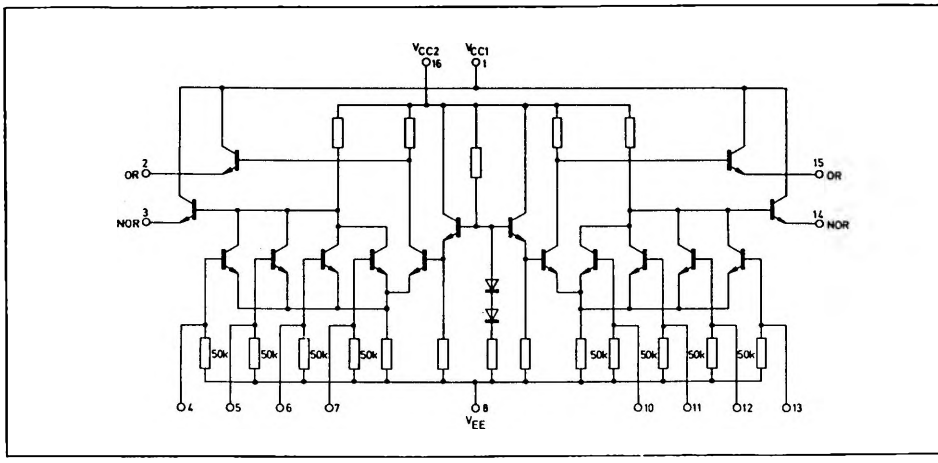

Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL circuit has been designed to meet the DC specifications shown in the characteristics table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC 14A2CB or equivalent) or a transverse air flow greater than 500 linear ft/min should be maintained while the circuit is in either a test socket or is mounted on a printed circuit board. Test procedures are shown for only one gate. The other gates are tested in the same manner. Outputs are tested with a 50 Ω resistor to −2.0V DC.

@ Test Temperature	$V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	−0.875	−1.890	−1.180	−1.515	−5.2
+25°C	−0.810	−1.850	−1.095	−1.485	−5.2
+85°C	−0.700	−1.830	−1.025	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	SP16F60 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Units	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	V_{CC} (Gnd)
Power Supply Drain Current	I_E	8	–	–	–	28	–	–	mA	–	–	–	–	8	1,16
Input Current	I_{inH}	*	–	–	–	350	–	–	μA	*	–	–	–	8	1,16
	I_{inL}	*	–	–	0.5	–	–	–	μA	–	*	–	–	8	1,16
NOR Logic 1 Output Voltage	V_{OH}	3	-1.045	-0.875	-0.960	-0.810	-1.890	-0.700	V	–	4	–	–	8	1,16
										–	5	–	–		
										–	6	–	–		
										–	7	–	–		
NOR Logic 0 Output Voltage	V_{OL}	3	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	V	4	–	–	–	8	1,16
										5	–	–	–		
										6	–	–	–		
										7	–	–	–		
OR Logic 1 Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	V	4	–	–	–	8	1,16
										5	–	–	–		
										6	–	–	–		
										7	–	–	–		
OR Logic 0 Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	V	–	4	–	–	8	1,16
										–	5	–	–		
										–	6	–	–		
										–	7	–	–		
NOR Logic 1 Threshold Voltage	V_{OHA}	3	-1.065	–	-0.980	–	-0.910	–	V	–	–	–	4	8	1,16
										–	–	–	5		
										–	–	–	6		
										–	–	–	7		
NOR Logic 0 Threshold Voltage	V_{OLA}	3	–	-1.630	–	-1.600	–	-1.555	V	–	–	4	–	8	1,16
			–		–		–			–	–	5	–		
			–		–		–			–	–	6	–		
			–		–		–			–	–	7	–		
OR Logic 1 Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	V	–	–	4	–	8	1,16
			–		–		–			–	–	5	–		
			–		–		–			–	–	6	–		
			–		–		–			–	–	7	–		
OR Logic 0 Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	V	–	–	–	4	8	1,16
			–		–		–			–	–	–	5		
			–		–		–			–	–	–	6		
			–		–		–			–	–	–	7		
Switching Times (50Ω Load)			Typ	Max	Typ	Max	Typ	Max		Pulse In	Pulse Out			-3.2V	+2.0V
Propagation Delay	t_{4+3-}	3	–	–	0.55	0.8	–	–	ns	4	3	–	–	8	1,16
	t_{4-2-}	2	–	–			–	–			2	–	–		
	t_{4+2+}	2	–	–			–	–			2	–	–		
	t_{4-3+}	3	–	–			–	–			3	–	–		
Rise Time 20% to 80%	t_{3+}	3	1.5	2.1	0.4	0.6	–	–	ns	4	3	–	–	8	1,16
	t_{2+}	2	1.5	2.1	0.35	0.6	–	–	ns	4	2	–	–	8	1,16
Fall Time 20% to 80%	t_{3-}	3	1.4	2.1	0.4	0.6	–	–	ns	4	3	–	–	8	1,16
	t_{2-}	2	1.4	2.1	0.35	0.6	–	–	ns	4	2	–	–	8	1,16

* Individually test each input applying V_{IH} or V_{IL} to the input under test

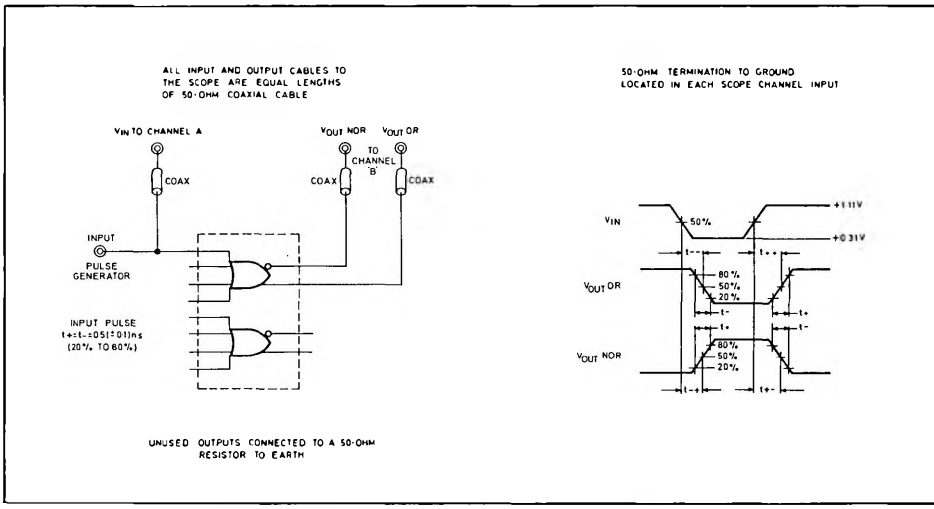

Fig. 3 Switching time test circuit and waveforms at +25°C

PACKAGE DETAILS

Dimensions are shown thus : mm (in)