PLESSEY
SEMICONDUCTORS

SP1600 SERIES
ECL III

SP1674B (HIGH Z)
SP1675B (LOW Z)
TRIPLE 2-INPUT EXCLUSIVE-NOR GATE

This three gate array is designed to provide the positive logic Exclusive-NOR function in high speed applications. These devices contain a temperature compensated internal bias which insures that the threshold point remains in the centre of the transition region over the temperature range (0° to +75°). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

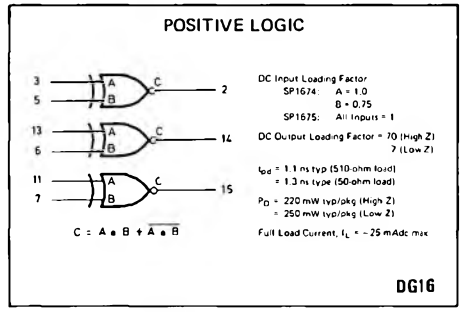

Fig. 1 Logic diagram of SP1674/1675

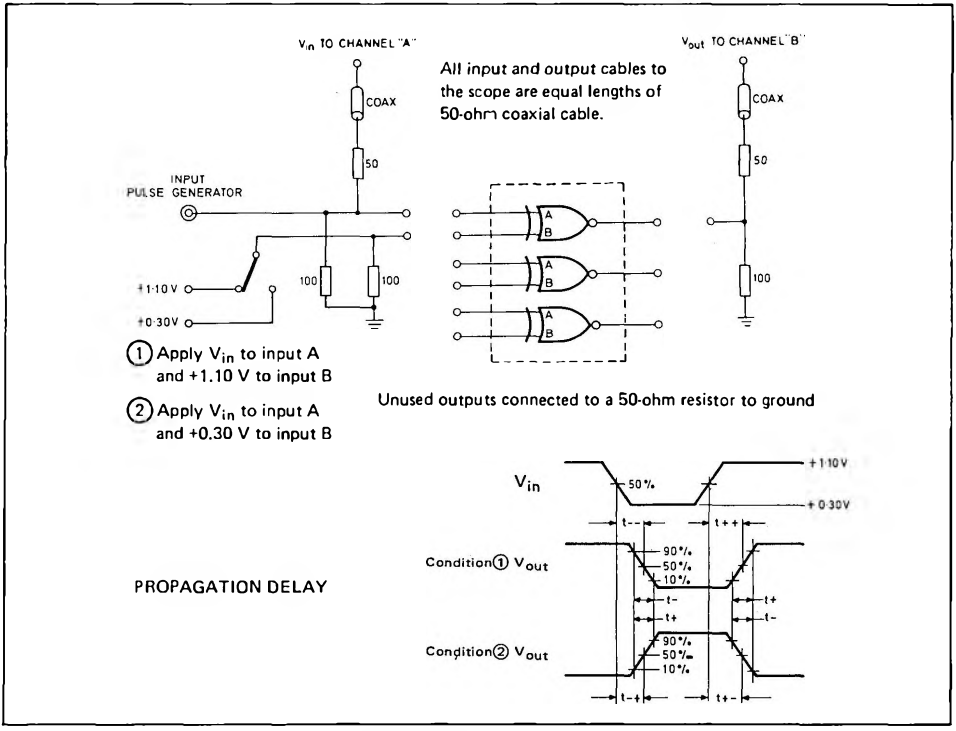

Fig. 2 Switching time test circuit and waveforms at +25°C

ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-14A2CB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is in either a test socket or is mounted on a printed circuit board. Outputs are tested with a 50-ohm resistor to −2.0 V.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
0°C	−0.840	−1.870	−1.135	−1.500	−5.2
+25°C	−0.810	−1.850	−1.095	−1.485	−5.2
+75°C	−0.720	−1.830	−1.035	−1.460	−5.2

Characteristic	Symbol	Pin Under Test	SP1674/SP1675 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75° Min	+75° Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	Gnd
Power Supply Drain Current	I_E (Hi-Z)	8	–	–	–	55	–	–	mAdc	All Inputs	–	–	–	8	1,16
	I_E (Lo-Z)	8	–	–	–	70	–	–	mAdc	All Inputs	–	–	–	8	1,16
Input Current (Hi-Z)	$I_{in\ H}$	3,11,13	–	–	–	350	–	–	μAdc	*	–	–	–	8	1,16
	0.75 $I_{in\ H}$	5,6,7	–	–	–	270	–	–	μAdc	*	–	–	–	8	1,16
	$I_{in\ L}$	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	8	1,16
Input Current (Lo-Z)	$I_{in\ H}$	*	–	–	–	3.1	–	–	mAdc	*	–	–	–	8	1,16
	$I_{in\ L}$	*	–	–	1.3	–	–	–	mAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	3,5	–	–	–	8	1,16
		2	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	–	3,5	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	Vdc	3,5	–	–	–	8	1,16
		2	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	Vdc	–	3.5	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	−1.020	–	−0.980	–	−0.920	–	Vdc	–	–	3,5	–	8	1,16
		2	−1.020	–	−0.980	–	−0.920	–	Vdc	–	–	–	3,5	8	1,16
Logic "0" Treshold Voltage	V_{OLA}	2	–	−1.615	–	−1.600	–	−1.575	Vdc	–	–	3	5	8	1,16
		2	–	−1.615	–	−1.600	–	−1.575	Vdc	–	–	5	3	8	1,16
Switching Times (50Ω Load)			Typ	Max	Typ	Max	Typ	Max				Pulse In	Pulse Out	−3.2V	+2.0V
Propagation Delay	t_{3+2+}	2	1.3	1.8	1.3	1.8	1.5	2.2	ns	–	–	3	2	8	1,16
	t_{3-2+}	2	1.3	1.8	1.3	1.8	1.5	2.2		–	–				
	t_{3+2-}	2	1.4	1.9	1.4	1.9	1.6	2.3		–	–				
	t_{3-2-}	2	1.4	1.9	1.4	1.9	1.6	2.3		–	–				
	t_{5+2+}	2	1.7	2.3	1.7	2.3	1.9	2.7		–	–	5			
	t_{5-2+}	2								–	–				
	t_{5+2-}	2								–	–				
	t_{5-2-}	2								–	–				
Rise Time	t_{2+}	2	1.9	2.5	1.9	2.5	2.1	2.8	ns	–	–	3	2	8	1,16
Fall Time	t_{2-}	2	1.6	2.2	1.6	2.2	1.8	2.5	ns	–	–	3	2	8	1,16

* Individually test each input applying V_{IH} or V_{IL} to input under test.