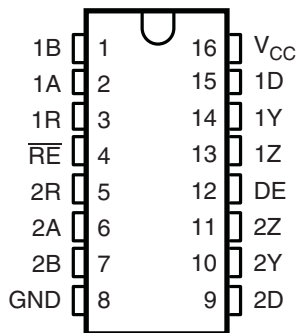


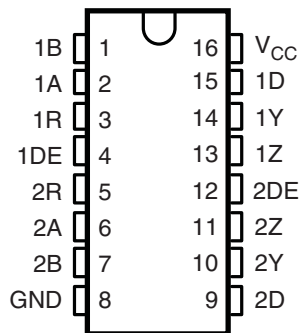
## FEATURES

- Meet or Exceed Standards TIA/EIA-422-B and ITU Recommendation V.11
- Operate From Single 5-V Power Supply
- Driver Positive and Negative Current Limiting
- Receiver Input Sensitivity:  $\pm 200\text{mV}$
- Receiver Input Impedance:  $12\text{ k}\Omega$  Min
- Driver 3-State Outputs
- Receiver 3-State Outputs (SN7534050 Only)

SN7534050...N OR NS PACKAGE  
(TOP VIEW)



SN7534051...N OR NS PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

The SN7534050 and SN7534051 dual differential drivers and receivers are monolithic integrated circuits designed to meet the requirements of ANSI standards TIA/EIA-422-B and ITU Recommendations V.11.

The driver outputs provide limiting for both positive and negative currents and thermal shutdown protection from line fault conditions on transmission bus line.

The SN7534050 combines dual 3-state differential drivers and dual 3-state differential input receivers. The drivers and receivers have active-high and active-low enables, respectively which can be externally connected together to function as direction control. SN7534051 drivers each have an individual active-high enable.

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1)(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–20°C to 85°C	PDIP – N	Tube of 25	SN7534050N	SN7534050N
		Reel of 1000	SN7534050NS	SN7534050
	SOP – NS	Reel of 2000	SN7534050NSR	SN7534050
		Tube of 25	SN7534051N	SN7534051N
	SOP – NS	Reel of 1000	SN7534051NS	SN7534051
		Reel of 2000	SN7534051NSR	SN7534051

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**FUNCTION TABLES**

**SN7534050, SN7534051**  
**Each Driver<sup>(1)</sup>**

INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

- (1) H = high level, L = low level,  
X = irrelevant, Z = high impedance (off)

**SN7534050**  
**Each Receiver<sup>(1)</sup>**

DIFFERENTIAL INPUTS, A–B	ENABLE RE	OUTPUT R
$V_{ID} \geq 0.2 \text{ V}$	L	H
$-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$	L	?
$V_{ID} \leq -0.2 \text{ V}$	L	L
X	H	Z

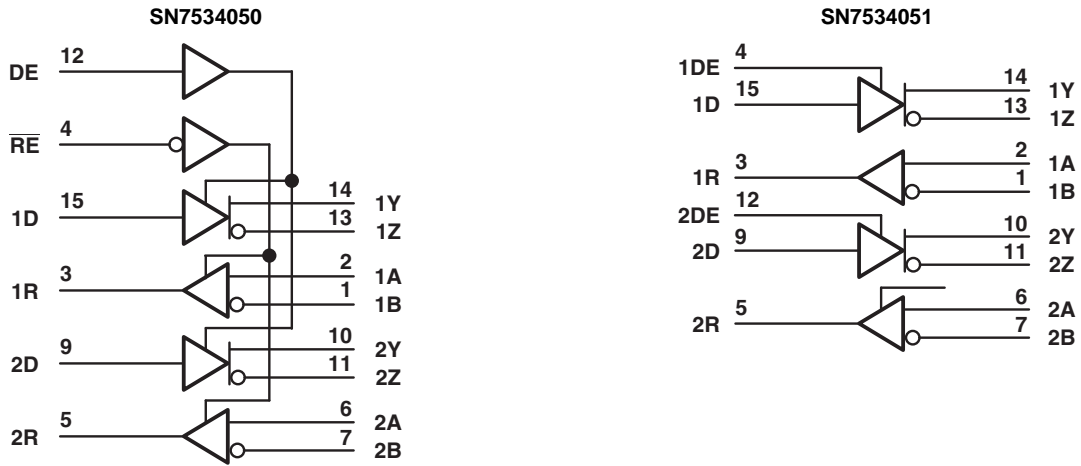
- (1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

**SN7534051**  
**Each Receiver<sup>(1)</sup>**

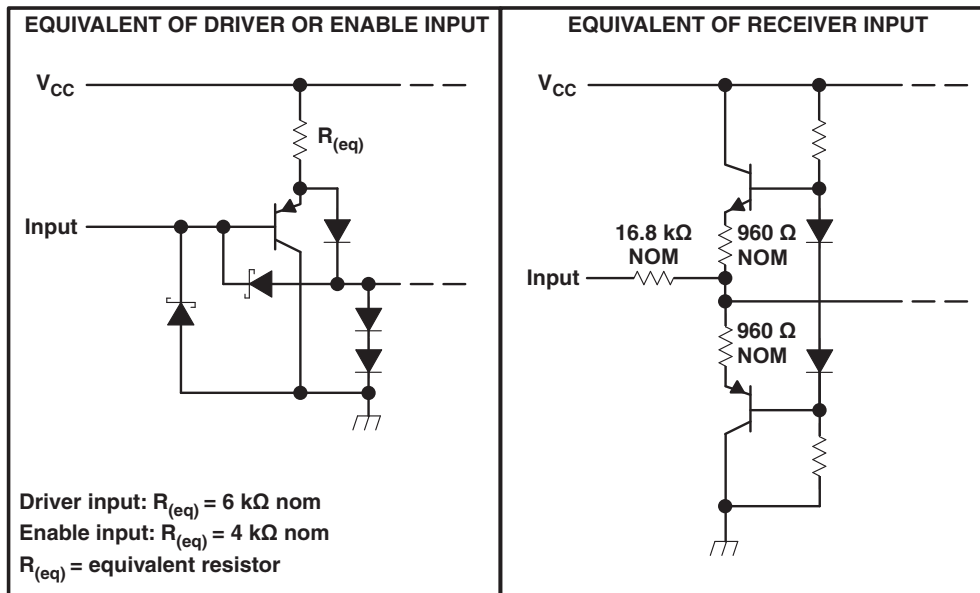
DIFFERENTIAL INPUTS, A–B	OUTPUT R
$V_{ID} \geq 0.2 \text{ V}$	H
$-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$	?
$V_{ID} \leq -0.2 \text{ V}$	L

- (1) H = high level, L = low level,  
? = indeterminate

**LOGIC DIAGRAMS**

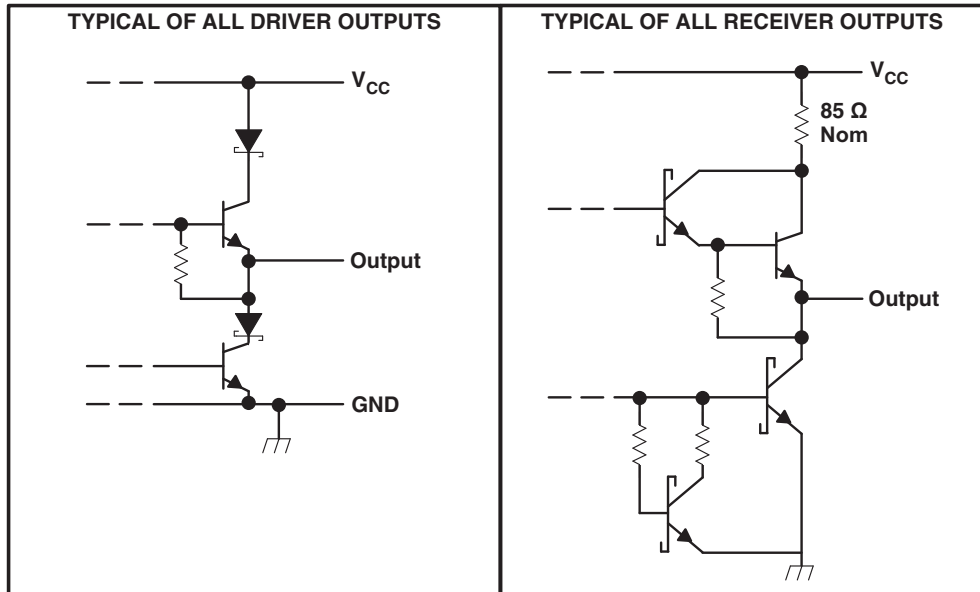


**SCHEMATIC OF INPUTS**



All resistor values are nominal.

**SCHEMATIC OF OUTPUTS**



All resistor values are nominal.

**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage <sup>(2)</sup>		7	V
V <sub>I</sub>	Input voltage	DE, $\overline{RE}$ , D inputs		7 V
V <sub>I</sub>	Receiver input voltage	A or B inputs		±25 V
V <sub>ID</sub>	Receiver differential output voltage <sup>(3)</sup>			±25 V
V <sub>O</sub>	Driver output voltage range	-10	15	V
I <sub>OL</sub>	Receiver low-level output current			50 mA
θ <sub>JA</sub>	Package thermal impedance <sup>(4)</sup>	N package		66 °C/W
		NS package		68 °C/W
Operating free-air temperature range		-20	85	°C
T <sub>stg</sub>	Storage temperature range	-65	150	°C
Lead temperature, 1.6 mm (1/16 in) from case for 10 s				260 °C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages, except differential input voltage, are with respect to the network GND.
- (3) Differential input voltage is measured at the noninverting terminal, with respect to the inverting terminal.
- (4) The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.75	5		V5.25
V <sub>IH</sub>	High-level input voltage	2			V
V <sub>IL</sub>	Low-level input voltage				
V <sub>IC</sub>	Common-mode input voltage <sup>(1)</sup>	Receiver		±7	V
V <sub>ID</sub>	Differential input voltage	Receiver		±12	V
I <sub>OH</sub>	High-level output current	Driver		40	mA
		Receiver		–400	μA
I <sub>OL</sub>	Low-level output current	Driver		–40	mA
		Receiver		16	
T <sub>A</sub>	Operating free-air temperature	–20		85	°C

(1) Refer to TIA/EIA-422-B for exact conditions.

## DRIVER SECTION

### Electrical Characteristics

over recommended supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = –20 mA		3.7		V
V <sub>OL</sub>	Low-level output voltage	V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 20 mA		1.1		V
V <sub>OD1</sub>	Differential output voltage	I <sub>O</sub> = 0 mA	1.5		6	V
V <sub>OD2</sub>	Differential output voltage <sup>(2)</sup>	R <sub>L</sub> = 100 Ω, See <a href="#">Figure 1</a>	2			V
ΔV <sub>OD</sub>	Change in magnitude of differential output voltage <sup>(2)</sup>	R <sub>L</sub> = 100 Ω, See <a href="#">Figure 1</a>			±0.4	V
V <sub>OC</sub>	Common-mode output voltage <sup>(2)</sup>	R <sub>L</sub> = 100 Ω, See <a href="#">Figure 1</a>			±3	V
ΔV <sub>OC</sub>	Change in magnitude of differential common-mode voltage <sup>(2)</sup>	R <sub>L</sub> = 100 Ω, See <a href="#">Figure 1</a>			±0.4	V
I <sub>off</sub>	Output current with power off <sup>(2)</sup>	V <sub>CC</sub> = 0 V	V <sub>O</sub> = 6 V		100	μA
			V <sub>O</sub> = –0.25 V		–100	
I <sub>OZ</sub>	High-impedance-state output current	V <sub>O</sub> = –0.25 V to 6 V			±100	μA
I <sub>IH</sub>	High-level input current	V <sub>I</sub> = 2.7 V			20	μA
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> = 0.4 V			–100	μA
I <sub>OS</sub>	Short-circuit output current <sup>(2)(3)</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND	–30		–150	mA
I <sub>CC</sub>	Supply current (total package)	No load	Output enabled		80	mA
			Output disabled		50	

(1) All typical values are at V<sub>CC</sub> = 5 V and T<sub>A</sub> = 25°C.

(2) Refer to TIA-EIA-422-B for exact conditions.

(3) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## Switching Characteristics

$V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$ Differential output delay time	$R_L = 100\ \Omega$ , $C_L = 50\text{ pF}$ , See <a href="#">Figure 3</a>		20	25	ns
$t_{t(OD)}$ Differential output transition time	$R_L = 100\ \Omega$ , $C_L = 50\text{ pF}$ , See <a href="#">Figure 3</a>		27	35	ns
$t_{PLH}$ Propagation delay time, low- to high-level output	$R_L = 27\ \Omega$ , See <a href="#">Figure 4</a>		20	25	ns
$t_{PHL}$ Propagation delay time, high- to low-level output	$R_L = 27\ \Omega$ , See <a href="#">Figure 4</a>		20	25	ns
$t_{PZH}$ Output enable time to high level	$R_L = 110\ \Omega$ , See <a href="#">Figure 5</a>		80	120	ns
$t_{PZL}$ Output enable time to low level	$R_L = 110\ \Omega$ , See <a href="#">Figure 6</a>		40	60	ns
$t_{PHZ}$ Output disable time from high level	$R_L = 110\ \Omega$ , See <a href="#">Figure 5</a>		90	120	ns
$t_{PLZ}$ Output disable time from low level	$R_L = 110\ \Omega$ , See <a href="#">Figure 6</a>		30	45	ns

## RECEIVER SECTION

### Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{IT+}$ Positive-going input threshold voltage, differential input				0.2	V
$V_{IT-}$ Negative-going input threshold voltage, differential input		-0.2 <sup>(2)</sup>			V
$V_{hys}$ Input hysteresis ( $V_{IT+} - V_{IT-}$ )			50		mV
$V_{IK}$ Input clamp voltage, $\overline{RE}$	SN7534050 $I_I = -18\text{ mA}$			-1.5	V
$V_{OH}$ High-level output voltage	$V_{ID} = 200\text{ mV}$ , $I_{OH} = -400\ \mu\text{A}$ , See <a href="#">Figure 2</a>		2.7		V
$V_{OL}$ Low-level output voltage	$V_{ID} = -200\text{ mV}$ , See <a href="#">Figure 2</a>			0.45 0.5	V
$I_{OZ}$ High-impedance-state output current	SN7534050 $V_O = 0.4\text{ V to }2.4\text{ V}$			$\pm 20$	$\mu\text{A}$
$I_I$ Line input current	Other input at 0 V			1.5 -2.5	mA
$I_{IH}$ High-level enable input current, $\overline{RE}$	SN7534050 $V_{IH} = 2.7\text{ V}$			20	$\mu\text{A}$
$I_{IL}$ Low-level enable input current, $\overline{RE}$	SN7534050 $V_{IL} = 0.4\text{ V}$			-100	$\mu\text{A}$
$r_I$ Input resistance			12		k $\Omega$
$I_{OS}$ Short circuit output current			-15	-85	mA
$I_{CC}$ Supply current (total package)	No load, enabled		80	110	mA

(1) All typical values are at  $V_{CC} = 5\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

(2) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels.

### Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ Propagation delay time, low- to high-level output	$V_{ID} = 1.5\text{ V}$ , $C_L = 15\text{ pF}$ , See <a href="#">Figure 7</a>		20	35	ns
$t_{PHL}$ Propagation delay time, high- to low-level output	$V_{ID} = 1.5\text{ V}$ , $C_L = 15\text{ pF}$ , See <a href="#">Figure 7</a>		22	35	ns
$t_{PZH}$ Output enable time to high level	SN7534050 $C_L = 15\text{ pF}$ , see <a href="#">Figure 8</a>		17	25	ns
$t_{PZL}$ Output enable time to low level	SN7534050 $C_L = 15\text{ pF}$ , See <a href="#">Figure 8</a>		20	27	ns
$t_{PHZ}$ Output disable time from high level	SN7534050 $C_L = 15\text{ pF}$ , See <a href="#">Figure 8</a>		25	40	ns
$t_{PLZ}$ Output disable time from low level	SN7534050 $C_L = 15\text{ pF}$ , See <a href="#">Figure 8</a>		30	40	ns

PARAMETER MEASUREMENT INFORMATION

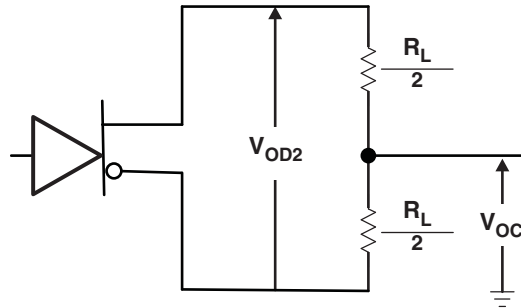


Figure 1. Driver Test Circuit,  $V_{OD}$  and  $V_{OC}$

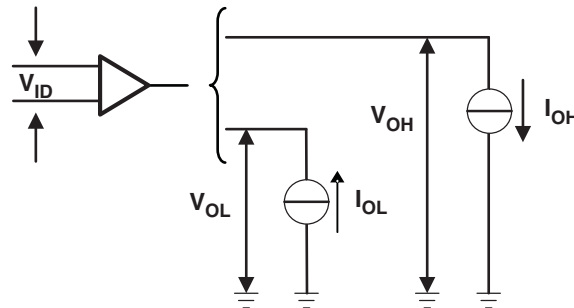
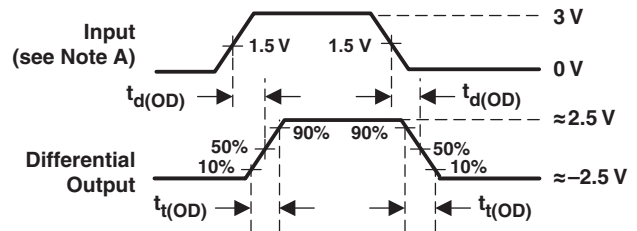
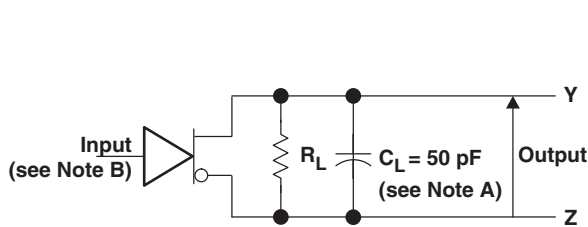


Figure 2. Receiver Test Circuit,  $V_{OH}$  and  $V_{OL}$

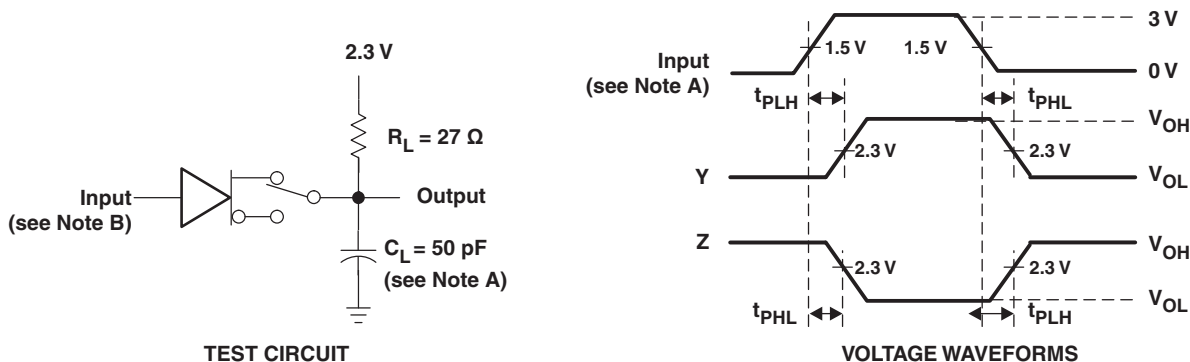


TEST CIRCUIT

- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics:  $PRR \leq 1$  MHz, duty cycle = 50%,  $t_r = t_f \leq 6$  ns.

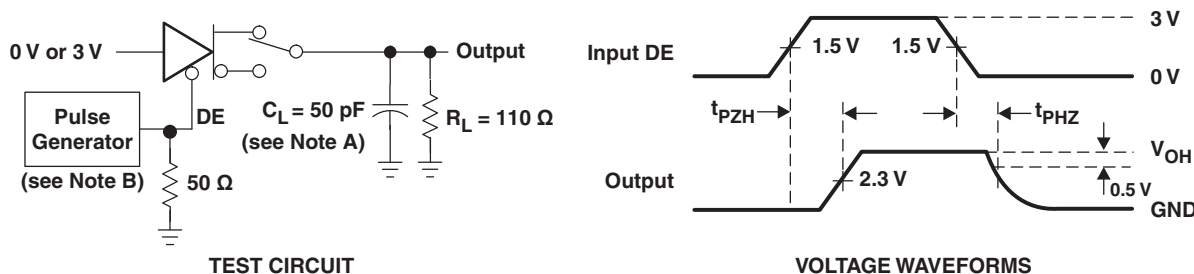
Figure 3. Driver Test Circuit and Voltage Waveforms,  $t_{d(OD)}$  and  $t_{t(OD)}$

PARAMETER MEASUREMENT INFORMATION (continued)



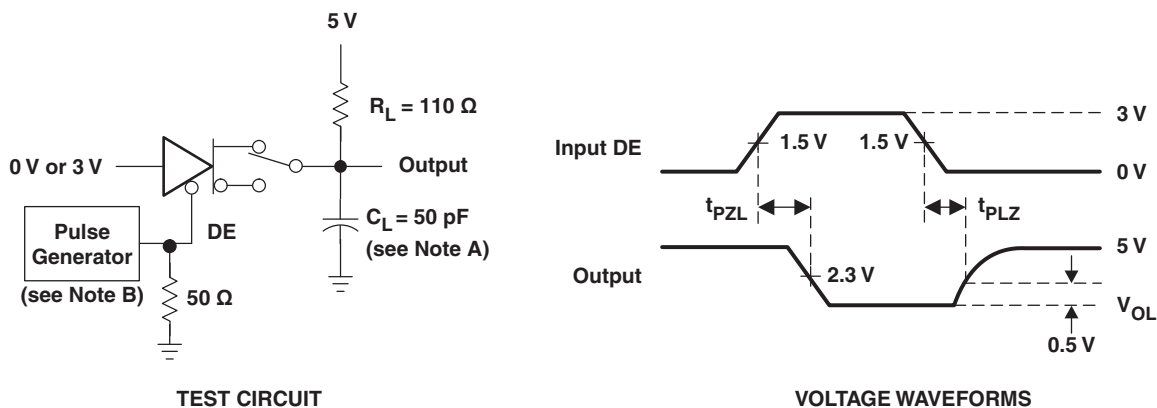
- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR  $\leq$  1 MHz, duty cycle = 50%,  $t_r = t_f \leq$  6 ns.

Figure 4. Driver Test Circuit and Voltage Waveforms,  $t_{PLH}$  and  $t_{PHL}$



- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR  $\leq$  1 MHz, duty cycle = 50%,  $t_r = t_f \leq$  6 ns.

Figure 5. Driver Test Circuit and Voltage Waveforms,  $t_{PZH}$  and  $t_{PHZ}$

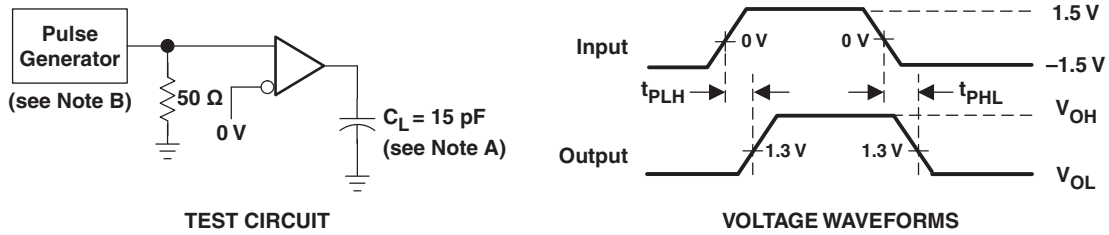


- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR  $\leq$  1 MHz, duty cycle = 50%,  $t_r = t_f \leq$  6 ns.

Figure 6. Driver Test Circuit and Voltage Waveforms,  $t_{PZL}$  and  $t_{PLZ}$

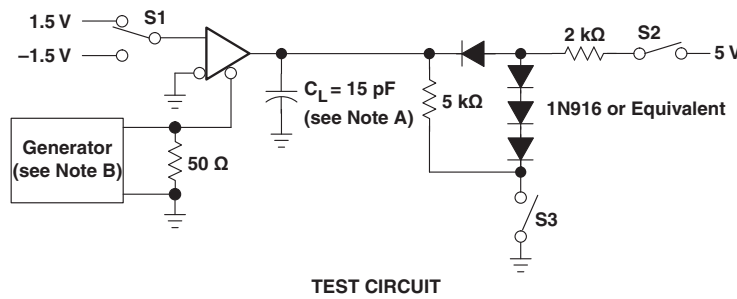


PARAMETER MEASUREMENT INFORMATION (continued)



- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR  $\leq$  1 MHz, duty cycle = 50%,  $t_r = t_f \leq$  6 ns.

Figure 7. Receiver Test Circuit and Voltage Waveforms,  $t_{PLH}$  and  $t_{PHL}$



- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR  $\leq$  1 MHz, duty cycle = 50%,  $t_r = t_f \leq$  6 ns.

Figure 8. Receiver Test Circuit and Voltage Waveforms,  $t_{PZH}$ ,  $t_{PZL}$ ,  $t_{PHZ}$ ,  $t_{PLZ}$  (SN7534050)

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN7534050N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN7534050NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN7534050NS	ACTIVE	SO	NS	16	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN7534050NSE4	ACTIVE	SO	NS	16	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN7534050NSG4	ACTIVE	SO	NS	16	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN7534050NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN7534050NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN7534050NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN7534051N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN7534051NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN7534051NS	ACTIVE	SO	NS	16	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN7534051NSE4	ACTIVE	SO	NS	16	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN7534051NSG4	ACTIVE	SO	NS	16	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN7534051NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN7534051NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN7534051NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN7534050NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN7534051NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN7534050NSR	SO	NS	16	2000	346.0	346.0	33.0
SN7534051NSR	SO	NS	16	2000	346.0	346.0	33.0

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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