

SN75161B, SN75162B

OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVERS

SLLS005B – OCTOBER 1980 – REVISED MAY 1995

- Meets IEEE Standard 488-1978 (GPIB)
- 8-Channel Bidirectional Transceivers
- Power-Up/Power-Down Protection (Glitch Free)
- Designed to Implement Control Bus Interface
- SN75161B Designed for Single Controller
- SN75162B Designed for Multiple Controllers
- High-Speed, Low-Power Schottky Circuitry
- Low Power Dissipation . . . 72 mW Max Per Channel
- Fast Propagation Times . . . 22 ns Max
- High-Impedance pnp Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device Is Powered Down ($V_{CC} = 0$)

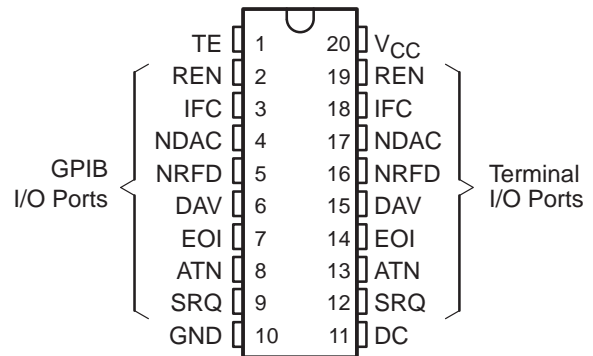
description

The SN75161B and SN75162B eight-channel, general-purpose interface bus transceivers are monolithic, high-speed, low-power Schottky devices designed to meet the requirements of IEEE Standard 488-1978. Each transceiver is designed to provide the bus-management and data-transfer signals between operating units of a single- or multiple-controller instrumentation system. When combined with the SN75160B octal bus transceiver, the SN75161B or SN75162B provides the complete 16-wire interface for the IEEE-488 bus.

The SN75161B and SN75162B feature eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. A power-up/-down disable circuit is included on all bus and receiver outputs. This provides glitch-free operation during V_{CC} power up and power down.

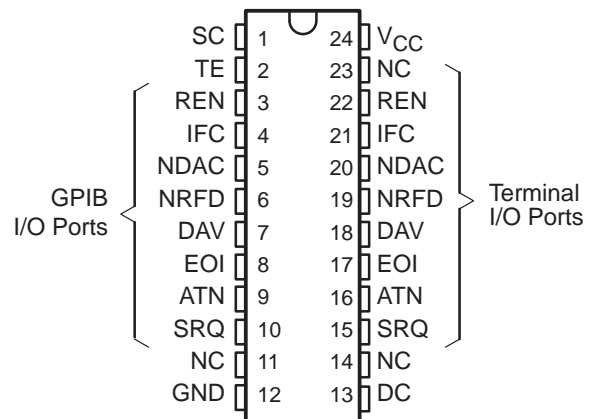
SN75161B . . . DW OR N PACKAGE

(TOP VIEW)



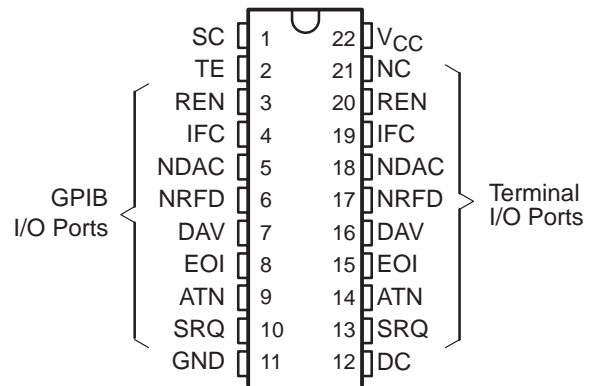
SN75162B . . . DW PACKAGE

(TOP VIEW)



SN75162B . . . N PACKAGE

(TOP VIEW)



NC—No internal connection



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description (continued)

The direction of data through these driver-receiver pairs is determined by the DC, TE, and SC (on SN75162B) enable signals. The SC input on the SN75162B allows the REN and IFC transceivers to be controlled independently.

The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when supply voltage V_{CC} is 0. The drivers are designed to handle loads up to 48 mA of sink current. Each receiver features pnp transistor inputs for high input impedance and hysteresis of 400 mV for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

The SN75161B and SN75162B are characterized for operation from 0°C to 70°C.

Function Tables

SN75161B RECEIVE/TRANSMIT

CONTROLS			BUS-MANAGEMENT CHANNELS				DATA-TRANSFER CHANNELS			
DC	TE	ATN†	ATN†	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
				(Controlled by DC)				(Controlled by TE)		
H	H	H	R	T	R	R	T	T	R	R
H	H	L					R			
L	L	H	T	R	T	T	R	R	T	T
L	L	L					T			
H	L	X	R	T	R	R	R	T	T	T
L	H	X	T	R	T	T	T	T	R	R

H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

† ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

SN75162B RECEIVE/TRANSMIT

CONTROLS				BUS-MANAGEMENT CHANNELS				DATA-TRANSFER CHANNELS				
SC	DC	TE	ATN†	ATN†	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD	
				(Controlled by DC)		(Controlled by SC)			(Controlled by TE)			
	H	H	H	R	T			T	T	R	R	
	H	H	L					R				
	L	L	H	T	R			R	R	T	R	T
	L	L	L					T				
	H	L	X	R	T			R	R	T	T	T
	L	H	X	T	R			R	T	T	R	R
H						T	T					
L						R	R					

H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

† ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.



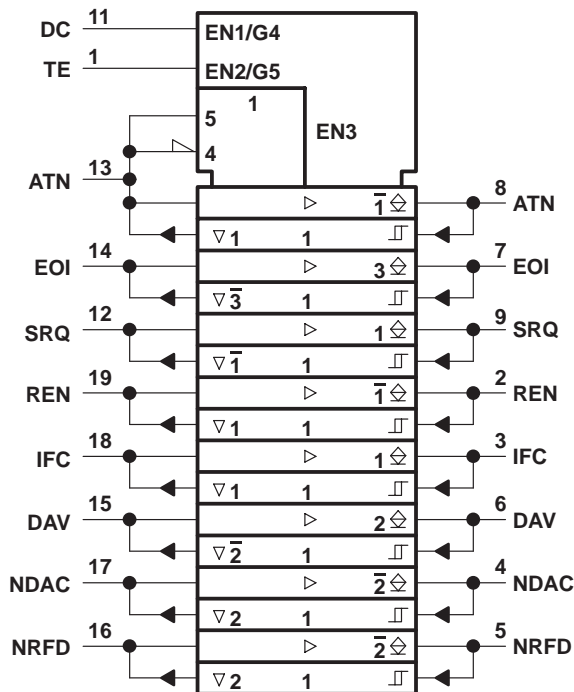
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CHANNEL-IDENTIFICATION TABLE

NAME	IDENTITY	CLASS
DC	Direction Control	Control
TE	Talk Enable	
SC	System Control (SN75162B only)	
ATN	Attention	
SRQ	Service Request	
REN	Remote Enable	Bus Management
IFC	Interface Clear	
EOI	End of Identity	Data Transfer
DAV	Data Valid	
NDAC	Not Data Accepted	
NRFD	Not Ready for Data	

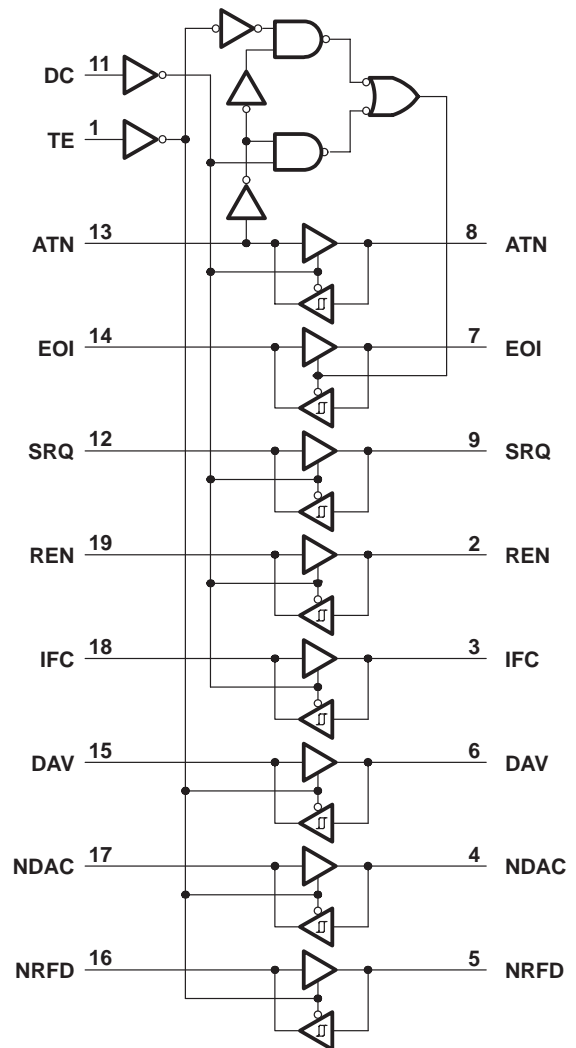
SN75161B logic symbol†



† This symbol is in accordance with IEEE Std 91-1984 and IEC Publication 617-12.

- ▽ Designates 3-state outputs
- ◇ Designates passive-pullup outputs

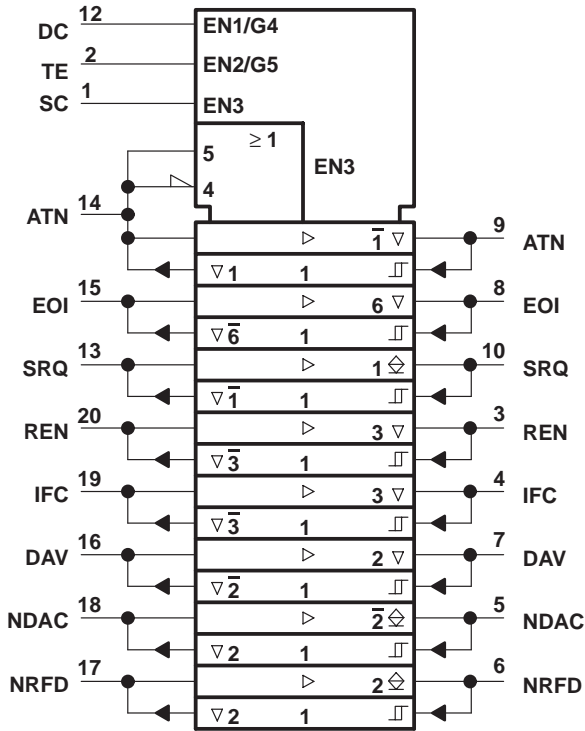
SN75161B logic diagram (positive logic)



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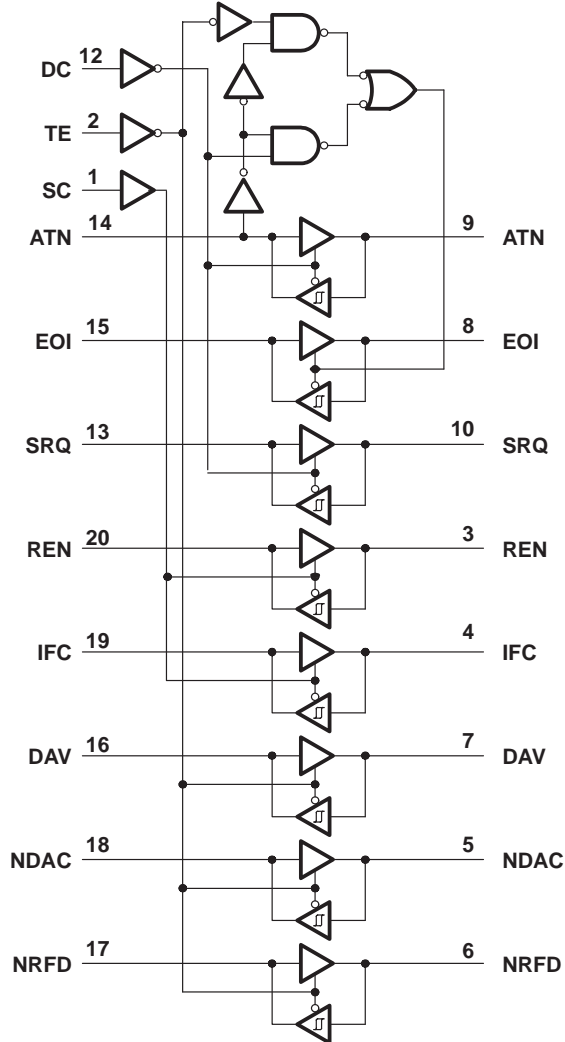
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SN75162B logic symbol†



†This symbol is in accordance with IEEE Std 91-1984 and IEC Publication 617-12.
 ∇ Designates 3-state outputs
 ⊕ Designates passive-pullup outputs

SN75162B logic diagram (positive logic)

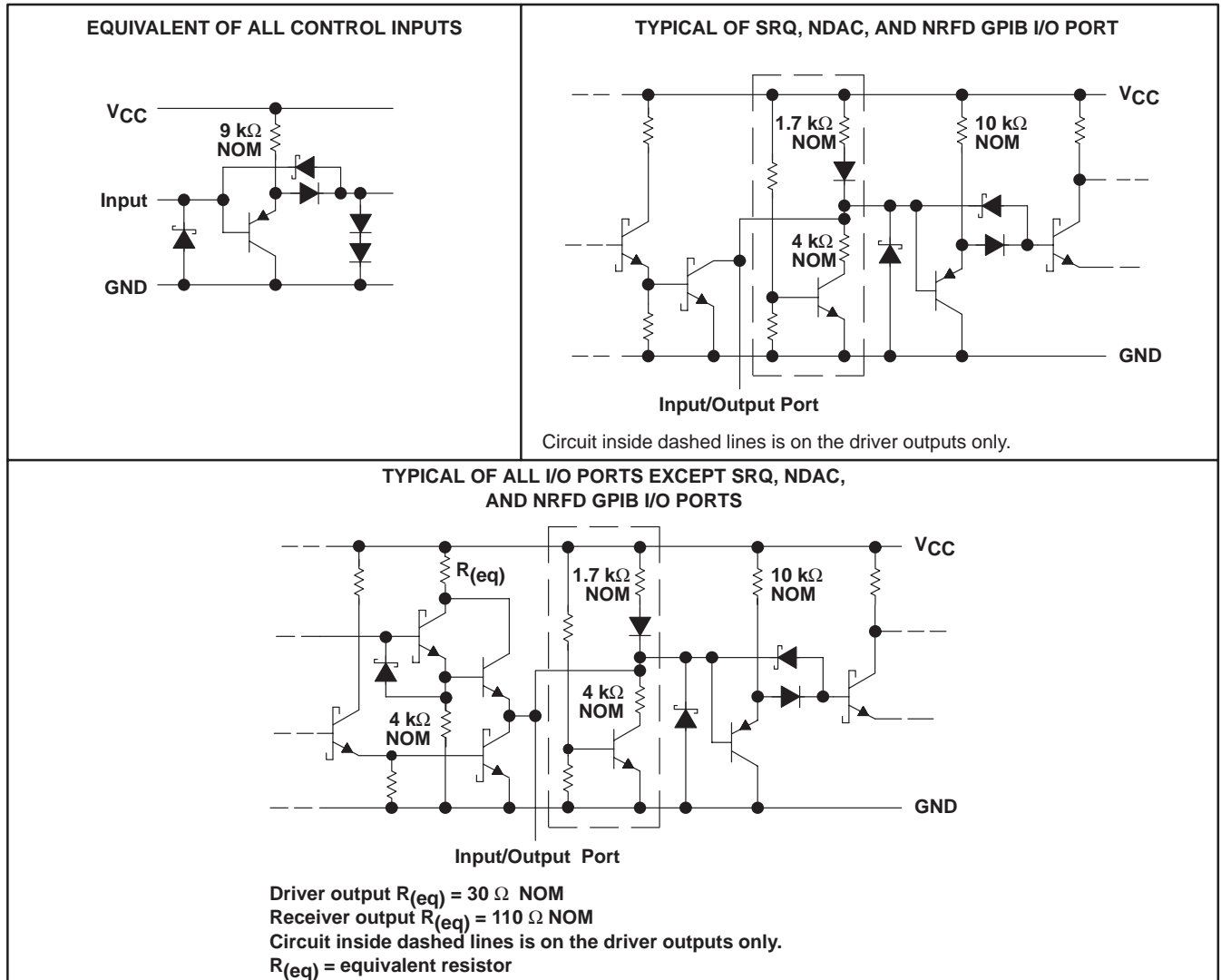


Pin numbers shown are for the N package.

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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I	5.5 V
Low-level driver output current, I_{OL}	100 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

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DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
DW (20 pin)	1125 mW	9.0 mW/°C	720 mW
DW (24 pin)	1350 mW	10.8 mW/°C	864 mW
N (20 pin)	1150 mW	9.2 mW/°C	736 mW
N (22 pin)	1700 mW	13.6 mW/°C	1088 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}		0.8			V
High-level output current, I_{OH}	Bus ports with 3-state outputs	-5.2			mA
	Terminal ports	-800			μA
Low-level output current, I_{OL}	Bus ports	48			mA
	Terminal ports	16			
Operating free-air temperature, T_A		0	70		°C



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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
V_{IK}	Input clamp voltage	$I_I = -18 \text{ mA}$	-0.8	-1.5		V	
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)	Bus See Figure 7	0.4	0.65		V	
$V_{OH}‡$	High-level output voltage	Terminal	$I_{OH} = -800 \mu\text{A}$			V	
		Bus	$I_{OH} = -5.2 \text{ mA}$				
V_{OL}	Low-level output voltage	Terminal	$I_{OL} = 16 \text{ mA}$		0.3	V	
		Bus	$I_{OL} = 48 \text{ mA}$		0.35		
I_I	Input current at maximum input voltage	Terminal $V_I = 5.5 \text{ V}$		0.2	100	μA	
I_{IH}	High-level input current	Terminal and control inputs $V_I = 2.7 \text{ V}$		0.1	20	μA	
I_{IL}	Low-level input current		$V_I = 0.5 \text{ V}$		-10	-100	μA
$V_{I/O(\text{bus})}$	Voltage at bus port	Driver disabled	$I_{I(\text{bus})} = 0$	2.5	3.0	3.7	V
			$I_{I(\text{bus})} = -12 \text{ mA}$			-1.5	
$I_{I/O(\text{bus})}$	Current into bus port	Power on	Driver disabled	$V_{I(\text{bus})} = -1.5 \text{ V to } 0.4 \text{ V}$	-1.3		mA
				$V_{I(\text{bus})} = 0.4 \text{ V to } 2.5 \text{ V}$	0	-3.2	
				$V_{I(\text{bus})} = 2.5 \text{ V to } 3.7 \text{ V}$		-3.2	
				$V_{I(\text{bus})} = 3.7 \text{ V to } 5 \text{ V}$	0	2.5	
				$V_{I(\text{bus})} = 5 \text{ V to } 5.5 \text{ V}$	0.7	2.5	
		Power off	$V_{CC} = 0, V_{I(\text{bus})} = 0 \text{ V to } 2.5 \text{ V}$		-40	μA	
I_{OS}	Short-circuit output current	Terminal		-15	-35	-75	mA
		Bus		-25	-50	-125	
I_{CC}	Supply current	No load, TE, DE, and SC low			110	mA	
$C_{I/O(\text{bus})}$	Bus-port capacitance	$V_{CC} = 5 \text{ V to } 0, V_{I/O} = 0 \text{ to } 2 \text{ V}, f = 1 \text{ MHz}$		16		pF	

† All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

‡ V_{OH} applies for 3-state outputs only.

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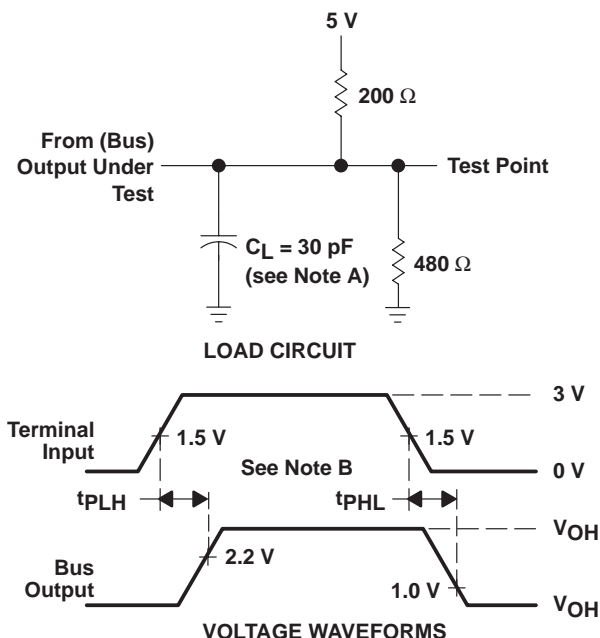
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switching characteristics, $V_{CC} = 5\text{ V}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	Terminal	Bus	C _L = 30 pF, See Figure 1		14	20	ns
t _{PHL}	Propagation delay time, high- to low-level output					14	20	
t _{PLH}	Propagation delay time, low- to high-level output	Terminal	Bus (SRQ, NDAC, NRFD)	C _L = 30 pF, See Figure 1		29	35	ns
t _{PLH}	Propagation delay time, low- to high-level output	Bus	Terminal	C _L = 30 pF, See Figure 2		10	20	ns
t _{PHL}	Propagation delay time, high- to low-level output					15	22	
t _{PZH}	Output enable time to high level	TE,DC, or SC	Bus (ATN, EOI, REN, IFC, and DAV)	See Figure 3			60	ns
t _{PHZ}	Output disable time from high level						45	
t _{PZL}	Output enable time to low level						60	
t _{PLZ}	Output disable time from low level						55	
t _{PZH}	Output enable time to high level	TE,DC, or SC	Terminal	See Figure 4			55	ns
t _{PHZ}	Output disable time from high level						50	
t _{PZL}	Output enable time to low level						45	
t _{PLZ}	Output disable time from low level						55	

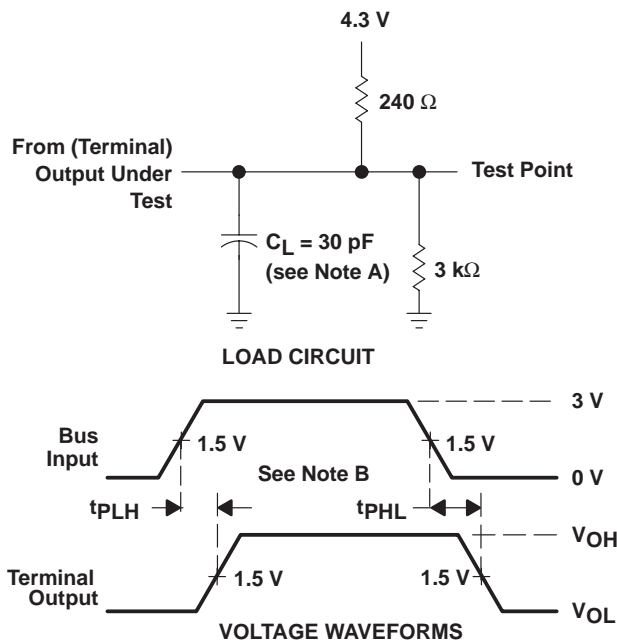


PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_O = 50 \Omega$.

Figure 1. Terminal-to-Bus Load Circuit and Voltage Waveforms



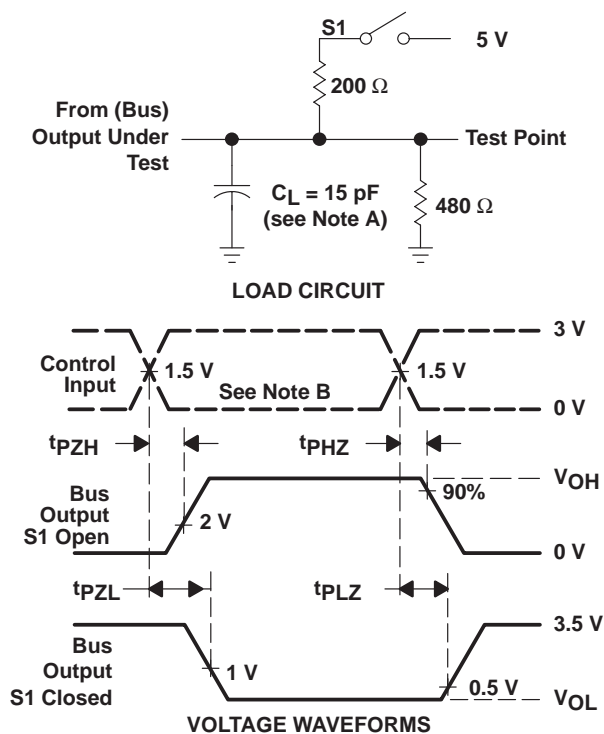
- NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_O = 50 \Omega$.

Figure 2. Bus-to-Terminal Load Circuit and Voltage Waveforms

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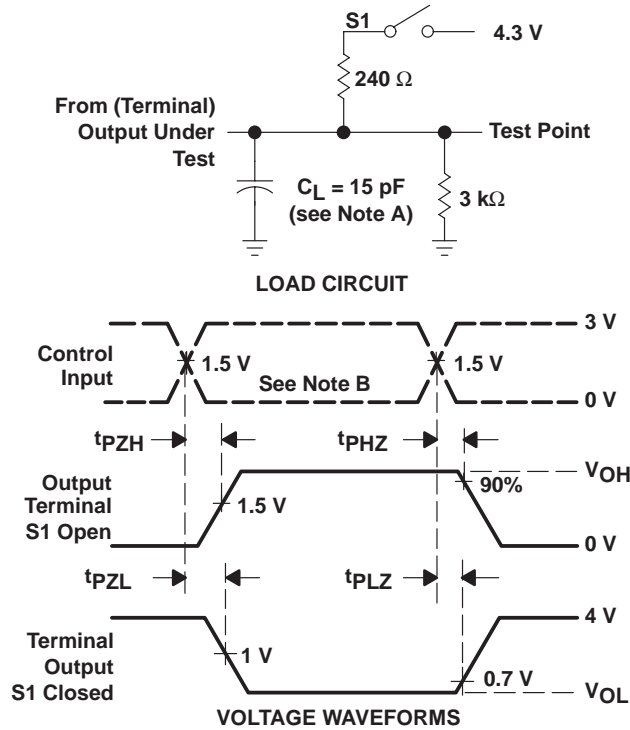
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 3. Bus Enable and Disable Times Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. The Input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 4. Terminal Enable and Disable Times Load Circuit and Voltage Waveforms

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TYPICAL CHARACTERISTICS

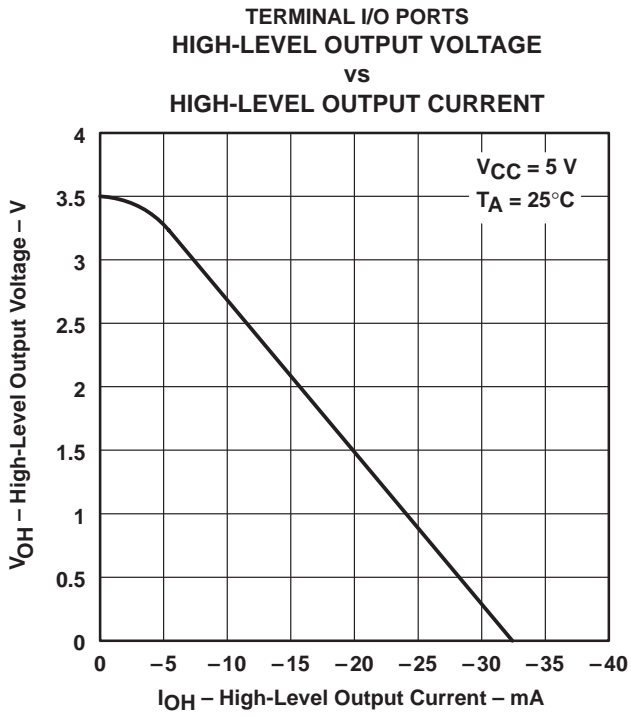


Figure 5

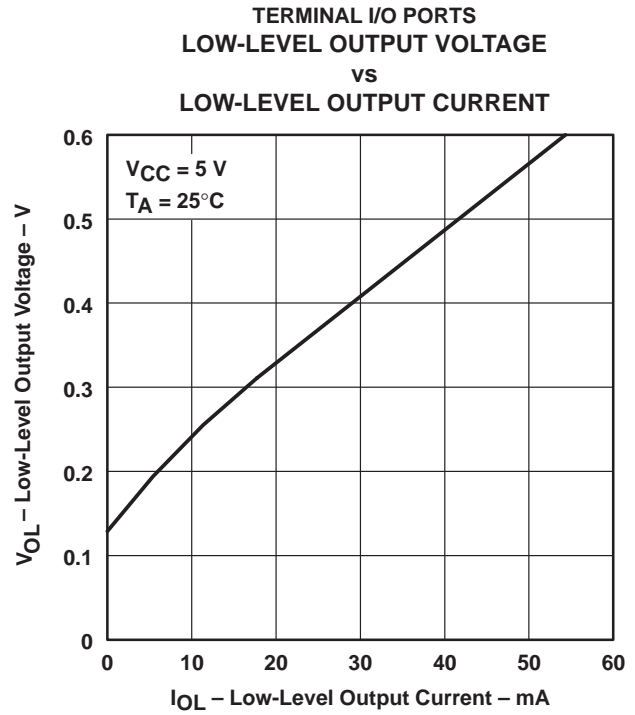


Figure 6

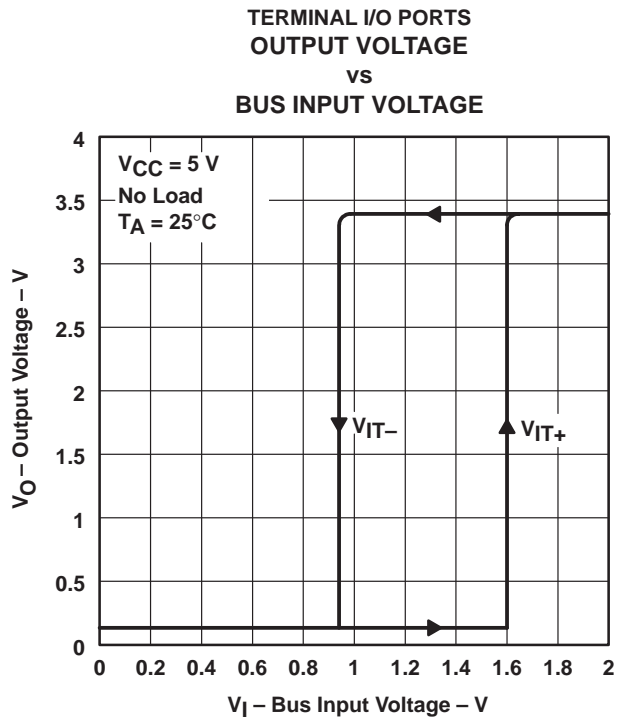


Figure 7



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TYPICAL CHARACTERISTICS

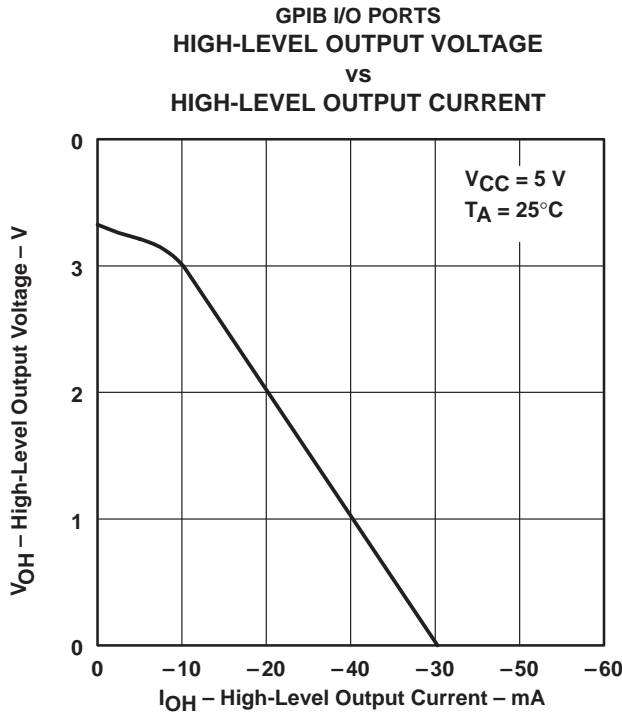


Figure 8

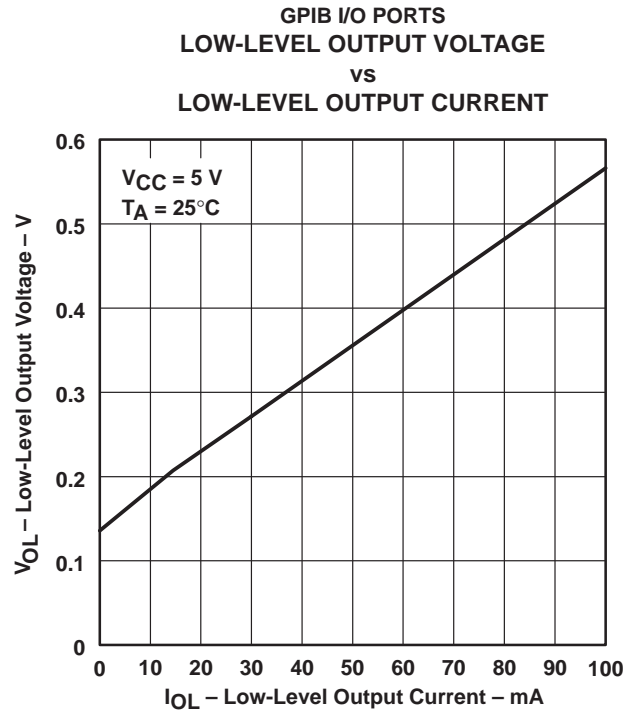


Figure 9

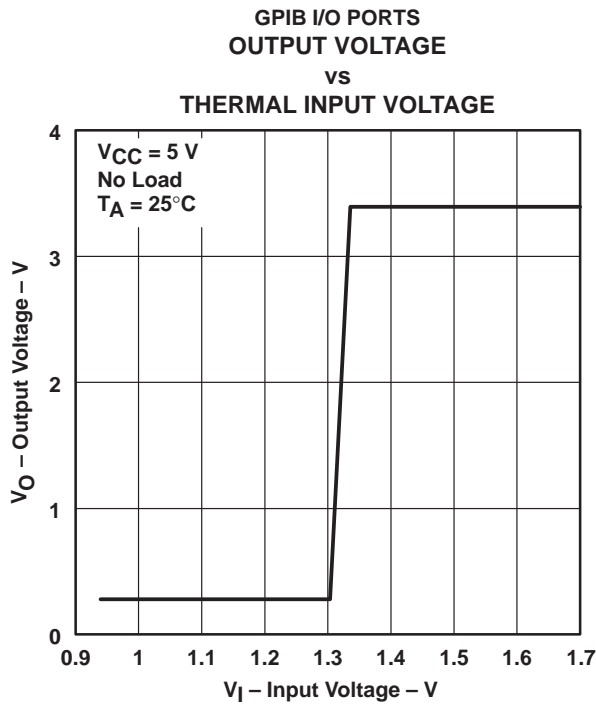


Figure 10

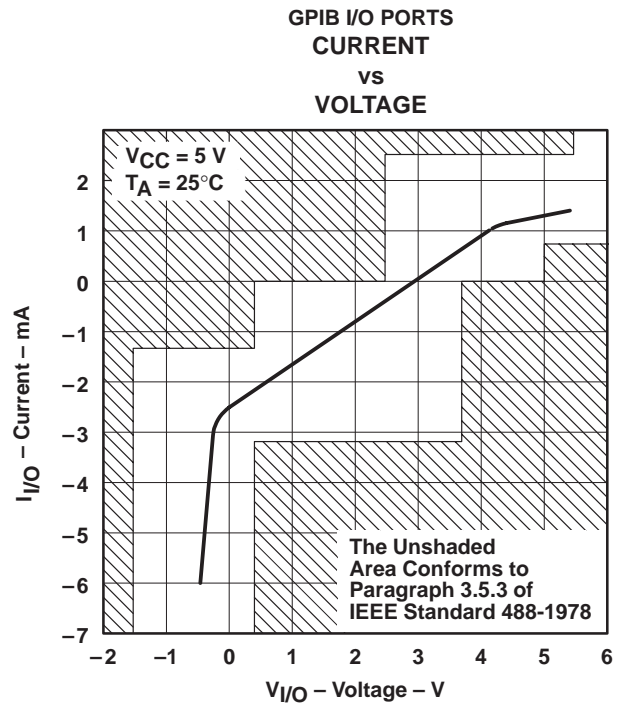


Figure 11

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