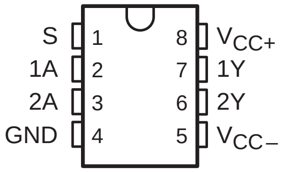
- **Meets or Exceeds the Requirement of TIA/EIA-232-F and ITU Recommendation V.28**
- **Withstands Sustained Output Short Circuit to Any Low-Impedance Voltage Between –25 V and 25 V**
- **2-µs Maximum Transition Time Through the 3-V to –3-V Transition Region Under Full 2500-pF Load**
- **Inputs Compatible With Most TTL Families**
- **Common Strobe Input**
- **Inverting Output**
- **Slew Rate Can Be Controlled With an External Capacitor at the Output**
- **Standard Supply Voltages . . . ±12 V**

D OR P PACKAGE
(TOP VIEW)

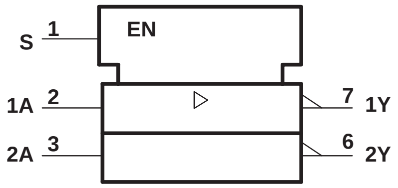


description

The SN75150 is a monolithic dual line driver designed to satisfy the requirements of the standard interface between data-terminal equipment and data-communication equipment as defined by TIA/EIA-232-F. A rate of 20 kbits/s can be transmitted with a full 2500-pF load. Other applications are in data-transmission systems using relatively short single lines, in level translators, and for driving MOS devices. The logic input is compatible with most TTL families. Operation is from 12-V and –12-V power supplies.

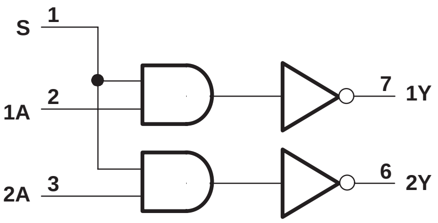
The SN75150 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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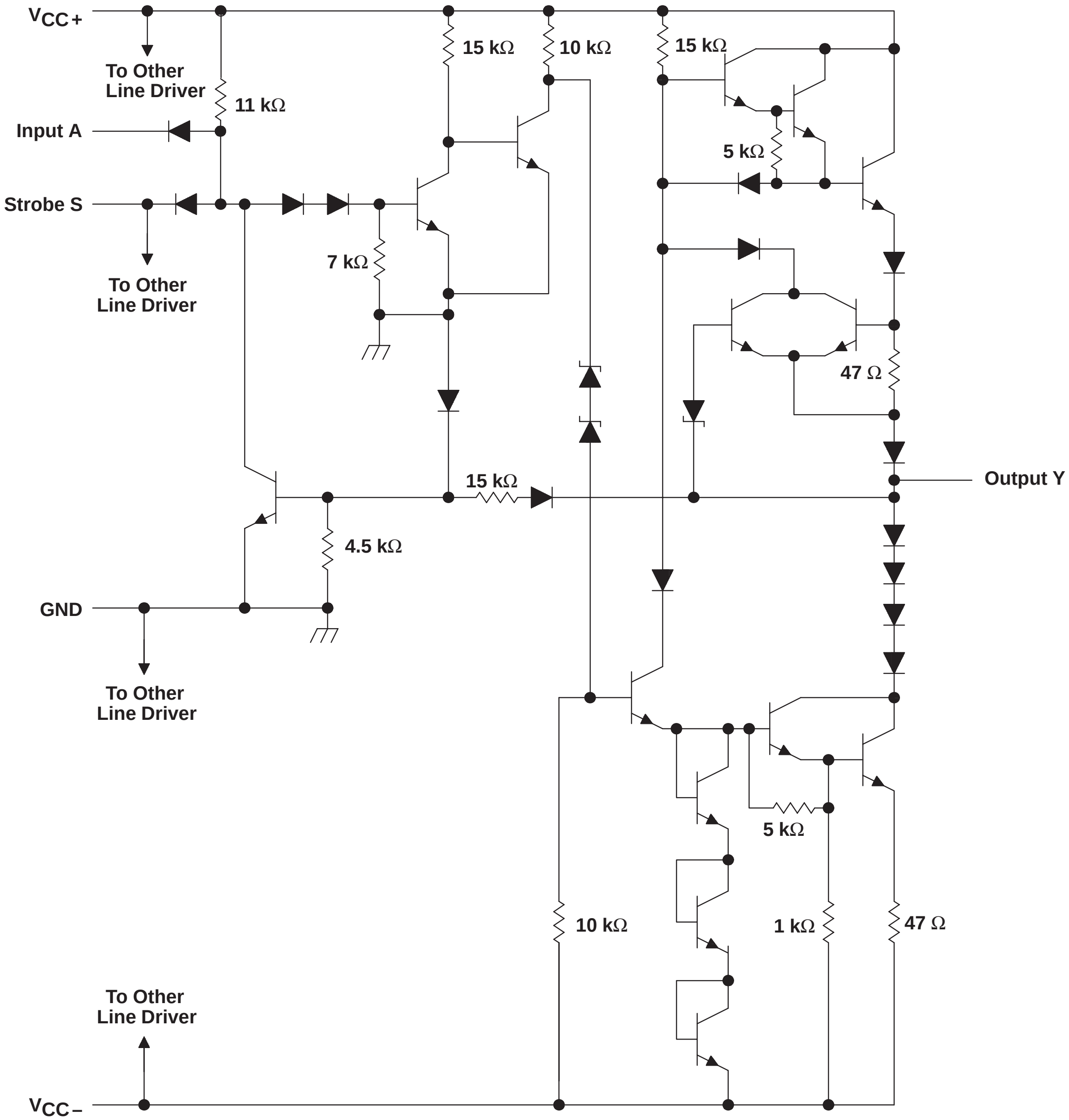
schematic (each line driver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) . . . . 15 V
Supply voltage, V_{CC-} . . . . –15 V
Input voltage, V_I . . . . 15 V
Applied output voltage . . . . ±25 V
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package . . . . 197°C/W
P package . . . . 104°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage	V_{CC+}	10.8	12	13.2	V
	V_{CC-}	–10.8	–12	–13.2	
High-level input voltage, V_{IH}		2		5.5	V
Low-level input voltage, V_{IL}		0		0.8	V
Driver output voltage, V_O				±15	V
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature range, $V_{CC\pm} = \pm 13.2$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP[†]	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC+} = 10.8 V, V_{CC-} = –10.8 V, V_{IL} = 0.8 V, R_L = 3 kΩ to 7 kΩ	5	8		V
V_{OL}	Low-level output voltage (see Note 4)		V_{CC+} = 10.8 V, V_{CC-} = –10.8 V, V_{IH} = 2 V, R_L = 3 kΩ to 7 kΩ		–8	–5	V
I_{IH}	High-level input current	Data input	V_I = 2.4 V		1	10	µA
		Strobe input			2	20	
I_{IL}	Low-level input current	Data input	V_I = 0.4 V		–1	–1.6	mA
		Strobe input			–2	–3.2	
I_{OS}	Short-circuit output current[‡]		V_O = 25 V		2	8	mA
			V_O = –25 V		–3	–8	
			V_O = 0, V_I = 3 V	10	15	30	
			V_O = 0, V_I = 0	–10	–15	–30	
I_{CCH+}	Supply current from V_{CC+}, high-level output		V_I = 0, R_L = 3 kΩ, T_A = 25°C		10	22	mA
I_{CCH-}	Supply current from V_{CC-}, high-level output				–1	–10	mA
I_{CCL+}	Supply current from V_{CC+}, low-level output		V_I = 3 V, R_L = 3 kΩ, T_A = 25°C		8	17	mA
I_{CCL-}	Supply current from V_{CC-}, low-level output				–9	–20	mA

[†] All typical values are at V_{CC+} = 12 V, V_{CC-} = –12 V, T_A = 25°C.

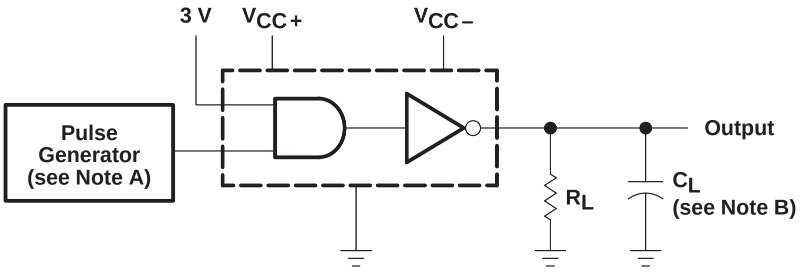
[‡] Not more than one output should be shorted at a time.

NOTE 4: The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic levels only, e.g., when –5 V is the maximum, the typical value is a more negative voltage.

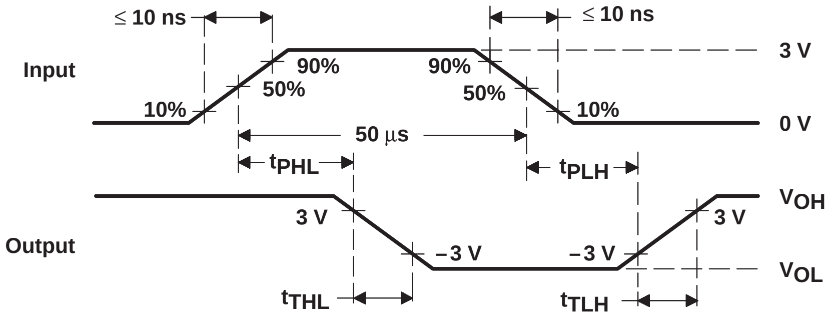
switching characteristics, V_{CC+} = 12 V, V_{CC-} = –12 V, T_A = 25°C (see Figure 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{TLH}	Transition time, low-to-high-level output	C_L = 2500 pF, R_L = 3 kΩ to 7 kΩ	0.2	1.4	2	µs
t_{THL}	Transition time, high-to-low-level output		0.2	1.5	2	µs
t_{TLH}	Transition time, low-to-high-level output	C_L = 15 pF, R_L = 7 kΩ		40		ns
t_{THL}	Transition time, high-to-low-level output			20		ns
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 7 kΩ		60		ns
t_{PHL}	Propagation delay time, high-to-low-level output			45		ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 50%, Z_O ≈ 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT CURRENT
vs
APPLIED OUTPUT VOLTAGE

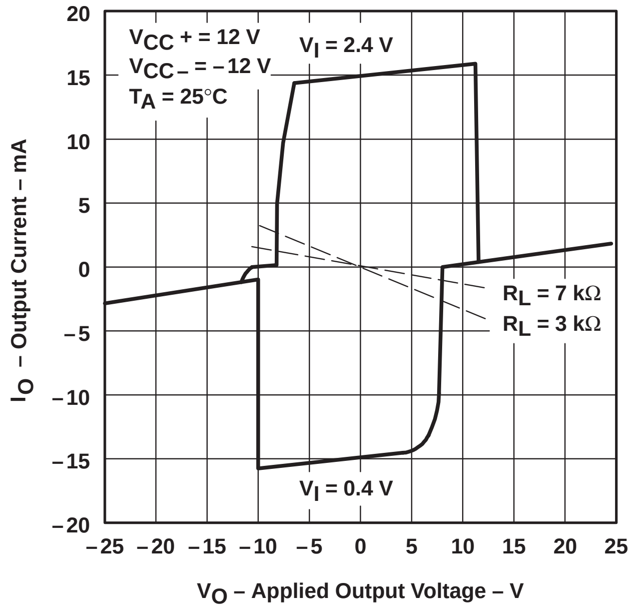


Figure 2

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN75150D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75150DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75150DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75150DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75150DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75150DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75150JG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
SN75150P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75150PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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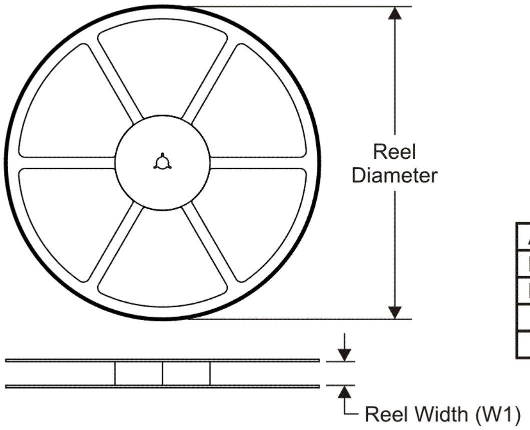
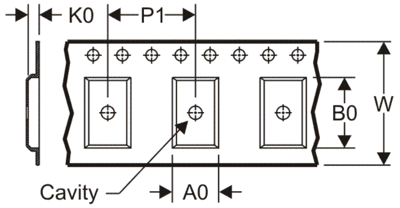
TAPE AND REEL INFORMATION

REEL DIMENSIONS

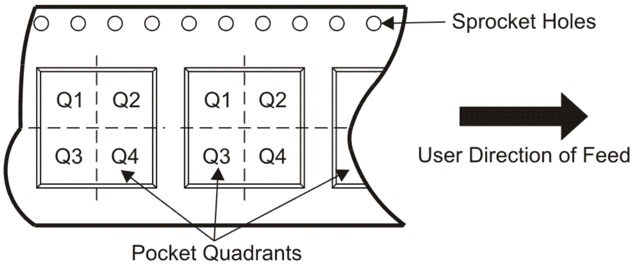


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

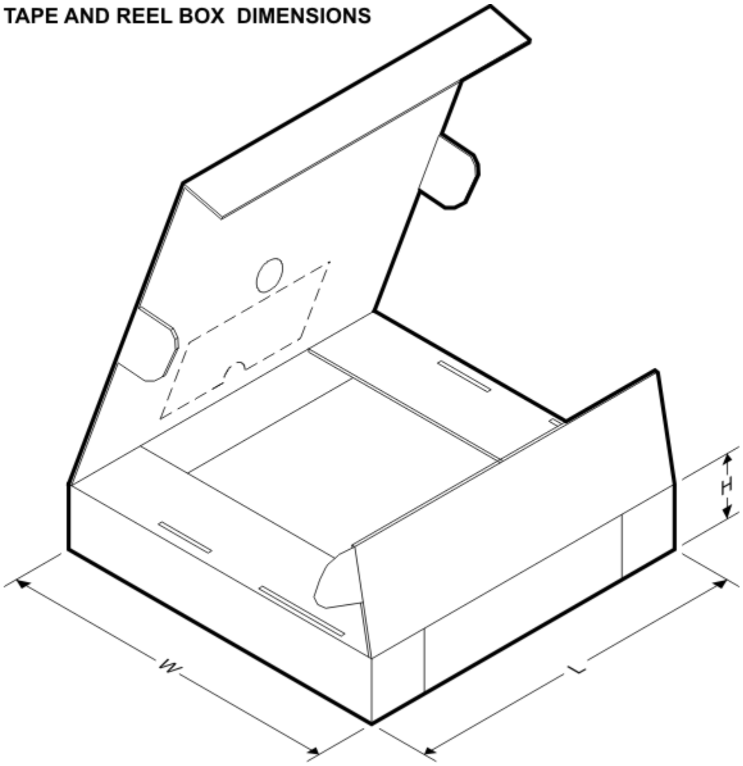
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75150DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

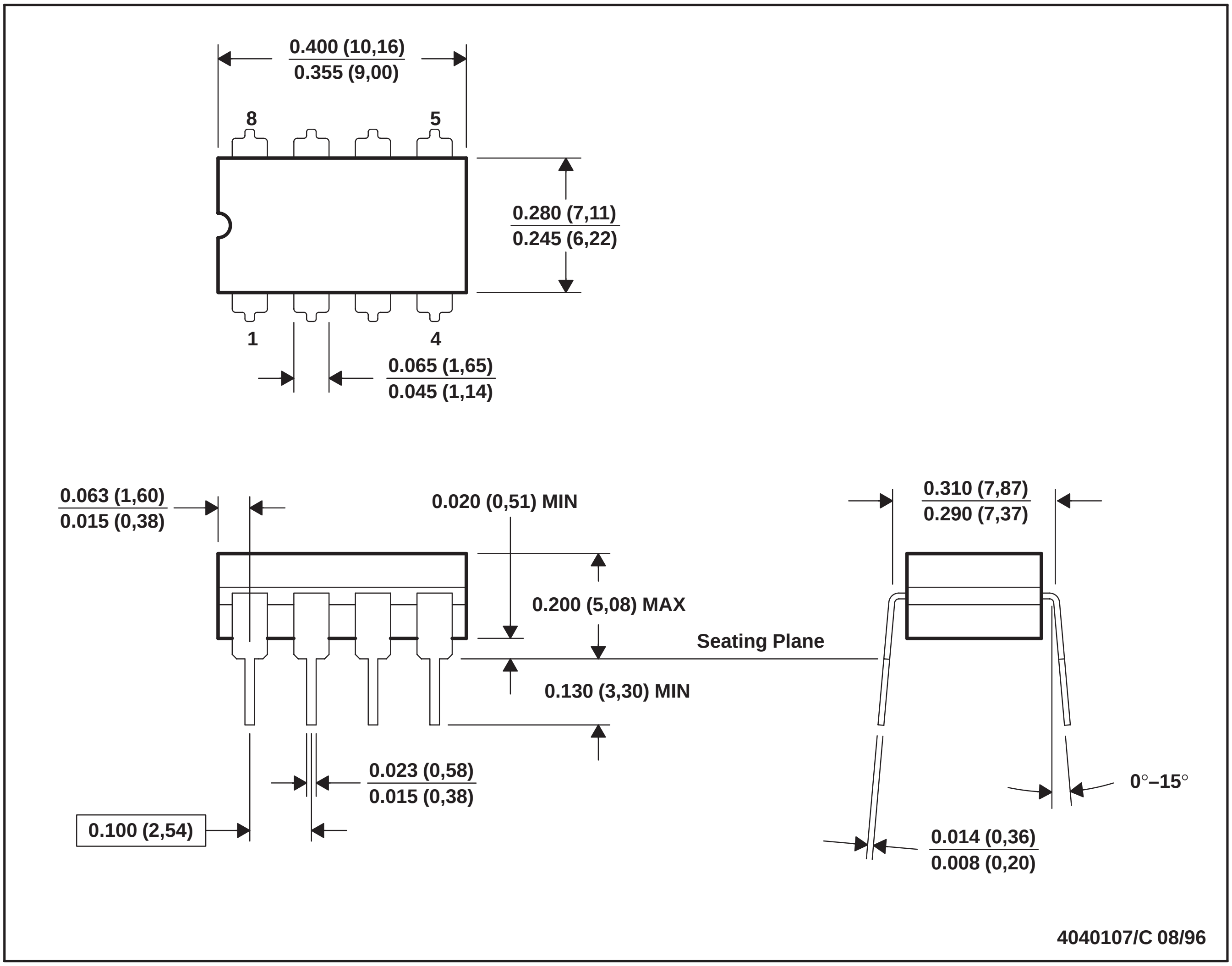
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

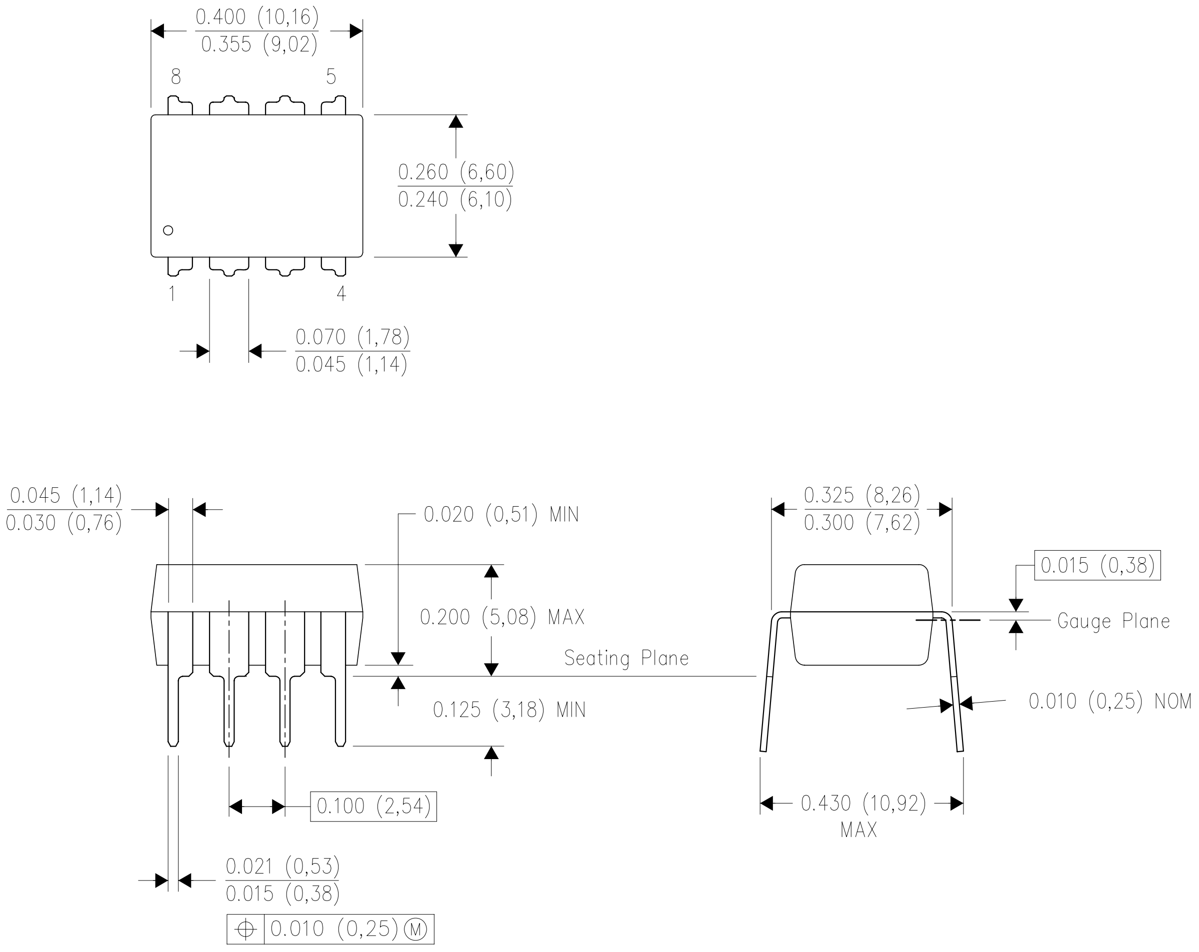
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75150DR	SOIC	D	8	2500	340.5	338.1	20.6

JG (R-GDIP-T8) CERAMIC DUAL-IN-LINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP1-T8

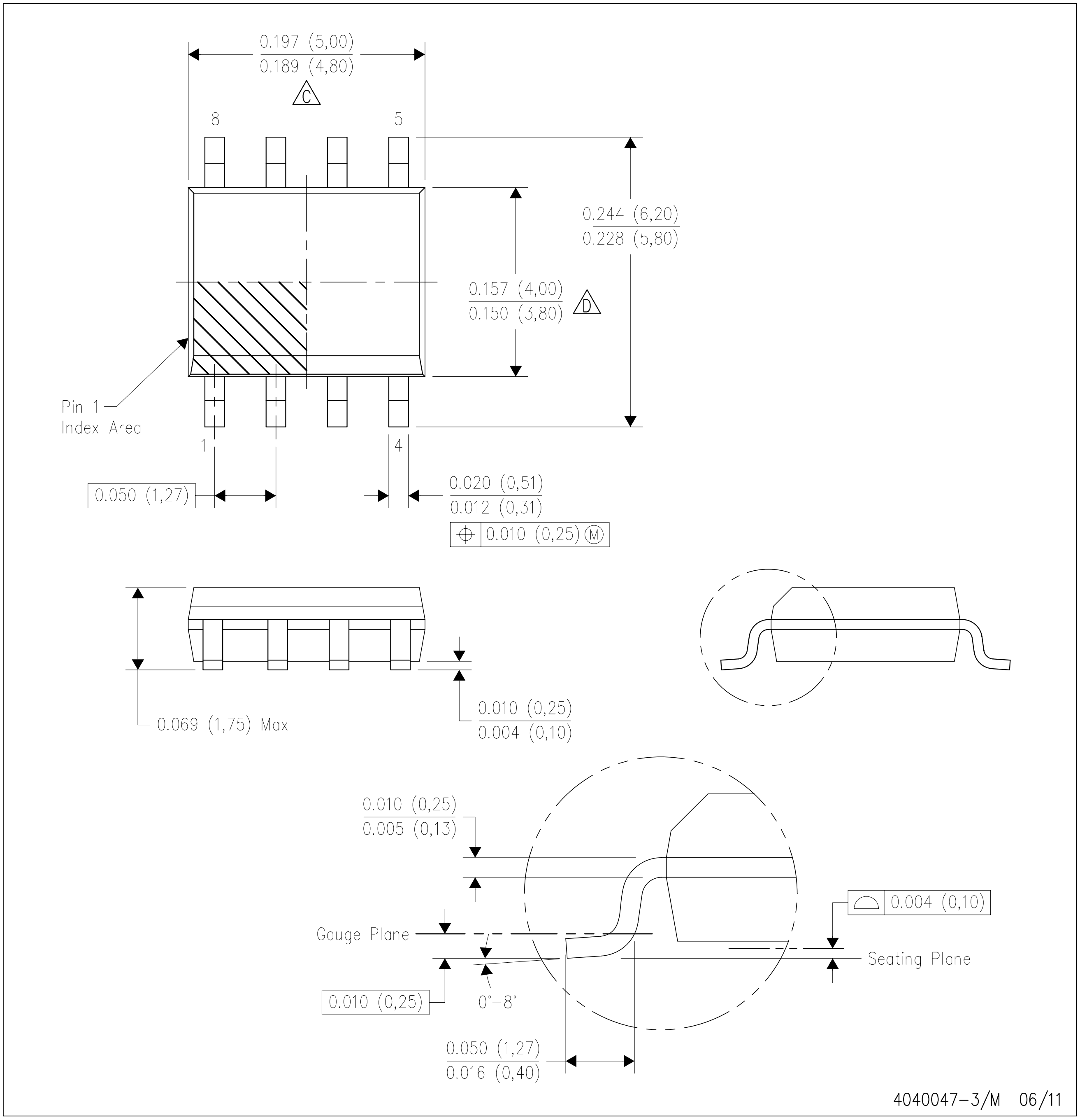
P (R-PDIP-T8) PLASTIC DUAL-IN-LINE PACKAGE



4040082/E 04/2010

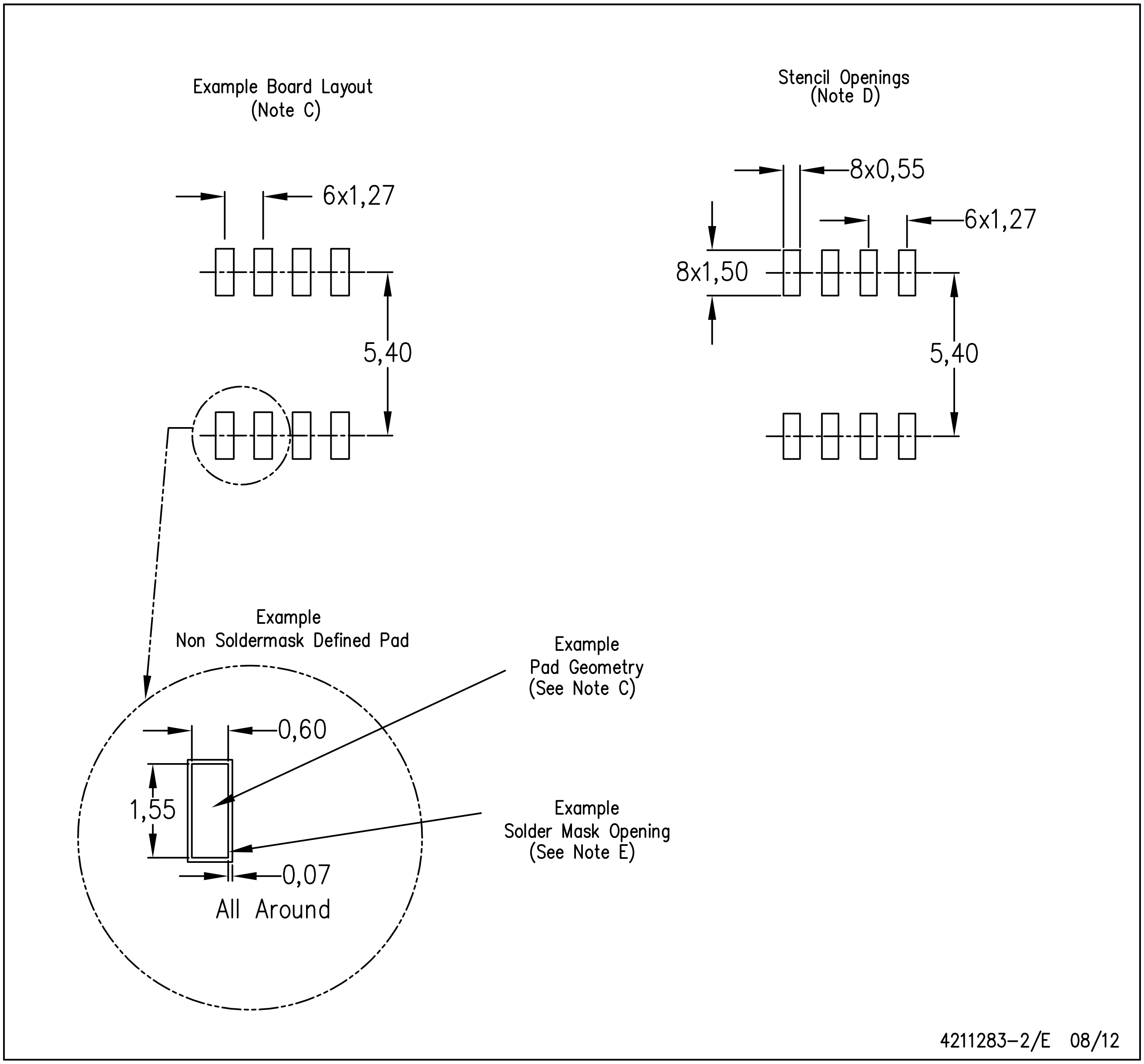
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- △D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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