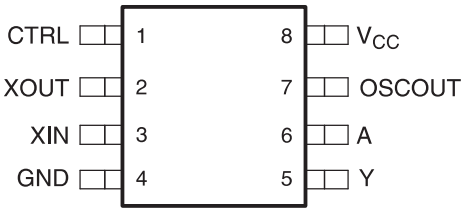
SN74LVC1404
OSCILLATOR DRIVER
FOR CRYSTAL OSCILLATOR OR CERAMIC RESONATOR

SCES469D – AUGUST 2003 – REVISED JANUARY 2007

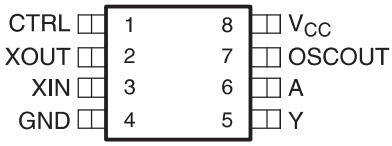
FEATURES

- **Available in the Texas Instruments NanoFree™ Package**
- **Supports 5-V V_{CC} Operation**
- **Inputs Accept Voltages to 5.5 V**
- **One Buffered Inverter With Schmitt-Trigger Input and Two Unbuffered Inverters**
- **Integrated Solution for Oscillator Applications**
- **Suitable for Commonly Used Clock Frequencies:**
  - **15 kHz, 3.58 MHz, 4.43 MHz, 13 MHz, 25 MHz, 26 MHz, 27 MHz, 28 MHz**
- **Control Input to Disable the Oscillator Circuit**
- **Low Power Consumption (10-μA Max I_{CC}) in Standby State**
- **±24-mA Output Drive at 3.3 V**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

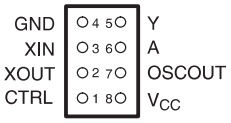
DCT PACKAGE
(TOP VIEW)



DCU PACKAGE
(TOP VIEW)



YZP PACKAGE
(BOTTOM VIEW)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This device consists of one inverter with a Schmitt-trigger input and two unbuffered inverters. It is designed for 1.65-V to 5.5-V V_{CC} operation.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74LVC1404YZPR	_ _ _44_
	SSOP – DCT	Reel of 3000	SN74LVC1404DCTR	CA4_ _ _
	VSSOP – DCU	Reel of 3000	SN74LVC1404DCUR	CA4_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
DCU: The actual top-side marking has one additional character that designates the assembly/test site.
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

XIN and XOUT pins can be connected to a crystal or resonator in oscillator applications. The device provides an additional unbuffered inverter (OSCOUT) and a Schmitt-trigger input inverter for signal conditioning (see Figure 3). The control (CTRL) input disables the oscillator circuit to reduce power consumption. The oscillator circuit is disabled and the XOUT output is set to low level when CTRL is low. To ensure the oscillator circuit remains disabled during power up or power down, CTRL should be connected to GND through a pulldown resistor. The minimum value of the resistor is determined by the current-sourcing capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

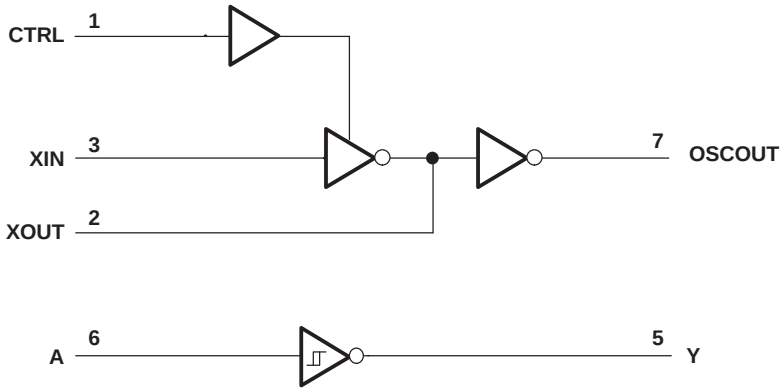
NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

FUNCTION TABLES

INPUTS		OUTPUTS	
CTRL	XIN	XOUT	OSCOUT
H	L	H	L
H	H	L	H
L	X	L	H

INPUT A	OUTPUT Y
L	H
H	L

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range(2)	XIN, A, CTRL inputs	–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)	Y output	–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state(2)(3)	XOUT, OSCOUT	–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance(4)	DCT package		220	°C/W
		DCU package		227	
		YZP package		102	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_I	Input voltage (XIN, CTRL, A inputs)		0	5.5	V
V_O	Output voltage (XOUT, OSCOUT, Y outputs)		0	V_{CC}	V
I_{OH}	High-level output current (OSCOUT, XOUT, Y outputs)	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 3 V		–16	
				–24	
		V_{CC} = 4.5 V		–32	
I_{OL}	Low-level output current (OSCOUT, XOUT, Y outputs)	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
I_{OL}(2)	Low-level output current (XOUT)	V_{CC} = 1.65 V		2	mA
$\Delta t/\Delta v$	Input transition rise/fall time (CTRL input)	V_{CC} = 1.8 V ± 0.15 V		20	ns/V
		V_{CC} = 2.5 V ± 0.2 V		20	
		V_{CC} = 3.3 V ± 0.3 V		10	
		V_{CC} = 5 V ± 0.5 V		5	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(2) CTRL = Low, XIN = GND

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{T+} Positive-going threshold	A input			1.65 V	0.79		1.16	V
				2.3 V	1.11		1.56	
				3 V	1.5		1.87	
				4.5 V	2.16		2.74	
				5.5 V	2.61		3.33	
V_{T-} Negative-going threshold	A input			1.65 V	0.39		0.62	V
				2.3 V	0.58		0.87	
				3 V	0.84		1.14	
				4.5 V	1.41		1.79	
				5.5 V	1.87		2.29	
ΔV_T hysteresis ($V_{T+} - V_{T-}$)	A input			1.65 V	0.37		0.62	V
				2.3 V	0.48		0.77	
				3 V	0.56		0.87	
				4.5 V	0.71		1.04	
				5.5 V	0.71		1.11	
V_{OH}(2)		I_{OH} = –100 µA		1.65 V to 5.5 V	V_{CC} – 0.1			V
		I_{OH} = –4 mA		1.65 V	1.2			
		I_{OH} = –8 mA		2.3 V	1.9			
		I_{OH} = –16 mA		3 V	2.4			
		I_{OH} = –24 mA		3 V	2.3			
		I_{OH} = –32 mA		4.5 V	3.8			
V_{OL}(2)		I_{OL} = 100 µA		1.65 V to 5.5 V			0.1	V
		I_{OL} = 4 mA		1.65 V			0.45	
		I_{OL} = 8 mA		2.3 V			0.3	
		I_{OL} = 16 mA		3 V			0.4	
		I_{OL} = 24 mA		3 V			0.55	
		I_{OL} = 32 mA		4.5 V			0.55	
V_{OL}	XOUT	I_{OL} = 100 µA	CTRL = Low, XIN = GND	1.65 V to 5.5 V			0.1	V
		I_{OL} = 2 mA		1.65 V			0.65	
I_I	All inputs	V_I = 5.5 V or GND		0 to 5.5 V			±5	µA
I_{off}	Y output	V_I or V_O = 0 to 5.5 V		0			±10	µA
I_{CC}		$V_I = V_{CC}$ or GND,	I_O = 0	1.65 V to 5.5 V			10	µA
ΔI_{CC}	CTRL and A inputs	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		3 V to 5.5 V			500	µA
C_i	CTRL and A inputs	$V_I = V_{CC}$ or GND		3.3 V		3.5		pF
	XIN					6		

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) V_{IL} = 0 V and $V_{IH} = V_{CC}$ for XOUT and OSCOUT; the standard V_{T+} and V_{T-} levels should be applied for the Y output.

Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2.8	15.1	1.6	5.7	1.5	4.6	0.9	4.4	ns
	XIN	XOUT	1.7	9.6	1	3.2	1.1	2.4	0.9	1.8	
		OSCOUT	2.6	17.2	2	5.6	2	4.1	1.5	3.2	
	CTRL	XOUT	3	28.2	1.8	14.4	1.5	12.2	1.1	10.2	

Switching Characteristics

over recommended operating free-air temperature range, C_L = 30 pF or 50 pF (unless otherwise noted) (see Figure 2)

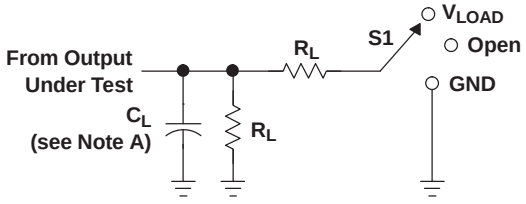
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	3	17.3	1.8	7.4	1.8	6.4	1	5.3	ns
	XIN	XOUT	1.2	15.8	0.8	5.8	1	5.4	0.6	4.6	
		OSCOUT	3.5	25.7	2.6	7.1	2.8	7.8	2	6.7	
	CTRL	XOUT	3.3	24.5	2.1	12	1.9	12.7	1.1	11.2	

Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	25	26	29	39	pF

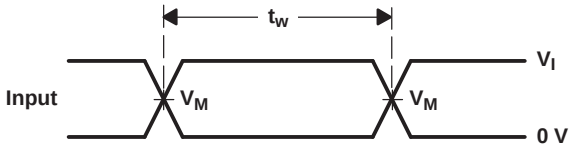
PARAMETER MEASUREMENT INFORMATION



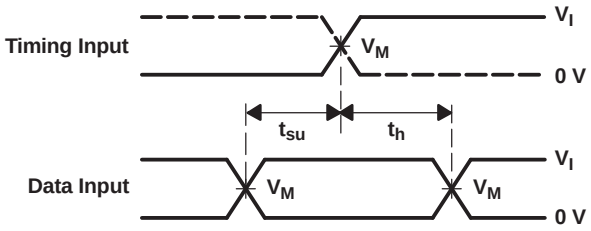
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

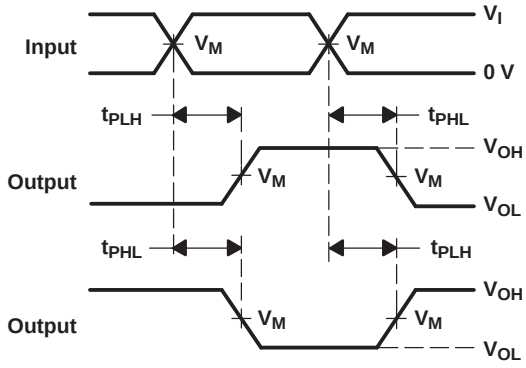
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L (Except t_{PZ})	R_L (t_{PZ})	V_Δ
	V_I	t_r/t_f						
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 MΩ	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 MΩ	1 kΩ	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 MΩ	1 kΩ	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 MΩ	1 kΩ	0.3 V



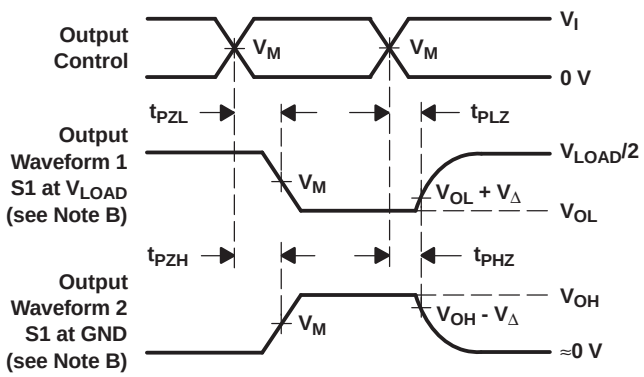
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

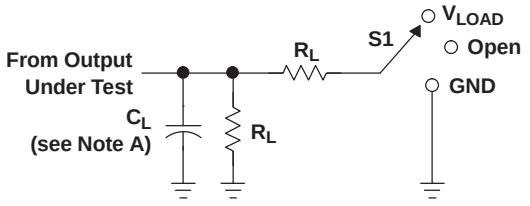


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

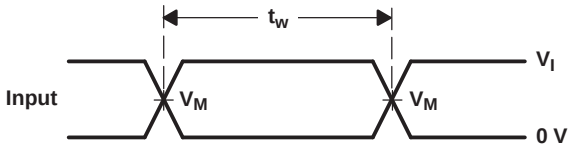
PARAMETER MEASUREMENT INFORMATION



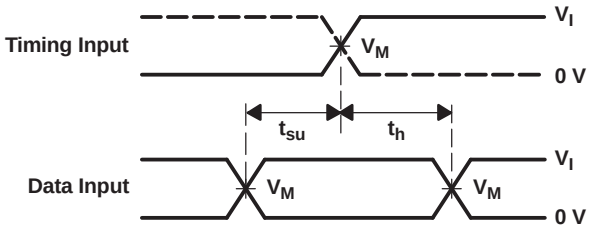
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

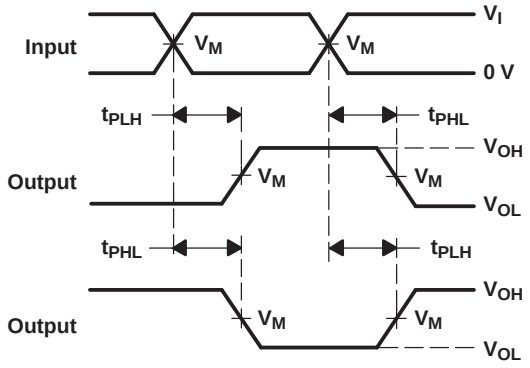
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



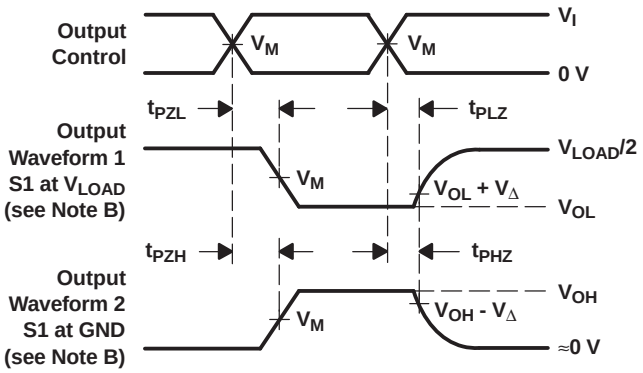
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

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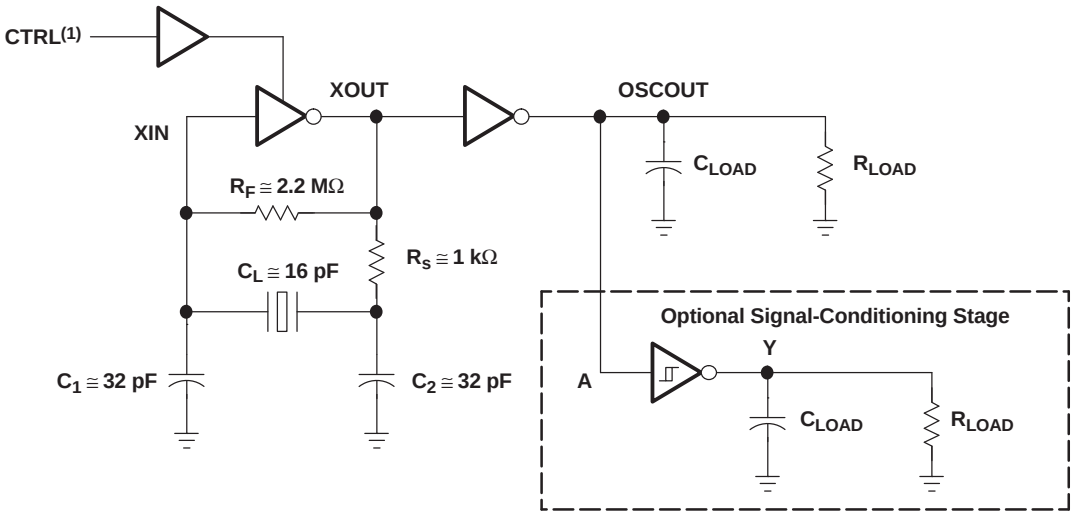
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

Figure 3 shows a typical application of the SN74LVC1404 in a Pierce oscillator circuit. The output voltage can be conditioned further by connecting OSCOUT to the Schmitt-trigger input inverter. The Schmitt-trigger input inverter produces a rail-to-rail voltage waveform. The recommended load for the crystal, shown in this example, is 16 pF. The value of the recommended load (C_L) can be found in the crystal manufacturer's data sheet. Values of C_1 and C_2 are chosen so that $C_L = \frac{C_1 C_2}{C_1 + C_2}$ and $C_1 \approx C_2$. R_s is the current-limiting resistor, and the value depends on the maximum power dissipation of the crystal. Generally, the recommended value of R_s is specified in the crystal manufacturer's data sheet and, usually, this value is approximately equal to the reactance of C_2 at resonance frequency, i.e., $R_s = X_{C_2}$. R_F is the feedback resistor that is used to bias the inverter in the linear region of operation. Usually, the value is chosen to be within 1 MΩ to 10 MΩ.

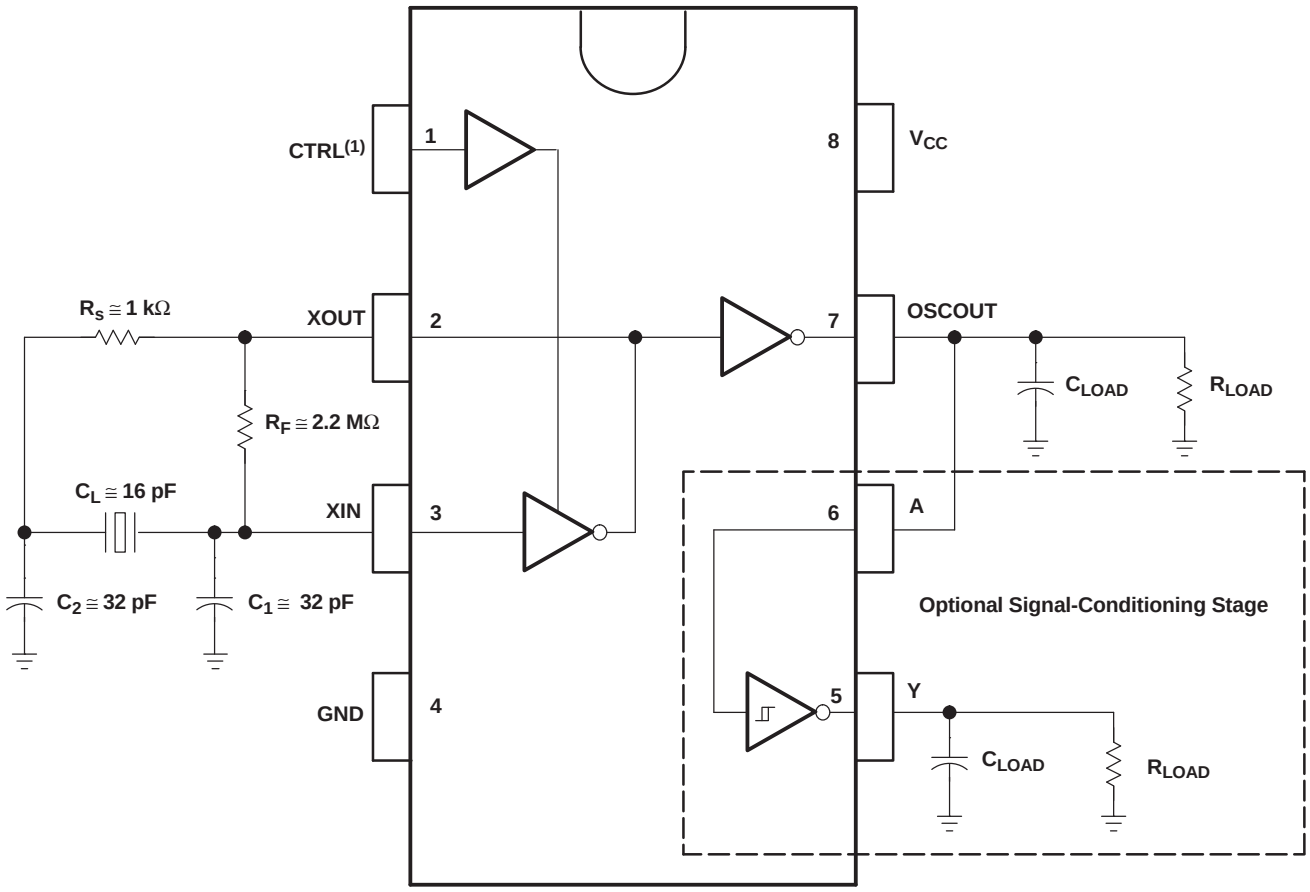


A) Logic Diagram View

(1) CTRL should be tied to logic high during normal operation of the oscillator circuit. To disable the oscillator circuit, connect CTRL to logic low.

Figure 3. Oscillator Circuit

APPLICATION INFORMATION



B) Oscillator Circuit in DCT or DCU Pinout

(1) CTRL should be tied to logic high during normal operation of the oscillator circuit. To disable the oscillator circuit, connect CTRL to logic low.

Practical Design Tips

- The open-loop gain of the unbuffered inverter decreases as power-supply voltage decreases. This decreases the closed-loop gain of the oscillator circuit. The value of R_S can be decreased to increase the closed-loop gain, while maintaining the power dissipation of the crystal within the maximum limit.
- R_S and C_2 form a low-pass filter and reduce spurious oscillations. Component values can be adjusted, based on the desired cutoff frequency.
- C_2 can be increased over C_1 to increase the phase shift and help in start-up of the oscillator. Increasing C_2 may affect the duty cycle of the output voltage.
- At high frequency, phase shift due to R_S becomes significant. In this case, R_S can be replaced by a capacitor to reduce the phase shift.

APPLICATION INFORMATION

Testing

After the selection of proper component values, the oscillator circuit should be tested, using these components, to ensure that the oscillator circuit shows required performance over the recommended operating conditions.

- Without a crystal, the oscillator circuit should not oscillate. To check this, the crystal can be replaced by its equivalent parallel-resonant resistance.
- When the power-supply voltage drops, the closed-loop gain of the oscillator circuit reduces. Ensure that the circuit oscillates at the appropriate frequency at the lowest V_{CC} and highest V_{CC}.
- Ensure that the duty cycle, start-up time, and frequency drift over time is within the system requirements.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74LVC1404DCTR	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CA4 Z	Samples
SN74LVC1404DCTRE4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CA4 Z	Samples
SN74LVC1404DCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CA4R	Samples
SN74LVC1404DCURE4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CA4R	Samples
SN74LVC1404DCURG4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CA4R	Samples
SN74LVC1404YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(447, 44N)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

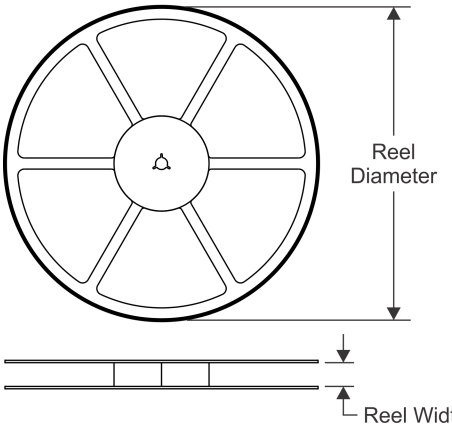
(4) Only one of markings shown within the brackets will appear on the physical device.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

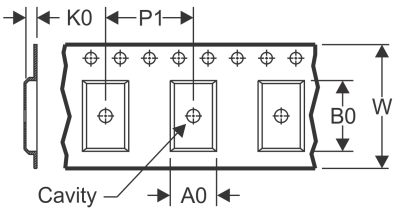
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

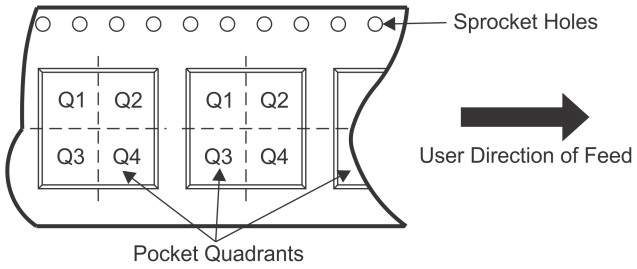


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

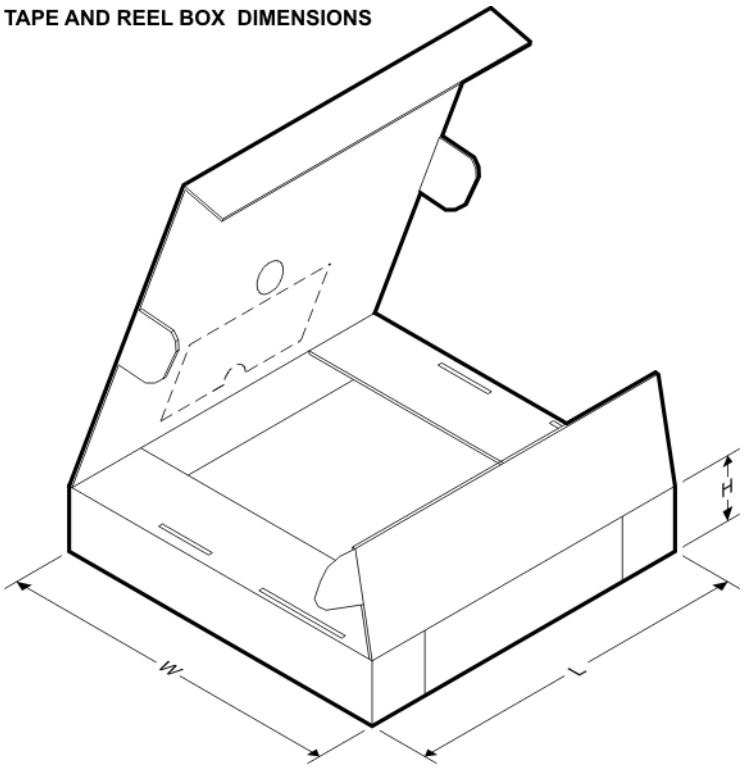
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1404DCUR	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1404YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1404DCUR	US8	DCU	8	3000	202.0	201.0	28.0
SN74LVC1404YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

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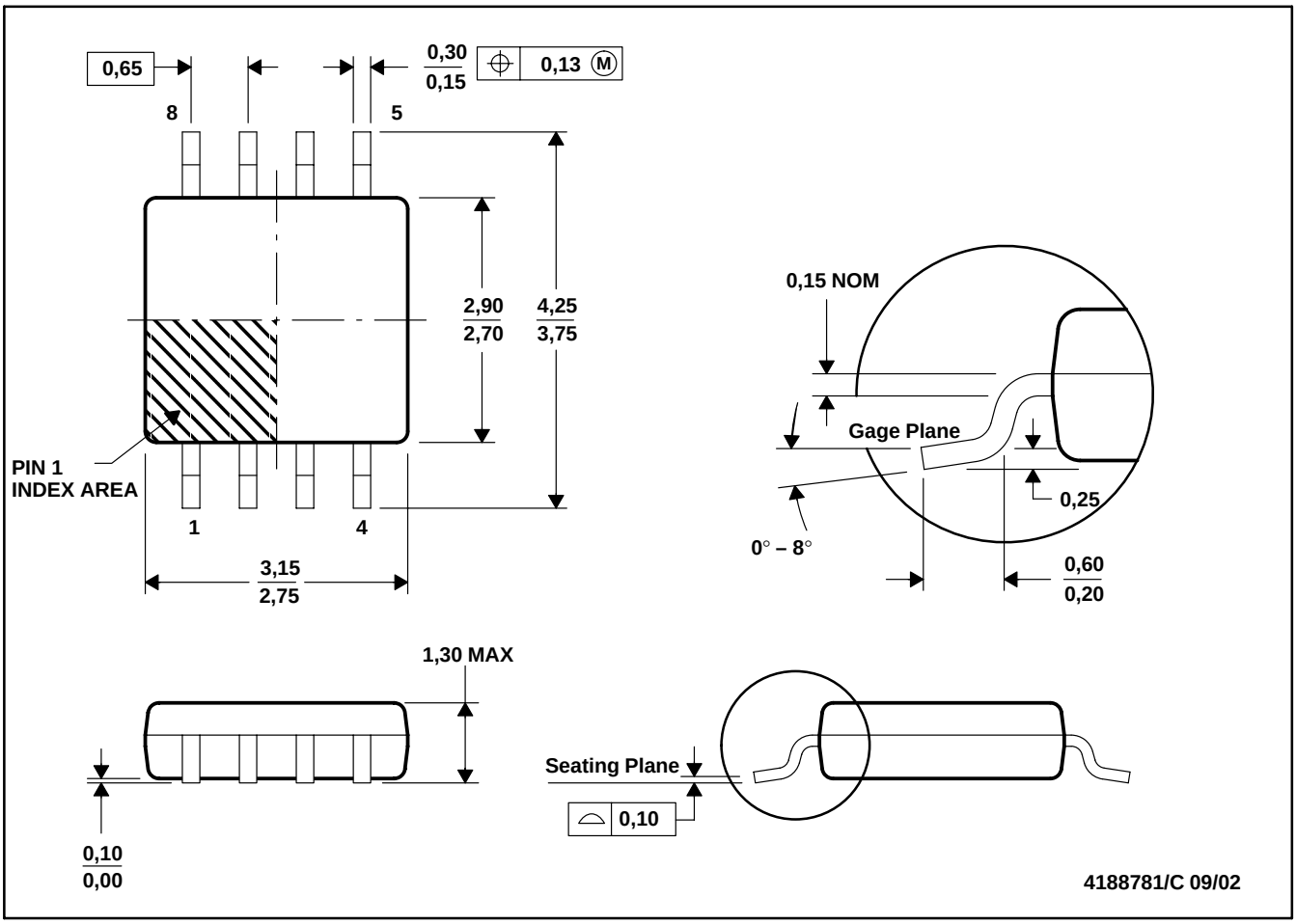
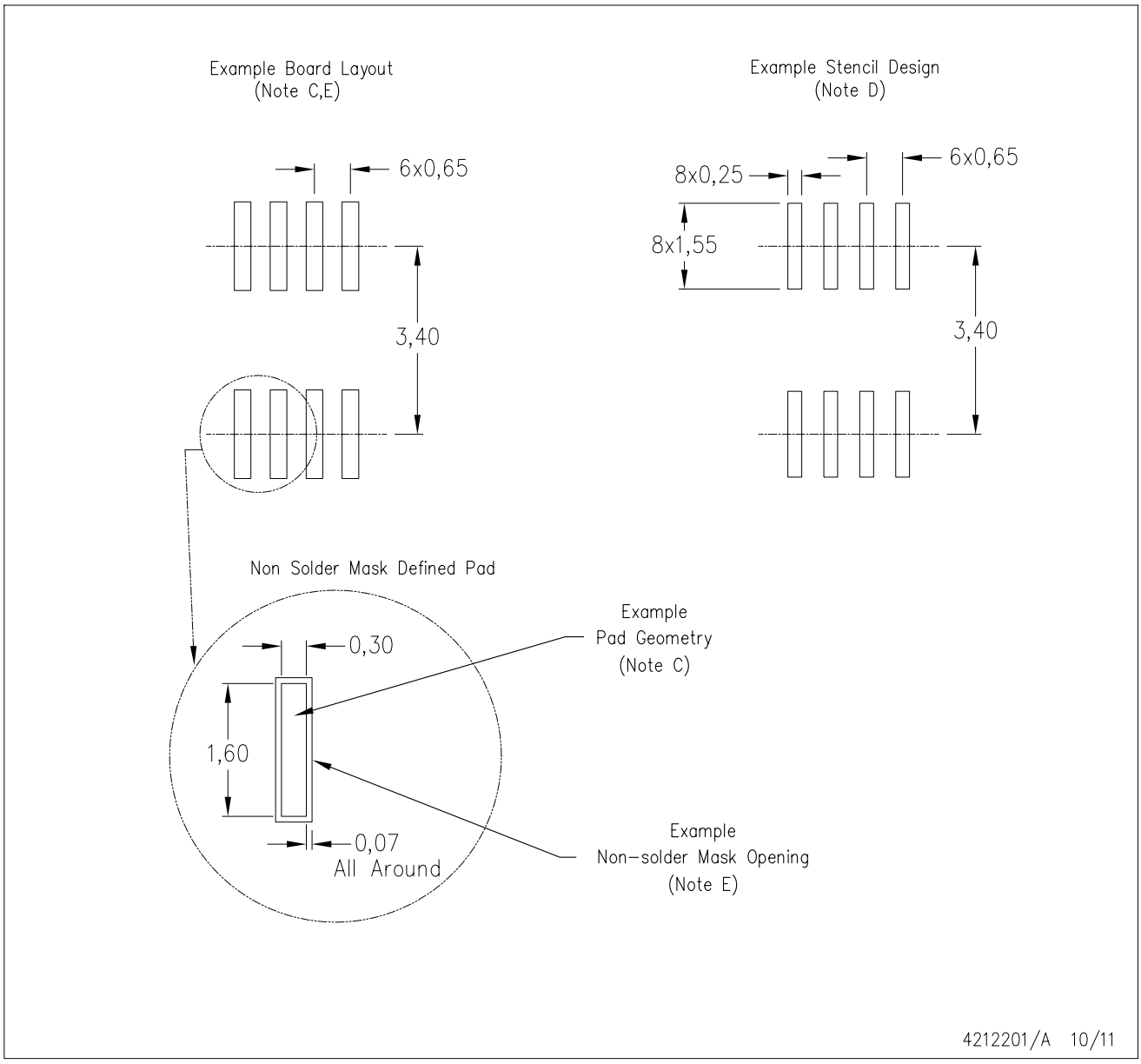
DCT (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



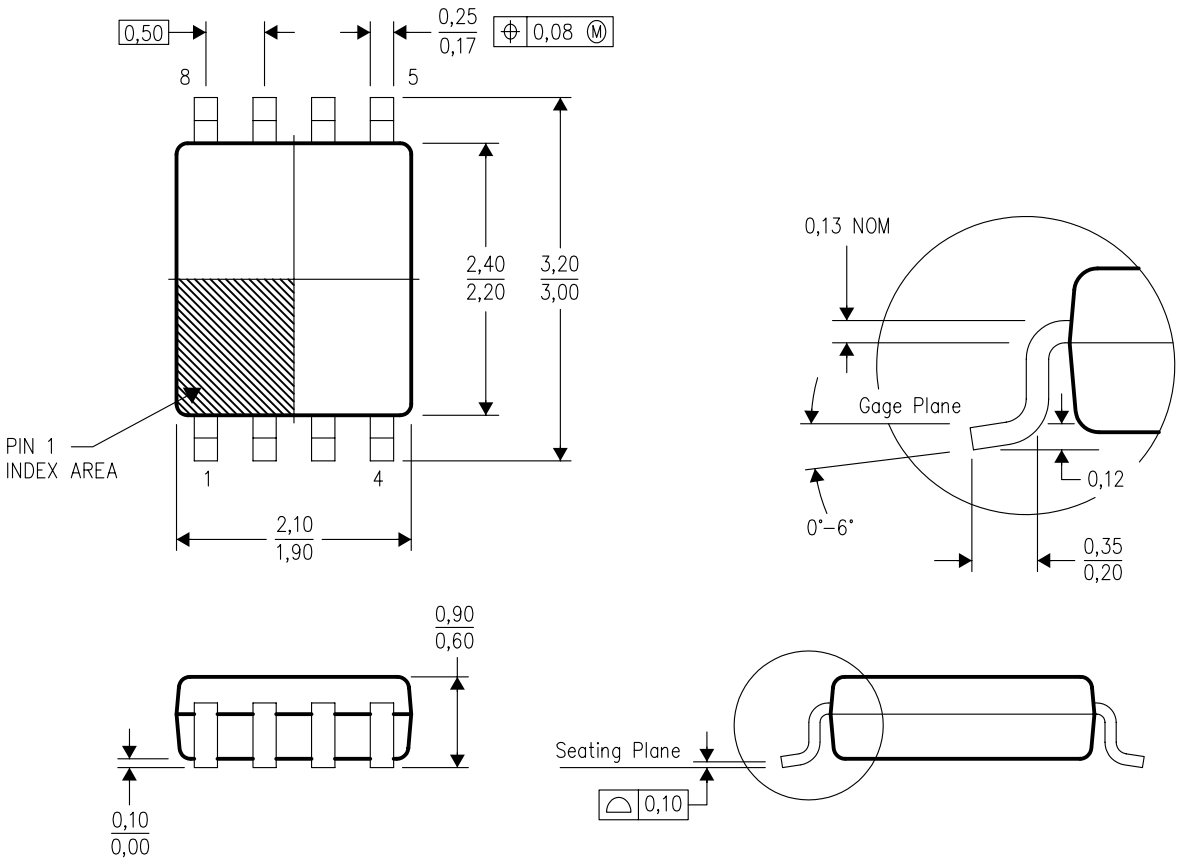
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. Falls within JEDEC MO-187 variation DA.

DCT (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

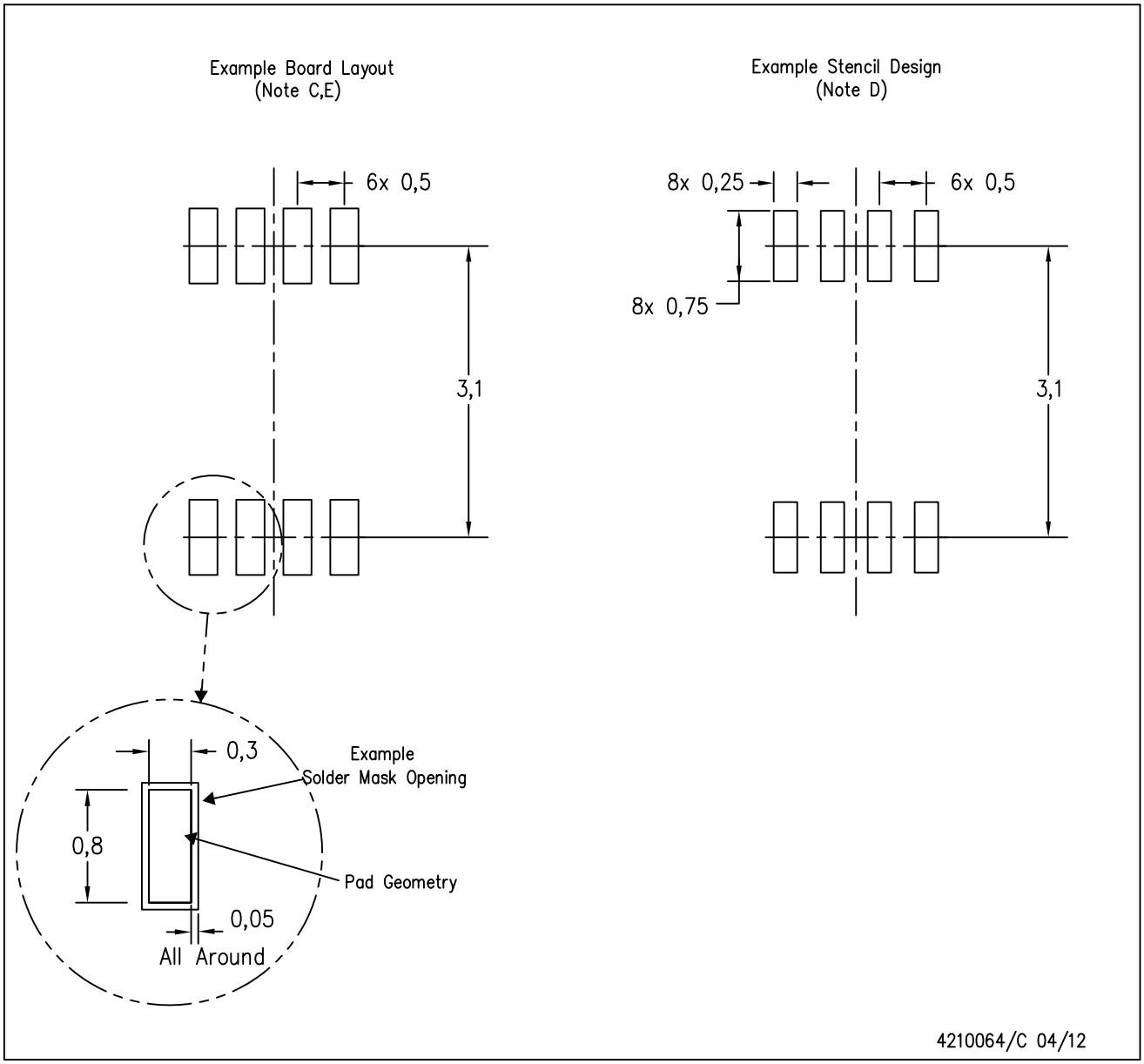
DCU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



4200503/F 07/05

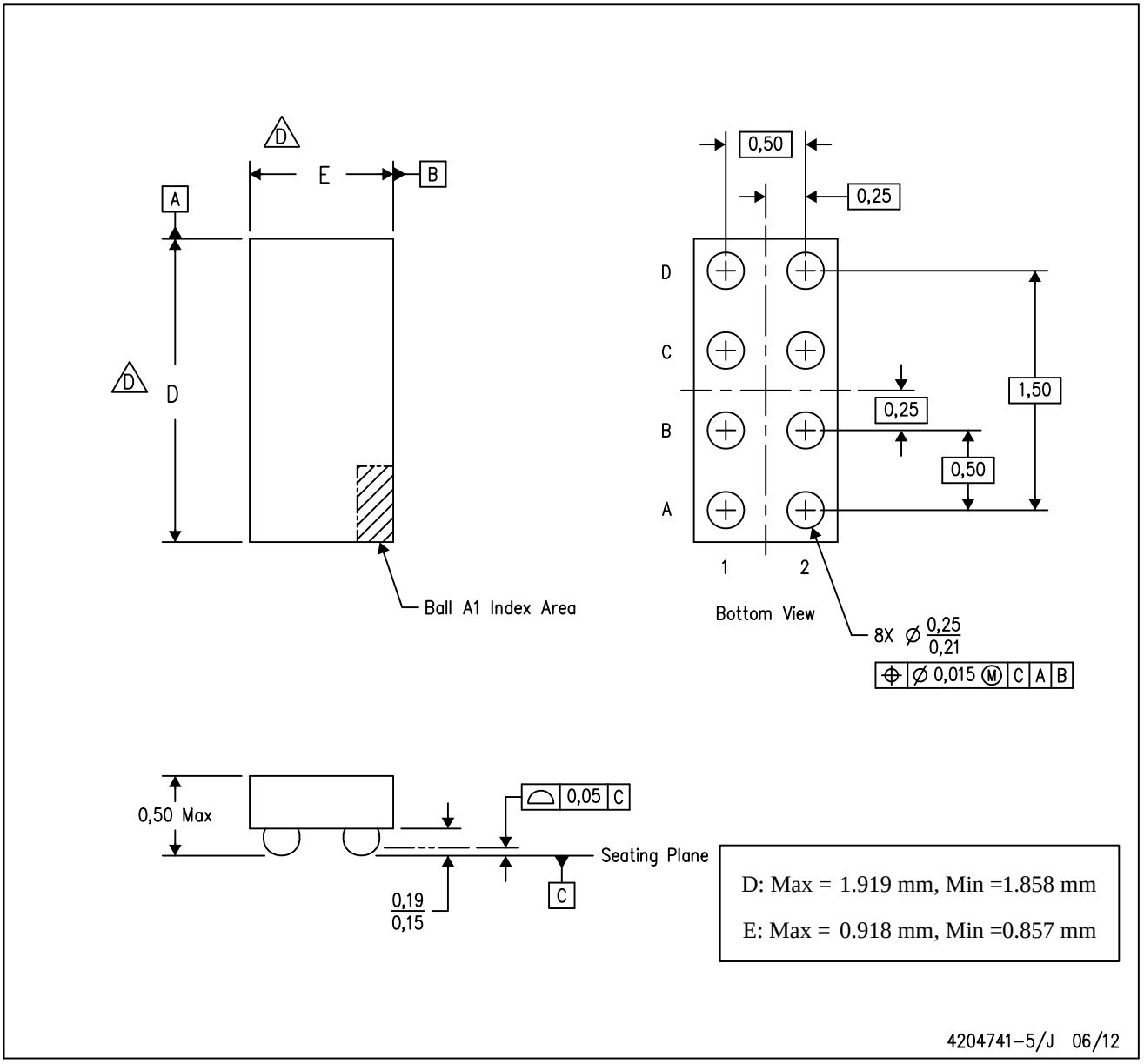
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–187 variation CA.

DCU (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

YZP (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
E. This package is a Pb–free solder ball design. Refer to the 8 YEP package (drawing 4204725) for tin–lead (SnPb).

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