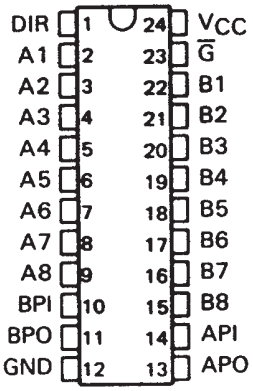
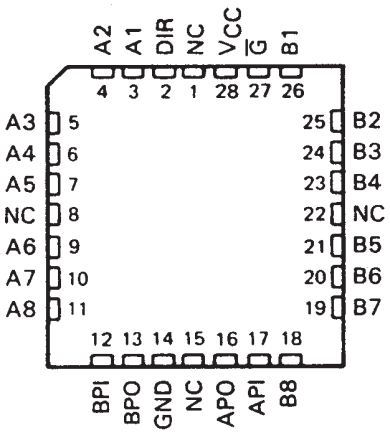
SCLS152 – D2839, MARCH 1984 – REVISED SEPTEMBER 1987

- **Bus Transceivers with Inverting Outputs ('HC664) or True Outputs ('HC665)**
- **Generates a Parity Bit for A Bus and B Bus**
- **Easily Cascadable**
- **Internal Active Pull-Ups and Pull-Downs**
- **High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC664, SN54HC665 . . . JT PACKAGE
SN74HC664, SN74HC665 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54HC664, SN54HC665 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These octal bus transceivers are designed for asynchronous, bidirectional communication between data buses. The devices transmit data from the A Bus to the B Bus or from the B Bus to the A Bus, depending on the level at the direction control input, DIR. The enable input $\overline{G}$, can be used to disable the device so that the buses are isolated. These devices will also generate parity outputs, APO and BPO, which reflect the number of high levels at the A Bus and B Bus, respectively, taking into account the parity inputs API and BPI.

The bidirectional I/O ports feature active circuitry on the input stage that, when the output shared by that pin is disabled, will maintain the input in the last state taken by the output. This state will be maintained until changed by the activity on the bus. The advantage of this arrangement is that when all outputs on the bus are disabled, the inputs will be prevented from floating, resulting in minimum power dissipation and minimum susceptibility to noise. This eliminates any need for external pull-up or pull-down resistors. The parity inputs API and BPI have similar circuitry. For futher information, see the Typical Application Data.

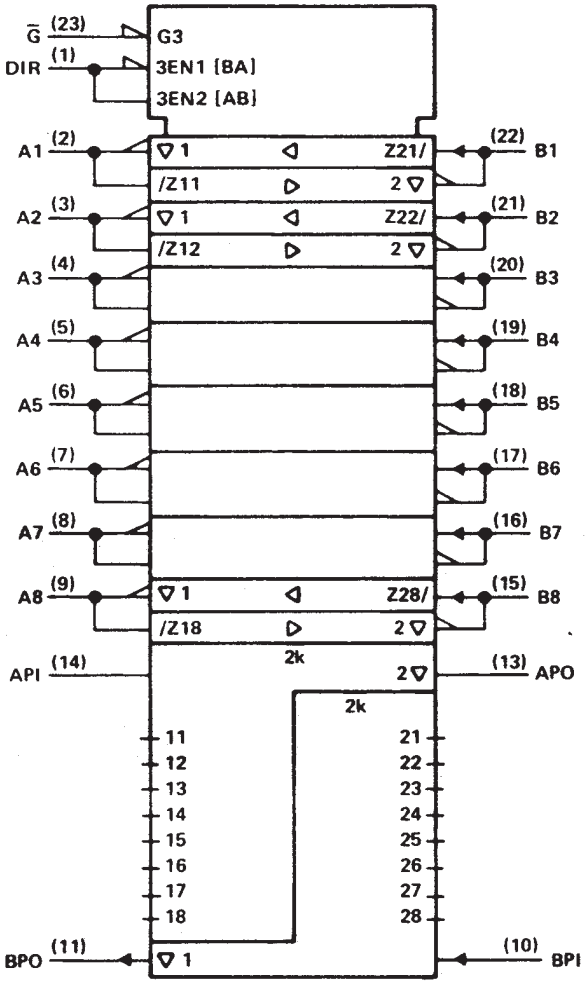
The SN54HC664 and SN54HC665 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC664 and SN74HC665 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE

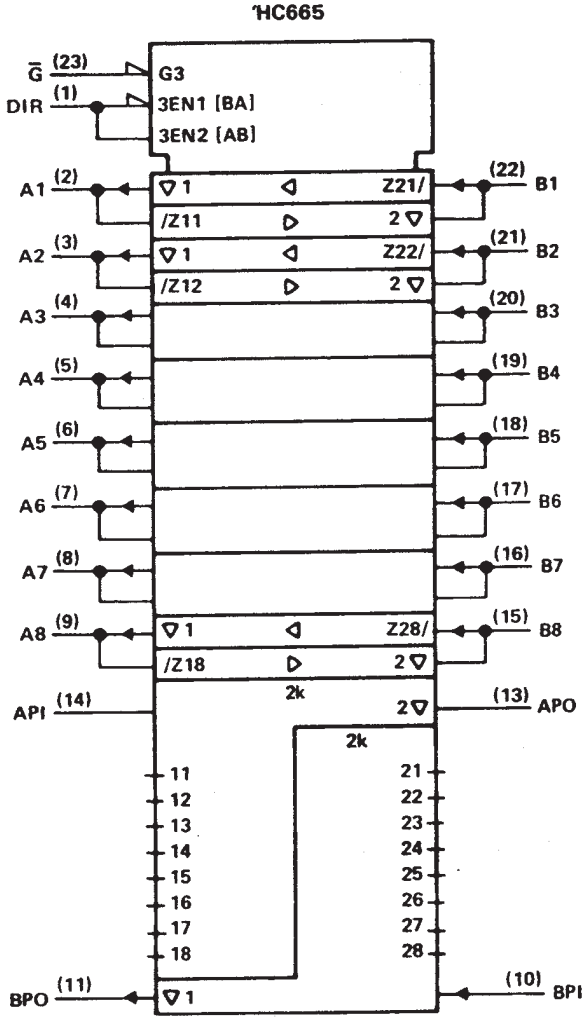
CONTROL INPUTS		NUMBER OF HIGH INPUTS ON A BUS AND API	NUMBER OF HIGH INPUTS ON B BUS AND BPI	OUTPUTS		OPERATION	
$\overline{G}$	DIR			APO	BPO	'HC664	'HC665
L	L	X	0, 2, 4, 6, 8	Z	H	$\overline{B}$ Data to A Bus	B Data to A Bus
		X	1, 3, 5, 7, 9	Z	L		
L	H	0, 2, 4, 6, 8	X	H	Z	$\overline{A}$ Data to B Bus	A Data to B Bus
		1, 3, 5, 7, 9	X	L	Z		
H	X	X	X	Z	Z	Isolation	Isolation

logic symbols†

'HC664

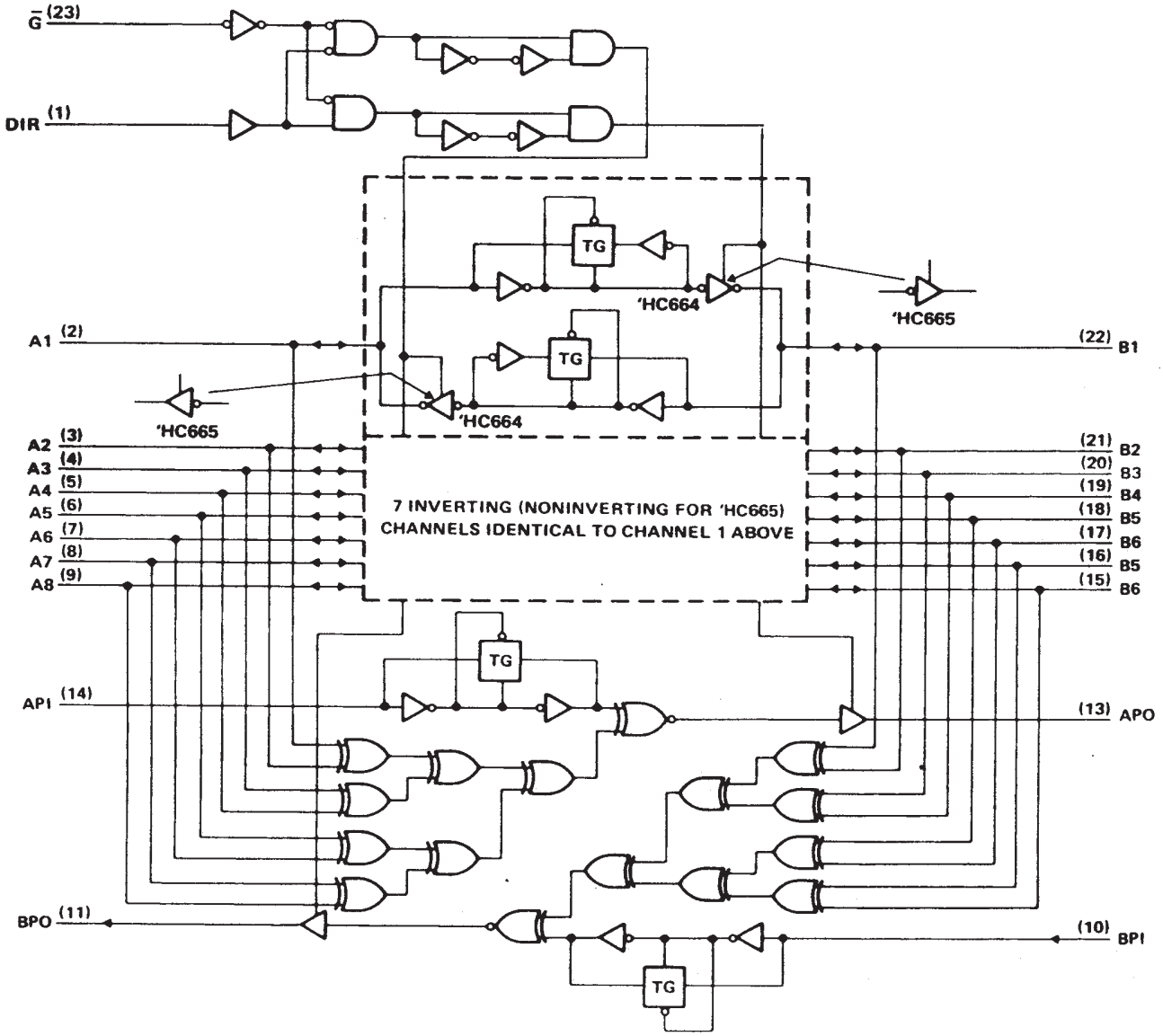


'HC665



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or JT package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or NT package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC664 SN54HC665			SN74HC664 SN74HC665			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC664 SN54HC665		SN74HC664 SN74HC665		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
V_{OH}	All outputs except APO & BPO	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
		V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
	APO or BPO	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
		V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}		V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
V_{OL}	All outputs except APO & BPO	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
	APO or BPO	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$\overline{G}$, DIR, API or BPI	V_I = V_{CC} or 0	6 V			±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	V_O = V_{CC} or 0	6 V			±0.01	±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i†			2 to 6 V		3	10		10		10	pF

†This parameter, C_i, does not apply to I/O ports.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC664		SN74HC664		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		75	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_{pd}	A or B	APO or BPO	2 V		115	230		345		290	ns
			4.5 V		23	46		69		58	
			6 V		20	39		59		49	
t_{pd}	API or BPI	APO or BPO	2 V		77	155		235		195	ns
			4.5 V		15	31		47		39	
			6 V		13	26		40		33	
t_{en}	$\overline{G}$ or DIR	A or B	2 V		125	255		385		320	ns
			4.5 V		25	51		77		64	
			6 V		22	43		65		54	
t_{dis}	$\overline{G}$ or DIR	A or B	2 V		125	255		385		320	ns
			4.5 V		25	51		77		64	
			6 V		22	43		65		54	
t_t		Any	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	56 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC664		SN74HC664		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		116	235		355		295	ns
			4.5 V		23	47		71		59	
			6 V		20	41		60		51	
t_{pd}	A or B	APO or BPO	2 V		157	315		475		395	ns
			4.5 V		31	63		95		79	
			6 V		27	54		81		68	
t_{pd}	API or BPI	APO or BPO	2 V		120	240		365		300	ns
			4.5 V		24	48		73		60	
			6 V		20	41		62		52	
t_{en}	$\overline{G}$ or DIR	A or B	2 V		170	340		515		425	ns
			4.5 V		34	68		103		85	
			6 V		29	58		87		73	
t_t		Any	2 V		37	210		315		265	ns
			4.5 V		12	42		63		53	
			6 V		10	36		53		45	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC665		SN74HC665		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		70	140		210		175	ns
			4.5 V		14	28		42		35	
			6 V		12	24		36		30	
t_{pd}	A or B	APO or BPO	2 V		115	230		345		290	ns
			4.5 V		23	46		69		58	
			6 V		20	39		59		49	
t_{pd}	API or BPI	APO or BPO	2 V		77	155		235		195	ns
			4.5 V		15	31		47		39	
			6 V		13	26		40		33	
t_{en}	$\overline{G}$ or DIR	A or B	2 V		125	255		385		320	ns
			4.5 V		25	51		77		64	
			6 V		22	43		65		54	
t_{dis}	$\overline{G}$ or DIR	A or B	2 V		125	255		385		320	ns
			4.5 V		25	51		77		64	
			6 V		22	43		65		54	
t_t		Any	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	56 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC665		SN74HC665		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		112	225		340		280	ns
			4.5 V		22	45		68		56	
			6 V		20	39		58		49	
t_{pd}	A or B	APO or BPO	2 V		157	315		475		395	ns
			4.5 V		31	63		95		79	
			6 V		27	54		81		68	
t_{pd}	API or BPI	APO or BPO	2 V		120	240		365		300	ns
			4.5 V		24	48		73		60	
			6 V		20	41		62		52	
t_{en}	$\overline{G}$ or DIR	A or B	2 V		170	340		515		425	ns
			4.5 V		34	68		103		85	
			6 V		29	58		87		73	
t_t		Any	2 V		37	210		315		265	ns
			4.5 V		12	42		63		53	
			6 V		10	36		53		45	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

The unique structure used on the I/O ports and the parity inputs of these devices deserves some special consideration (see Figure 1). Only the input structure is shown. The conventional 3-state output structure associated with each I/O port has been omitted to facilitate understanding.

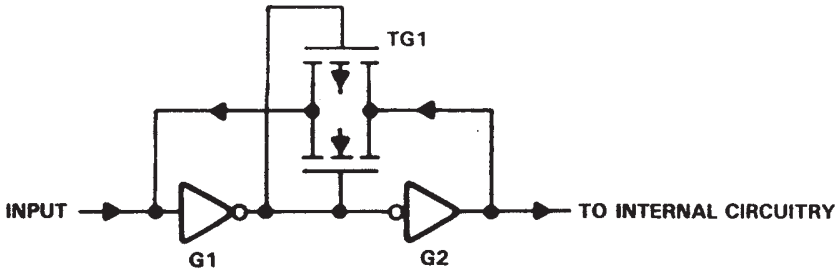


FIGURE 1. INPUT STRUCTURE

The two inverters (G1 and G2) have a transmission gate (TG1) connected in a feedback loop around them. This transmission gate is connected in an unusual fashion, that is, with the gates of both transistors connected to the output of G1. Thus, with the output of G1 at either a high or a low level, one or the other of the transistors will be turned on allowing feedback of the output of G2 to the input of G1. The effect of TG1 is that the input level will be maintained at whatever level existed prior to the bus being disabled or the level currently existing on the bus will be reinforced.

To understand the operation of this input, assume that initially the input is at a low logic level. As the input voltage is raised, TG1 sinks current to attempt to maintain the low level. However, TG1 consists of small geometry transistors and appears resistive as current flows thus allowing the input voltage to rise toward the threshold voltage of G1. When the threshold voltage is reached, G1 changes state causing G2 to change state. G2 then attempts to maintain a high level on the input through TG1. A similar operation occurs when the input voltage is decreased toward the threshold voltage of G1. G2 sources current through TG1 until the threshold is reached.

This characteristic of the input stage has some implications for the input current levels. With the input held at either V_{CC} or GND, there is no voltage across TG1 and negligible input current. However, as the input voltage is raised from GND or lowered from V_{CC}, the input current rises as the voltage across TG1 increases. The input current continues to rise until it reaches a maximum just as the threshold voltage of G1 is reached.

This configuration provides for minimum power dissipation when the bus is inactive (all outputs on the bus in the high-impedance state) and minimum susceptibility to noise on the bus during this time. The increase in input current may go unnoticed as it only occurs during transitions on the bus. Care must be taken when measuring input currents (e.g., at incoming inspection) to ensure that the input voltage is set to the correct value.

The use of these devices for interfacing to 8-, 16-, 24-bit-wide memory arrays with parity is illustrated in Figures 2, 3 and 4.

TYPICAL APPLICATION DATA

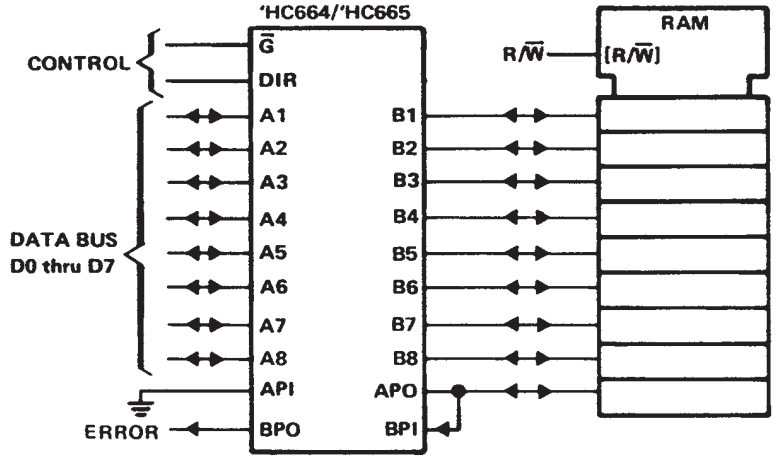


FIGURE 2. 8-BIT-WIDE MEMORY ARRAY WITH PARITY

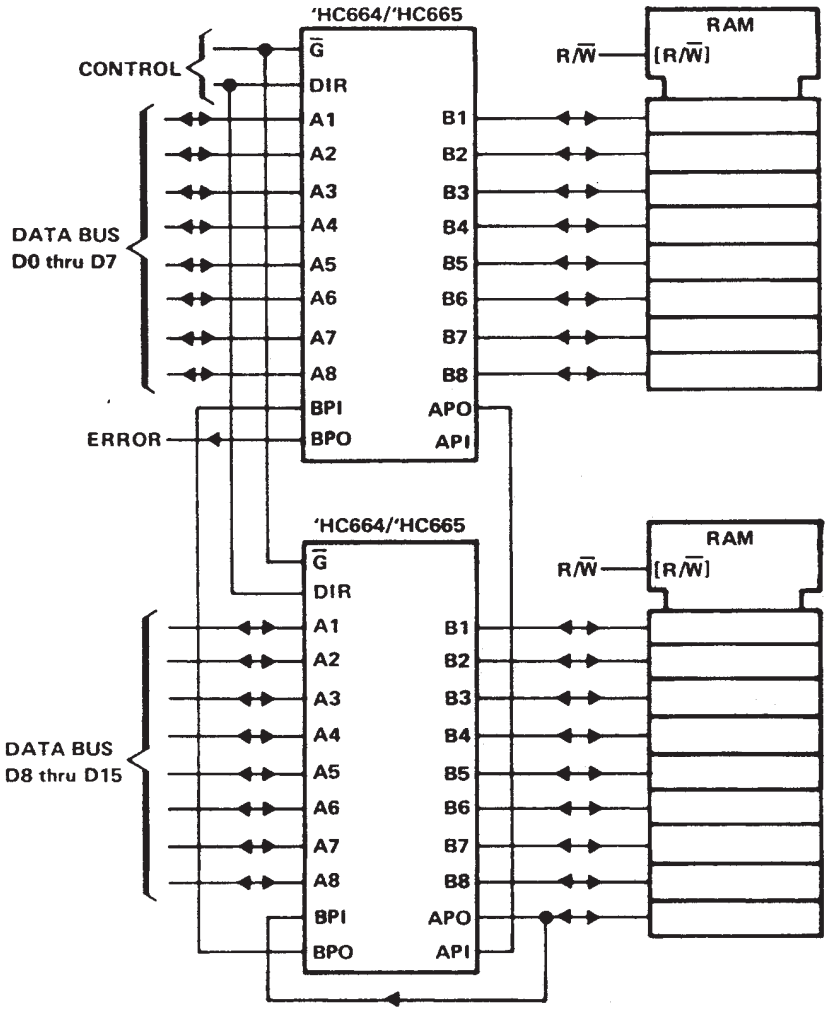


FIGURE 3. 16-BIT-WIDE MEMORY ARRAY WITH PARITY

TYPICAL APPLICATION DATA

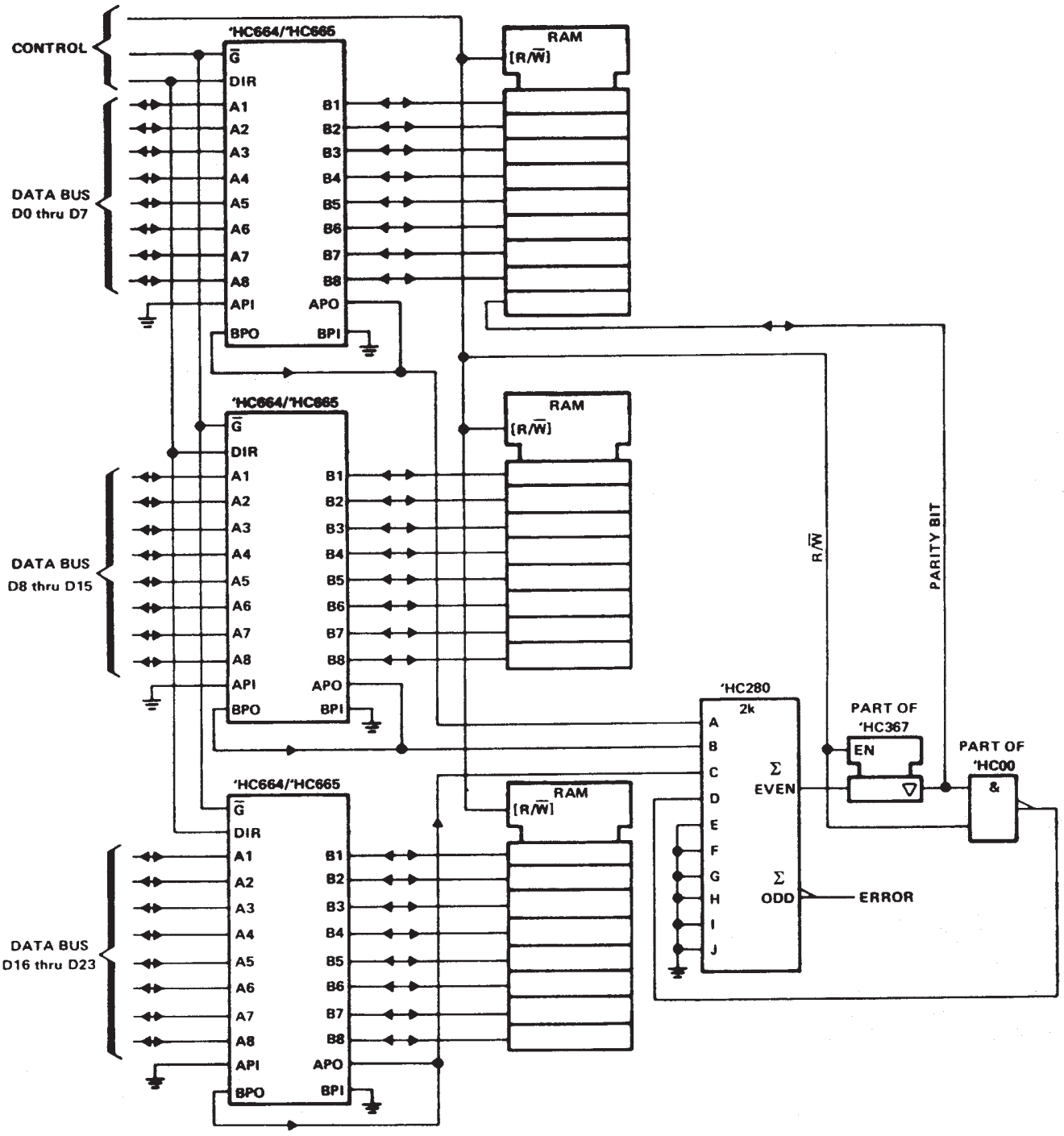


FIGURE 4. 24-BIT-WIDE MEMORY ARRAY WITH PARITY

NOTE: The 'HC280 eliminates ripple carry delays associated with Figures 2 and 3. However, in those two cases the delays are probably too small to be of concern.

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