DM74H01(SN74H01) quad 2-input NAND gate (open collector)
DM74H05(SN74H05) hex inverter (open collector)
DM74H22(SN74H22) dual 4-input NAND gate (open collector)

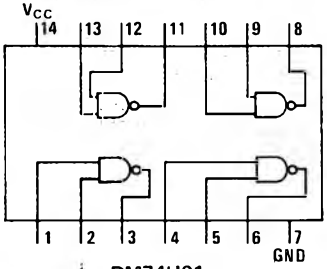
general description

These TTL circuits provide higher speed in wire-OR applications than Series 74 open-collector gates. Key features include:

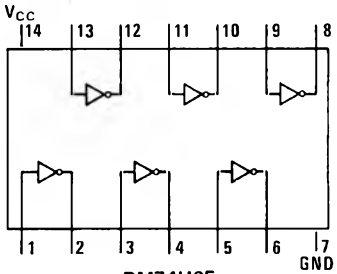
- Typical gate propagation delays of 7.5 ns to logical "0" output and 10 ns to logical "1" output
- Typical DC noise margin of 1V and low susceptibility to AC noise
- Fanout of 10 Series 74H loads when not wire-OR'd and up to 9 74H loads when wire-OR'd.

An output resistor connected to V_{CC} is needed. The load resistor value is calculated by the same method used for Series 74 open-collector circuits, except that the current values are higher. Series 74H input current maximums are 50 μA at logical "1" voltage and 2 mA at logical "0" voltage. Maximum output sink current is 20 mA.

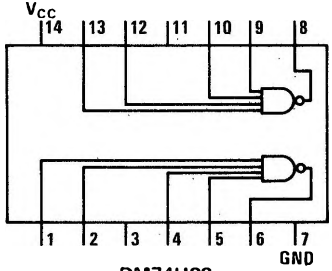
connection diagrams



DM74H01



DM74H05



DM74H22