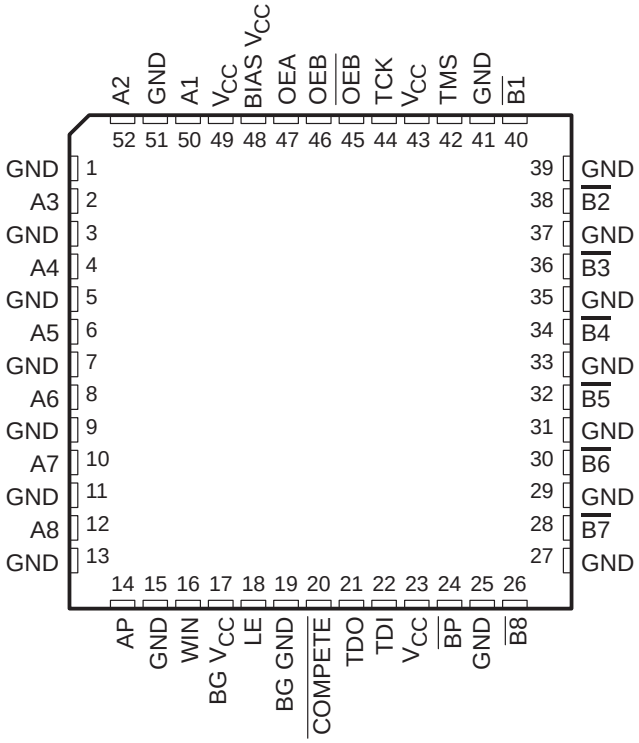
- **Compatible With IEEE Std 1194.1-1991 (BTL)**
- **TTL A Port, Backplane Transceiver Logic (BTL) $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion or Withdrawal**
- **High-Impedance State During Power Up and Power Down**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage**
- **TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination**
- **Packaged in Plastic Quad Flatpack**

RC PACKAGE
(TOP VIEW)



description

The SN74FB2032 device is a 9-bit transceiver designed to translate signals between TTL and backplane transceiver logic (BTL) environments and to perform bus arbitration. It is designed specifically to be compatible with IEEE Std 1194.1-1991.

The $\overline{B}$ port operates at BTL-signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA and have minimum output edge rates of 2 ns. Two output enables (OEB and $\overline{OEB}$) are provided for the $\overline{B}$ outputs. When OEB is low, $\overline{OEB}$ is high, or V_{CC} is less than 2.1 V, the $\overline{B}$ port is turned off.

description (continued)

The A port operates at TTL-signal levels. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable, OEA, is high. When OEA is low or when V_{CC} is less than 2.1 V, the A outputs are in the high-impedance state.

The A-port data is latched when the latch enable (LE) is high. When LE is low, the latches are transparent.

The Futurebus protocol logic can be activated by taking $\overline{\text{COMPETE}}$ low. The module (device) then compares its A data (arbitration number) against the A data of another identical module also connected to the $\overline{B}$ arbitration bus, and sets WIN high if the A data is greater than the A data of the other module (i.e., has higher priority). A8 and $\overline{B8}$ are the most-significant bits, and A1 and $\overline{B1}$ are the least-significant bits. If OEB is high and $\overline{OEB}$ is low during this operation, and the A bus of the first module wins priority, the A bus asserts its arbitration number on the $\overline{B}$-arbitration bus.

AP and $\overline{BP}$ are the bus-parity bits. The winning module can assert $\overline{BP}$ low if its parity bit (AP) is high.

In a typical operating sequence, a Futurebus arbitration controller latches its arbitration number into the A port and waits for the results of a competition. When the competition is complete, and if the controller's arbitration number did not win, the controller reads back the current value of the $\overline{B}$ bus (by taking OEA high) and determines the winning arbitration number. This allows the module to change its arbitration number for the next competition cycle, if desired.

Pins are allocated for the four-wire IEEE Std 1149.1 (JTAG) test bus. TMS and TCK are not connected and TDI is shorted to TDO.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

BG V_{CC} and BG GND are the supply inputs for the bias generator.

The SN74FB2032 is characterized for operation from 0°C to 70°C.

Function Tables

TRANSCEIVER

INPUTS			FUNCTION
OEA	OEB	$\overline{OEB}$	
L	H	L	$\overline{A}$ data to B bus
H	L	X	$\overline{B}$ data to A bus
H	X	H	
H	H	L	$\overline{A}$ data to B bus, $\overline{B}$ data to A bus
L	L	X	Isolation
L	X	H	

WIN

INPUTS				WIN
OEB	$\overline{OEB}$	$\overline{COMPETE}$	DATA A1, A2†	
H	H	X	X	L
H	L	H	X	L
H	L	L	A1 < A2	L
H	L	L	A2 ≤ A1	H

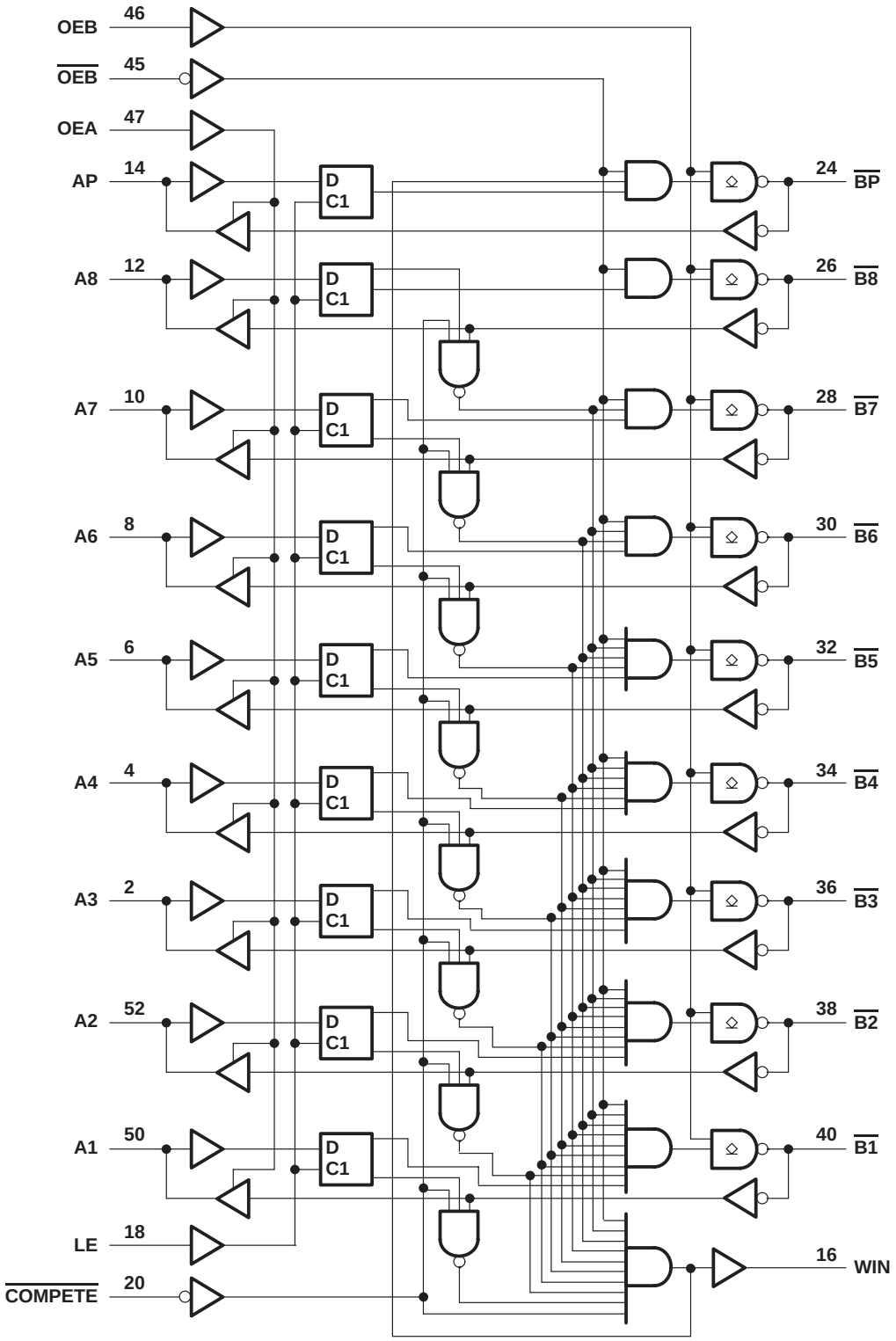
† A1 refers to the A data of Module 1 and A2 refers to the A data of Module 2. If LE = L, A = current A data. If LE = H, A = the value of A8–A1 prior to the most recent low-to-high transition of LE.

$\overline{BP}$

INPUTS				$\overline{BP}$
OEB	$\overline{OEB}$	WIN	AP‡	
L	X	X	X	H
X	H	X	X	H
H	L	L	X	H
H	L	H	L	H
H	L	H	H	L

‡ If LE = L, AP = current AP data. If LE = H, AP = the level of AP prior to the most recent low-to-high transition of LE.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I: Except $\overline{BP}$, $\overline{B}$ port . . . . . –1.2 V to 7 V
$\overline{BP}$, $\overline{B}$ port . . . . . –1.2 V to 3.5 V
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state, V_O . . . . . –0.5 V to 3.5 V
Voltage range applied to any output in the high state, V_O . . . . . –0.5 V to V_{CC}
Input clamp current, I_{IK}: Except $\overline{B}$ port . . . . . –40 mA
$\overline{B}$ port . . . . . –18 mA
Current applied to any single output in the low state, I_O: A port . . . . . 48 mA
$\overline{B}$ port . . . . . 200 mA
Package thermal impedance, θ_{JA} (see Note 1) . . . . . 44°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}, BG V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{BP}$, $\overline{B}$ port	1.62		2.3	V
		Except $\overline{B}$ port	2			
V_{IL}	Low-level input voltage	$\overline{BP}$, $\overline{B}$ port	0.75		1.47	V
		Except $\overline{B}$ port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	AP, WIN, A port			–3	mA
I_{OL}	Low-level output current	AP, WIN, A port			24	mA
		$\overline{BP}$, $\overline{B}$ port			100	
T_A	Operating free-air temperature		0		70	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{BP}$, $\overline{B}$ port	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
	Except $\overline{BP}$, $\overline{B}$ port	V_{CC} = 4.5 V,	I_I = –40 mA			–0.5	
V_{OH}	AP, WIN, A port	V_{CC} = 4.5 V	I_{OH} = –1 mA				V
			I_{OH} = –3 mA	2.5	3.3		
V_{OL}	AP, WIN, A port	V_{CC} = 4.5 V	I_{OL} = 20 mA				V
			I_{OL} = 24 mA		0.35	0.5	
	$\overline{BP}$, $\overline{B}$ port	V_{CC} = 4.5 V	I_{OL} = 80 mA	0.75		1.1	
			I_{OL} = 100 mA			1.15	
I_I	Except $\overline{BP}$, $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 5.5 V			50	µA
I_{IH}‡	Except $\overline{BP}$, $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 2.7 V			50	µA
I_{IL}‡	Except $\overline{BP}$, $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.5 V			–50	µA
	$\overline{BP}$, $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.75 V			–100	
I_{OZH}	AP, WIN, A port	V_{CC} = 2.1 V to 5.5 V,	V_O = 2.7 V			50	mA
I_{OZL}	AP, WIN, A port	V_{CC} = 2.1 V to 5.5 V,	V_O = 0.5 V			–50	mA
I_{OZPU}	AP, WIN, A port	V_{CC} = 0 V to 2.1 V,	V_O = 0.5 V to 2.7 V			50	mA
I_{OZPD}	AP, WIN, A port	V_{CC} = 2.1 V to 0 V,	V_O = 0.5 V to 2.7 V			–50	mA
I_{OH}	$\overline{BP}$, $\overline{B}$ port	V_{CC} = 0 to 5.5 V,	V_O = 2.1 V			100	µA
I_{OS}§	AP, WIN, A port	V_{CC} = 5.5 V,	V_O = 0	–30		–150	mA
I_{CC}	A port to $\overline{B}$ port	V_{CC} = 5.5 V,	I_O = 0			55	mA
	$\overline{B}$ port to A port					65	
C_i	Control Inputs	V_I = 0.5 V or 2.5 V			4		pF
C_o	WIN port	V_O = 0.5 V or 2.5 V			8		pF
C_{io}	A port	V_O = 0.5 V to 2.5 V			7		pF
	$\overline{B}$ port per IEEE Std 1194.1-1991	V_{CC} = 0 V to 5.5 V				5	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		450	µA
		V_{CC} = 4.5 V to 5.5 V				10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 5 V		1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0 ,	V_B = 1 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	–1		µA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V			100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V			100	

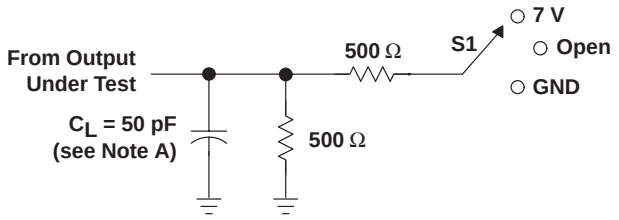
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			V_{CC} = 5 V, T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration	LE high or low	3.3		3.3		ns
t_{su}	Setup time	Data high before LE↑ (A to B)	1.5		1.5		ns
		Data low before LE↑	1.4		1.4		
		Data high before LE↑ (A to WIN)	1.9		1.9		
		Data low before LE↑	1.7		1.7		
t_h	Hold time	Data high before LE↑ (A to B)	1.7		1.7		ns
		Data low after LE↑	1.3		1.3		
		Data high before LE↑ (A to WIN)	1.6		1.6		
		Data low after LE↑	0.9		0.9		

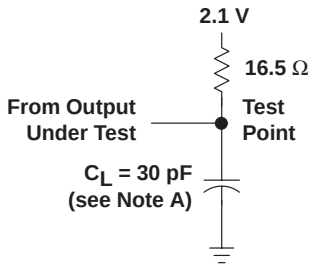
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}		A or AP	$\overline{B}$ or $\overline{BP}$	2.9	5.2	6.5	2.7	7	ns
t_{PHL}				3	4.9	6.3	2.8	6.6	
t_{PLH}		A	$\overline{B}_{n-1}$	3.1	5.6	7.4	2.5	8.4	ns
t_{PHL}				3.4	5.6	7.4	3.2	9	
t_{PLH}		A	$\overline{BP}$	4.5	6.6	8.1	4	8.9	ns
t_{PHL}				4.1	6.3	7.7	3.8	8.4	
t_{PLH}		$\overline{B}$	$\overline{B}_{n-1}$	5.5	8.4	10.8	4.8	11.4	ns
t_{PHL}				5.5	7.4	8.9	4.9	10	
t_{PLH}		LE	$\overline{B}$ or $\overline{BP}$	3.7	5.6	6.8	3.4	7.3	ns
t_{PHL}				3.5	5.1	6.1	3.1	6.8	
t_{PLH}		$\overline{B}$ or $\overline{BP}$	A or AP	3	5.3	7	2.9	7.2	ns
t_{PHL}				2.8	4.6	5.9	2	6.1	
t_{PLH}		$\overline{B}$	WIN	4	6	7.2	3.4	8.2	ns
t_{PHL}				4.2	6.6	8.6	3.9	8.9	
t_{PLH}		A	WIN	1.9	4.1	5.4	1.7	5.9	ns
t_{PHL}				1.9	4	5.3	1.6	6	
t_{PLH}		LE	WIN	2.4	4.4	5.7	2.1	6.4	ns
t_{PHL}				1.9	3.5	4.5	1.6	4.9	
t_{PLH}		$\overline{COMPETE}$	WIN	1.6	3.4	4.5	1.3	5	ns
t_{PHL}				1.7	3.4	4.4	1.5	4.9	
t_{PLH}		$\overline{OEB}$	WIN	1.7	3.5	4.7	1.4	5.4	ns
t_{PHL}				2.2	3.8	4.7	2	5	
t_{PLH}		$\overline{COMPETE}$	$\overline{B}$	3.2	5.2	6.6	2.7	7.3	ns
t_{PHL}				3.8	5.6	6.7	3.5	7.3	
t_{PLH}		$\overline{COMPETE}$	$\overline{BP}$	3.9	6.2	7.6	3.8	7.8	ns
t_{PHL}				3.9	5.7	7	3.4	7.8	
t_{PLH}		OEB	$\overline{B}$	3.1	5.3	6.7	2.9	7.3	ns
t_{PHL}				3.4	5.4	6.7	3.2	7.2	
t_{PLH}		$\overline{OEB}$	$\overline{B}$	4.6	6.7	8.1	4.4	8.6	ns
t_{PHL}				3.7	5.9	8.1	3.4	8.9	
t_{PZH}		OEA	A	2.5	4.3	6	2.2	6.3	ns
t_{PZL}				2.2	3.9	5.3	2.2	5.8	
t_{PHZ}		OEA	A	1.7	3.4	4.9	1.3	5.5	ns
t_{PLZ}				1.9	3.7	5.4	1.7	5.7	
$t_{sk(p)}$	Pulse skew	A	$\overline{B}$		0.8				ns
		$\overline{B}$	A		0.5				
$t_{sk(o)}$	Pulse skew	A	$\overline{B}$		0.8				ns
		$\overline{B}$	A		0.6				
t_r	Rise time, 1.3 V to 1.8 V, $\overline{B}$ outputs			1	2.2	3.2	1	3.2	ns
t_f	Fall time, 1.3 V to 1.8 V, $\overline{B}$ outputs			1	1.3	2.3	1	2.5	ns
$\overline{B}$-port input pulse rejection				1			1		ns

PARAMETER MEASUREMENT INFORMATION

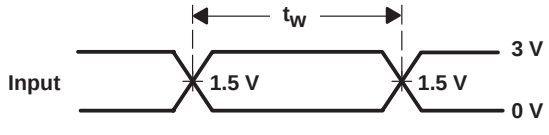


LOAD CIRCUIT FOR A OUTPUTS

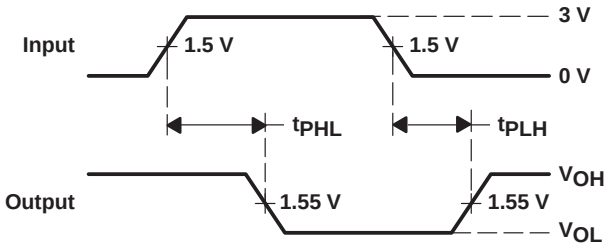


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

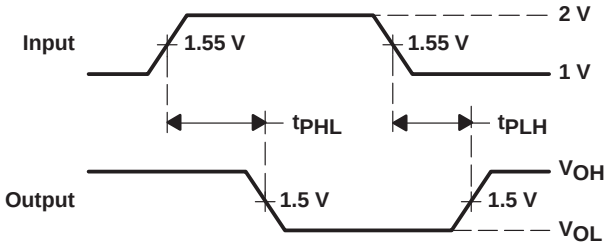
LOAD CIRCUIT FOR B OUTPUTS



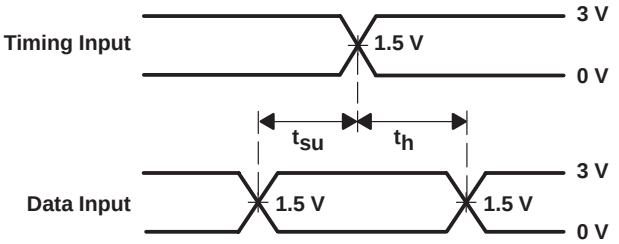
VOLTAGE WAVEFORMS
PULSE DURATION



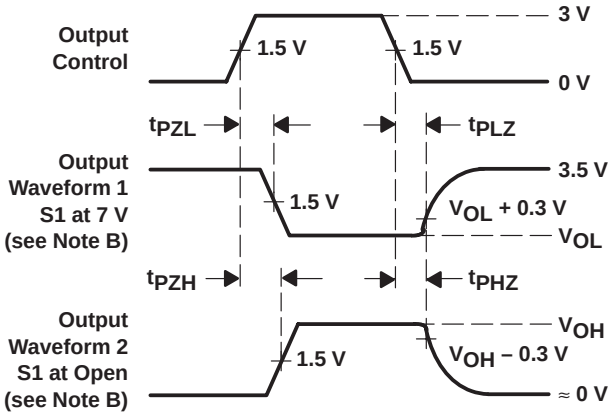
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A TO B)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B TO A)



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A PORT)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: TTL inputs: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns; BTL inputs: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

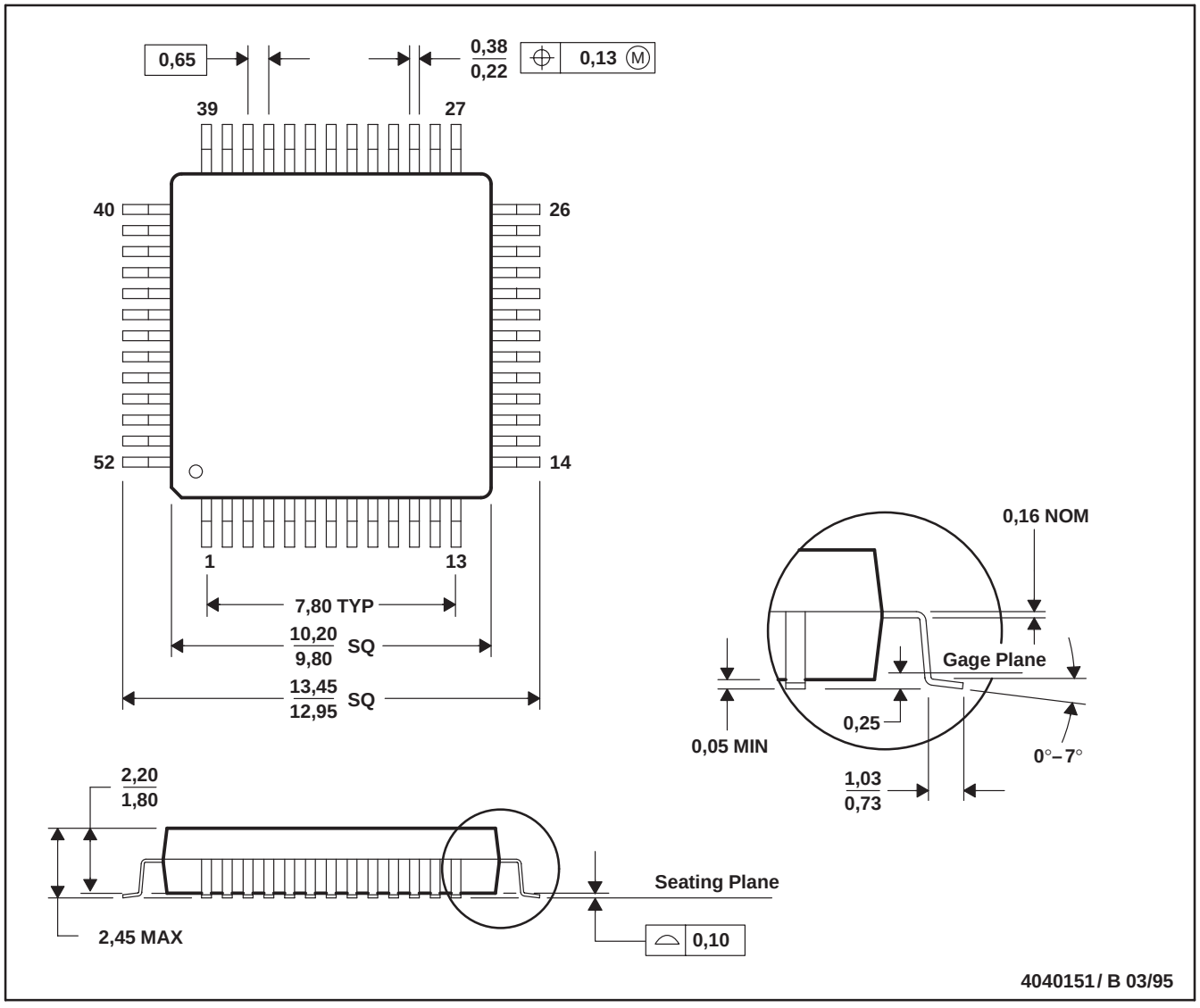
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SN74FB2032RC	OBSOLETE	QFP	RC	52		TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RC (S-PQFP-G52) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-022

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