- **Member of Texas Instruments' Widebus+™ Family**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Flow-Through Architecture Optimizes PCB Layout**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

description

The SN74CBT34X245 provides 32 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as four 8-bit bus switches, two 16-bit bus switches, or one 32-bit bus switch. When output enable ($\overline{OE}$) is low, the switch is on, and port A is connected to port B. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the two ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

DBB PACKAGE
(TOP VIEW)

NC	1	80	V_{CC}
1A1	2	79	$1\overline{OE}$
1A2	3	78	1B1
1A3	4	77	1B2
1A4	5	76	1B3
1A5	6	75	1B4
1A6	7	74	1B5
1A7	8	73	1B6
1A8	9	72	1B7
GND	10	71	1B8
NC	11	70	V_{CC}
2A1	12	69	$2\overline{OE}$
2A2	13	68	2B1
2A3	14	67	2B2
2A4	15	66	2B3
2A5	16	65	2B4
2A6	17	64	2B5
2A7	18	63	2B6
2A8	19	62	2B7
GND	20	61	2B8
NC	21	60	V_{CC}
3A1	22	59	$3\overline{OE}$
3A2	23	58	3B1
3A3	24	57	3B2
3A4	25	56	3B3
3A5	26	55	3B4
3A6	27	54	3B5
3A7	28	53	3B6
3A8	29	52	3B7
GND	30	51	3B8
NC	31	50	V_{CC}
4A1	32	49	$4\overline{OE}$
4A2	33	48	4B1
4A3	34	47	4B2
4A4	35	46	4B3
4A5	36	45	4B4
4A6	37	44	4B5
4A7	38	43	4B6
4A8	39	42	4B7
GND	40	41	4B8

NC – No internal connection

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ORDERING INFORMATION

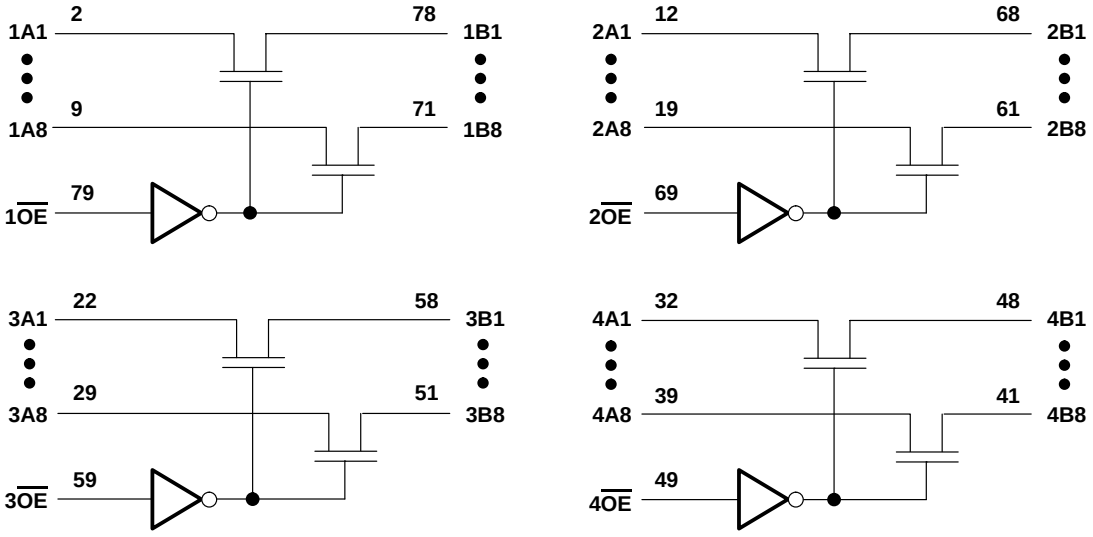
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TVSOP – DBB	Tape and reel	SN74CBT34X245DBBR	CBT34X245

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 8-bit bus switch)

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Continuous channel current . . . . . 128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2) . . . . . 64°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±5	µA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 5.5 V				10	µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			6	µA
ΔI_{CC}‡	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			3.5	mA
C_i	Control inputs	V_I = 3 V or 0				3.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			5.5		pF
r_{on}§		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		11	17	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	Ω
				I_I = 30 mA		5	7	Ω
			V_I = 2.4 V,	I_I = 15 mA		8	13	Ω

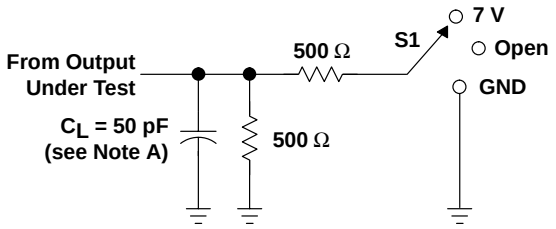
† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A				0.25	ns
t_{en}	$\overline{OE}$	A or B	2.2	6.5	1.9	6	ns
t_{dis}	$\overline{OE}$	A or B	1.9	6.2	2.2	6.7	ns

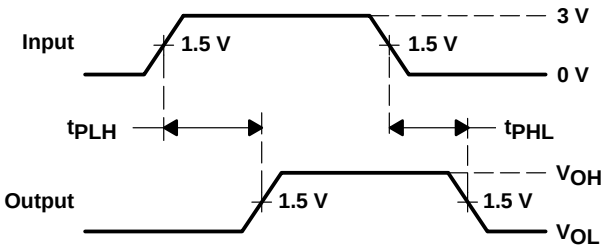
¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

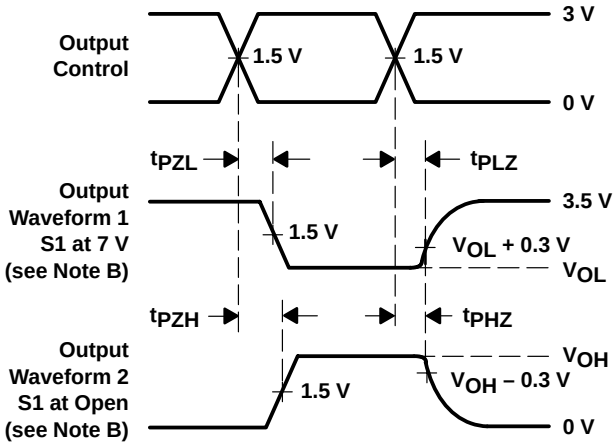


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
74CBT34X245DBBRE4	ACTIVE	TSSOP	DBB	80	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBT34X245DBBRG4	ACTIVE	TSSOP	DBB	80	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT34X245DBBR	ACTIVE	TSSOP	DBB	80	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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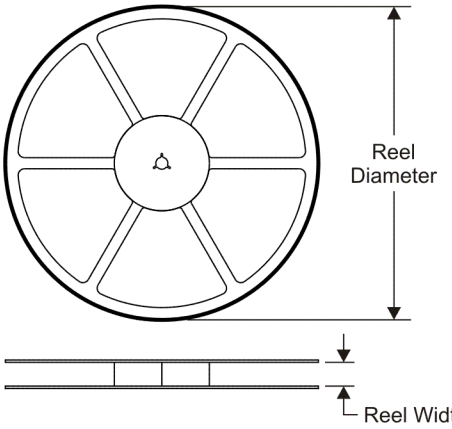
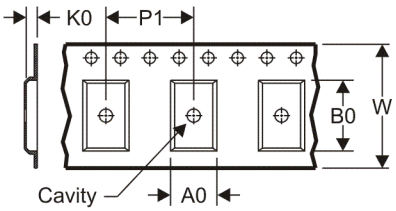
REEL DIMENSIONS

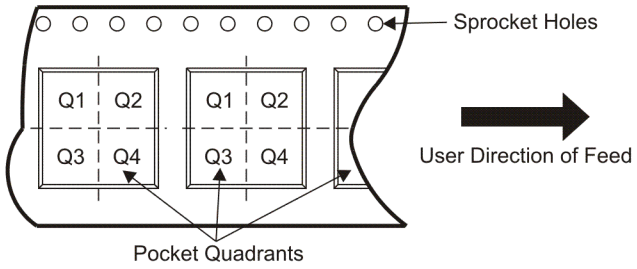


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

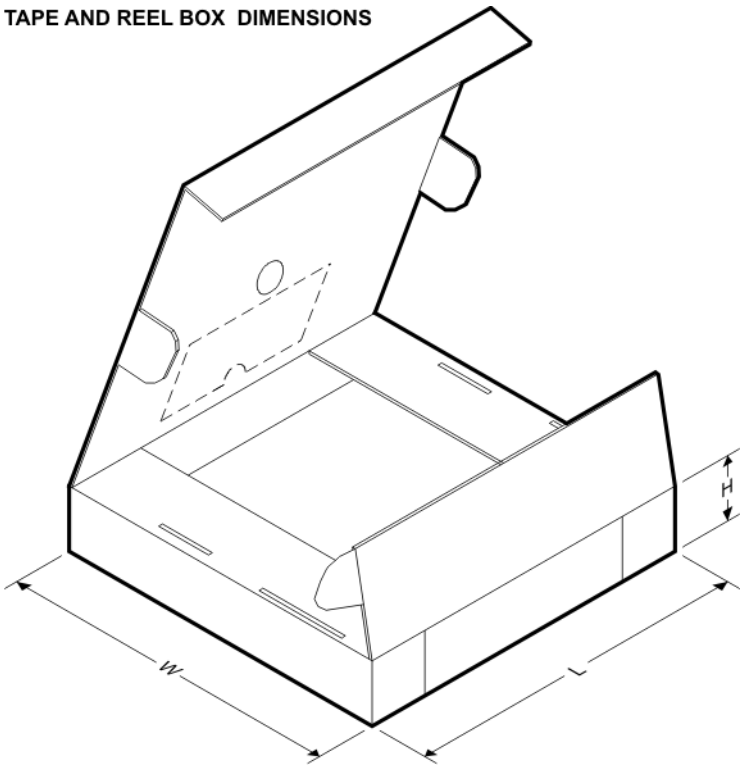
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT34X245DBBR	TSSOP	DBB	80	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



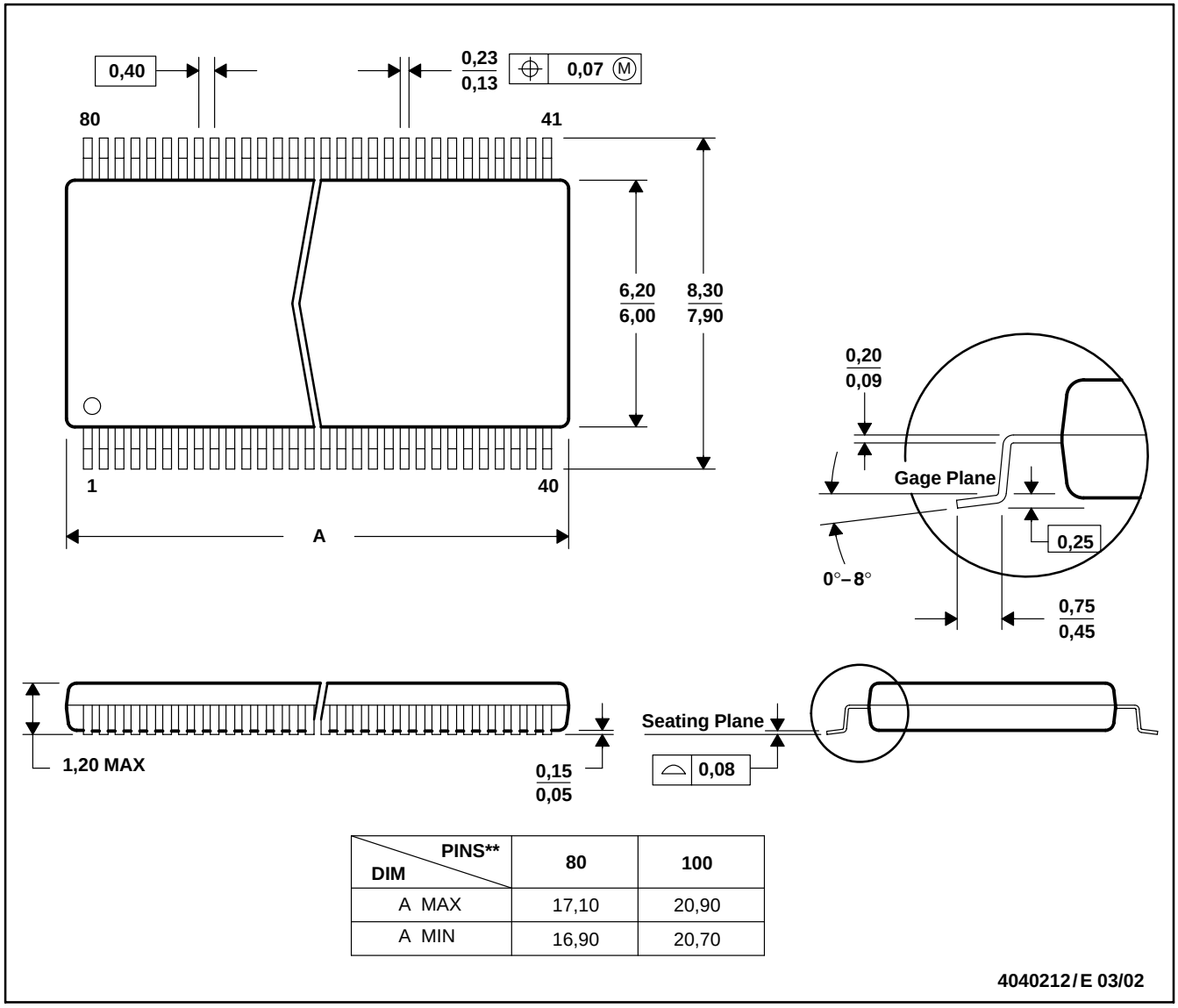
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT34X245DBBR	TSSOP	DBB	80	2000	346.0	346.0	41.0

MTSS005D – JANUARY 1995 – REVISED MARCH 2002

DBB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

80 PINS SHOWN



DIM \ PINS**	80	100
A MAX	17,10	20,90
A MIN	16,90	20,70

4040212/E 03/02

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC : 80 Pin – MO-153 Variation FF
100 Pin – MO-194 Variation BB

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