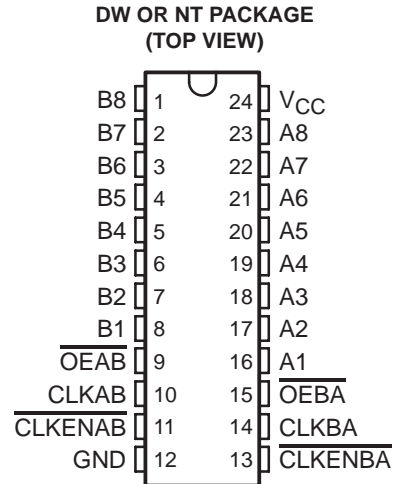


SN74BCT2953 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCBS105B – DECEMBER 1990 – REVISED NOVEMBER 1993

- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015
- Two 8-Bit, Back-to-Back Registers Store Data Flowing in Both Directions
- A Port Sinks 24 mA and Sources 3 mA
- B Port Sinks 64 mA and Sources 15 mA
- Inverting Outputs
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (NT)



description

The SN74BCT2953 octal bus transceiver contains two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable (CLKENAB or CLKENBA) input is low. Taking the output-enable (OEAB or OEBA) input low allows access of the data on the output port (B port or A port).

The SN74BCT2953 is characterized for operation from 0°C to 70°C.

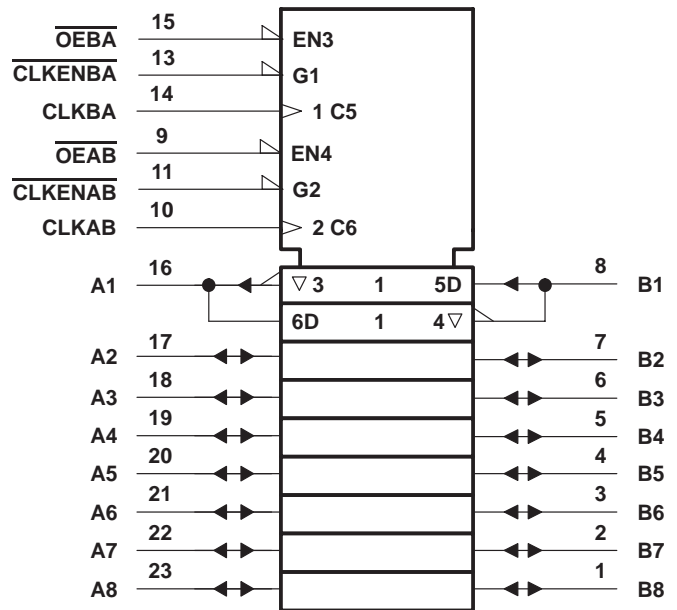
FUNCTION TABLE†

INPUTS				OUTPUT
CLKENAB	CLKAB	OEAB	A	B
H	X	L	X	B_0 ‡
X	H or L	L	X	B_0 ‡
L	↑	L	L	H
L	↑	L	H	L
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA, CLKBA, and OEBA.

‡ Level of B before the indicated steady-state input conditions were established.

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current	A ports		-3	mA
		B ports		-15	
I_{OL}	Low-level output current	A ports		24	mA
		B ports		64	
T_A	Operating free-air temperature	0		70	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V
V_{OH}	A port	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -1\text{ mA}$	2.5	3.4		V
			$I_{OH} = -3\text{ mA}$	2.4	3.3		
	B port	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -3\text{ mA}$	2.4	3.3		
			$I_{OH} = -12\text{ mA}$		3.2		
			$I_{OH} = -15\text{ mA}$	2	3.1		
V_{OL}	A port	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 24\text{ mA}$		0.35	0.5	V
	B port		$I_{OL} = 64\text{ mA}$		0.42	0.55	
I_I^\ddagger	Control inputs	$V_{CC} = 5.5\text{ V}$,	$V_I = 5.5\text{ V}$			1	mA
	A or B ports					0.1	
I_{IH}^\ddagger	Control inputs	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$			70	μA
	A or B ports					20	
I_{IL}^\ddagger	Control inputs	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.5\text{ V}$			-70	μA
	A or B ports					-20	
I_{OS}^\S	Any A	$V_{CC} = 5.5\text{ V}$,	$V_O = 0$			-60	mA
	Any B					-100	
I_{CCH}^\parallel		$V_{CC} = 5.5\text{ V}$			2	5	mA
I_{CCL}^\parallel		$V_{CC} = 5.5\text{ V}$			38	55	mA
I_{CCZ}		$V_{CC} = 5.5\text{ V}$			2	5	mA
C_i	Control inputs	$V_{CC} = 5\text{ V}$,	$V_I = 2.5\text{ V}$ or 0.5 V		6		pF
C_{io}	A or B ports	$V_{CC} = 5\text{ V}$,	$V_O = 2.5\text{ V}$ or 0.5 V		12.5		pF

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-shoot output current.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

¶ I_{CCH} and I_{CCL} are measured in the A-to-B mode.



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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		$V_{CC} = 5\text{ V},$ $T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	0	110	0	110	MHz
t_w	Pulse duration	CLK high	4.5	4.5	ns	
		CLK low	4.5	4.5		
t_{su}	Setup time before $\text{CLK}\uparrow$	A or B	2.5	2.5	ns	
		$\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$	2	2		
t_h	Hold time after $\text{CLK}\uparrow$	A or B	1.5	1.5	ns	
		$\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$	2	2		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V},$ $T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			110			110		MHz
t_{PLH}	CLKBA or CLKAB	A or B	2.5	6.3	8	2.5	9.5	ns
t_{PHL}			4.3	7.8	9.4	4.3	10.2	
t_{PZH}	$\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$	A or B	2.1	5.8	7.3	2.1	8.8	ns
t_{PZL}			5.2	10.3	12.1	5.2	14	
t_{PHZ}	$\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$	A or B	2.3	5.5	7.6	2.3	9.1	ns
t_{PLZ}			1.8	5.5	7.1	1.8	7.6	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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