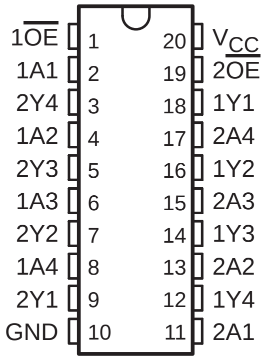
# SN74AS230A
# OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SDAS213B − DECEMBER 1982 − REVISED DECEMBER 1994

- **True and Complementary Outputs**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **High Capacitive-Drive Capability**
- **Current-Sinking Capability Up to 64 mA**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (N) 300-mil DIPs**

**DW OR N PACKAGE**
**(TOP VIEW)**



## description

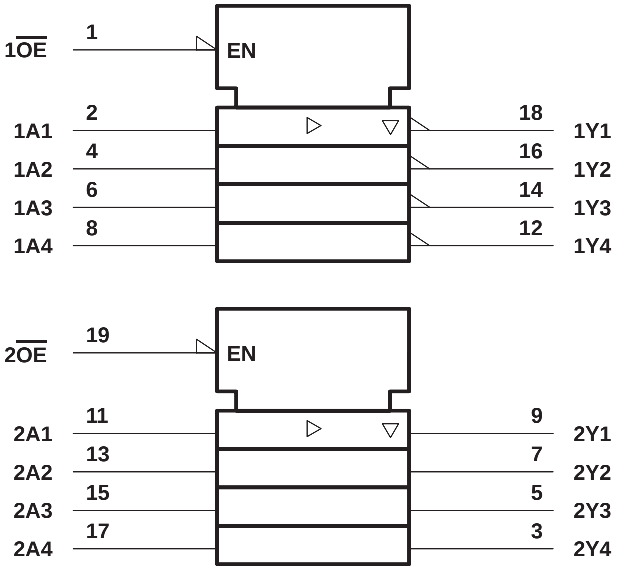
This octal buffer/driver is designed specifically to improve the performance of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. When used together, multiples of this device provide the choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable ($\overline{\mathrm{OE}}$) inputs, and complementary OE and $\overline{\mathrm{OE}}$ inputs.

The SN74AS230A is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(each buffer)**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{\mathrm{OE}}$ | A | Y |
| L | H | L |
| L | L | H |
| H | X | Z |

## logic symbol†



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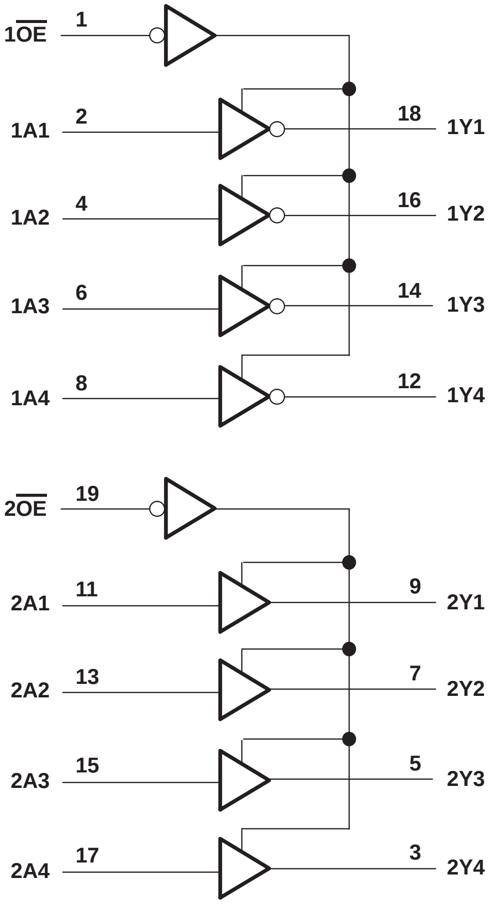
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage, $V_{CC}$ | 7 V |
| Input voltage, $V_I$ | 7 V |
| Voltage applied to a disabled 3-state output | 5.5 V |
| Operating free-air temperature range, $T_A$ | 0°C to 70°C |
| Storage temperature range | −65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | −15 | mA |
| $I_{OL}$ | Low-level output current | | | 64 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = −2 mA | $V_{CC}$ −2 | | | V |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = −3 mA | 2.4 | 3.4 | | |
| | | | $I_{OH}$ = −15 mA | 2.4 | | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 64 mA | | 0.31 | 0.55 | V |
| $I_{OZH}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | µA |
| $I_{OZL}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.4 V | | | −50 | µA |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | µA |
| $I_{IL}$ | 2A inputs | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | −1 | mA |
| | All other inputs | | | | | −0.5 | |
| $I_O$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | −50 | | −150 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V | Outputs high | | 16 | 25 | mA |
| | | | Outputs low | | 55 | 87 | |
| | | | Outputs disabled | | 29 | 46 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

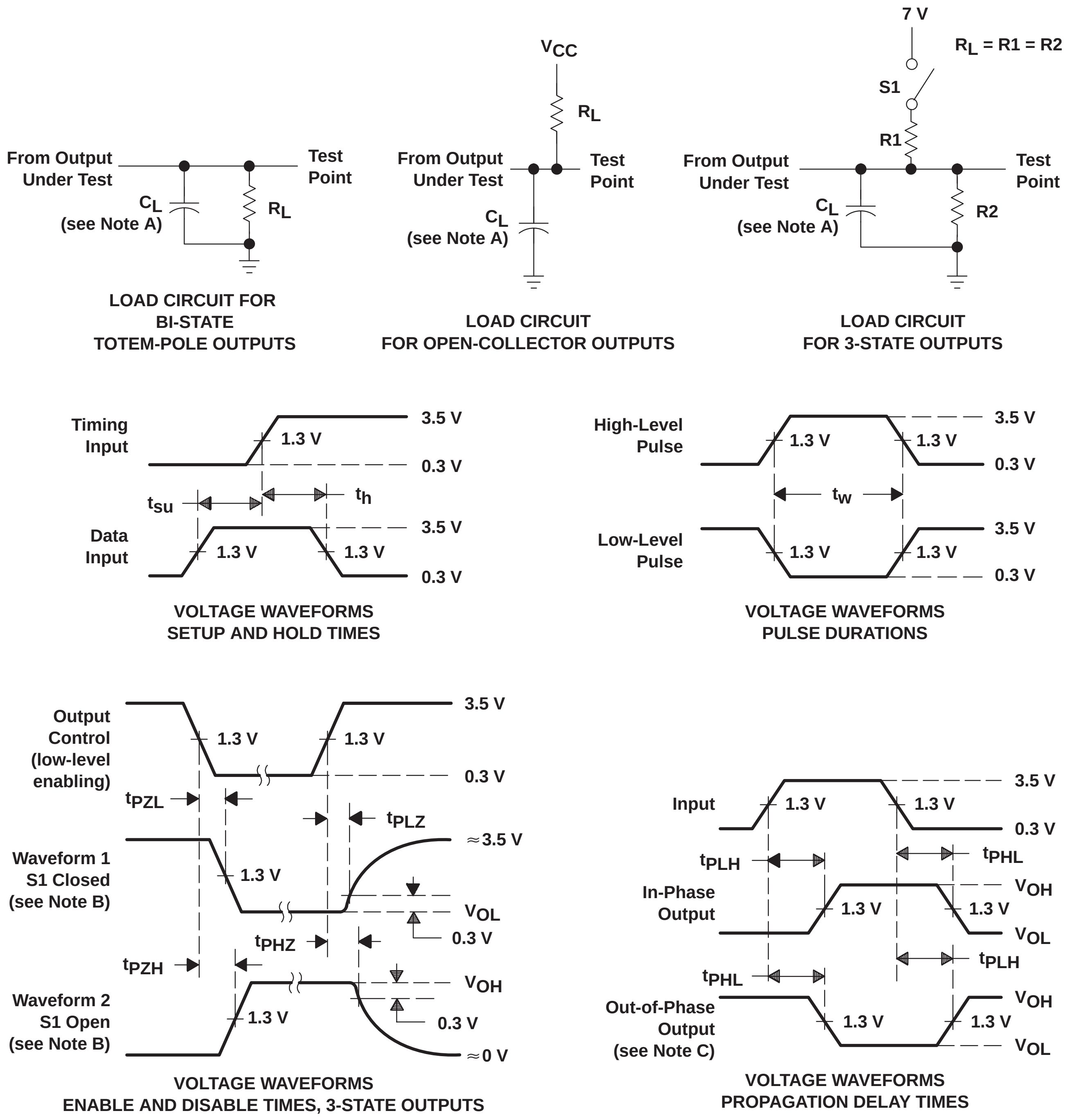
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

## switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = MIN to MAX§ | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $t_{PLH}$ | 1A | 1Y | 2 | 6.5 | ns |
| $t_{PHL}$ | | | 1 | 5.7 | |
| $t_{PLH}$ | 2A | 2Y | 2 | 6.2 | ns |
| $t_{PHL}$ | | | 1 | 6.2 | |
| $t_{PZH}$ | $1\overline{OE}$ | 1Y | 2 | 6.4 | ns |
| $t_{PZL}$ | | | 2 | 8.5 | |
| $t_{PHZ}$ | $1\overline{OE}$ | 1Y | 2 | 6 | ns |
| $t_{PLZ}$ | | | 2 | 9.5 | |
| $t_{PZH}$ | $2\overline{OE}$ | 2Y | 2 | 9 | ns |
| $t_{PZL}$ | | | 2 | 7.5 | |
| $t_{PHZ}$ | $2\overline{OE}$ | 2Y | 2 | 6 | ns |
| $t_{PLZ}$ | | | 2 | 9 | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

## PARAMETER MEASUREMENT INFORMATION
## SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

LOAD CIRCUIT FOR 3-STATE OUTPUTS

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS PULSE DURATIONS

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

NOTES:
A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| SN74AS230ADW | OBSOLETE | SOIC | DW | 20 |  | TBD | Call TI | Call TI | Samples Not Available |
| SN74AS230ADWR | OBSOLETE | SOIC | DW | 20 |  | TBD | Call TI | Call TI | Samples Not Available |
| SN74AS230AN | OBSOLETE | PDIP | N | 20 |  | TBD | Call TI | Call TI | Samples Not Available |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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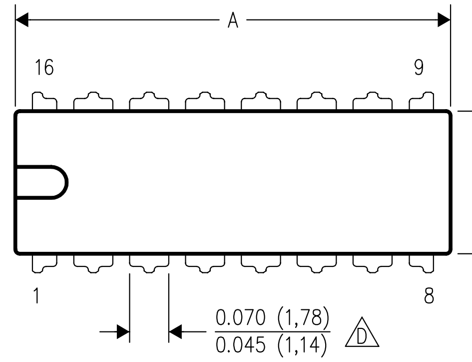
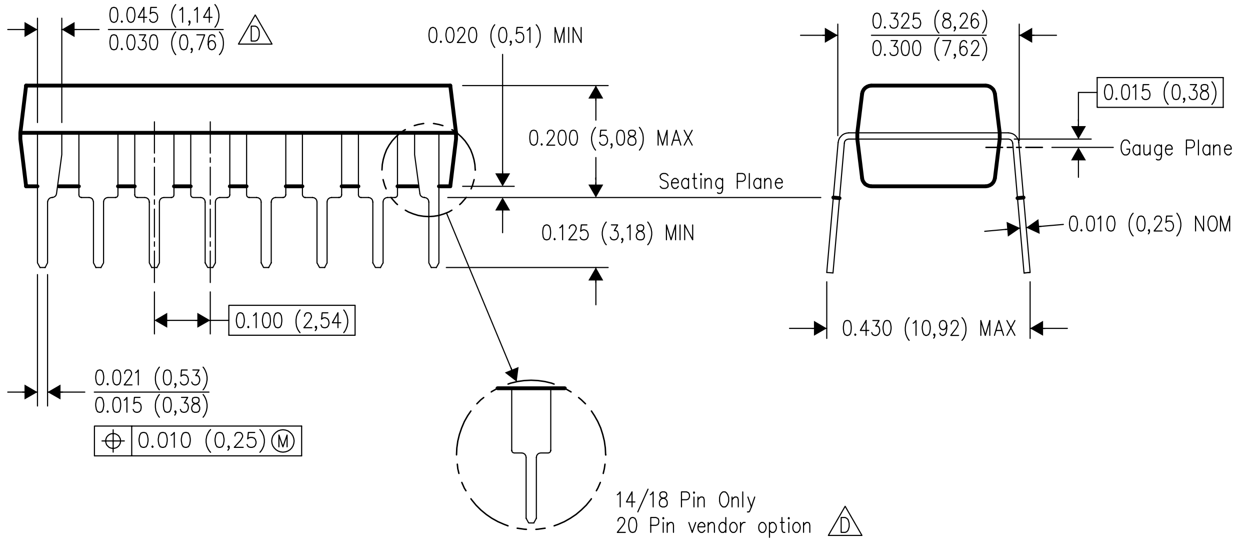
## N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



| PINS **<br>DIM | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| △C MS–001 VARIATION | AA | BB | AC | AD |



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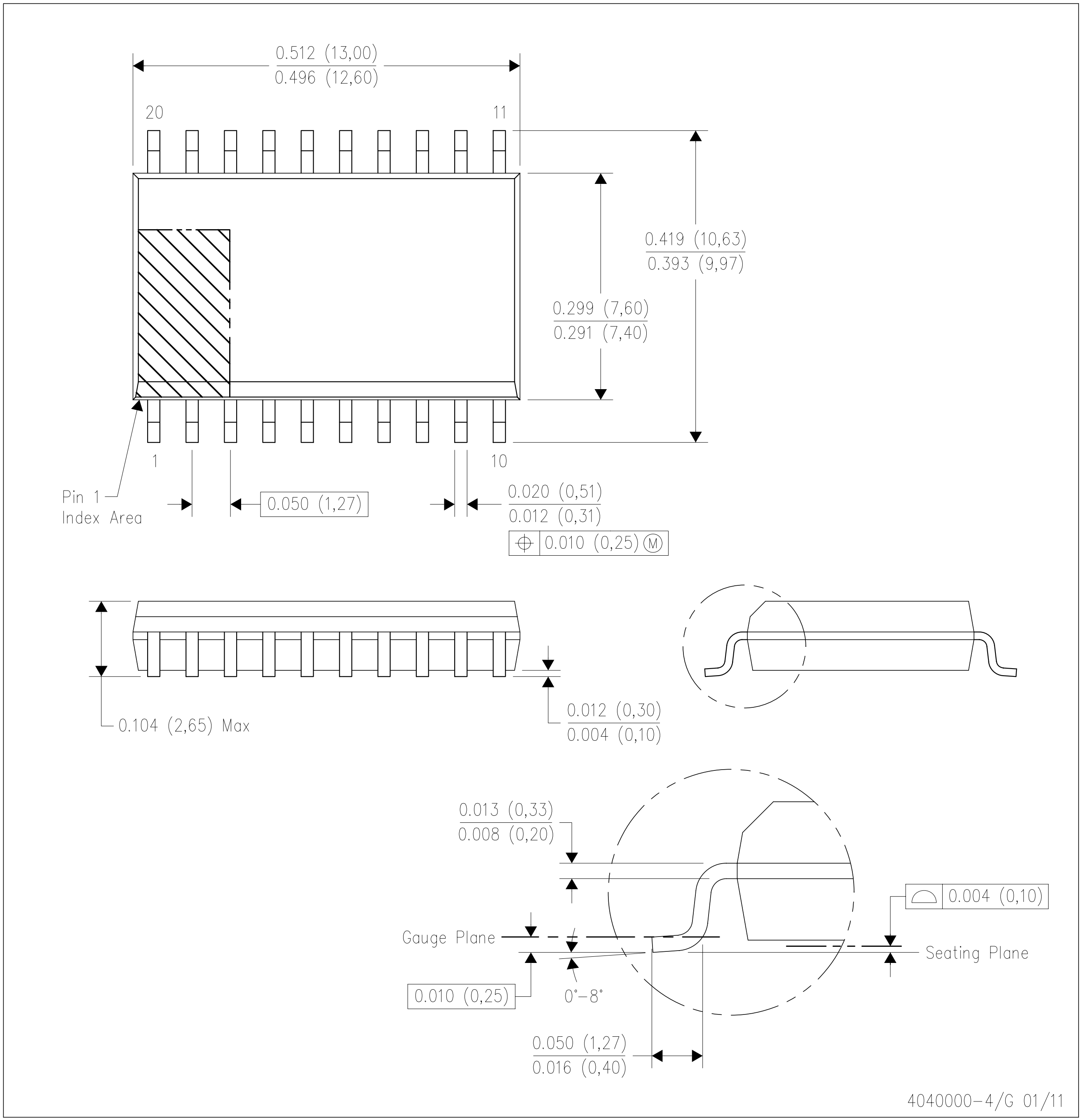
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- △C Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- △D The 20 pin end lead shoulder width is a vendor option, either half or full width.

## DW (R-PDSO-G20) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS–013 variation AC.

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